NTEGRATED CIRCUITS

FAST TTL
Logic Series

Data Handbook IC15
1999



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FAST TTL Logic Series
Data Handbook

CONTENTS

		page
SECTION 1	GENERAL INFORMATION	5
SECTION 2	FAST TTL LOGIC DEVICES	57
SECTION 3	APPLICATION NOTES	861
SECTION 4	PACKAGE INFORMATION	927
APPENDIX A	DATA HANDBOOK SYSTEM	951

DEFINITIONS

Data Sheet Identification	Product Status	Definition (Note)
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.
Short-form specification	—	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

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NOTE: Always check with your local Philips Semiconductors Sales Office to be certain that you have the latest data sheet(s) before completing a design.

Preface

FAST TTL Logic from Philips Semiconductors

Philips Semiconductors Logic Products Group thanks you for continued interest in our FAST TTL Series product line. FAST TTL Logic is still the preferred high performance bipolar logic family and has wide customer acceptance. Philips Semiconductors offers the widest selection of FAST TTL Logic products with an emphasis on integrated MSI and LSI solutions.

This Handbook replaces and updates the 1992 FAST Data Handbook (IC15). Products, which have been discontinued since the last issued Data Handbook, have been highlighted to alert the user.

For your convenience each data sheet contained in this Handbook is designed to stand alone, and, reflect the listed DC and AC specification for a particular product. Each commercial 74F product is specified over a 10% V_{CC} range, both for AC and DC parameters. Additionally, DC specifications for V_{OH} and V_{OL} are provided over the 5% V_{CC} range.

For additional information such as SPICE models, product announcements, FAQs and other information, please visit our web site at "www.philipslogic.com".

Our ongoing goal is to become your first choice for all Logic Products.

Section 1
General Information

FAST TTL Logic Series

CONTENTS

Functional Index 7
Introduction 13
Quality and Reliability 17
Availability Guide 18
Discontinued Products 23
Function Selection Guide 24
Circuit characteristics 30
FAST User's guide 43
  Datasheet Specification Guide 43
  Design Considerations 52
Ordering Information 55

IC15: FAST TTL LOGIC SERIES

Preface 3

Section 1 – General Information

Functional Index 7
Introduction 13
Quality and Reliability 17
Availability Guide 18
Discontinued Products 23
Function Selection Guide 24
Circuit characteristics 30
FAST User's guide 43
Datasheet Specification Guide 43
Design Considerations 52
Ordering Information 55

Section 2 – FAST TTL Logic Devices

74F00 Quad 2-input NAND gate 61
74F02 Quad 2-input NOR gate 64
74F04 Hex inverter 67
74F06 Hex Inverter Buffer/Driver, Open-Collector 70
74F06A Hex Inverter Buffer/Driver, Open-Collector 70
74F07 Hex Buffer/Driver, Open-Collector 70
74F07A Hex Buffer/Driver, Open-Collector 70
74F08 Quad 2-input AND gate 76
74F10 Triple 3-Input NAND Gate 79
74F11 Triple 3-Input AND Gate 79
74F14 Hex inverter Schmitt trigger 83
74F20 Dual 4-input NAND gate 87
74F27 Triple 3-input NOR gate 90
74F30 8-input NAND gate 94
74F32 Quad 2-input OR gate 98
74F37 Quad 2-input NAND buffer 101
74F38 Quad 2-input NAND buffer (open collector) 104
74F51 Dual 2-wide 2-input, 2-wide 3-input AND-OR-invert gate 108
74F64 4-2-3-2-input AND-OR-invert gate 111
74F74 Dual D-type flip-flop 115
74F85 4-bit magnitude comparator 119
74F86 Quad 2-input Exclusive-OR gate 124
74F109 Positive J-K positive edge-triggered flip-flops 127
74F112 Dual J-K negative edge-triggered flip-flop 132
74F113 Dual J-K negative edge-triggered flip-flops without reset 138
74F125 Quad buffers (3-State) 143
74F126 Quad buffers (3-State) 143
74F132 Quad 2-input NAND Schmitt trigger 148
74F133 13-input NAND gate 152
74F138 1-of-8 decoder/demultiplexer 156
74F139 1-of-4 decoder/demultiplexer 160
74F148 8-input priority encoder 164
74F151A 8-input multiplexer 169
74F153 Dual 4-line to 1-line multiplexer 174
74F154 Decoder/demultiplexer 178
74F157A Quad 2-Input Data Selector/Multiplexer, Non–inverting 182
74F158A Quad 2-Input Data Selector/Multiplexer, Inverting 182
74F161A 4-bit binary counters, asynchronous reset 187
74F163A 4-bit binary counters, synchronous reset 187

Section 2 – FAST TTL Logic Devices (continued)

74F164	8-bit serial-in parallel-out shift register	196
74F166	8-bit bidirectional universal shift register	201
74F169	4-bit up/down binary synchronous counter	208
74F173	Quad D-type flip–flop (3-State)	216
74F174	Hex D-type flip-flop	222
74F175A	Quad D-type flip-flop	226
74F189A	64-bit TTL bipolar RAM, inverting (3-State)	231
74F191	Up/Down binary counter with reset and ripple clock	237
74F193	Up/down binary counter with separate up/down clocks	246
74F194	4-bit bidirectional universal shift register	253
74F195A	4-bit parallel-access shift register	259
74F198	8-bit bidirectional universal shift register	265
74F219A	64-bit TTL bipolar RAM, non-inverting (3-State)	272
74F225	16 x 5 asynchronous FIFO (3-State)	278
74F240	Octal inverter buffer (3-state)	287
74F240A	Octal inverter buffer (3-state)	287
74F241	Octal buffer (3-state)	287
74F241A	Octal buffer (3-state)	287
74F242	Quad transceiver, inverting (3–state)	294
74F243	Quad transceiver (3–state)	294
74F244	Octal buffers (3-State)	300
74F244B	Octal buffers (3-State)	300
74F245	Octal transceiver (3-State)	306
74F253	Dual 4-input multiplexer (3-State)	310
74F256	Dual addressable latch	316
74F257A	Quad 2-line to 1-line selector/multiplexer, non-inverting (3-State)	323
74F258A	Quad 2-line to 1-line selector/multiplexer, inverting (3-State)	328
74F259	8-bit addressable latch	332
74F260	Dual 5-input NOR gate	339
74F269	8–bit bidirectional binary counter	342
74F273A	Octal D-type flip–flop	350
74F280B	9-bit odd/even parity generator/checker	356
74F283	4-bit binary full adder with fast carry	360
74F298	Quad 2-input multiplexer with storage	365
74F299	8-bit universal shift/storage register (3-State)	369
74F365	Hex buffer driver (3-state)	377
* 74F366	Hex inverter buffer driver (3-state)	377
74F367	Hex buffer driver (3-state)	377
* 74F368	Hex inverter buffer driver (3-state)	377
74F373	Octal transparent latch (3-state)	383
74F374	Octal D-type flip-flop (3-state)	383
74F377A	Octal D-type flip-flop with enable	390
74F378	Hex D-type flip-flop with enable	395
74F379A	Quad register	400
74F382	Arithmetic logic unit	405
74F393	Dual 4-bit binary ripple counter	413
* 74F398	Quad 2-port register with true and complimentary outputs	417
74F399	Quad 2-port register	417
* 74F455	Octal buffer driver with parity, inverting (3-state)	423
74F456	Octal buffer driver with parity, non-inverting (3-state)	423
74F521	8-bit identity comparator	430
74F524	8-bit register comparator (open collector + 3-State)	434
* 74F533	Octal transparent latch, inverting (3-state)	443
74F534	Octal D-type flip-flop inverting (3-state)	443

** Discontinued part. Please see the Discontinued Products List.*

Section 2 – FAST TTL Logic Devices (continued)

74F538	1-of-8 decoder (3-State)	450
74F540	Octal inverted buffer (3-state) (broad side pinout of 74F240)	455
74F541	Octal buffer (3-state) (broad side pinout of 74F244)	455
74F543	Octal registered transceiver, non-inverting (3-state)	461
74F544	Octal registered transceiver, inverting (3-state)	461
74F545	Octal bidirectional transceiver (with 3-State inputs/outputs)	471
74F552	Octal registered transceiver with parity and flags (3-State)	476
74F564	Octal D-type flip-flop (3-State)	485
74F569	4-bit bidirectional binary synchronous counter (3-State)	490
74F573	Octal transparent latch (3-state) (broad side pinout of 74F373)	499
74F574	Octal D-type flip-flop (3-state) (broad side pinout of 74F374)	499
74F579	8-bit bidirectional binary counter (3-State)	507
74F595	8-bit shift register with output latches (3-State)	516
74F597	8-bit shift register with input storage registers	523
74F598	8-bit shift register with input storage registers (3-State)	530
74F620	Octal bus transceiver, inverting (3-state)	540
74F623	Octal bus transceiver, non-inverting (3-state)	540
74F621	Octal bus transceiver, non-inverting (open collector)	547
74F640	Octal bus transceiver, inverting (3-State)	552
74F641	Octal bus transceiver with common output enable, non-inverting (open collector)	557
* 74F642	Octal bus transceiver with common output enable, inverting (open collector)	557
* 74F646	Octal transceiver/register, non-inverting (3-state)	563
74F646A	Octal transceiver/register, non-inverting (3-state)	563
* 74F648	Octal transceiver/register, inverting (3-state)	563
74F648A	Octal transceiver/register, inverting (3-state)	563
74F647	Octal transceivers/registers, non–inverting open-collector	563
74F649	Octal transceivers/registers, non–inverting open-collector	574
* 74F651	Octal transceivers/registers, inverting (3-state)	581
74F651A	Octal transceivers/registers, inverting (3-state)	581
* 74F652	Octal transceivers/registers, non-inverting (3-state)	581
74F652A	Octal transceivers/registers, non-inverting (3-state)	581
* 74F655A	Octal buffer/driver with parity, inverting (3-state)	592
74F656A	Octal buffer/driver with parity, non-inverting (3-state)	592
74F657	Octal transceiver with 8-bit parity generator/checker	599
74F670	4 x 4 register file (3-State)	606
74F676	16-bit serial/parallel-in, serial-out shift register (3-State)	613
74F711A	Quint 2-to-1 data selector multiplexer (3-state)	618
74F711–1	Quint 2-to-1 data selector multiplexer with 30Ω series termination resistors (3-state)	618
74F712A	Quint 3-to-1 data selector multiplexer	618
74F712–1	Quint 3-to-1 data selector multiplexer with 30Ω series termination resistors	618
74F723A	Quint 3-to-1 data selector multiplexer (3-state)	627
74F723–1	Quint 3-to-1 data selector multiplexer with 30Ω series termination resistors (3-state)	627
74F725A	Quad 4-to-1 data selector multiplexer	627
74F725–1	Quad 4-to-1 data selector multiplexer with 30Ω series termination resistors	627
74F756	Octal inverter buffer (open collector 74F240)	636
74F757	Octal buffer (open collector 74F241)	636
74F760	Octal buffer (open collector 74F244)	636
74F776	Pi–bus transceiver	643
74F777	Triple bidirectional latched bus transceiver (3–State + Open Collector)	651
74F779	8-bit bidirectional binary counter (3-State)	658
74F786	4-bit asynchronous bus arbiter	665
74F804	Hex 2-input NAND drivers	672
74F1804	Hex 2-input NAND drivers (center power pin 74F804)	672
74F805	Hex 2-input NOR drivers	676

** Discontinued part. Please see the Discontinued Products List.*

Section 2 – FAST TTL Logic Devices (continued)

74F1805	Hex 2-input NOR drivers (center power pin 74F805)	676
74F808	Hex 2-input AND drivers	680
74F1808	Hex 2-input AND drivers (center power pin 74F808)	680
74F821	10-bit interface register, non-inverting (3-state)	684
74F822	10-bit interface register, inverting (3-state)	684
74F823	9-bit interface register, non-inverting (3-state)	684
74F824	9-bit interface register, inverting (3-state)	684
74F825	8-bit interface register, non-inverting (3-state)	684
74F826	8-bit interface register, inverting (3-state)	684
74F827	10-bit buffer/line-driver, non-inverting (3-state)	697
74F828	10-bit buffer/line-driver, inverting (3-state)	697
74F832	Hex 2-input OR drivers	704
74F1832	Hex 2-input OR drivers (center power pin 74F832)	704
74F841	10-bit bus interface latch, non-inverting (3-state)	708
74F842	10-bit bus interface latch, inverting (3-state)	708
74F843	9-bit bus interface latch, non-inverting (3-state)	708
* 74F844	9-bit bus interface latch, inverting (3-state)	708
74F845	8-bit bus interface latch, non-inverting (3-state)	708
74F846	8-bit bus interface latch, inverting (3-state)	708
* 74F861	9-bit bus transceiver, non-inverting (3-state)	722
* 74F862	9-bit bus transceiver, inverting (3-state)	722
74F863	9-bit bus transceiver, non-inverting (3-state)	722
* 74F864	9-bit bus transceiver, inverting (3-state)	722
74F1240	Octal inverter buffer (3-state) (light load 74F240)	730
* 74F1241	Octal buffer (3-state) (light load 74F241)	730
74F1244	Octal buffer (3-State) (light load 74F244)	736
74F1245	Octal transceiver (3-State) (light load 74F245)	740
74F1604	Dual octal latch	745
74F1763	Intelligent DRAM controller (IDC)	750
74F1779	8-bit bidirectional binary counter (3-State)	762
74F2240	Octal inverter buffer with 30Ω equivalent output termination (3-state)	769
74F2241	Octal buffer with 30Ω equivalent output termination (3-state)	769
74F2244	Octal buffer with 30Ω equivalent output termination (3-State)	774
74F2245	Octal transceiver with 30Ω equivalent output termination (3-State)	778
74F2373	Octal transparent latch with 30Ω equivalent output termination (3-State)	783
74F2952	Octal registered transceiver, non-inverting (3–state)	788
74F2953	Octal registered transceiver, inverting (3–state)	788
74F3037	Quad 2-input NAND 30Ω driver	796
74F3038	Quad 2-input NAND 30Ω line driver (open collector)	800
74F3040	Dual 4-input NAND 30Ω line driver	804
74F3893	Quad Futurebus backplane transceiver	808
74F5074	Synchronizing dual D-type flip-flop/clock driver	814
74F5300	Fiber optic LED driver	821
74F5302	Fiber optic dual LED/clock driver	827
* 74F30240	Octal 30Ω line-driver with enable, inverting (open collector)	833
74F30244	Octal 30Ω line-driver with enable, non-inverting (open collector)	833
74F50109	Synchronizing dual J–K positive edge-triggered flip-flop with metastable immune characteristics	839
74F50728	Synchronizing cascaded dual positive edge-triggered D-type flip-flop	846
74F50729	Synchronizing dual D-type flip-flop with edge-triggered set and reset and metastable immune characteristics	853

** Discontinued part. Please see the Discontinued Products List.*

Section 3 – Application Notes

AN202	Testing and specifying FAST logic	863
AN203	Test fixtures for high speed logic	868
AN212	Package lead inductance considerations in high-speed applications	877
AN214	74F extended octal-plus family applications	883
AN215	74FXXXX "Light Load" input products	895
AN216	Arbitration in shared resource systems	901
AN217	Metastability tests for the 74F786 – 4-input asynchronous bus arbiter	906
AN219	A metastability primer	911
AN220	Synchronizing and clock driving solutions – using the 74F50XXX family	914
AN242	Skew definitions	917
AN2021	Thermal considerations for FAST logic products	918

Section 4 – Package Information

Soldering Information			928

Package Drawing No.	Description		
SO8:	plastic small outline package; 8 leads; body width 3.9mm	SOT96-1	931
DIP8:	plastic dual in-line package; 8 leads (300 mil)	SOT97-1	932
SO14:	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1	933
DIP14:	plastic dual in-line package; 14 leads (300 mil)	SOT27-1	934
SO16:	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1	935
SO16:	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1	936
DIP16:	plastic dual in-line package; 16 leads (300 mil)	SOT38-4	937
DIP20:	plastic dual in-line package; 20 leads (300 mil)	SOT146-1	938
SO20:	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1	939
SSOP20:	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1	940
PLCC20:	plastic leaded chip carrier; 20 leads	SOT380-1	941
SO24:	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1	942
DIP24:	plastic dual in-line package; 24 leads (300 mil)	SOT222-1	943
SSOP24:	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1	944
SO28:	plastic small outline package; 28 leads; body width 7.5mm	SOT136-1	945
DIP28:	plastic dual in-line package; 28 leads (600 mil); long body	SOT117-2	946
PLCC28:	plastic leaded chip carrier; 28 leads	SOT261-2	947
PLCC44:	plastic leaded chip carrier; 44 leads	SOT187-2	948
DIP48:	plastic dual in-line package; 48 leads (600 mil)	SOT240-1	949

Appendix A

Data Handbook Systems		952

Introduction

74F FAST TTL Product Description

Philips Semiconductors has combined advanced oxide-isolated fabrication techniques with standard TTL functions to create a family designed for use into the 3rd millenium. The high operating speeds of FAST can push system operating speeds into areas previously reserved for 10K ECL, but with simple TTL design rules and single 5V power supplies. Low input loading allows the user to mix LS, ALS, and HCMOS in the same system without the need for translators and restrictive fanout requirements.

FAST circuits are pin-for-pin replacements for 74S types. These circuits offer dissipation three to four times lower than the 74S types and higher operating speeds. Existing systems can achieve much lower power and improved performance by replacing the 74S types with the corresponding FAST devices.

The input structure provides better noise immunity because of higher thresholds, while the oxide-isolation and new circuit techniques create devices that have less variation with temperature or supply voltage than existing TTL logic families. Philips Semiconductors guarantees all AC parameters under realistic system conditions – across the supply voltage spread and the temperature range, and with 50pF output loads.

The use of high-capacitance PNP inputs has been avoided, and clamping diodes have been added to both the inputs and outputs to prevent negative overshoots. High input breakdown voltages allow unused inputs to be tied directly to V_{CC} without pull-up resistors.

Features

- 3ns Propagation delays
- 4mW/gate Power dissipation
- Guaranteed AC performance over temperature and extended V_{CC} range: 5V ±10%
- High impedance NPN base input structure on many types for reduced bus loading in LOW state (I_{IL} = 20μA)
- Standard TTL functions and pinouts
- Replacement for "S" types at 1/4 the power

Introduction

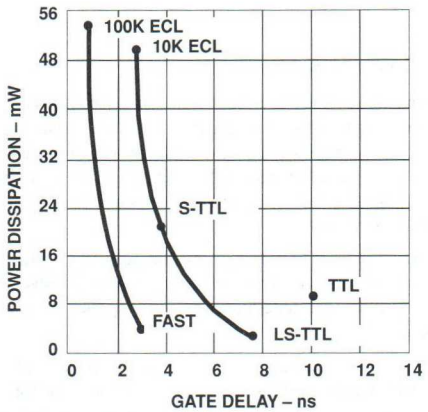


Figure 1. The Speed/Power Spectrum

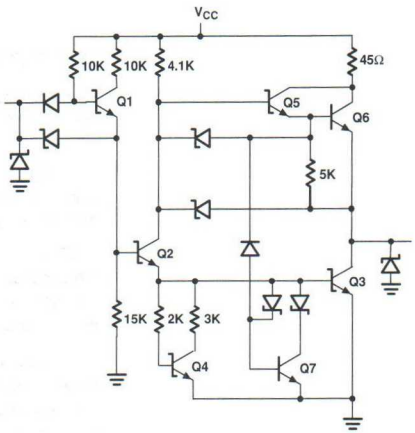


Figure 2. Basic FAST Gate

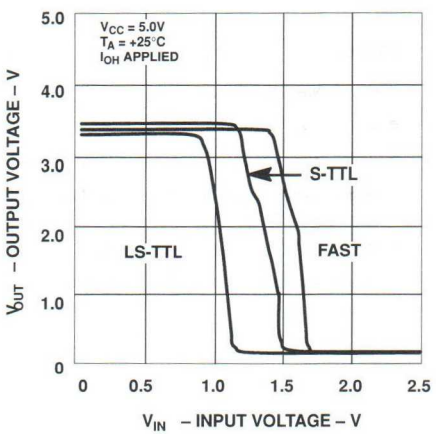


Figure 3. Transfer Functions at Room Temperature

Introduction

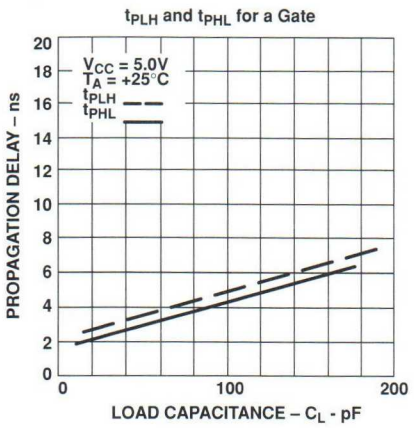


Figure 4. Propagation Delay vs. Load Capacitance (74F00)

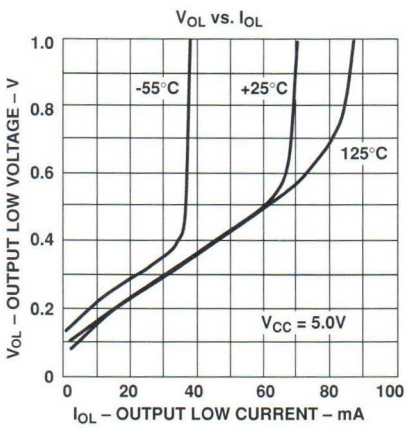


Figure 5. Output LOW Characteristics (74F00)

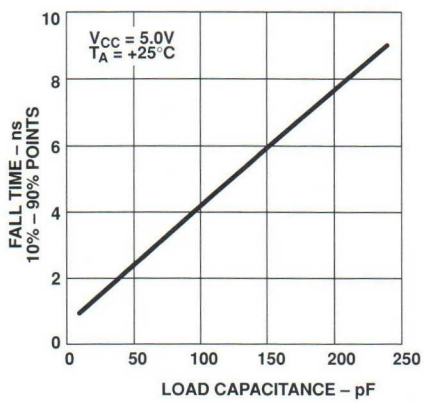


Figure 6. Fall Time vs. Load Capacitance (74F00)

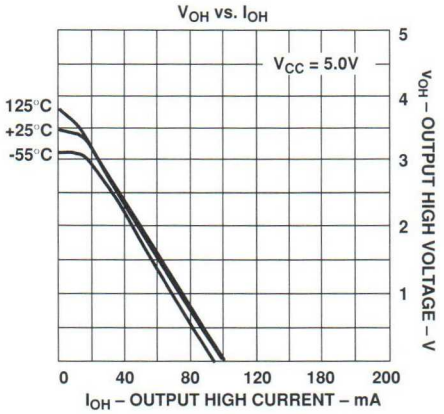


Figure 7. Output HIGH Characteristics (74F00)

TOTAL QUALITY MANAGEMENT

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is described in the following paragraphs.

Quality assurance

Based on ISO 9000 standards, customer standards such as Ford TQE and IBM MDQ. Our factories are certified to ISO 9000 by external inspectorates.

Partnerships with customers

PPM co-operations, design-in agreements, ship-to-stock, just-in-time and self-qualification programmes, and application support.

Partnerships with suppliers

Ship-to-stock, statistical process control and ISO 9000 audits.

Quality improvement programme

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

ADVANCED QUALITY PLANNING

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through Failure Mode Effects Analysis (FMEA) the critical parameters are detected and measures taken to ensure good performance on these parameters. This method is also used to evaluate the capability of process steps.

PRODUCT CONFORMANCE

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers.
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications.
- Periodic inspections to monitor and measure the conformance of products.

PRODUCT RELIABILITY

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, components reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the product reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action and continuous improvement.

CUSTOMER RESPONSES

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

RECOGNITION

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organizations.

DEVICE	NO. OF PINS	DESCRIPTION
74F00	14	Quad 2-Input NAND Gate
74F02	14	Quad 2-Input NOR Gate
74F04	14	Hex Inverter
74F06	14	Hex Inverter Buffer/Driver (OC)
74F06A	14	Hex Inverter Buffer/Driver (OC)
74F07	14	Hex Buffer/Driver (OC)
74F07A	14	Hex Buffer/Driver (OC)
74F08	14	Quad 2-Input AND Gate
74F10	14	Triple 3-Input NAND Gate
74F11	14	Triple 3-Input AND Gate
74F14	14	Hex Inverter Schmitt Trigger
74F20	14	Dual 4-Input NAND Gate
74F27	14	Triple 3-Input NOR Gate
74F30	14	8-Input NAND Gate
74F32	14	Quad 2-Input OR Gate
74F37	14	Quad 2-Input NAND Buffer (OC)
74F38	14	Quad 2-Input NAND Buffer
74F51	14	Dual 2-Wide 2-Input, 2-Wide 3-Input AND-OR-INVERT Gate
74F64	14	4-2-3-2 Input AND-OR-INVERT Gate
74F74	14	Dual D-Type Flip-Flop
74F85	16	4-Bit Magnitude Comparator
74F86	14	Quad 2-Input Exclusive-OR Gate (Industrial)
74F109	16	Dual $\overline{JK}$ Positive Edge Triggered Flip-Flop
74F112	16	Dual JK Negative Edge Triggered Flip-Flop
74F113	14	Dual JK Negative Edge Triggered Flip-Flop without Reset
74F125	14	Quad Buffer
74F126	14	Quad Buffer
74F132	16	Quad 2-Input NAND Schmitt Trigger
74F133	16	13-Input NAND Gate
74F138	16	1-of-8 Decoder/Demultiplexer
74F139	16	Dual 1-of-4 Decoder/Demultiplexer
74F148	16	8 Line to 3 Line Priority Encoder
74F151A	16	8-Input Multiplexer
74F153	16	Dual 4-Input Multiplexer
74F154	14	1-of-16 Decoder/Demultiplexer
74F157A	16	Quad 2-Input Data Selector/Multiplexer NINV
74F158A	16	Quad 2-Input Data Selector/Multiplexer INV
74F161A	16	4-Bit Binary Counter, Asynchronous Reset
74F163A	16	4-Bit Binary Counter, Synchronous Reset
74F164	14	8-Bit Serial/Parallel-In, Serial Out Shift Register
74F166	16	8-Bit Bidirectional Universal Shift Register
74F169	16	4-Bit Up/Down BCD Binary Synchronous Counter
74F173	16	Quad D Flip-Flop (3-State)
74F174	16	Hex D Flip-Flop with Master Reset
74F175A	16	Quad D Flip-Flop with Master Reset
74F189A	16	64-Bit Random Access Memory, INV (3-State)
74F191	16	Asynchronous Presettable Up/Down BCD Binary Counter
74F193	16	Up/Down BCD Binary Counter with Separate Up/Down Clocks
74F194	16	4-Bit Bidirectional Universal Shift Register

DEVICE	NO. OF PINS	DESCRIPTION
74F195A	16	4-Bit Parallel Access Shift Register
74F198	24	8-Bit Bidirectional Universal Shift Register
74F219A	16	64-Bit Random Access Memory, NINV (3-State)
74F225	20	16 × 5 Asynchronous FIFO (3-State)
74F240	20	Octal Inverter Buffer, INV (3-State)
74F240A	20	Octal Inverter Buffer, INV (3-State)
74F241	20	Octal Buffer, NINV (3-State)
74F241A	20	Octal Buffer, NINV (3-State)
74F242	14	Octal Bus Transceiver, INV (3-State)
74F243	14	Octal Bus Transceiver, NINV (3-State)
74F244	20	Octal Buffer, NINV (3-State)
74F244B	20	Octal Buffer, NINV (3-State)
74F245	20	Octal Transceiver (3-State)
74F253	16	Dual 4-Input Multiplexer
74F256	16	Dual Addressable Latch
74F257A	16	Quad 2-Line to 1-Line Selector/Multiplexer, NINV (3-State)
74F258A	16	Quad 2-Line to 1-Line Selector/Multiplexer, INV (3-State)
74F259	16	8-Bit Addressable Latch
74F260	14	Dual 5-Input NOR Gate
74F269	24	8-Bit Bidirectional Binary Counter (3-State)
74F273A	20	Octal D Flip-Flop
74F280B	14	9-Bit Odd/Even Parity Generator/Checker (Higher Speed 74F280A)
74F283	16	4-Bit Binary Adder with Fast Carry
74F298	16	Quad 2-Input Multiplexer with Storage
74F299	20	8-Bit Universal Shift/Storage Register (3-State)
74F365	16	Hex Buffer Driver (3-State)
74F367	16	Hex Buffer Driver (3-State)
74F373	20	Octal Transparent Latch (3-State)
74F374	20	Octal D Flip-Flop (3-State)
74F377A	20	Octal D Flip-Flop with Enable
74F378	16	Hex D Flip-Flop with Enable
74F379A	16	Quad D Flip-Flop with Enable
74F382	20	4-Bit Arithmetic Logic Unit
74F393	16	Dual 4-Bit Binary Ripple Counter
74F399	16	Quad 2-Port Register
74F456	24	Octal Buffer with Parity Generator Checker, NINV (3-State)
74F521	20	Octal Identity Comparator
74F524	20	8-Bit Register Comparator (OC + 3-State)
74F533	20	Octal Transparent Latch,, INV (3-State)
74F534	20	Octal D Flip-Flop, INV (3-State)
74F538	20	1-of-8 Decoder (3-State)
74F540	20	Octal Inverted Buffer (3-State) (Broadside Pin-out of 74F240)
74F541	20	Octal Buffer (3-State) (Broadside Pin-out of 74F244)
74F543	24	Octal Registered Transceiver, NINV (3-State)
74F544	24	Octal Registered Transceiver, INV (3-State)
74F545	20	Octal Bidirectional Transceiver with 3-State Inputs/Outputs, NINV
74F552	28	Octal Registered Transceiver with Parity and Status Flags, NINV (3-State)
74F564	20	Octal D Flip-Flop (3-State) (Broadside Pin-out of 74F534)
74F569	20	4-Bit Bidirectional Binary Synchronous Counter

DEVICE	NO. OF PINS	DESCRIPTION
74F573	20	Octal Transparent Latch (3-State) (Broadside Pin-out of 74F373)
74F574	20	Octal D Flip-Flop (3-State) (Broadside Pin-out of 74F374)
74F579	20	8-Bit Bidirectional Binary Counter (3-State)
74F595	16	8-Bit Shift Register with Output Latches (3-State)
74F597	16	8-Bit Shift Register with Input Latches
74F598	20	8-Bit Shift Register with Input Latches (3-State)
74F620	20	Octal Bus Transceiver, INV (3-State)
74F621	20	Octal Bus Transceiver, NINV (OC)
74F623	20	Octal Bus Transceiver, NINV (3-State)
74F640	20	Octal Bus Transceiver, INV (3-State)
74F641	20	Octal Bus Transceiver with Common Output Enable, NINV (OC)
74F642	24	Octal Bus Transceiver with Common Output Enable, INV (OC)
74F646A	24	Octal Bus Transceiver/Register, NINV (3-State)
74F647	24	Octal Bus Transceiver/Register, NINV (OC)
74F648A	24	Octal Bus Transceiver/Register, INV (3-State)
74F649	24	Octal Bus Transceiver/Register, INV (OC)
74F651A	24	Octal Bus Transceiver/Register, INV (3-State)
74F652A	24	Octal Bus Transceiver/Register, NINV (3-State)
74F656A	24	Octal Buffer/Driver with Parity, NINV (3-State)
74F657	24	Octal Transceiver with 8-Bit Parity Generator/Checker (3-State)
74F670	16	4 × 4 Register File
74F676	24	16-Bit Parallel-In, Serial-Out Shift Register (3-State)
74F711A	20	Quint 2-to-1 Data Selector Multiplexer (3-State)
74F711-1	20	Quint 2-to-1 Data Selector Multiplexer with 30Ω Series Termination Resistors
74F712A	24	Quint 3-to-1 Data Selector Multiplexer (3-State)
74F712-1	24	Quint 3-to-1 Data Selector Multiplexer with 30Ω Series Termination Resistors
74F723A	24	Quint 3-to-1 Data Selector Multiplexer (3-State)
74F723-1	24	Quint 3-to-1 Data Selector Multiplexer with 30Ω Series Termination Resistors
74F725A	24	Quint 4-to-1 Data Selector Multiplexer (3-State)
74F725-1	24	Quint 4-to-1 Data Selector Multiplexer with 30Ω Series Termination Resistors
74F756	20	Octal Inverter Buffer, INV (Open Collector 74F240)
74F757	20	Octal Buffer, NINV (Open Collector 74F241)
74F760	24	Octal Buffer, NINV (Open Collector 74F244)
74F776	28	Octal Bidirectional Latched Pi-Bus Transceiver (3-State + OC)
74F777	20	Triple Bidirectional Latched Bus Transceiver (3-State + OC)
74F779	16	8-Bit Bidirectional Counter (3-State)
74F786	16	4-Input Asynchronous Bus Arbiter
74F804	20	Hex 2-Input NAND Driver
74F805	24	Hex 2-Input NOR Driver
74F808	20	Hex 2-Input AND Driver
74F821	20	10-Bit Interface Register, NINV (3-State)
74F822	24	10-Bit Interface Register, INV (3-State)
74F823	24	9-Bit Interface Register, NINV (3-State)
74F824	24	9-Bit Interface Register, INV (3-State)
74F825	24	8-Bit Interface Register, NINV (3-State)
74F826	24	8-Bit Interface Register, INV (3-State)
74F827	24	10-Bit Buffer/Line Driver, NINV (3-State)
74F828	24	10-Bit Buffer/Line Driver, INV (3-State)
74F832	20	Hex 2-Input OR Driver

DEVICE	NO. OF PINS	DESCRIPTION
74F841	20	10-Bit Bus Interface Latch, NINV (3-State)
74F842	24	10-Bit Bus Interface Latch, INV (3-State)
74F843	24	9-Bit Bus Interface Latch, NINV (3-State)
74F844	24	9-Bit Bus Interface Latch, INV (3-State)
74F845	24	8-Bit Bus Interface Latch, NINV (3-State)
74F846	24	8-Bit Bus Interface Latch, INV (3-State)
74F861	24	10-Bit Bus Transceiver, NINV (3-State)
74F862	24	10-Bit Bus Transceiver, INV (3-State)
74F863	24	9-Bit Bus Transceiver, NINV (3-State)
74F864	24	9-Bit Bus Transceiver, INV (3-State)
74F1240	20	Octal Inverter Buffer (3-State), Light Load 74F240
74F1244	20	Octal Buffer (3-State), Light Load 74F244
74F1245	20	Octal Bus Transceiver (3-State), Light Load 74F245
74F1604	28	Dual Octal Latch
74F1763	48	1-MBit Intelligent DRAM Controller
74F1779	16	8-Bit Up/Down Counter, Common I/O (3-State), Extended Function of 74F779
74F1804	20	Hex 2-Input NAND Driver (Center Power Pin 74F804)
74F1805	20	Hex 2-Input NOR Driver (Center Power Pin 74F805)
74F1808	20	Hex 2-Input AND Driver (Center Power Pin 74F808)
74F1832	20	Hex 2-Input OR Driver (Center Power Pin 74F832)
74F2240	20	Octal Buffers
74F2241	20	Octal Buffers
74F2244	20	Octal Buffer with 30Ω Equivalent Output Termination (3-State)
74F2245	20	Octal Bus Transceiver (3-State), Light Load 74F245
74F2373	20	Octal transparent latch with 30Ω equivalent output termination (3-State)
74F2952	24	Octal Transceiver, NINV (3-State)
74F2953	24	Octal Transceiver, INV (3-State)
74F3037	16	Quad 2-Input 30Ω Line Drive, NINV
74F3038	16	Quad 2-Input 30Ω Line Drive, NINV (OC)
74F3040	16	Dual 4-Input 30Ω Line Drive, NINV
74F3893	20	Quad Futurebus Backplane Transceiver (3-State + OC)
74F5074	14	Synchronizing Dual D-Type Flip-Flop
74F5300	8	LED Driver
74F5302	14	Fiber Optic Dual LED/Clock Driver
74F30244	24	Octal 30Ω Transmission Line/Backplane Driver, NINV (OC)
74F50109	16	Synchronizing Dual D-Type Flip-Flop
74F50728	14	Synchronizing Cascaded Dual D-Type Flip-Flop
74F50729	16	Synchronizing Dual D-Type Flip-Flop with Edge Triggered Set & Reset

DISCONTINUED PRODUCTS

74F13
74F40
74F83
74F114
74F151
74F157
74F158
74F160A
74F162A
74F168
74F175
74F181
74F182
74F190
74F192
74F195
74F199
74F222
74F224
74F251
74F251A
74F257
74F258
74F273
74F322
74F323
74F350
74F352
74F353
74F366
74F368
74F377
74F379
74F381
74F385
74F395
74F398
74F410
74F412
74F432
74F455
74F533
74F537
74F539
74F547
74F548
74F563
74F568
74F582
74F583
74F588
74F604
74F605
74F622
74F642
74F646
74F648
74F653
74F654
74F655A
74F657A
74F674
74F732
74F733
74F755
74F764
74F764–1
74F765
74F765–1
74F807
74F835
74F844
74F861
74F862
74F864
74F881
74F882
74F899
74F1241
74F1242
74F1243
74F1760
74F1764
74F1764–1
74F1765
74F1765–1
74F1766
74F8960
74F8961
74F8962
74F8963
74F8965
74F8966
74F30240
74F30245
74F30640

GATES

FUNCTION		DEVICE NUMBER
Inverters	Hex Inverter Hex Inverter, Schmitt Trigger	74F04 74F14
NAND	Quad 2-Input Triple 3-Input Dual 4-Input 8-Input Quad 2-Input, Schmitt Trigger 13-Input	74F00 74F10 74F20 74F30 74F132 74F133
AND	Quad 2-Input Triple 3-Input	74F08 74F11
NOR	Quad 2-Input Triple 3-Input Dual 5-Input	74F02 74F27 74F260
OR	Quad 2-Input	74F32
Exclusive-OR	Quad 2-Input	74F86
Combination Gates	Dual 2-Wide 2-Input, 2-Wide 3-Input AND/OR-Invert 4-2-3-2 Input AND-OR	74F51 74F64

FLIP-FLOPS

FUNCTION	DEVICE NUMBER	CLOCK EDGE	SET	RESET	METASTABLE IMMUNITY
Dual D	74F74	↑	Low	Low	
Dual D	74F5074	↑	Low	Low	Yes
Dual D	74F50728	↑	Low	Low	Yes
Dual D	74F50729	↑	↑	↑	Yes
Dual JK	74F109	↑	Low	Low	
Dual JK	74F50109	↑	Low	Low	Yes
Dual JK	74F112	↓	Low	Low	
Dual JK	74F113	↓	Low	–	

MULTIPLE FLIP-FLOPS

FUNCTION	DEVICE NUMBER	CLOCK EDGE	RESET	OUTPUT
Quad D	74F173	↑	High	NINV
Quad D with Master Reset	74F175A	↑	Low	NINV INV
Quad D with Enable	74F379A	↑		NINV INV
Hex D with Master Reset	74F174	↑	Low	NINV
Hex D with Enable	74F378	↑		NINV
Octal D	74F273A	↑	Low	NINV
Octal D, 3-State	74F374	↑		NINV
Octal D, 3-State	74F534	↑		INV
Octal D with Enable	74F377A	↑		NINV
Octal D, 3-State	74F564	↑		INV
Octal D, 3-State	74F574	↑		NINV

OTHER REGISTERS, REGISTER FILES

FUNCTION	DEVICE NUMBER	CLOCK EDGE	PARALLEL ENTRY	BITS
Quad 2-Port, NINV	74F399	↑	2D (Mux)	4 × 2
Register File	74F670	↑	2D	4 × 4
10-Bit, NINV, 3-State	74F821	↑	2D	10
10-Bit, INV, 3-State	74F822	↑	2D	10
9-Bit, NINV, 3-State	74F823	↑	2D	9
9-Bit, INV, 3-State	74F824	↑	2D	9
8-Bit, NINV, 3-State	74F825	↑	2D	8
8-Bit, INV, 3-State	74F826	↑	2D	8

LATCHES

FUNCTION	DEVICE NUMBER	ENABLE LEVEL	RESET LEVEL	OUTPUT
Dual Addressable	74F256	1 (Low)	Low	NINV
Dual Octal	74F1604	1 (Low)		NINV
Octal Transparent, 3-State	74F373	1 (High)		NINV
Octal Transparent, 3-State (Broadside version of 74F373)	74F573	1 (High)		NINV
Octal Transparent with 30Ω Equivalent Output Termination, 3-State	74F2373	1 (High)		NINV
8-Bit Addressable	74F259	1 (Low)	Low	NINV
8-Bit Interface, 3-State	74F845	1 (High)	Low	NINV
8-Bit Interface, 3-State	74F846	1 (High)	Low	INV
9-Bit Interface, 3-State	74F843	1 (High)	Low	NINV
10-Bit Interface, 3-State	74F841	1 (High)		NINV
10-Bit Interface, 3-State	74F842	1 (High)		INV

MULTIPLEXERS

FUNCTION	DEVICE NUMBER	ENABLE LEVEL	SELECT INPUTS	OUTPUT
Dual 4-Input	74F153	2 (Low)	2 (High)	NINV
Dual 4-Input, 3-State	74F253		2 (High)	NINV
Quad 2-Input	74F157A	1 (Low)	1 (High)	NINV
Quad 2-Input	74F158A	1 (Low)	1 (High)	INV
Quad 2-Input, 3-State	74F257A		1 (High)	NINV
Quad 2-Input, 3-State	74F258A		1 (High)	INV
Quad 2-Input	74F298		1 (High)	NINV
Quad 3-Input	74F712A/712-1		2 (High)	NINV
Quad 3-Input	74F723A/723-1	1	2 (High)	INV Control
Quad 4-Input	74F725A/725-1		2 (High)	NINV
Quint 2-Input	74F711A/711-1		1 (High)	INV Control
8-Input	74F151A	1 (Low)	3 (High)	NINV, INV

DECODER/MULTIPLEXERS

FUNCTION	DEVICE NUMBER	ADDRESS INPUTS	ENABLE LEVEL	OUTPUT
Dual 1-of-4	74F139	2 + 2	1 (Low) + 1 (Low)	4 (Low) + 4 (Low)
1-of-8	74F138	3	2 (Low), 1 (High)	8 (Low)
1-of-8	74F538	3	2 (Low), 1 (High)	8 (High)
1-of-16	74F154	4	2 (Low)	16 (Low)

BUFFERS, DRIVERS AND TRANSCEIVERS

FUNCTION	DEVICE NUMBER	OUTPUT
Dual 4-Input NAND Transmission Line Driver	74F3040	INV
Quad 2-Input NAND Buffer	74F37	INV
Quad 2-Input NAND Buffer, OC	74F38	INV
Quad 2-Input NAND Transmission Line Driver	74F3037	INV
Quad 2-Input Transmission Line Driver	74F3038	INV
Quad Futurebus Backplane Transceiver, OC + 3-State	74F3893	INV
Hex Inverter Buffer/Driver, OC	74F06/A	INV
Hex Inverter Buffer/Driver, OC	74F07/A	NINV
Hex 2-Input NAND Driver, OC (Corner V_{CC} and GND)	74F804	INV
Hex 2-Input NAND Driver, OC (Corner V_{CC} and GND)	74F1804	INV
Hex 2-Input NOR Driver, OC (Corner V_{CC} and GND)	74F805	INV
Hex 2-Input NOR Driver, OC (Corner V_{CC} and GND)	74F1805	INV
Hex 2-Input AND Driver, OC (Corner V_{CC} and GND)	74F808	NINV
Hex 2-Input AND Driver, OC (Corner V_{CC} and GND)	74F1808	NINV
Hex 2-Input OR Driver, OC (Corner V_{CC} and GND)	74F832	NINV
Hex 2-Input OR Driver, OC (Corner V_{CC} and GND)	74F1832	NINV
Octal Inverter Buffer, OC	74F756	INV
Octal Buffer, OC	74F757	NINV
Octal Buffer, OC	74F760	NINV
Octal 30Ω Transmission Line/Backplane Driver, OC	74F30244	NINV
Octal Transceiver, OC	74F621	NINV
Octal Transceiver, OC	74F623	NINV
Octal Transceiver, OC	74F641	NINV
Octal Transceiver/Register, OC	74F647	NINV
Octal Transceiver/Register, OC	74F649	INV
Pi-Bus Transceiver (Octal Bidirectional Latched Transceiver), OC	74F776	NINV
Bus Transceiver (Triple Bidirectional Latched Transceiver), OC + 3-State	74F777	NINV

SHIFT REGISTERS

FUNCTION	DEVICE NUMBER	BITS	SERIAL ENTRY	PARALLEL ENTRY	CLOCK EDGE
Serial-In/Parallel-Out	74F164	8	D_{sa}, D_{sb}		↑
Serial-In/Parallel-Out Output Latch, 3-State	74F595	8	D_S		↑
Serial-In/Parallel-In/Serial-Out, Parallel-Out	74F195A	4	J, K	4D	↑
Serial-In/Parallel-In/Serial-Out, Parallel-Out	74F598	8	D_{s0}, D_{s1}	8 I/O	↑
Serial-In/Parallel-In/Serial-Out	74F676	16	SI	16D	↓
Serial-In/Parallel-In/Parallel-Out	74F194	4	D_{sr}, D_{sl}	4D	↑
Serial-In/Parallel-In/Serial-Out	74F166	8	D_S		↑
Serial-In/Parallel-In/Parallel-Out, Bidirectional	74F198	8	D_{sr}, D_{sl}	8D	↑
Serial-In/Parallel-In/Serial-Out, Parallel-Out, 3-State	74F299	8	D_{s0}, D_{s7}	8 I/O	↑
Parallel-In/Serial-Out, Input Latch	74F597	8	D_S	8D	↑
Parallel-In/Parallel-Out	74F399	8	S	I_{0a}–I_{0d}, I_{1a}–I_{1d}	↑

COUNTERS

FUNCTION	DEVICE NUMBER	MODULUS	PRESETTABLE	PARALLEL ENTRY	CLOCK EDGE
Synchronous (Asynchronous Reset)	74F161A	16	X	Synchronous	↑
Synchronous (Synchronous Reset)	74F163A	16	X	Synchronous	↑
Up/Down, Binary	74F169	16	X	Synchronous	↑
Up/Down, BCD Binary	74F191	16	X	Asynchronous	↑
Up/Down, BCD Binary	74F193	16	X	Asynchronous	↑
Bidirectional, Binary	74F269	256	X	Synchronous	↑
Up/Down, 3-State	74F569	16	X	Synchronous	↑
Up/Down	74F579	256	X	Synchronous (I/O)	↑
Up/Down, 3-State Multiplexed	74F779	256	X	Synchronous (I/O)	↑
Up/Down, 3-State Multiplexed	74F1779	256	X	Synchronous (I/O)	↑
Ripple Counter	74F393	10	X		↓

THREE-STATE BUFFERS, DRIVERS AND TRANSCEIVERS

FUNCTION	DEVICE NUMBER	OUTPUT
Quad Buffer	74F125	NINV
Quad Buffer	74F126	NINV
Quad Bus Transceiver	74F242	INV
Quad Bus Transceiver	74F243	NINV
Hex Buffer	74F365	NINV
Hex Buffer, 4-Bit and 2-Bit	74F367	NINV
Octal Buffer	74F240/240A	INV
Octal Buffer	74F241/241A	NINV
Octal Buffer	74F244/244B	NINV
Octal Buffer	74F1240	INV
Octal Buffer	74F1244	NINV
Octal Buffer with 30Ω Equivalent Output Termination, 3-State	74F2240	INV
Octal Buffer with 30Ω Equivalent Output Termination, 3-State	74F2241	NINV
Octal Buffer with 30Ω Equivalent Output Termination, 3-State	74F2244	NINV
Octal transceiver with 30Ω equivalent output termination, 3-State	74F2245	NINV
Octal Buffer with Parity	74F456	NINV
Octal Buffer with Parity	74F656A	NINV
Octal Driver	74F540	INV
Octal Driver	74F541	NINV
Octal Transceiver	74F245	NINV
Octal Transceiver	74F545	NINV
Octal Transceiver	74F620	INV
Octal Transceiver	74F640	INV
Octal Transceiver	74F1245	NINV
Octal Transceiver with Parity	74F657	NINV
Octal Transceiver/Register	74F646A	NINV
Octal Transceiver/Register	74F648A	INV
Octal Transceiver/Register	74F651A	INV
Octal Transceiver/Register	74F652A	NINV
10-Bit Buffer	74F827	NINV
10-Bit Buffer	74F828	INV
9-Bit Transceiver	74F863	NINV
Octal Registered Transceiver	74F543	NINV
Octal Registered Transceiver	74F544	INV
8-Bit Registered Transceiver	74F2952	NINV
8-Bit Registered Transceiver	74F2953	INV
Octal Registered Transceiver with Parity and Status Flags	74F552	NINV

PRIORITY ENCODERS

FUNCTION	DEVICE NUMBER	ENABLE LEVEL	INPUT/OUTPUT LEVEL
8-to-3	74F148	Low	Active Low

ARITHMETIC FUNCTIONS

FUNCTION	DEVICE NUMBER
4-Bit ALU with Overflow Output for Two's Complement	74F382
4-Bit Binary Full Adder with Fast Carry	74F283

COMPARATORS

FUNCTION	DEVICE NUMBER
4-Bit Identity Comparator	74F85
8-Bit Identity Comparator	74F521
8-Bit Register Comparator	74F524

PARITY

FUNCTION	DEVICE NUMBER
9-Bit Odd/Even Parity Generator/Checker	74F280B

SPECIAL FUNCTIONS

FUNCTION	DEVICE NUMBER
16 × 5 Asynchronous FIFO (3-State)	74F225
64-Bit RAM	74F189A/219A
4-Bit Asynchronous Bus Arbiter	74F786
1-MBit Intelligent DRAM Controller	74F1763
LED Driver	74F5300
Fiber Optic Dual LED/Clock Driver	74F5302

Circuit characteristics

INPUT STRUCTURES

There are three types of input structures used in FAST circuits: diffusion diode, PNP vertical transistor, and NPN transistor. Each of these are discussed below.

The diffusion diode input is most often used with FAST circuits. The input diode is labeled as D1 in Figure 1. There can be more than one if NAND logic is to be performed. In the oxide-isolated processes these are base-collector diffusions. Each input pin also has a Schottky clamp diode D2. This diode is standard for most TTL circuits, and is included to limit negative input voltage excursions that are generally the result of inductive undershoot.

The static diode input function of voltage versus current is shown in Figure 2. If the pin voltage is negative, most of the relatively high negative current flows through the clamp Schottky D2. At 0V the current flows from V_{CC} through R1 and D1 to the pin. Switching from a logic Low level to a logic High level occurs when the input pin voltage rises high enough to force the current from the D1 path to the Q3–Q2–Q1 path. This happens when the base voltage of transistor Q3 is at three base-emitter drops ($3V_{BE}$), and the pin is at $2V_{BE}$, which is the standard FAST threshold switching voltage. At this voltage the input current is very small, just the leakage currents of diodes D1, D3, and clamp diode D2. The current remains at this small, positive value until breakdown voltage is reached.

Transistor Q3 and resistor R2 provide a current gain by increasing the amount of current available to Q2 and Q1 when the pin voltage is high. R3 bleeds current off the base of Q2 to pull it low when the pin voltage is low. D3 speeds up this process during the High-to-Low pin transition. When the switching transients are over, D3 is reverse biased.

The current of Figure 2 is scaled for the case where the pin is required to pull down a single 10KΩ resistor R1 (20μA maximum in the High state and 0.6mA maximum in the Low state), which is defined as a standard FAST Unit Load (UL). For some parts, pin current can exceed a UL, especially in the logic Low state. This will happen if the pin must sink the current from more than one R1 resistor, or if the value of R1 is less than 10KΩ, which will be the case it the capacitance at the base of the transistor Q3 is too large for the required switching speed. In this event, the actual number of ULs is listed for each input in the specification sheet for the part. Note: UL, as defined here, is less than the normally defined Schottky TTL Unit Load. The correlation is one Schottky Unit Load – 1.67 ULs. This is an important point to remember for fan-in and fan-out calculations in systems that mix FAST with other TTL families.

The PNP vertical transistor has found wide acceptance in its various forms in low power Schottky logic because it provides a high-impedance input which is usually desirable. It was not used with early FAST circuits because the original oxide-isolated processes did not provide a fully suitable PNP vertical structure. It is now frequently the input of choice for new parts built with improved processes. The PNP transistor Q3 is fabricated with the P-type substrate as the grounded collector, the N-type Epi as the base, and the P-type normal base diffusion as the emitter. The process must be tailored to provide a suitable current gain for this vertical structure and must have provision to remove the considerable substrate current without an appreciable rise in substrate voltage. Referring to Figure 3, Q3 functions as an emitter follower for pin voltages low enough to provide an emitter-base forward bias. This occurs at an emitter voltage below the $3V_{BE}$ value provided by the D3–Q2–Q1 stack, and gives the desired $2V_{BE}$ pin threshold. At pin voltages above this value, Q3 turns off and the current through R1 is directed to Q2–Q1 through D3. The Schottky diode D2 speeds up the High to Low transition if the pin voltage falls more rapidly than the base of Q2; otherwise, D2 is off. The PNP input characteristics are shown in Figure 4. If the input voltage is negative with respect to ground, a large clamp current flows through D1. As the voltage rises, D1 turns off and the input current falls to the base current of Q3, for the usual values of R1, this is in the range of about I0μA. This decreases as the lead voltage rises. At threshold, Q3 turns off and the input current drops to a low value determined by the leakage of D1, D2, and Q3. The current remains at this low value until the onset of breakdown. Since all PNP inputs are protected with ESD structures, the breakdown current is set by this, and not the actual PNP device.

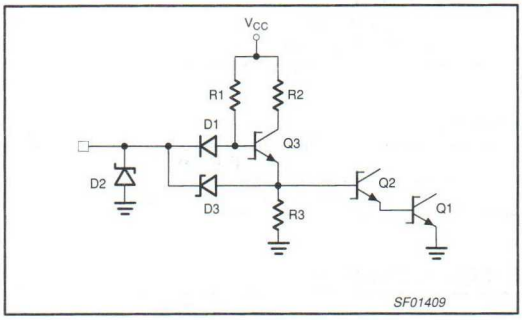


Figure 1. Diode input

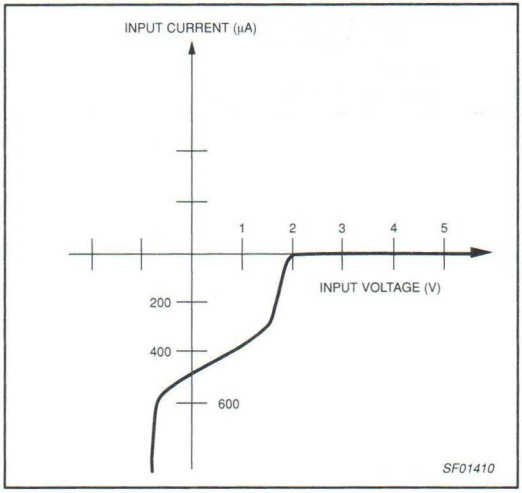


Figure 2. Static diode input function of voltage vs. Current

Circuit characteristics

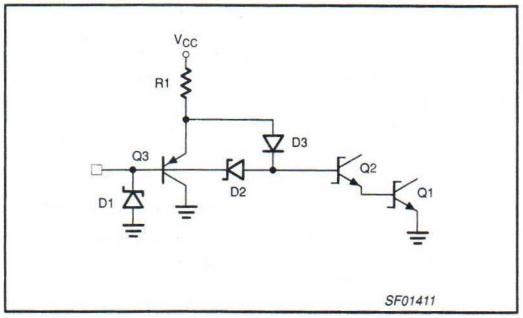


Figure 3. PNP input

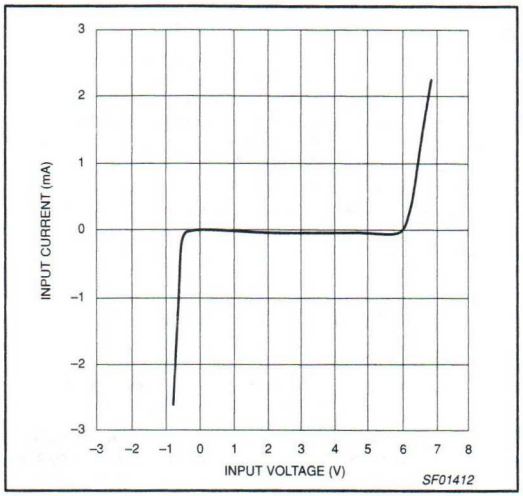


Figure 4. PNP input characteristics

The NPN input is shown with two variations in Figures 5 and 6. It has limited use in standard TTL circuits, and is used in selected FAST devices, especially where its superior high-impedance input characteristics are useful. A typical plot of static input current versus input voltage is shown in Figure 7.

There are some significant differences between this function and that of the diffusion diode input shown in Figure 2, the most important being the much lower input current in the region from 0V to threshold and the controlled increase of input current above V_{CC}.

When the pin voltage is negative, the large negative clamp current is supplied through the clamp Schottky diode D3. For positive voltages, from 0V to the switching threshold of $2V_{BE}$, Q1 is off, and the input current I_{IL} is very small, just the leakage current of Q1, D2, and D3 with low reverse bias. As the input voltage rises above $2V_{BE}$ Q1 turns on, and the current that had been flowing through D4 now flows through Q1, and the blocking Schottky diode D1. The value of this current is determined by the current source transistor Q2 with its base connected to voltage reference V_{CS}, and by the size of the emitter resistor R2. The current is nearly constant within the normal operating range of input voltages and has a typical value of 0.1 mA to 1.0mA. The pin must supply only a small fraction of this bias current, the ratio of Q1 collector current to base current being the bipolar β factor. Typically, I_{IH} base input current is less than 20μA in the voltage range from 0V to V_{CC}. This value is the specification for a standard FAST NPN Unit Load. When currents are greater than the UL are needed to reduce delay times or to provide for multiple-input transistors connected to the same input input, the specification sheet will identify those input pins which have NPN ULs greater than one, and will list their values.

In normal operation, the pin voltage will be limited in the negative direction by the diode clamp D3, and will be less than V_{CC} in the positive direction. The actual input voltage may exceed V_{CC} for three reasons: there may be inductive overshoot in badly terminated systems; the V_{CC} pin may be floating or grounded; or the input pin may be forced high by electrostatic discharge or incoming inspection testing.

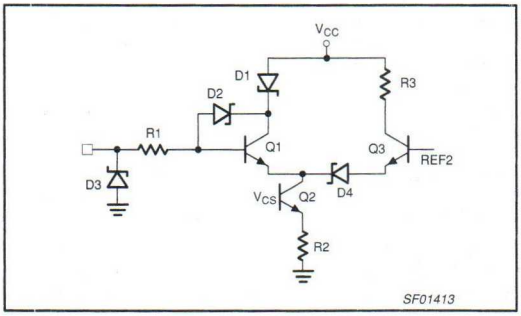


Figure 5. NPN input

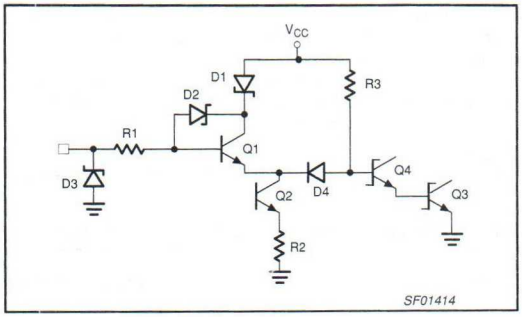


Figure 6. NPN input

Circuit characteristics

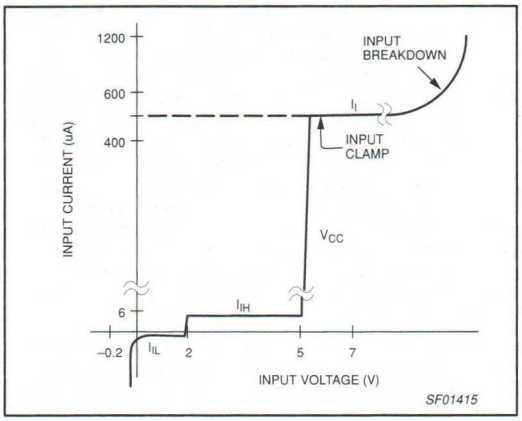


Figure 7. NPN input characteristics (not to scale)

For the inductive overshoot case, when the pin voltage exceeds V_{CC} part of the Q1 collector current begins to flow from the pin through limiting resistor R1 and Schottky diode D2. The current from V_{CC} through D1 decreases by exactly this amount, since Q2 is a constant current source. As the voltage continues to rise, D1 becomes reverse biased and prevents high currents flowing from the pin into V_{CC}. All the Q2 current flows into the pin through the R1–D2–Q1–Q2–R2 path to ground. As stated before, this current is typically small, in the range of 0.1 mA to 1.0 mA, and nearly independent of pin voltage, as shown by the I_I plateau in Figure 7. I_I provides a clamping action to ground for pin voltages in excess of V_{CC} which is usually desirable to reduce overshoot.

For the case where V_{CC} is grounded or floating, the input current is nearly zero for positive voltages between zero and approximately 7V. The conducting path through R1–D2–Q1 is available, but the current source Q2 will be shut off because, without V_{CC} drive, the Q2 base reference V_{CS} will be at 0V. This is the specified standard setup for incoming inspection. For the incoming inspection testing case where V_{CC} is connected to a 5V source, the response is shown in Figure 7. The current remains on the Q2-limited plateau until the pin voltage is high enough to cause non-destructive collector-emitter reach-through of Q2. At this point, input current increases as the pin voltage rises and R1 functions to limit this current and prevent damage to Q2.

The electrostatic discharge case is similar to the incoming inspection case except that Q2 may be off if the V_{CC} pad is floating, in which case it breaks down at a slightly higher voltage. The NPN input produces reach-through at a relatively low voltage compared with the diode input. The effect of this non-destructive reach-through is to greatly increase the ability of the device to survive electrostatic discharge. The discharge current is passed through the chip at a relatively low power dissipation, and this is shared by elements R1, D2, Q1, Q2 and R2, so that none of them dissipate enough power to do damage. By way of contrast, with a diode input, the clamp Schottky diode breaks down at high voltage with high dissipation in a localized area, and may suffer damage.

Another advantage of the NPN input is its ability to interface on the chip to either a conventional TTL interior design, or to the increasingly popular current-mode interior logic. The conventional TTL interface is shown in Figure 6. In this case the Q2 current source is designed to provide sufficient current to insure that in the Low state, with current flowing through the R3–D4–Q2 path, the base-emitter stack of Q3–Q4 is shut off. The $2V_{BE}$ input threshold is set by the forward drops of Q1, D4, Q4 and Q3.

The current-mode logic interface is shown in Figure 5. The output voltage is the drop across R3, and is referenced to V_{CC} (or some on-chip regulated voltage lower than V_{CC}) as is required for current-mode logic. For this case, voltage reference REF2 is normally fixed at $2V_{BE}$ + 1 Schottky drop to provide a pin threshold voltage of $2V_{BE}$. In fact, REF2 can be tailored to set the switching threshold voltage to any desirable level; it can be set to something other than an integral number of base emitter drops, or it can be designed to reduce the sometimes undesirable temperature variations of input threshold.

INPUT CONSIDERATIONS

Static Input Current

A comparison of input current for various input voltage ranges for each of the three types of inputs is shown in Table 1.

The majority of FAST devices available to date have diode inputs and supply current to their drivers that may be as large as 600μA at V_{IN} of 0.5V for a single unit load input. If a driver cannot sink the necessary current for a particular number of loads, the system designer must either add a buffer circuit designed to drive with higher current, or switch to devices that have high-impedance inputs. These are available on many Philips Semiconductors FAST designs, and are specified to have input current less than 20μA over the full switching range from 0V to V_{CC}. Typical input current for the NPN structure at room temperature is less than 1 μA below switching threshold voltage and 3μA above threshold. Typical PNP input current is less than 10μA below threshold voltage and 1 μA above threshold.

Table 1. Input current for input voltage ranges

INPUT VOLTAGE RANGE	INPUT CURRENT		
	DIODE	PNP	NPN
Below Ground	Schottky Clamp	Schottky Clamp	Schottky Clamp
Ground to V_T	High (to 600 μA)	Low (to 20 μA)	Leakage
V_T to V_{CC}	Leakage	Leakage	Low (to 20 μA)
Above V_{CC}	Leakage	Leakage	Clamp 100 to 1000 μA

Circuit characteristics

Input Capacitance

Input capacitance, measured using a small-signal variation about a static DC operating point, is usually the least for the NPN. When one includes the added capacitance of the elements common to each input, such as the pin, pad, bond wire, and clamp Schottky diode, the percentage difference for total static input capacitance for any of the three types of inputs is not very large.

Dynamic Input Current

In many applications the total current an input pin draws during a switching transition is a more important consideration than its input capacitance. This dynamic input current is often larger than the value of static capacitance would predict because each of the three types of input structure normally includes some sort of speed–up mechanism, usually a "kicker" Schottky diode, connected to an internal node of the circuit. The kickers deliver current, related in a non-linear way to input edge-rates. High-dynamic input current does not always equate to fast circuit switching. NPN inputs are usually faster than diode or PNP inputs, but in general have the lowest total dynamic current. The percentage differences for dynamic current tend to be larger than the respective differences for static capacitance.

Switching Threshold Voltage

The FAST input switching threshold voltage is set quite high for TTL at two base-emitter junction forward-bias drops. FAST input structures have enough gain that the voltage range in which they switch from one state to the other, as shown by a static DC transfer function curve, is completed within about 100 mV of the $2V_{BE}$ threshold. For a typical part at room temperature, V_{BE} is about 800mV, and the switching threshold is nominally at 1.6V; the static transfer range uncertainty of about 100mV gives a nominal threshold for solid Lows and Highs of about 1.55V and 1.65V respectively. The FAST threshold voltage was chosen higher than other TTL families to give a larger noise margin with respect to ground, and to be more nearly centered in the region where a FAST output driver stage switches with maximum edge rates, which occurs between about 0.6V and 2.6V.

Because the FAST threshold is set by the base-emitter junction voltage, it is dependent on junction temperature and current density. V_{BE} increases by about 1.2mV for each degree Celsius drop in junction temperature; current density changes by about a decade for a 60mV change in V_{BE}. The total variation due to processing differences, temperature, and current density is about 150mV per junction, or 300mV total change in input threshold to give limits of 1.25V Low and 1.95V High. The FAST V_{IL} and V_{IH} limits are 0.8V and 2.0V respectively, a tight spec for V_{IH}.

HYSTERESIS CONSIDERATIONS

Hysteresis has frequently been added to the inputs of TTL circuits in the past. The purpose is to increase noise immunity, which is accomplished by adjusting threshold voltages in a direction to reinforce an input level once a critical value has been reached. The procedure works well for slow circuits where the likelihood of slow, noisy inputs is high. It does not accomplish what is intended for FAST parts. There are several reasons: FAST threshold is already high and well centered so noise problems are automatically minimized. Inductive ground bounce, which is discussed at length later, causes problems with fast edge rates that completely swamp the typical benefits of hysteresis. It thus becomes a further complication in an already complicated picture and is more apt to hurt noise margins than to help. Because of this, the two major suppliers of FAST have eliminated hysteresis circuits except those specifically designed as Schmitt triggers, the 'FI3, 'FI4, and 'FI32.

ELECTROSTATIC DISCHARGE (ESD) CONSIDERATIONS

It is universally true that no bipolar integrated circuit process can provide devices with such high breakdown voltages that they are able to withstand ESD without some structure punching through or breaking down. The necessary condition for survival when this occurs is that the energy dissipation in any volume of the chip must be kept low enough so that neither the silicon nor the interconnecting metal can melt. This can be accomplished in two ways: the breakdown voltage should be as low as practical, consistent with normal circuit operation, and the energy should be dissipated in as large a volume as is possible. Circuit components that are particularly sensitive to charge damage must be protected by structures that are less fragile. All Philips Semiconductors FAST parts are designed with these requirements in mind, and although, as a rule of thumb, a sophisticated oxide-isolated process used to fabricate these parts tends to be more ESD damage-prone than a junction-isolated process, FAST is about as rugged as other TTL families in general. If FAST parts are handled with the same care afforded any other high-technology parts, they will not be damaged.

ESD sources usually fit into one of two categories: people or other objects that have accumulated static charge and touch the parts; or, they generate their own charge, as is the case when a circuit makes sliding contact with an insulator. In the first instance, static voltages tend to be high, over 10,000V, and discharge is usually limited by relatively high series resistance. In the second case, voltages are lower, around 200V, but there is very little series resistance to limit discharge current. Both possibilities are simulated with discharge models that are used in the majority of the test setups, and parts are designed in a way to improve survival for both ESD conditions.

Experience has shown that inputs of TTL circuits are much more likely to suffer ESD damage than outputs. Since negative voltages are discharged through clamp ground diodes with low chip dissipation, only voltages positive with respect to substrate ground are apt to produce input damage.

Circuits with diode inputs have a positive voltage breakdown in the relatively high range of from 15V to 25V. Schottky diodes connected to an input pin usually break down before junction diodes, and it they are stressed beyond their limits the Schottky diodes usually sustain damage in the corners. A diffusion guard-ring around the diode increases the uniformity of the breakdown, and as a result maximizes the dissipation volume at break-down and increases the ability of the device to survive ESD. All Philips Semiconductors FAST circuits have guard-rings on Schottky diodes that connect to input or output pins.

NPN inputs are designed to have low hold off voltage for positive voltages in excess of V_{CC}. Under static discharge the input structure forward biases, and the current-source transistor conducts the ESD current to substrate with a relatively low collector-emitter reach-through voltage. The input current for normal operation is low enough that a series limiting resistor can be added; this limits ESD current, especially for the case where the ESD source has no appreciable series resistance itself.

Circuit characteristics

As processes improve, it is often possible to improve ESD protection. Most new releases and many parts that have been recently redesigned onto new processes have specific ESD structures included which protect up to 2000V for the standard resistance limited case - the human body model.

FLOATING INPUTS

FAST inputs should not be allowed to float. All unused inputs, even those on unused gates, should be tied to a voltage source of relatively low impedance that will get them out of the logic picture and out of trouble. For a Low input this can be ground, or the output of a permanently low driver. For a High input this can be V_{CC}, protected by a series resistor if circuit damaging voltage spikes are possible in the system, or a permanently high driver.

Properly tied High or Low inputs will not pick up enough spurious noise to cause problems. If they are allowed to float, the results can be disastrous. Floating diode inputs usually pull to within a few Mv of $3V_{BE}$ above ground, a V_{BE} above threshold. The input voltage will fall about 1 V per 0.1 mA of current that is capacitively coupled from an adjacent Low-going pin. Since pin-to-pin input capacitance is in the order of one pF for an IC in a PC environment, an adjacent pin falling at 1.0V/ns couples in about 1.0mA of current, enough to switch the input to a Low state for as long as the current lasts. The normal FAST circuit response will be to switch or oscillate. The problem is even worse for high-impedance low-capacitance NPN or PNP inputs. In this case the static voltage to which they float is determined in part by leakage, and is not predictable.

To reiterate, FAST inputs must not be allowed to float. To do so is to invite serious system problems.

OUTPUT CONSIDERATIONS

The purpose of the output stage is to supply current to a load to force it to a High state or to sink current from the load to force it to a Low state. The speed at which the load can be switched from one state to the other depends on how much supply current or sink current is available from the output driver. There must be an amount in excess of that which is required to maintain the static load voltage, and it is the excess current that is available to charge or discharge the load capacitance. Most FAST circuits are designed to fit into one of those categories, based on output drive capability; the normal output stage, the buffer driver which can supply approximately twice as much current, and the high current drivers designed to drive low-impedance terminations.

Both normal drivers and buffers may be 3-State, which means that, in addition to Low and High states, they can be forced to a high-impedance OFF state as a third possible choice. This allows multiple components to be connected to a bus simultaneously, with only the single-selected device providing actual drive capability.

The basic components of an output stage are shown in Figure 8.

The pull-down drive-components sink load currents to force a Low state at the output pin; the pull-up driver components supply current to force a High state. The control components turn on the selected driver and turn off the nonselected driver in response to the logic input signal. For 3-State parts, the control components turn off both drivers if the 3-State control signal is active. The output Schottky clamp is included to suppress inductive undershoots, and is a part of every FAST circuit. The load requires a static current to keep it in either a logic High or Low state. The drivers must also charge and discharge the load capacitance C_L, which is generally one of the major factors that influence switching speed.

Since to a large extent, they function independently of each other, the pull-up driver, pull-down driver and control blocks are discussed independently.

PULL-UP DRIVERS

Open-Collector

The simplest pull-up driver consists of no more than a fixed pull-up resistor tied to V_{CC}. For this case, the control stage interacts only with the pull-down driver. In the Low state, this must sink the current from both the pull-up resistor and load. In the High state, the pull-up resistor must supply all of the load current. Most often, the pull-up resistor is not physically a part of the integrated circuit chip itself, but is added externally. In this case the only circuit element connected to the output pad (in addition to the ever-present Schottky clamp) is the collector of the pull-down driver transistor, hence the name "Open-Collector." Parts with this output stage can be tied together for bus applications. If any of the connected pull-down stages is active, it will pull the bus Low; only if all of them are off can the external resistor pull the bus High. This action provides a "wired" logical function that is free in the sense that no additional components are required to achieve it. Some Open-Collector FAST parts also have 3-State inputs that serve to disable output pull-down stages regardless of the action of the normal logic function.

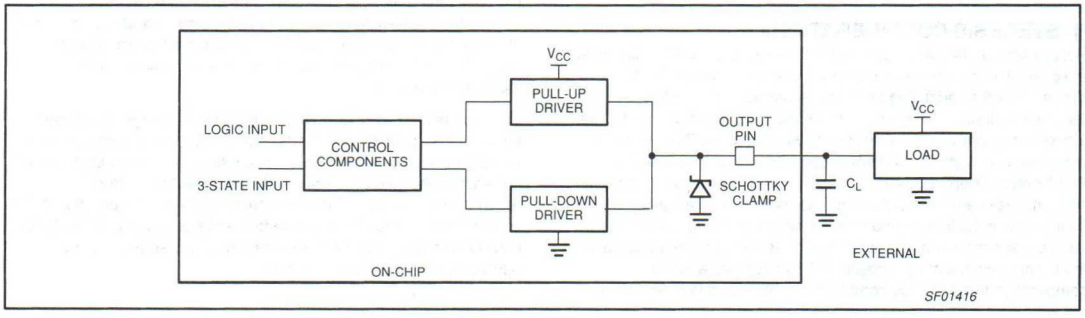


Figure 8. Output stage basic components

Circuit characteristics

The Open-Collector output voltage depends on the load, the value of the pull-up resistor, and the voltage to which this is connected. If the resistor value is Low, the output will rise to nearly the full value of the pull-up source voltage; in particular, the Open-Collector output can rise to V_{CC}, a voltage higher than that obtainable with a standard Darlington totem-pole pull-up.

High-drive Open-Collector parts are ideal as drivers for terminated transmission lines. In this application the line is terminated at the receiving end with a resistor network that provides the proper impedance and an equivalent source voltage of about 3V. The circuit pull-down drive sinks the termination current through the line at relatively low chip power dissipation when it is on. When it is turned off, the line pulls the output high, charging the stray capacitance from an impedance equal to the line characteristic impedance. Since the current is supplied by the line, the chip power dissipation falls. Very fast rise times approaching 1 ns can be obtained with this scheme. Rise times, in general, for open-collector outputs are determined by the R_c product of the pull-up resistor and the stray capacitance, and are limited only by the ability of the chip to pull the load Low.

Philips Semiconductors has a new family of parts designed specifically for driving heavy loads in terminated or unterminated environments. The majority of these are Open-Collector functions. They are discussed in detail later.

Standard Darlington

Most FAST pull-up drivers use dual transistors, connected as shown in Figure 9, with the emitter of the first device Q_b delivering current to the base of the driver Q_a. This configuration is called a Darlington Circuit and provides a composite current gain nearly as large as the product of the current gains of Q_b and Q_a.

The major advantage of the Darlington pull-up, as compared to the Open-Collector, is that the pin is actively pulled high by the emitter-follower action of Q_a which is capable of supplying large currents to quickly charge output capacitance. Despite the large output current that is available, the drive requirements of Q_b are low, so that the voltage drop across R_c is small, and the pad will pull up to a voltage nearly as high as $V_{CC} - 2V_{BE}$.

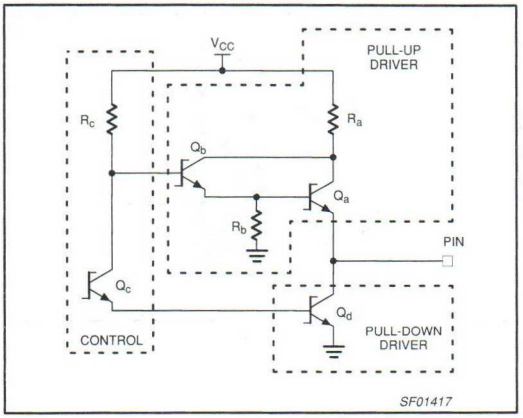


Figure 9. Basic Darlington pull-up

For the case where the output pin voltage is High, the phase-splitter transistor Q_c is off, and the base of Q_b is pulled high by resistor R_c. The current which flows through R_c is just sufficient to provide base drive to Q_b. The base voltage of Q_b will be just slightly below V_{CC}, and the output pin voltage will be less than this by the sum of the V_{BE} drops of Q_b and Q_a, both of which are on. Most of the base current for Q_a and the current through pull-down resistor R_b is supplied from V_{CC} through R_a and Q_b. Q_b has a Schottky clamp to prevent saturation when the current through R_a is large. Resistor R_a limits the amount of current flowing from V_{CC} through Q_a to a value small enough that Q_a will not be damaged if the output pin is accidentally grounded for a short period of time. This short circuit output current is called I_{OS}, and its value is approximately the maximum current available to charge the output capacitance at the beginning of a Low-to-High transition. The minimum current available when the pin has reached the minimum guaranteed high voltage V_{OH} is called output high current (I_{OH}) and is specified to be either 1mA or 3mA, depending on the type of driver. The maximum output voltage that the pull-up driver can achieve occurs at maximum V_{CC} and at high temperatures with corresponding low values of transistor V_{BE} and high current gain. Conversely, the minimum high voltage occurs at low V_{CC} and low temperatures.

In the Low state, the pull-down driver Q_d is on and the pin voltage is the Q_d saturation voltage V_{SAT}. Q_c is on and its collector resistor R_c is pulled down to $V_{BE} + V_{SAT}$; the V_{BE} of Q_d, V_{SAT} of Q_c. Q_b is also on, with its emitter at V_{SAT}, and the current through R_b is low. The base-emitter voltage of Q_a is nearly zero and Q_a is off.

The rate at which the pull-up driver can force a Low-to-High transition depends on a number of factors. The first, and obvious, consideration is that the control components must turn off the pull-down driver very quickly. During the short time that both pull-up and pull-down are on, there is a large feed-through current spike that is wasted as far as switching the load is concerned; it also increases chip power dissipation and produces undesirable voltage spikes in V_{CC} and ground. Assuming the pull-down is off, the Low-to-High transition speed is governed by: 1) the rate at which R_c can pull-up the base of Q_b; 2) the amount of pin current required to drive the load and charge the load capacitance; 3) the value of R_a; 4) the physical size and current gain of Q_a; and 5) the amount of Q_a base drive current that is lost through R_b to ground. The amount of R_b drive current lost can be reduced by connecting R_b to the output pin instead of ground, and this is done in a number of FAST parts. For this case, the static current through R_b with the pin high is less than if R_b is grounded, but switching feed-through current spike for a High-to-Low transition may be increased because R_b cannot effectively pull-down the base of Q_a until after the pin voltage falls.

The pin can be driven above its maximum high value by an external pull-up or by positive reflections from a transmission line. When this happens, Q_a and Q_b do not have sufficient base-emitter drive to keep them on. If the pin voltage rises significantly above V_{CC}, Q_a will begin to leak current into V_{CC}. For the case where R_b is tied to the pin instead of ground, the reverse transistor action of Q_a allows a high pin-to-V_{CC} current. This is not usually a problem in normal operation, but should be avoided in system applications where the V_{CC} pin may be intentionally grounded.

Circuit characteristics

3-State

For all 3-State FAST parts, the leakage paths to a grounded V_{CC} pin are blocked with Schottky diodes. A typical 3-State pull-up is shown in Figure 10. S_a is the series Schottky blocking diode. 3-State Schottkys S_{t1} and S_{t2} serve to simultaneously turn off the pull-up and pull-down drivers. The 3-State control is active when it is pulled low to within V_{SAT} of ground. In this state it sinks all the available drive current for Q_b and Q_c and pulls their bases down to (V_{SAT} + $V_{Schottky}$) which is essentially one V_{BE}. The voltage drop across R_c is large and 3-State power dissipation is typically high. Q_a and Q_b are off for normal TTL voltage ranges of the output pin; a negative undershoot large enough to drive the pin about one V_{BE} below ground will allow them to turn on and supply current from V_{CC}; this action aids the clamping Schottky diode in preventing the pin voltage from falling lower.

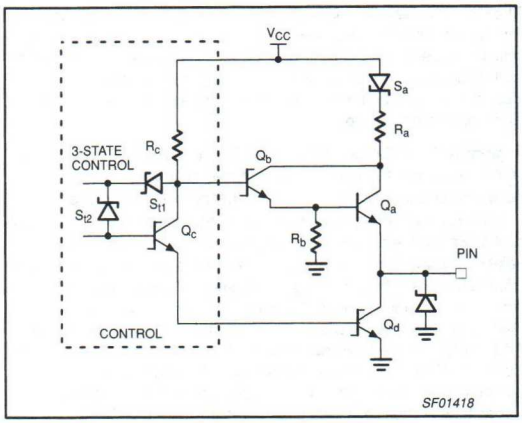


Figure 10. Basic 3-state pull-up

PULL-DOWN DRIVERS

The basic FAST pull-down driver is shown in Figure 11. Q_d is the pull-down driver transistor, a big Schottky-clamped device capable of sinking large currents. C_d is the stray base-collector capacitance of Q_d and its unavoidable presence has an important effect on the performance of the pull-down driver. Q_c is the Schottky-clamped phase splitter. It functions as a current-limited, low-impedance driver for Q_d when the logic input voltage V_{IN} is high, and as an inverting driver for pull-up Q_b by virtue of the current through R_c when V_{IN} is low and Q_c is off. Z_d is the pull-down impedance network which insures that Q_d is off when V_{IN} is low.

Switching to the logic Low state occurs when V_{IN} becomes greater than the V_{BE} drops of Q_c plus Q_d both of which are initially off. Part of the total emitter current available from Q_c comes from R_c which has a voltage drop of $V_{CC} - V_{BE} - V_{SAT}$. The remainder of the Q_c emitter current is supplied through its base Schottky clamp or by other components not shown in Figure 11 but discussed in the section on control components. A portion of the total Q_c emitter current is lost in the pull-down network Z_d; the remainder is available as base current for pull-down driver Q_d. The amount of current Q_d can sink depends on its base drive, its current gain, and its collector voltage. This current is specified on a per-part basis in the data sheets at output low voltage (V_{OL}) of 0.5V. The current which Q_d can sink in the switching range with the pin voltage at 2.5V is called available current (I_{AVL}) and is usually at least 70mA for FAST. The manner in which this current varies as the pin voltage decreases from 2.5V to V_{OL} is not specified as a FAST family parameter, since it is critically dependent on circuit design for a particular part, but is included as a specification for selected parts, especially those tailored to drive transmission lines. Several innovative circuit improvements that increase I_{AVL} by increasing the drive current for Q_d are shown in Figures 12 and 13. Speed-up Schottky diodes S_{s1} and S_{s2} have been added to the standard pull-down circuit as shown in Figure 12. Both are reverse-biased and off in the High state, since R_c pulls the collector of Q_c nearly to V_{CC}. Both connect the collector of Q_c to nodes that need to be discharged during a High-to-Low transition. S_{s1} to the base of Q_a, S_{s2} to the pin. They will conduct if these node voltages are higher than V_{BE} + V_{SAT} + $V_{Schottky}$, or approximately $2V_{BE}$. they are quite effective above $2V_{BE}$. Other networks are available which function down to lower voltages; these are especially useful for transmission line drivers. Figure 13 shows a dynamic kicker that gives an impulse of current which is especially useful in discharging high capacitive loads.

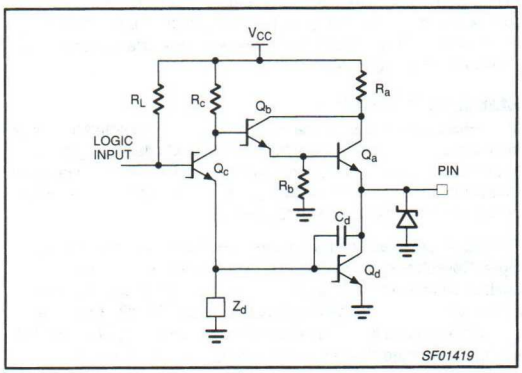


Figure 11. Basic FAST pull-down

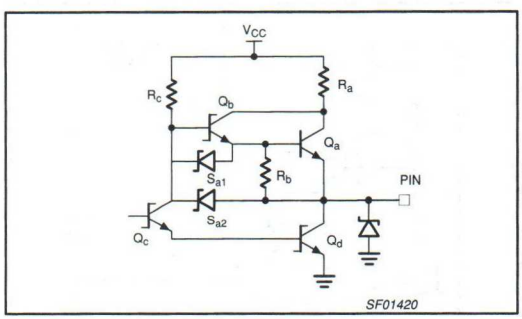


Figure 12.

Circuit characteristics

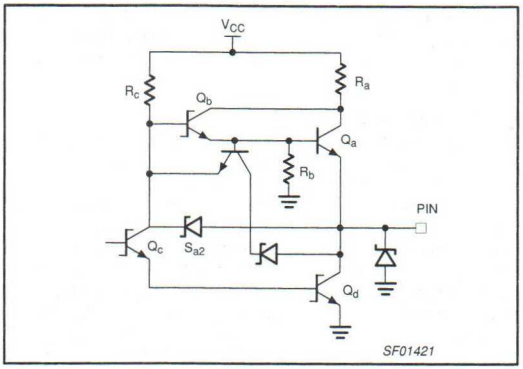


Figure 13.

The network of elements labeled Z_d in Figure 11 is the pull-down impedance which insures that Q_d is off when the value of V_{IN} falls below $2V_{BE}$. When the voltage at the base of Q_d is being pulled high by Q_c or low by Z_d, the output pin voltage responds by moving in the opposite direction. This produces a change in voltage across C_d, which is the sum of the base voltage change and the collector voltage change, so the amount of charge required by C_d is magnified by a factor which is larger than unity.

This well-known Miller-effect causes the apparent value of C_d, as perceived by the drivers, to be a factor of about five times larger than the already large physical junction capacitance, all of which means that the drivers Q_c and Z_d need to supply or sink much more current during an output transition than is necessary to maintain static conditions. When static conditions do exist internally in the circuit, noise voltage spikes on the output pin, V_{CC} or ground can momentarily force the base of Q_d in the direction to produce a serious output glitch, and the drivers must respond quickly to counter this coupled noise.

The simplest Z_d element is a resistor R_{z1} tied to ground, as shown in Figure 14. It will pull the base of Q_d all the way down to 0V if V_{IN} is less than one V_{BE}. This provides good immunity to coupled noise, but slows down the High-to-Low pad transition somewhat because the base of Q_d must rise a full V_{BE} before the output can begin to change. The value of R_{z1} needs to be relatively large to prevent a serious loss of base drive current when Q_d is on, which makes it easier to capacitively couple voltage spikes to the base of Q_d and, in part, nullifies the good noise immunity the full V_{BE} swing provides.

The addition of a series Schottky diode solves most of the problems. This is shown in Figure 15. The Q_d base voltage cannot pull below a Schottky drop, so the switching speed is unimpaired. The value of R_{z2} can be less than R_{z1} for the same current when the base is high, so the effect of coupled charge is less and the noise margin is acceptable.

The circuit of Figure 16 is standard with many TTL families. It pulls the base of Q_d down even less than does $R_{z2} - S_{d2}$, but it has a relatively high dynamic impedance and is somewhat noise sensitive. It has the advantage that it tends to "square up" the input voltage-to-output voltage transfer function, hence its popular name "squaring circuit." It is frequently used in simple gates where the shape of the transfer function may be important. For more complicated circuits, where there are one or more stages of logic with gain between input and output pins, the squaring ability is pretty much lost; in fact, it is likely that high-gain, multiple-logic level FAST circuits will oscillate if the input voltage is held near threshold for any length of time.

Figure 17 shows a popular dynamic circuit that is used in conjunction with a resistor or squaring circuit pull-down, and which insures that C_d cannot couple enough charge to the base of Q_d to slow down a Low-to-High transition. In operation, as the emitter of Q_b rises, charge is coupled through C_{Z4} into the base of Q_{Z4} which turns on and shunts the Miller current flowing through C_d to ground. When the transition is finished, the current through C_{Z4} stops and Q_{Z4} turns off. When the High to-Low transition of Q_b occurs, C_{Z4} discharges through S_{d4}. Because Q_{Z4} reduces the problems associated with Miller current, the circuit is called a "Miller Killer."

Figure 18 shows an active pull-down for the base of Q_d. The drive for Q_{Z5} (not shown) must be generated from the same signal that drives the base of Q_C. When Q_C is on, Q_{Z5} must be off, and when Q_C is off, Q_{Z5} turns on to hold the base of Q_d low. The impedance is very low, eliminating the capacitive-coupling noise problem.

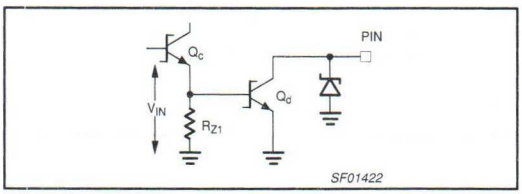


Figure 14.

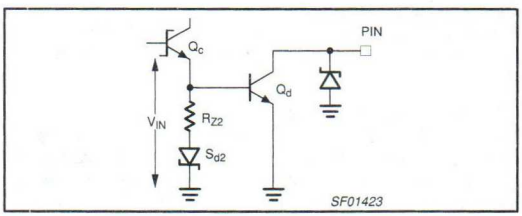


Figure 15.

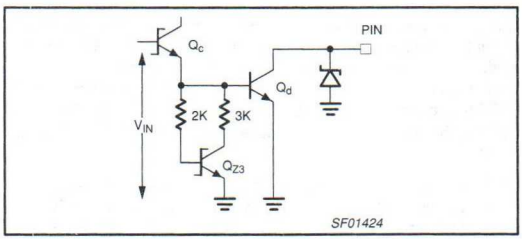


Figure 16.

Circuit characteristics

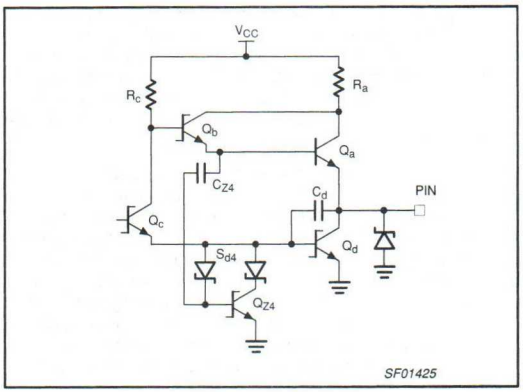


Figure 17.

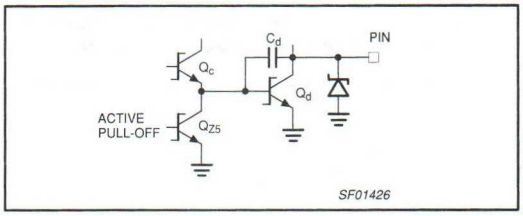


Figure 18.

CONTROL COMPONENTS

This section covers 3-State control drivers, special 3-State problems, and V_{CC} turn-on current and 3-State glitches during power-up.

3-State Control Drivers

The normal TTL 3-State scheme is shown in Figure 10. The 3-State control voltage in the OFF state is high enough that S_{t1} and S_{t2} are reverse-biased; in the active state the control voltage is low, usually V_{SAT}, so that the Q_a–Q_b base emitter stack is off, as is the Q_c–Q_d stack. In the 3-State mode, R_c is dissipating maximum power. Blocking Schottky diode S_a prevents current from flowing backwards through Q_a if the V_{CC} pin is grounded; the output pin high voltage can be about 4.5V before there is any significant 3-State leakage current. The only exception to this general rule with FAST is for the diode input transceiver function, where the same pin acts as an input or an output. In this case, the pin supplies one or more normal FAST unit loads of current if it is Low, and tends to pull to $2V_{BE}$ if it is floating. NPN and PNP input transceivers have normal low 3-State leakage.

There are several innovative improvements to the basic 3-State circuit, as shown in Figure 19. The addition of inverter Q_{c2} – R_{C2} with a blocking Schottky S_{C2} allows the addition of feedback diodes S_{S1} and S_{S2} to increase I_{AVL}; S_{C2} cannot be included in series with R_{c1}, because its forward voltage drop would lower V_{OH}. 3-State power is not increased, since only one R_{c1} is pulled low. The current through Q_{c2} is available as added base drive to Q_d. So nothing is wasted. An additional transistor may be paralleled with Q_{c1} and Q_{c2} to control an active pull-down version of impedance Z_d which, discussed in a previous section, eliminates the Miller turn-on problem.

I_{CC} Considerations

There is no formal family specification that limits the amount of V_{CC} current a FAST circuit may draw during turn-on as V_{CC} rises from zero to 4.5V. However, for most now designs, and especially for circuits that have high I_{CC} requirements, an effort has been made to limit maximum turn-on I_{CC} to 110% of I_{CCmax}. This precaution prevents an undesirable system situation where the V_{CC} power supply is large enough to drive the devices, but can't power them up. The major component of turn-on current is V_{CC} to ground feed-through of output stages. Unless specific steps are taken to prevent it, the pull-up Darlington turns on if V_{CC} is greater than $2V_{BE}$, and remains on until the on-chip voltage is high enough to set the phase splitter solidly in one or the other of its two states. The solution is to incorporate extra circuit components that will set the phase splitter at voltages nearly as low as $2V_{BE}$, or turn off the top device with a separate 3-State type structure which activates at low V_{CC} voltages and becomes inoperative when V_{CC} is high.

The amount of current that can be fed from an output pin back into a grounded V_{CC} pin, or through the chip to ground for an open V_{CC} pin, depends on the design. Generally, 3-State feedback current is specifically limited to low values which are leakage or break-down related. Other parts have medium to high current. Those with Darlington pull-downs connected to the output pin conduct the most.

Some 3-State parts, especially selected buffer functions, have additional circuit elements to insure that, as they power on, they source or sink no appreciable output current, provided the 3-State control pins are in the active state as V_{CC} rises. This means that V_{CC} can be turned on or off at will in the system to conserve power, and bus voltages will not be affected. Parts with this capability are identified in the specific data sheets.

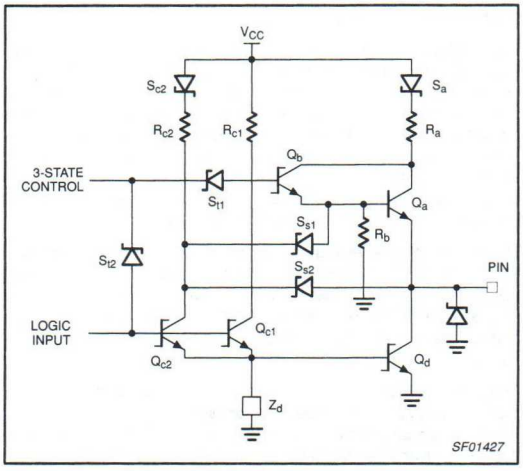


Figure 19. Improved 3-state circuit

Circuit characteristics

GROUND VOLTAGE AND OTHER NOISE PROBLEMS

Ground Voltage As a Serious Problem

Excessive ground noise voltage in a system usually produces serious degradation of switching speed. It may also produce unwanted glitches on outputs, or spurious clocks which cause flip-flops to lose data, or relaxation oscillations that completely disrupt a system. It is, without doubt, one of the major causes of logic systems failure . . . difficult to accommodate, and difficult to eliminate.

The problem is not unique with FAST, but is greatly aggravated by the high transition rates and large currents for which FAST is designed. Because of this, FAST can optimally replace other TTL families only in systems that have been carefully designed at the PC board level. Well planned layout is vital, and multi-layer boards with ground and V_{CC} planes are often necessary. Great care must be taken to insure adequate bypassing for V_{CC}. The problems are not trivial, but they can be solved satisfactorily to yield systems whose performance is not exceeded in the TTL world.

Sources of Ground Noise

Ground lead inductance is the source of most ground noise voltage; it causes a voltage drop proportional to the rate at which the current through it changes.

Inductance is a measure of the amount of energy stored in the magnetic field associated with a current. Low values of inductance imply low energy, which means low voltage required to affect a change in current. As a general rule, inductance decreases as current is allowed to spread out in space, and current interactions decrease. The inductance of a thin wire far removed from the return current path is high; that of a large conductor coaxially encircled by the return path is low. Inductance tends to increase faster than linearly with conductor length, but only approximately logarithmically with decreasing cross-section dimensions. From a logic system viewpoint, ground planes are better than ground traces; wide lines are better than narrow lines; close spacing to planes is good; loops that allow magnetic flux linkages are bad; wire lengths of fractions of inches count; and sockets with long pins add significant inductance to a PC Card.

Ground noise voltage is increased by feed-through current spikes. These occur when both top and bottom devices of the output totem-pole driver are on simultaneously, and heavy currents are allowed to flow directly from V_{CC} to ground. They can be minimized in one of two ways: drive the devices such that one is turned off before the other can turn on, or more commonly, drive them together, but very fast, so the feed-through current can flow for only a short time.

Although most ground noise results from ground inductance, resistance also contributes. Static ground offsets unrelated to rates of current change occur, and add to the total ground voltage. Generally speaking, those measures which reduce ground inductance also reduce ground resistance.

Estimating The Magnitude of Ground Noise

The accurate modeling of ground noise related problems in logic design is a complex procedure that requires numerical analysis to determine system currents and voltages as a function of time. This can only be accomplished in a satisfactory manner if one has reasonable electrical models, especially for input stages and output drivers of the integrated circuits used in the system. These data are available on request for many of the FAST logic functions. Philips Semiconductors is prepared to assist customers in solving the sometimes formidable problems associated with large system simulation.

The following discussion derives the minimum peak-value of ground noise that will occur as an integrated circuit discharges a capacitor through ground lead inductance. It points out the minimum problems that will exist. In the real world, the peak ground voltage will always be larger than the simple derivation predicts.

The load capacitor C and its discharge path are shown in Figure 20. The capacitor has been previously charged to a positive voltage, and is discharging through pull-down transistor Q_d and lead ground inductance L_g. As the current changes, it develops a ground voltage V_g across L_g that is equal to the product of L_g times the rate at which it changes.

The discharge current I_d will vary with time: starting from zero, it will increase to a maximum value, and then eventually return to zero. There are an infinite number of ways I_d can vary, depending on how the transistor allows charge to flow at any instant in time, but each of the possible current-versus-time discharge curves must define the same area, equal in value to the total charge Q that is removed from the capacitor as its voltage falls by an amount V.

The voltage drop V_g across the inductor at any instant in time will be determined by the slope of the current-versus-time curve, that is, by the rate at which current is changing. The unique curve that has the required area and minimum slope is triangular, as shown in Figure 21. The ground voltage for this case is a square wave as shown in Figure 22. It will be positive while the current is increasing, and negative when the current is decreasing.

The equations of interest in estimating V_g are:

Charge = Q = CV = $I_{MAX}\ T/2$ = triangle area

$$\text{Ground voltage} = V_g = (\text{triangle slope})\ (L) = \frac{2\ I_{MAX}\ L}{T}$$

Combining the two equations to eliminate I_{MAX} gives:

$$V_g = \frac{4CVL}{T^2}$$

This lower limit of peak ground voltage will always be exceeded in the real world, where ground voltages are usually spikes, not square waves. If a spike is large enough and long enough, the chip will erroneously recognize it as a valid input, and respond either by glitching, slowing down, clocking incorrectly, or oscillating.

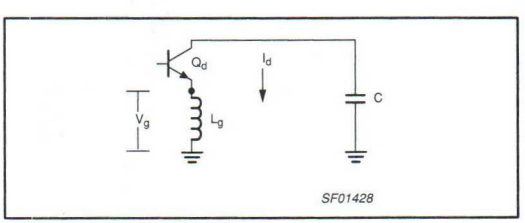


Figure 20.

Circuit characteristics

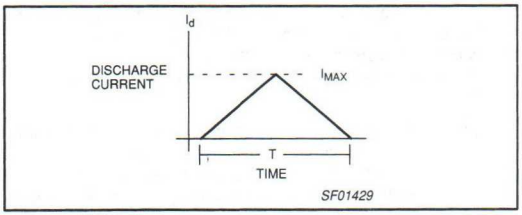


Figure 21.

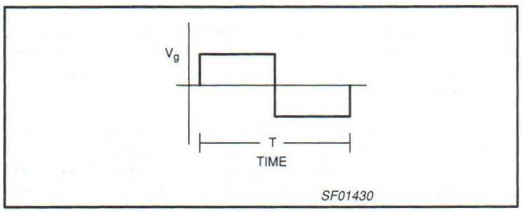


Figure 22.

An example using values typical for a FAST circuit in a 16-pin DIP illustrates the potential for trouble. If the circuit discharges one standard FAST load of 50pF in 2ns with a voltage change of 3V through a ground inductance of 10nH, the minimum ground voltage will be:

$$V_g = \frac{4 \times 50 \times 10^{-12} \times 3 \times 10 \times 10^{-9}}{(2 \times 10^{-9})^2} = 1.5V$$

This value is high, and suggests that if transition times are not to be seriously degraded, inductances must be kept as small as possible, and loads must be minimized.

Effects of Ground Noise on Input Stages

FAST TTL input voltages are referenced to system ground as illustrated in Figure 23 which shows an equivalent input and output stage. The equivalent input circuit is represented by R_{IN} and the four diodes D1 through D4. These components establish an input switching threshold voltage of $2V_{BE}$ relative to chip ground. The on-chip voltage V_{IN} must be different from this value by a margin large enough to guarantee a static Low or High with sufficient overdrive to insure switching speed. The on-chip voltage V_{IN} that is actually available is the difference between the input pin voltage V_{PIN} and the total ground voltage noise V_g. V_g is the sum of the steady state voltage due to ground current flowing through R_g, and the inductive voltage drop across L_g. The inductive voltage is usually the larger of the two, and since it depends on current changes, it will have both positive and negative polarities for each switching cycle. This means that either Low or High input voltages which are too close to switching threshold will allow the noise margin to be exceeded, and if the ground voltage noise persists long enough, the input will switch erroneously. The result of this depends on the chip function. Combinatorial logic usually slows down or produces output glitches. Latches and flip-flops may be clocked inadvertently, and stored data will be lost. Complex circuits that have multiple outputs may oscillate, particularly if one polarity of ground noise results in a rapid change of ground current that produces the opposite polarity ground noise.

Ground noise adds a dimension of difficulty in measuring input threshold voltage. FAST parts are guaranteed to have input thresholds between the limits 0.6V and 2.0V. A typical method of verifying this is to determine the voltage at which the input actually switches. This requires some care, since the true threshold voltage is masked by any noise voltage contributed by the test system or ground inductance. For accurate results, the input pin voltage should approach the switching threshold slowly and smoothly. At threshold the input will switch. Sensing this point is easy for those circuits where an output also switches, glitches, or oscillates. It is much harder to sense this point for those circuits where an input change produces no output change, for example, with flip-flops which change state only when clocked. The input switch point for these devices can be inferred by measuring the input current as a function of input voltage. Clocking the part may produce enough ground noise to distort the measurement, even if the output doesn't switch.

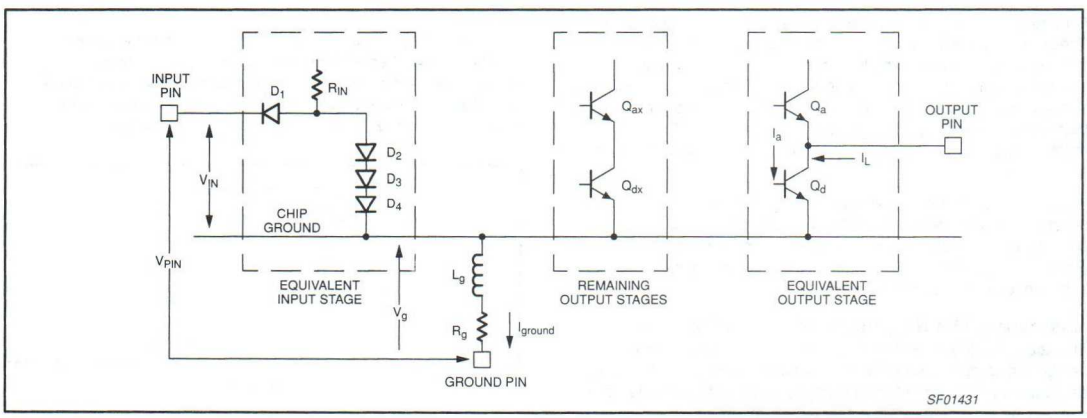


Figure 23. Equivalent input and output stage

Circuit characteristics

Effects of Ground Noise on Output Stages

The most obvious effect that ground noise has on output stages is to directly change the voltage available to force discharge current through the pull-down device. If the only source of ground voltage is from the particular output of interest, the ground and output pin inductances will always slow down a High-to-Low transition. They produce a voltage in opposition to the output pin voltage at the beginning of the discharge when currents tend to be high and voltage changes rapidly. As discharge continues, the available drive decreases, and currents increase less rapidly. Eventually the current begins to fall, and the ground voltage reverses polarity, which tends to limit the rate at which the current decreases. It currents have been high, and the inductances are large, there may be substantial undershoot at the end of the switching cycle which can drive the output pin below ground.

If multiple outputs are switching simultaneously, the total ground noise needs to be considered to determine the result for a particular output. For this case, it can happen that ground noise will, in fact, speed up an output; on the other hand, it may introduce delays that are much larger than those possible with single output switching. This behavior makes it difficult to predict, except on a case by case basis, what the actual effects of multiple output switching will be. Curves of delay versus multiple switching have been published, but these serve only as rough guides to indicate potential problems, and need to be backed up with actual analysis for any particular application.

In addition to the direct influence on discharge voltage, excessive ground noise can affect the operation of the control components, and alter both rise and fall times by driving pull up or pull-down stages incorrectly, One example of this can be understood with reference to Figure 24. The scenario is that the output pin is Low, but on the verge of switching High, with V_{IN} falling and Q_c ready to turn off. A problem occurs if, at the instant before the pull-up transistor Q_a, turns on to pull the output pin high, the voltage from output pin to chip ground falls. This can happen as a result of inductive undershoot driving the output pin down, or by a rise in ground voltage caused by currents completely unrelated to the output of interest. The low output-pin-to-chip-ground voltage pulls down the emitter of Q_a through Schottky clamp diode S_d, and if V_{IN} is not low enough to counteract this, Q_c will not turn off. The net result is that the collector of Q_c cannot rise, and the transition is delayed until the noise voltage from output to ground disappears.

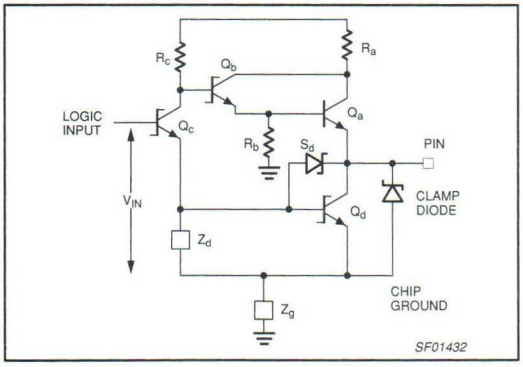


Figure 24.

V_{CC} Noise As an Additional Problem

Inductance in the V_{CC} lead produces noise in the on-chip V_{CC} voltage that is entirely analogous to ground voltage. The effects of V_{CC} noise can be nearly as harmful as those produced by ground noise, the only significant difference being the fact that TTL input voltages are referenced to ground instead of V_{CC}. If multiple outputs are switching simultaneously, the total ground noise needs to be considered to determine the result for a particular output. For this case, it can happen that ground noise will, in fact, speed up an output; on the other hand, it may introduce delays that are much larger than those possible with single output switching. This behavior makes it difficult to predict, except on a case by case basis, what the actual effects of multiple output switching will be. Curves of delay versus multiple switching have been published, but these serve only as rough guides to indicate potential problems, and need to be backed up with actual analysis for any particular application.

The first symptom of excessive V_{CC} inductive voltage drop is a change in the edge rate for a Low-to-High transition. This will decrease if the on-chip V_{CC} falls, and increase if it rises. If the ground to V_{CC} voltage falls below a minimum value, internal circuit delays or glitches can occur, and functions with flip -flops or other storage elements may lose data. As is the case with excessive ground noise, FAST circuits may break into relaxation oscillation.

Because V_{CC} to ground voltage must remain above a minimum value to avoid logic errors and glitches, it is absolutely vital that V_{CC} to ground bypassing is adequate. This requires low inductance V_{CC} and ground PC traces, and low inductance bypass capacitors. FAST parts are guaranteed to function property for low V_{CC} of 4.5V. This means that pin voltages must not fall below this value for any appreciable time: fractions of nanoseconds. V_{CC} system voltage should be close to the maximum guaranteed value for safe system design.

Designing To Reduce the Effects of Ground Noise

The typical 1.5V minimum value for ground noise, calculated in the preceding example, points out the possibility of noise-related problems when only one standard 50pF load is being driven by an output stage.

Simultaneous switching of more than one such load obviously increases the risk of trouble, and raises the question of how an octal part can work at all. Fortunately, the real world, with careful PC layout, is not usually so grim.

The standard 50pF load is a lot of capacitance, chosen so one can estimate the chip response for a single output switching under conditions that approach worst case. On a modem PC board a wire trace that has 50pF stray capacitance is several feet long and looks like a resistive delay line instead of a lumped capacitor.

Traces on a PC card must be short to behave like lumped capacitance for an output stage. For this case, a major contributor to driver current is the load presented by the input stages of the driven circuits, and the associated stray capacitance as previously mentioned, the input current for FAST parts is related to edge rates, and is generally larger than the measured static value of input capacitance would predict. Because of this, the useful fan-out of FAST circuits may be more dependent on ground noise of drivers with heavy capacitive loads than on the amount of current available to a static DC load, which is the guaranteed data sheet value.

Circuit characteristics

Most of Philips Semiconductors' FAST parts are available in surface mount packages, and these have lower ground inductance than the standard DIP parts.

Inductance of output signal pins reduces the rate at which associated ground current can change, and this reduces ground noise voltage without a corresponding reduction of static output voltage. This inductance may be intentionally increased by adding trace length on the PC board; one needs to be careful, and anticipate the increase in output ringing during switching transitions

In summary, there are many potential problems that one can anticipate in logic systems with fast edge rates. Some of these are dependent on the available components and their respective packages, and the system designer must be certain that the demands made of them are not more than they can handle. A second major consideration is the system layout, especially from the standpoint of ground, V_{CC}, and signal lead inductance. If one is careful with PC design and layout, and chooses components wisely, FAST systems deliver performance second to none in the TTL world.

Heavy Current Drivers

Philips Semiconductors has a new family of parts defined that are capable of driving currents much larger than those achieved with standard FAST parts.

The parts presently available are:

F3037	Quad 2-input NAND
F3038	Quad 2-input NAND, Open-Collector
F3040	Dual 4-input NAND
F30240	Octal Line Driver, Open-Collector
F30244	Octal Line Driver, Open-Collector
F30245	Octal Transceiver, Open-Collector
F30640	Octal Transceiver, Open-Collector

Others are in the planning stage.

The drivers are husky enough to assure incident wave-switching driving transmission lines with impedance levels as low as 30Ω. They are the best choice available for applications that need the ultimate in speed and drive capability.

All the parts use multiple center ground and V_{CC} pins. Special precautions have been taken to insure minimum feed-through current during switching, and this, coupled with the low V_{CC} and ground inductance, results in minimum V_{CC} and ground noise, and allows maximum edge-rate and speed.

The parts are available in several different packages, including ceramic. Because the power dissipation is application dependent, the user needs to choose a package and an environment carefully to be sure the maximum temperature ratings are not exceeded. These maximum ratings are part of the individual data sheets.

INTRODUCTION

Philips Semiconductors' FAST data sheets have been configured for quick usability. They are self-contained and should require minimum reference to other sections for amplifying information.

TYPICAL PROPAGATION DELAY AND SUPPLY CURRENT

The typical propagation delays listed at the top of the data sheets are the average between t_{PLH} and t_{PHL} for the most significant data path through the part.

In the case of clocked product, this is sometimes the maximum frequency of operation. In any event, this number is under the operation conditions of V_{CC} = 5.0V and T_A = 25°C.

The typical I_{CC} current shown in that same specification block is the average current (in the case of gates, this will be the average of the I_{CCH} and I_{CCL} currents) at V_{CC} = 5.0V and T_A = 25°C. It represents the total current through the individual functions.

LOGIC SYMBOLS

There are two types of logic symbols. The conventional one, "Logic Symbol," explicitly shows the internal logic (except for complex logic). The other is "Logic Symbol (IEEE/IEC)" as developed by the IEC and IEEE. The International Electrotechnical Commission (IEC) has developed a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without explicitly showing the internal logic. Internationally, Working Group 2 of IEC Technical Committee TC3 is preparing a new document (Publication 17-12) that will consolidate the original work started in the mid-1960s and published in 1972 (Publication 117-15), and the amendments and supplements that have followed. Similarly, for the USA, IEEE Committee SCC11 has revised the publication IEEE Std 91/ANSI Y32.14-1973.

The updated version IEEE Standard Graphic Symbols for Logic Functions ANSI/IEEE Std 91-1984 (revision of ANSI/IEEE Std-1973) ANSI 732.14-1973 can be ordered through:

IEEE Service Center
445 Hoes Lane
Piscataway, New Jersey
Phone: (201) 981-0060

ABSOLUTE MAXIMUM RATINGS

The Absolute Maximum Ratings table carries the maximum limits to which the part can be subjected without damaging it. There is no implication that the part will function at these extreme conditions. Thus, specifications such as the most negative voltage that may be applied to the outputs only guarantees that if less than -0.5V is applied to the output pin, after the voltage is removed, the part will not have been shorted.

Input and output voltage specifications in this table reflect the device breakdown voltages in the positive direction (+7.0V) and the effect of the clamping diodes in the negative direction.

Absolute Maximum Ratings imply that any transient voltages, currents, and temperatures will not exceed the maximum ratings. Absolute Maximum Ratings are shown in Table 1.

RECOMMENDED OPERATING CONDITIONS

The Recommended Operating Conditions table has dual purposes. It sets environmental conditions (operating free-air temperature), and it sets the conditions under which the limits set forth in the DC Electrical Characteristics table and AC Electrical Characteristics table will be met. Another way of looking at this table is to think of it not as a set of limits guaranteed by Philips Semiconductors, but as the conditions Philips Semiconductors uses to test the parts and guarantee that they will then meet the limits set forth in DC and AC Electrical Characteristics tables.

Some care must be used in interpreting the numbers in these tables. Philips Semiconductors feels strongly that the specifications set forth in a data sheet should reflect as accurately as possible the operation of the part in an actual system. In particular, the input threshold values of V_{IH} and V_{IL} can be tested by the user with parametric test equipment. If V_{IH} and V_{IL} are applied to the inputs, the outputs will be at the voltage guaranteed by the DC Electrical Characteristics table. There is a tendency on the part of some users to use V_{IH} and V_{IL} as conditions applied to the inputs test the part for functionality in a "truth table exerciser" mode. This frequently causes problems because of the noise present at the test head of automated test equipment. Parametric tests, such as those used for the output levels under the V_{IH} and V_{IL} conditions are done fairly slowly, on the order of milliseconds, and any noise present at the inputs has settled out before the outputs are measured. But in functionality testing, the outputs are examined much faster, before the noise on the inputs has settled out and the part has assumed its final and correct output state. Thus, V_{IH} and V_{IL} should never be used in testing the functionality of any FAST part type. For these types of tests, input voltages of +4.5V and 0.0V should be used for the High and Low states, respectively.

TABLE 1. ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply Voltage		-0.5 to +7.0	V
V_{IN}	Input Voltage		-0.5 to +7.0	V
I_{IN}	Input Current		-30 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	Standard outputs	40	mA
		3-State outputs	48	mA
		All Buffer outputs	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

In no way does this imply that the devices are noise sensitive in the final system. The use of "hard" Highs and Lows during functional testing is done primarily to reduce the effects of the large amounts of noise typically present at the test heads of automated test equipment with cables that may at times reach several feet. The situation in a system on a PC board is less severe than in a noisy production environment. Typical recommended operating conditions are shown in Table 2.

DC ELECTRICAL CHARACTERISTICS

This table reflects the DC limits used by Philips Semiconductors during their testing operations conducted under the conditions set forth in the Recommended Operating Conditions table. V_{OH}, for example, is guaranteed to be no less than 2.7V when tested with V_{CC} = +4.7V, V_{IH} = 0.8V across the temperature range of 0°C to +70°C, and with an output current of I_{OH} = -1.0mA.

In this table, one sees the heritage of the original junction isolated Schottky family — V_{OL} = 0.5V at I_{OL} = 20mA. This gives the user a guaranteed worst case Low-state noise immunity of 0.3V. In the High state the noise immunity is 0.7V worst case. Although at first glance it would seem one-sided to have greater noise immunity in the High state than in the Low state, more noise immunity is a useful state of affairs. Because the impedance of an output in the High state is generally much higher than in the Low state, more noise immunity in the High state is needed. This is because the noise source couples noise onto the output connection of the device. That output tries to pull the noise source down by sinking the energy to ground or to V_{CC} depending on the state. The ability of the output to do that is determined by its output impedance. The lower half of the output stage is a very low-impedance transistor which can effectively pull the noise source down. Because of the higher impedance of the upper stage of the output, it is not as effective as shunting the noise energy to V_{CC}, so than an extra 0.4V of noise immunity in the High state compensates for the higher impedance. The result is a nice balance of sink-and-drive current capabilities with the optimum amount of noise immunity in both states.

V_{OH} and V_{OL} values may vary depending on whether 5% or 10% V_{CC} swings are specified. The type of output structure, standard, 3-State, or buffer will also affect the value of V_{OH} and V_{OL}. Generally, as the output current and V_{CC} variation increase, the guaranteed minimum V_{OH} decreases and the maximum V_{OL} increases. Philips Semiconductors specifies and tests V_{OH} and V_{OL} for both 5% and 10% V_{CC} swing.

I_I, the maximum input current at maximum input voltage, is a measure of the input leakage current at a guaranteed minimum input breakdown voltage. The test conditions for I_I vary according to the type of input structure being tested. Diode inputs are tested with the V_{CC} = MAX and 7.0V at the input. It is necessary to turn off V_{CC} for the NPN input test to measure leakage. Otherwise, the current source is on and the leakage is undetectable. When I_I is being measured on transceiver I/O pins, both V_{CC} and the input voltage is 5.5V. The reduced input voltage is necessary because of the output structure connected to the input structure. Output structures break down faster than input structures and it is impossible to test the input without testing the output also.

I_{IH} for both Diode and NPN input structures is less than 20µA typically. I_{IL} is less than 20µA for NPN inputs and less than 600µA for Diode inputs. If multiple structures are tied together in the design, then the input current values also multiply. The fan-out for the devices with NPN inputs is 30 times greater than those with Diode inputs. This means the output current sinking ability of the device driving the input to the Low state could be 30 times less when driving NPN devices. For transceiver I/O pins, the outputs are in the high-impedance state when the inputs are tested. Therefore, a maximum of 50µA extra leakage is allowed and combined with the I_{IH} and I_{IL} values. These tests are called I_{IH} + I_{OZH} and I_{IL} + I_{OZL} to more accurately describe the true measurement being made.

I_{OZH} is tested only on Open Collector outputs as a leakage test with setup conditions that would put the output in the High state if it were not in the 3-State high impedance condition. I_{OZL} is similar except the setup condition is for the Low state.

I_{OH} is tested only on Open Collector outputs as leakage test for the lower output transistor structure. Both V_{CC} and V_{OH} are at the same value so that there is not a current path to or from V_{CC} that would mask the leakage path.

Short circuit output current is a parameter that has appeared on digital data sheets since the inception of integrated circuit logic devices, but the meaning and implications of that specification has totally changed. Originally, I_{OS} was an attempt to reassure the user that if a stray oscilloscope probe accidentally shorted an output to ground, the device would not be damaged. In this manner, an extremely long time was associated with the I_{OS} test. However, thermally induced malfunctions could occur after several seconds of sustained test.

TABLE 2. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min.	Norm.	Max.	
V_{CC}	Supply Voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
V_{OH}	High-level output voltage	Open Collector			4.5	V
I_{OH}	High-level output current	Standard			-1	mA
		3-State			-3	mA
		Buffer			-15	mA
I_{OL}	Low-level output current	Standard			20	mA
		3-State			24	mA
		Buffer			64	mA
T_A	Operating free-air temperature range		0		70	°C

Over a period of time, I_{OS} became a measure of the ability of an output to charge line capacitance. Assume a device is driving a long line and is in the Low state. When the output is switched High, the rise time of the output waveform is limited by the rate at which the line capacitance can be charged to the new state of V_{OH}. At the instant the output switches, the line capacitance looks like a short to ground. I_{OS} is the current demanded by the capacitive load as the voltage begins to rise and the demand decreases. We now reach the critical point in our discussion. The full value of I_{OS} need only be supplied for a few hundred microseconds at most, even with 1.0μF of line capacitance tied to the output, a load that is unrealistically high by several order of magnitude.

The effect of a large I_{OS} surge through the relatively small transistors that make up the upper part of the output stage is not serious – *as long as that current is limited to a short duration.* If the hard short is allowed to remain, the full I_{OS} current will flow through the output state and may cause functional failure or damage to the structure. As test induced failure may occur if the I_{OS} test time is excessive. As long as the condition is brief, typically 50ms or less with ATE equipment, the local heating does not reach the point where damage or functional failures may occur. As we have already seen, this is considerably longer than the time of the effective current surge that must be supplied by the device in the case of charging the capacitance. The Philips Semiconductors data sheet limits for I_{OS} reflect the conditions that the part will see in the system — full I_{OS} spikes for extremely short periods of time. Problems could occur if slow test equipment or test methods ground an output for too long a time, causing functional failure or damage. DC electrical characteristics are shown in Table 3.

AC ELECTRICAL CHARACTERISTICS

The AC Electrical Characteristics table contains the guaranteed limits when tested under the conditions set forth in the AC Test Circuits and Waveforms section. In some cases, the test conditions are further defined by the AC setup requirements (see Table 5) — this is generally the case with counters and flip-flops where setup and hold times are involved.

All of the AC Characteristics are guaranteed with 50pF load capacitance. The reason for choosing 50pF over 15pF as load capacitance is that it allows more leeway in dealing with stray capacitance, and also loads the device during rising or falling output transitions, which more closely resembles the loading to be expected in average applications, thus giving the designer more useful delay figures.

Although the 50pF load capacitance will increase the propagation delay by an average of about 1ns for FAST devices, it will increase several nanoseconds for standard Schottky devices.

The load resistor of 500Ω is conveniently specified as both a pull-up and pull-down load resistor.

Because of the reduced inductance inherent in the SO package, minimum propagation delays are being derated by 0.2ns. This is reflected by a note at the bottom of Table 4.

TABLE 3. DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]	LIMITS			UNIT	V_{CC} [4]
					Min.	Typ.[2]	Max.		
V_{IH}	High-level input voltage			Recognized as a High signal over recommended V_{CC} and T_A range	2.0			V	
V_{IL}	Low-level input voltage			Recognized as a Low signal over recommended V_{CC} and T_A range			0.8	V	
V_{IK} (V_{CD})	Input clamp diode voltage			I_{IN} = -18mA			0.8	V	
V_{OH}	High-level output voltage	Standard[5]	±10% V_{CC}	I_{OH} = -1mA	2.5	3.4		V	MIN
			±5% V_{CC}		2.7	3.4		V	MIN
		3-State	±10% V_{CC}	I_{OH} = -3mA	2.4	3.3		V	MIN
			±5% V_{CC}		2.7	3.3		V	MIN
		Buffers	±10% V_{CC}	I_{OH} = -15mA	2.0	3.2		V	MIN
			±5% V_{CC}		2.0	3.1		V	MIN
V_{OL}	Low-level output voltage	Standard[5]	±10% V_{CC}	I_{OL} = 20mA		0.30	0.5	V	MIN
			±5% V_{CC}			0.30	0.5	V	MIN
		3-State	±10% V_{CC}	I_{OL} = 24mA	2.4	0.35	0.5	V	MIN
			±5% V_{CC}		2.7	0.35	0.5	V	MIN
		Buffers	±10% V_{CC}	I_{OL} = 48mA	2.0	0.38	0.55	V	MIN
			±5% V_{CC}	I_{OL} = 64mA	2.0	0.42	0.55	V	MIN
I_I	High-level current breakdown test	Diode inputs		V_{IN} = 7.0V			100	µA	MAX
		NPN inputs		V_{IN} = 7.0V			100	µA	0.0V
		Transceiver I/O pins		V_{IN} = 5.5V			1.0	mA	5.5V
I_{IH}	High-level input current			V_{IH} = 2.7V (20µA × n High U.L.)			n(20)	µA	MAX
I_{IL}	Low-level input current	Diode inputs		V_{IL} = 0.5V (-0.6mA × n Low U.L.)			n(-0.6)	mA	MAX
		NPN inputs		V_{IL} = 0.5V (-20µA × n Low U.L.)			n(-20)	µA	0.0V
I_{IH} + I_{OZH}	High-level input current (I/O pins)			V_{IH} = 2.7V (20µA × n High U.L.)			n(20)+50	µA	MAX
I_{IL} + I_{OZH}	Low-level input current (I/O pins)	Diode inputs		V_{IL} = 0.5V (-0.6mA × n Low U.L.)			n(-0.6)	mA	MAX
		NPN inputs		V_{IL} = 0.5V (-20µA × n Low U.L.)			n(-20)-50	µA	MAX
I_{OZH}	3-State, High-level OFF current			V_{OUT} = 2.7V			50	µA	MAX
I_{OZL}	3-State, Low-level OFF current			V_{OUT} = 0.5V			-50	µA	MAX
I_{OH}	Open Collector output leakage			V_{OH} = 4.5V			250	µA	MAX
I_{OS}	Output short-circuit current	Standard[5], 3-State		V_{OUT} = 0V	-60		-150	mA	MAX
		Buffer driver			-100		-225	mA	MAX
I_{CEX}	Output High leakage current			V_{OUT} = 5.5V, not tested on NPN transceivers and Open Collector outputs			250	µA	MAX
I_{ZZ}	Bus drainage test			V_{OUT} = 5.5V, 3-State			500	µA	0.0V

NOTES:

1. Unless otherwise noted, conditions and limits apply throughout the temperature range for which the particular device is rated. The ground pin is the reference level for all applied and resultant voltages.
2. Unless otherwise stated on individual data sheets.
3. Typical characteristics refer to V_{CC} = 5V, T_A = 25°C.
4. MIN and MAX refer to the values listed in the data sheet table of recommended operating conditions.
5. Standard refers to the totem-pole pull-up circuitry commonly used for the particular family, as distinguished from buffers, line drivers or 3-state outputs.
6. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

TABLE 4. AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A=+25°C, V_{CC}=5V, C_L=50pF, R_L=500Ω			T_A=0°C to +70°C, V_{CC}=5V±10%, C_L=50pF, R_L=500Ω		
				Min.	Typ.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74F373	Waveform 3	3.0 2.0	5.3 3.7	7.0 5.0	3.0 2.0	8.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay E to Q_n		Waveform 2	5.0 3.0	9.0 4.0	11.5 7.0	5.0 3.0	13.0 8.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	5.0 5.6	11.0 7.5	2.0 2.0	12.0 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	4.5 3.8	6.5 5.0	2.0 2.0	7.5 6.0	ns
f_{MAX}	Maximum clock frequency	74F374	Waveform 1	100			70		ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1	4.0 4.0	6.5 6.5	8.5 8.5	4.0 4.0	10.0 10.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	9.0 5.3	11.5 7.5	2.0 2.0	12.5 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	5.3 4.3	7.0 5.5	2.0 2.0	8.0 6.5	ns

TABLE 5. AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A=+25°C, V_{CC}=5V, C_L=50pF, R_L=500Ω			T_A=0°C to +70°C, V_{CC}=5V±10%, C_L=50pF, R_L=500Ω		
				Min.	Typ.	Max.	Min.	Max.	
t_s (H) t_s (L)	Set-up time D_n to E	74F373	Waveform 4	2.0 2.0			2.0 2.0		ns
t_h (H) t_h (L)	Hold time D_n to E		Waveform 4	3.0 3.0			3.0 3.0		ns
t_w (H)	E Pulse width, High		Waveform 1	6.0			6.0		ns
t_s (H) t_s (L)	Set-up time D_n to CP	74F374	Waveform 5	2.0 2.0			2.0 2.0		ns
t_h (H) t_h (L)	Hold time D_n to CP		Waveform 5	2.0 2.0			2.0 2.0		ns
t_w (H) t_w (L)	CP Pulse width, High or Low		Waveform 1	7.0 6.0			7.0 6.0		ns

TEST CIRCUITS AND WAVEFORMS

The 500Ω load resistor, R_L to ground, as described in Figure 1, acts as a ballast to slightly load the totem-pole pull-up and limit the quiescent High-state voltage to about +3.5V. Otherwise, an output would rise quickly to about +3.5V, but then continue to rise slowly up to about +4.4V. On the subsequent High-to-Low transition, the observed t_{PHL} would vary slightly with duty cycle, depending on how long the output voltage was allowed to rise before switching to the Low state. Perhaps more importantly, the 500Ω load to ground can be a high frequency, passive probe for a sampling scope, which costs much less than the equivalent, high impedance probe. Alternately, the 500Ω load to ground can be simply a 450Ω resistor feeding into a 50Ω coaxial cable leading to a sampling scope input connector, with the internal 50Ω termination of the scope completing the path to ground. Note that with this scheme there should be a matching cable from the device input pin to the other input of the sampling scope; this also serves as a 50Ω termination for the pulse generator that supplies the input signal.

Figure 2, Test Circuit for 3-State outputs, shows a second 500Ω resistor from the device output to switch. For most measurements this switch is open; it is closed for measuring a device with Open Collector outputs and for measuring one set of the enable/disable parameters (Low-to-OFF and OFF-to-Low) of a 3-State output. With the switch closed, the pair of 500Ω resistors and the +7.0V supply establish a quiescent High level of +3.5V, which correlates with the High-level discussed in the preceding paragraph.

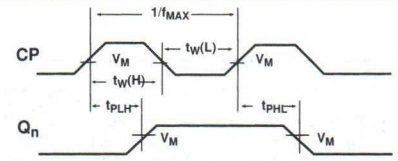
As shown in Figure 3, AC Waveforms for FAST 74F373 and 74F374, the disable times are measured at the point where the output voltage has risen or fallen by 0.3V from the quiescent level (i.e., Low for t_{PLH}[2] or High for t_{PHL}[2]).

Since the rising or falling waveform is RC-controlled, 0.3V of change is more linear and is less susceptible to external influences.

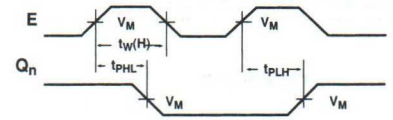
More importantly, from the system designer's point of view, 0.3V is adequate to ensure that a device output has turned OFF. It also gives system designers more realistic delay times to use in calculating minimum cycle times.

Good high frequency wiring practices should be used in constructing test jigs. Leads on the load capacitor should be as short as possible to minimize ripples on the output waveform transitions and to minimize undershoot. Generous ground metal should be used for the same reasons. A V_{CC} bypass capacitor should be provided at the test socket, also with minimum lead lengths. Input signals should have rise and fall times of 2.5ns, and signal swing of 0V to +3.0V, 1.0MHz square wave is recommended for most propagation delay tests. The repetition rate must necessarily be increased for testing f_{MAX}. Two pulse generators are usually required for testing such parameters

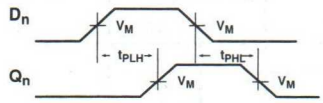
AC WAVEFORMS



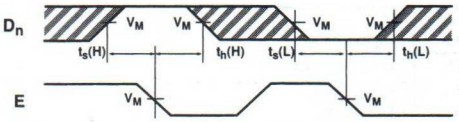
Waveform 1. Propagation Delay Clock to Output, Clock Pulse Widths, and Maximum Clock Frequency



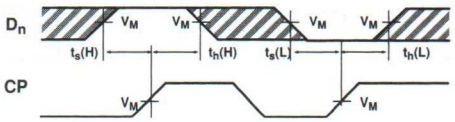
Waveform 2. Propagation Delay, Enable to Outputs and Enable Pulse Width



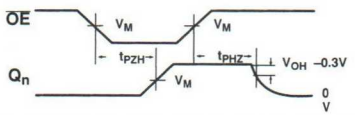
Waveform 3. Propagation Delay, Data to Outputs



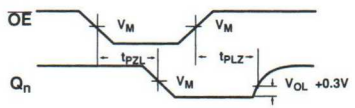
Waveform 4. Data Setup and Hold Times



Waveform 5. Data Setup and Hold Times

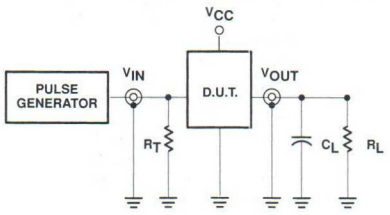


Waveform 6. 3-State Output Enable Time to High Level and Output Disable Time from High Level



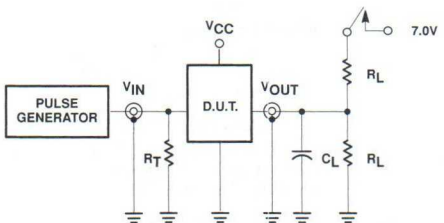
Waveform 7. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, VM = 1.5V. The shaded areas indicate when the input is permitted to change for predictable output performance.



DEFINITIONS:
R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Figure 1. Test Circuit for Totem-Pole Outputs



SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:
R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Figure 2. Test Circuit for 3-State Outputs

DC SYMBOLS AND DEFINITIONS

Voltages – All voltages are referenced to ground. Negative voltage limits are specified as absolute values (i.e., -10V is greater than -1.0V)

V_{CC} **Supply voltage:** The range of power supply voltage over which the device is guaranteed to operate within the specified range.

V_{IKMAX} **Input clamp diode voltage:** The most negative voltage at an input when the specified current is forced out of that input terminal. This parameter guarantees the integrity of the input diode intended to clamp negative ringing at the input terminal.

V_{IH} **High-level input voltage:** The range of input voltages recognized by the device as a logic High.

V_{IHMIN} **High-level Minimum Input voltage:** This value is the guaranteed input High threshold for the device. The minimum allowed input High in a logic system.

V_{IL} **Low-level input voltage:** The range of input voltages recognized by the device as a logic Low.

V_{ILMAX} **Low-level Maximum Input voltage:** This value is the guaranteed input Low threshold for the device. The maximum allowed input Low in a logic system.

V_M **Measurement voltage:** The reference voltage level on AC waveforms for determining AC performance. Usually specified as 1.5V for the FAST family.

V_{OHMIN} **High-level output voltage:** The minimum guaranteed High voltage at an output terminal for the specified output current I_{OH} and at the minimum V_{CC} value.

V_{OLMAX} **High-level output voltage:** The maximum guaranteed Low voltage at an output terminal sinking the specified load current I_{OL}.

V_{T+} **Positive-going threshold voltage:** The input voltage of a variable threshold device which causes operation according to specification as the input transition rises from below V_{T-} (Min).

V_{T-} **Negative-going threshold voltage:** The input voltage of a variable threshold device which causes operation according to specification as the input transition rises from below V_{T+} (Max).

Currents – Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device. All current limits are specified as absolute values.

I_{CC} **Supply current:** The current flowing into the V_{CC} supply terminal of the circuit with specified input conditions and open outputs. Input conditions are chosen to guarantee worst-case operation unless specified.

I_I **Input leakage current:** The current flowing into an input when the maximum allowed voltage is applied to the input.

I_{IH} **High-level input current:** The current flowing into an input when a specified High level voltage is applied to that input.

I_{IL} **Low-level input current:** The current flowing out of an input when a specified Low-level voltage is applied to that input.

I_O **Output current:** The output current that is approximately one half of the short-circuit output current (I_{OS}).

I_{OH} **High-level output current:** The leakage current flowing into a turned-off Open Collector output with a specified High-level output voltage applied. For devices with a pull-up circuit, the I_{OH} is the current flowing out of an output which is in the High-level state.

I_{OH1} **High-level output current:** The current necessary to guarantee the Low to High transition in a 30Ω transmission line on the incident wave.

I_{OL} **Low-level output current:** The current flowing into an output which is the Low-level state.

I_{OL1} **Low-level output current:** The current necessary to guarantee the High to Low transition in a 30Ω transmission line on the incident wave.

I_{OS} **Short-circuit output current:** The current flowing out of an output which is in the High-level state when that output is short-circuited to ground.

I_{OZH} **OFF-state output current High:** The current flowing into a disabled 3-state output with a specified High level output voltage applied.

I_{OZL} **OFF-state output current High:** The current flowing out of a disabled 3-state output with a specified Low level output voltage applied.

AC SYMBOLS AND DEFINITIONS

f_{MAX} **Maximum clock frequency:** The maximum input frequency at a clock input for predictable performance. Above this frequency the device may cease to function.

t_{PLH} **Propagation delay time:** The time between specified reference points on the input and the output waveforms with the output changing from the defined Low-level to High-level.

t_{PHL} **Propagation delay time:** The time between specified reference points on the input and the output waveforms with the output changing from the defined High-level to Low-level.

t_{PHZ} **Output disable time from High level to a 3-State output:** The delay time between the specified reference points on the input on the input and output voltage waveforms with the 3-State output changing from the High-level to a high impedance "OFF" state.

t_{PLZ} **Output disable time from Low level to a 3-State output:** The delay time between the specified reference points on the input on the input and output voltage waveforms with the 3-State output changing from the Low-level to a high impedance "OFF" state.

t_{PZH} **Output enable time to a Low level of a 3-State output:** The delay time between the specified reference points on the input on the input and output voltage waveforms with the 3-State output changing from a high impedance "OFF" state to a High-level.

t_{PZL} **Output enable time to a Low level of a 3-State output:** The delay time between the specified reference points on the input on the input and output voltage waveforms with the 3-State output changing from a high impedance "OFF" state to a Low-level.

t_s **Setup time:** The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_h **Hold time:** The interval immediately following the active transition of the timing pulse (usually the clock pulse) or immediately following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_w **Pulse width:** The time between the reference point on the leading and trailing edges of a pulse.

t_{REC} **Recovering time:** The time between the reference point on the trailing edge of an asynchronous input control pulse and the reference point on the activating edge of a synchronous (clock) pulse input such that the device will respond to the synchronous input.

t_{TLH} **Transition time, Low to High:** The time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from Low to High.

t_{THL} **Transition time, High to Low:** The time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from High to Low.

t_r, t_f **Clock input and rise and fall times:** 10% and 90% value.

INTRODUCTION

The properties of high-speed FAST logic circuits dictate that care be taken in the design and layout of a system.

Some general design considerations are included in this section. This is not intended to be a thorough guideline for designing FAST systems, but a reference for some of the constraints and techniques to be considered when designing a high-speed system.

HANDLING PRECAUTIONS

As described in the circuit characteristics section, FAST devices are susceptible to damage from electrostatic discharge (ESD).

- Philips Semiconductors' FAST devices are shipped in conducting foam or anti-static tubes and foil-lined boxes to minimize ESD during shipment and unloading.
- Before opening the shipment of FAST devices, make sure that the individual is grounded and all handling means (such as tools, fixtures and benches) are grounded.
- After removal from the shipping material, the leads of the FAST devices should always be grounded. In other words, FAST devices should be placed leads-down on a grounded surface, since ungrounded leads will attract static charge.
- Do not insert or remove devices in sockets with power applied. Ensure that power supply transients, such as occur during power turn on-off, do not exceed absolute maximum ratings.
- After assembly on PC boards, ensure that ESD is minimized during handling, storage or maintenance.
- FAST inputs should never be left floating on a PC board. This precaution applies to any TTL family. As a temporary measure, a resistor with a resistance greater than 10kΩ should be soldered on the input. The resistor will limit accidental damage if the PC board is removed and brought into contact with static-generating material.

INPUT CLAMPING

FAST circuits are provided with clamp diodes on the device inputs to minimize negative ringing effects. These diodes should not be used to clamp negative DC voltages or long duration, negative pulses. Certain FAST part types with the NPN base input structure also provide clamping of positive overshoots.

UNUSED INPUTS

Proper design rules dictate that all unused inputs on TTL devices be tied either High or Low. This is especially important with FAST logic.

Electrically open inputs can degrade AC noise immunity as well as the switching speed of the device. Small geometries make FAST more susceptible to damage by ESD than other TTL families. Tying inputs to V_{CC} or GND, directly or through a resistor, protects the device from in-circuit electrostatic damage. Additionally, while most unconnected TTL float High, FAST devices with NPN inputs float Low. FAST devices do not require an input resistor to tie the input High. Inputs can be connected directly to V_{CC} as well as ground.

Possible ways of handling unused inputs are:

1. Unused active-High NAND or AND inputs to V_{CC}. The inputs should be maintained at a voltage greater than 2.7V, but should not exceed the absolute maximum rating.
2. Connect unused active-High NOR or OR inputs to ground.
3. Tie unused active-High NAND or AND inputs to a used input of the same gate, provided that the High-level fan-out of the driving circuit is not impaired.
4. Connect the unused active-High NAND or AND inputs to the output of an unused gate that is forced High.

MIXING FAMILIES WITH OTHER TTL FAMILIES

Mixing the slower TTL families such as 74 and 74LS with the higher speed families such as 74F is possible but must be done with caution. Each family of TTL devices has unique input and output characteristics optimized to achieve the desired speed or power features.

The unique speed/power characteristics of FAST devices are achieved partially by the internal fast rise and fall times, as well as those at input and output modes. These fast transitions can cause noise of various types in a system. Power and ground line noise are generated by the faster transitions of the current in the output load capacitance. Signal line noise can also be generated by the fast output transitions.

The noise generated by 74F devices can be minimized in systems designed with shorter signal lines, good ground planes, well-bypassed power distribution networks, layouts that minimize adjacent signal lines that run parallel, and improved impedance matching in signal lines to reduce transmission line type reflections.

INPUT-OUTPUT LOADING AND FAN-OUT TABLE

For convenience in system design, the input-output loading and fan-out characteristics of each circuit are specified in terms of unit load and actual load value. One FAST Unit Load (U.L.) in the High state is defined as 20μA; thus both the input leakage current, I_I, and output High current-sourcing capability, I_{OH}, are normalized to 20μA.

Similarly, one FAST Unit Load (U.L.) in the Low state is defined as 0.6mA and both the input Low current, I_{IL}, and input Low current-sinking capability, I_{OL}, are normalized to 0.6mA.

For added convenience, the actual load value in amperes is listed in the column adjacent to U.L.

On some FAST devices, high-impedance NPN base input structure has been utilized. With this structure, the Low level input current, I_{IL}, has been reduced to 20μA. This characteristic is 30 times lower than the requirement of devices using the conventional input structure. This feature improves fan-out in the Low state and can help reduce part count in system design by eliminating buffers in some applications.

CLOCK PULSE REQUIREMENTS

All FAST clock inputs are buffered to increase their tolerance of slow positive-clock edges and heavy ground noise. Nevertheless, the rise time on positive-edge-triggered devices should be less than the nominal clock-to-output delay measured between 0.8 to 2.0V levels of the clock driver for added safety margin against heavy ground noise. Not only a fast rising, clean clock pulse is required, but the path between the clock drive and clock input of the device should be well-shielded from electromagnetic noise.

TABLE 1. LOADING COMPARISONS

DRIVING DEVICE FAMILY	I_{OL} (MIN.)	DRIVEN DEVICE FAMILY						
		74F	74F(NPN)	74LS	74	74S	8200/9300	82S00
		I_{IL} (MAX.)						
		0.6mA	20μA	0.4mA	1.6mA	2.0mA	1.6mA	0.4mA
		MAXIMUM NUMBER OF LOADS DRIVEN						
74F	20mA	33	1,000	50	12.5	10	12	50
74F(NPN)	64mA	106	3,200	160	40	32	40	160
74LS	8mA	13	400	20	5	4	5	20
74LS Buffer	24mA	40	1,200	60	15	12	15	60
74	16mA	26	800	40	10	8	10	40
74 Buffer	40mA	78	2,400	120	30	24	30	120
74S	20mA	33	1,000	50	12.5	10	12	50
74S Buffer	60mA	100	3,000	150	37.5	30	37	150

INPUT LOADING AND OUTPUT DRIVE COMPARISON

The logic levels of all TTL products are fully compatible with each other. However, the input loading and the output drive characteristics of each family are different and must be taken into consideration when mixing them in a system, Table 1 shows the relative drive capabilities of each family for commercial temperature and voltage ranges.

FAST OUTPUTS TIED TOGETHER

The only FAST outputs that are designed to be tied together are Open Collector and 3-State outputs. Standard FAST outputs should not be tied together unless their logic levels will always be the same; either High or Low. When connecting Open Collector or 3-State outputs together, some general guidelines must be observed.

Open Collector Outputs

These devices must be used whenever two or more OR-tied outputs will be at opposite logic levels at the same time. These devices devices must have a pull-up resistor(s) added between the OR-tie connector and V_{CC} to establish an active-High level. Only special high voltage buffers can be tied to a higher voltage than V_{CC}. The minimum and maximum size of the pull-up resistor is determined as follows.

$$R(\text{Min}) = \frac{V_{CC}(\text{Max}) - V_{OL}}{I_{OL} - N_2(I_{IL})}$$

$$R(\text{Max}) = \frac{V_{CC}(\text{Min}) - V_{OL}}{N_1(I_{OH}) - N_2(I_{IH})}$$

where:

I_{OL} = Minimum I_{OL} guarantee or OR tie elements.

$N_2(I_{IL})$ = Cumulative maximum input Low current for all inputs tied to OR-tie connection.

$N_1(I_{OH})$ = Cumulative maximum output High leakage current for all outputs tied to OR-tie connection.

$N_1(I_{IH})$ = Cumulative maximum input High leakage current for all outputs tied to OR-tie connection.

If a resistor divider network is used to provide the High level, the R(Max) must be decreased enough to provide the required $[V_{OH}/R(\text{pull-down})]$ current.

3-State Outputs

3-State outputs are designed to be tied together, but are not designed to be active simultaneously. In order to minimize noise and protect the outputs from excessive power dissipation, only one 3-State output should be active at any time. This generally requires that the output enable signals be non-overlapping. When TTL decoders are used to enable 3-State outputs, the decoder should be disabled while the address is being changed. Since all TTL decoder outputs are subject to decoding spikes, non-overlapping signals cannot normally guarantee when the address is changing.

Since most 3-State output enable signals are active-Low, shift register or edge-triggered storage registers provide good output enable buffers. Shift registers with one circulating Low bit, such as the 'F164 or 'F194, are ideal for sequential enable signals. The 'F174 or 'F273 can be used to buffer enable signals from TTL decoders or microcode (ROM) devices. Since the outputs of these registers will change from Low-to-High faster than from High-to-Low, the selection of one device at a time is assured.

GND

Good system design starts with a well thought out ground layout. Try to use ground plane if possible. This will save headaches later on. If ground strip is used, try to reduce ground path in order to minimize ground inductance. This prevents crosstalk problems. Quite often, jumper wire is used for connecting to ground at the breadboarding stage, but a solid ground must be used even at the breadboarding stage.

V_{CC}

Typical dynamic impedance of un-bypassed V_{CC} runs from 50Ω to 100Ω, depending on V_{CC} and GND configuration. This is why a sudden current demand, due to an IC output switching, can cause momentary reduction in V_{CC} unless a bypass (decoupling) capacitor is located near V_{CC}.

Not only is there a sudden current demand due to output switching transient, there is also a heavy current demand by the buffer driver. Assuming the buffer output sees a 50Ω dynamic load and the buffer Low-to-High transition is 2.5V, the current demand is 50mA per buffer. If it is an octal buffer, the current demand could be 0.4mA per package in 3ns time!

The next step is to figure out the capacitance requirement for each bypass capacitor. Using the previously mentioned octal buffer and assuming the V_{CC} droop is 0.1V, then C is:

$$C = 0.4A \times 3 \times 10^{-9} \text{ sec}/0.1V$$
$$= 12 \times 10F^{9}$$

This formula is derived as follows:

$Q = CV$

By differentiation:

$\Delta Q/\Delta t = C\Delta V/\Delta t$

since

$\Delta Q/\Delta t = i$

the equation becomes:

$i = C\Delta V/\Delta t$

hence

$C = i\Delta t/\Delta V$

Select the C bypass $\geq 0.02\mu F$ and try to use a high quality RF capacitor. Place one bypass capacitor for each buffer and one bypass capacitor every two other types of IC packages. Make sure that the leads are cut as short as possible.

In addition, place bypass capacitors on a board to care of board-level current transients.

CROSS-TALK

The best way to handle cross-talk is to prevent it from occurring in the first place; quick fixes are troublesome and costly. To prevent cross-talk, maximize spacing between signal lines and minimize spacing between signal lines and ground lines.

Preferably, place ground lines between signals. For added precaution, add a ground trace alongside either the potential cross-talker or the cross-listener.

For back-plane or wire-wrap, use twisted pair for sensitive functions such as clocks, asynchronous set or reset, or asynchronous parallel load. In flat cable, make every other conductor ground.

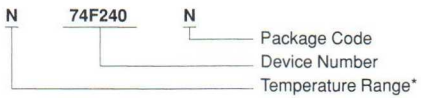
For multilayer PC boards, run signal lines in adjacent planes perpendicular to prevent magnetic coupling, and limit capacitive coupling. Use power shield (V_{CC} or ground plane) in between signal planes.

Since any voltage change, noise or otherwise, arriving at the unterminated end of transmission lines double in amplitude, even a partially terminated line reduces the amplitude of the signal (noise or otherwise) appearing at the end of the line; therefore, using a terminating resistor whose value is equal to the line characteristic impedance will help reduce cross-talk.

Ordering Information

Philips Semiconductors' commercial FAST products are generally available in both standard dual-in-line and surface mounted options. The ordering code specifies temperature range, device number, and package style as shown below. For commercial products, the standard temperature range is 0°C to 70°C. Available package options are shown on individual data sheets in the "Ordering Code" block. For surface mounted devices the SO plastic dual-in-line package is supplied up to and including 28 pins. Above 28 pins, the plastic leaded chip carrier is utilized.

ORDERING CODE EXAMPLES



TEMPERATURE RANGE	DEVICE NUMBER	PACKAGE CODE
Commercial Range: 0°C to 70°C	74FXXX	N = Plastic Dual In-Line Package (DIP) D = Plastic SO DIP (surface mounted) A = Plastic Leaded Chip Carrier (PLCC) DB = Shrink Small Outline Package

* Please note that the temperature range prefix "N" is omitted on the package due to dimensional constraints.

Section 2
FAST TTL Logic Devices

FAST TTL Logic Series

CONTENTS

74F00	Quad 2-input NAND gate	61
74F02	Quad 2-input NOR gate	64
74F04	Hex inverter	67
74F06	Hex Inverter Buffer/Driver, Open-Collector	70
74F06A	Hex Inverter Buffer/Driver, Open-Collector	70
74F07	Hex Buffer/Driver, Open-Collector	70
74F07A	Hex Buffer/Driver, Open-Collector	70
74F08	Quad 2-input AND gate	76
74F10	Triple 3-Input NAND Gate	79
74F11	Triple 3-Input AND Gate	79
74F14	Hex inverter Schmitt trigger	83
74F20	Dual 4-input NAND gate	87
74F27	Triple 3-input NOR gate	90
74F30	8-input NAND gate	94
74F32	Quad 2-input OR gate	98
74F37	Quad 2-input NAND buffer	101
74F38	Quad 2-input NAND buffer (open collector)	104
74F51	Dual 2-wide 2-input, 2-wide 3-input AND-OR-invert gate	108
74F64	4-2-3-2-input AND-OR-invert gate	111
74F74	Dual D-type flip-flop	115
74F85	4-bit magnitude comparator	119
74F86	Quad 2-input Exclusive-OR gate	124
74F109	Positive J-K positive edge-triggered flip-flops	127
74F112	Dual J-K negative edge-triggered flip-flop	132
74F113	Dual J-K negative edge-triggered flip-flops without reset	138
74F125	Quad buffers (3-State)	143
74F126	Quad buffers (3-State)	143
74F132	Quad 2-input NAND Schmitt trigger	148
74F133	13-input NAND gate	152
74F138	1-of-8 decoder/demultiplexer	156
74F139	1-of-4 decoder/demultiplexer	160
74F148	8-input priority encoder	164
74F151A	8-input multiplexer	169
74F153	Dual 4-line to 1-line multiplexer	174
74F154	Decoder/demultiplexer	178
74F157A	Quad 2-Input Data Selector/Multiplexer, Non–inverting	182
74F158A	Quad 2-Input Data Selector/Multiplexer, Inverting	182
74F161A	4-bit binary counters, asynchronous reset	187
74F163A	4-bit binary counters, synchronous reset	187
74F164	8-bit serial-in parallel-out shift register	196
74F166	8-bit bidirectional universal shift register	201
74F169	4-bit up/down binary synchronous counter	208
74F173	Quad D-type flip–flop (3-State)	216
74F174	Hex D-type flip-flop	222
74F175A	Quad D-type flip-flop	226
74F189A	64-bit TTL bipolar RAM, inverting (3-State)	231
74F191	Up/Down binary counter with reset and ripple clock	237
74F193	Up/down binary counter with separate up/down clocks	246
74F194	4-bit bidirectional universal shift register	253
74F195A	4-bit parallel-access shift register	259
74F198	8-bit bidirectional universal shift register	265
74F219A	64-bit TTL bipolar RAM, non-inverting (3-State)	272
74F225	16 x 5 asynchronous FIFO (3-State)	278

* *Discontinued part. Please see the Discontinued Products List.*

Section 2
FAST TTL Logic Devices

FAST TTL Logic Series

Section 2 – FAST TTL Logic Devices (continued)

74F240	Octal inverter buffer (3-state)	287
74F240A	Octal inverter buffer (3-state)	287
74F241	Octal buffer (3-state)	287
74F241A	Octal buffer (3-state)	287
74F242	Quad transceiver, inverting (3–state)	294
74F243	Quad transceiver (3–state)	294
74F244	Octal buffers (3-State)	300
74F244B	Octal buffers (3-State)	300
74F245	Octal transceiver (3-State)	306
74F253	Dual 4-input multiplexer (3-State)	310
74F256	Dual addressable latch	316
74F257A	Quad 2-line to 1-line selector/multiplexer, non-inverting (3-State)	323
74F258A	Quad 2-line to 1-line selector/multiplexer, inverting (3-State)	328
74F259	Latch	332
74F260	Dual 5-input NOR gate	339
74F269	8–bit bidirectional binary counter	342
74F273A	Octal D-type flip–flop	350
74F280B	9-bit odd/even parity generator/checker	356
74F283	4-bit binary full adder with fast carry	360
74F298	Quad 2-input multiplexer with storage	365
74F299	8-bit universal shift/storage register (3-State)	369
74F365	Hex buffer driver (3-state)	377
* 74F366	Hex inverter buffer driver (3-state)	377
74F367	Hex buffer driver (3-state)	377
* 74F368	Hex inverter buffer driver (3-state)	377
74F373	Octal transparent latch (3-state)	383
74F374	Octal D-type flip-flop (3-state)	383
74F377A	Octal D-type flip-flop with enable	390
74F378	Hex D-type flip-flop with enable	395
74F379A	Quad register	400
74F382	Arithmetic logic unit	405
74F393	Dual 4-bit binary ripple counter	413
* 74F398	Quad 2-port register with true and complimentary outputs	417
74F399	Quad 2-port register	417
* 74F455	Octal buffer driver with parity, inverting (3-state)	423
74F456	Octal buffer driver with parity, non-inverting (3-state)	423
74F521	8-bit identity comparator	430
74F524	8-bit register comparator (open collector + 3-State)	434
* 74F533	Octal transparent latch, inverting (3-state)	443
74F534	Octal D-type flip-flop inverting (3-state)	443
74F538	1-of-8 decoder (3-State)	450
74F540	Octal inverted buffer (3-state) (broad side pinout of 74F240)	455
74F541	Octal buffer (3-state) (broad side pinout of 74F244)	455
74F543	Octal registered transceiver, non-inverting (3-state)	461
74F544	Octal registered transceiver, inverting (3-state)	461
74F545	Octal bidirectional transceiver (with 3-State inputs/outputs)	471
74F552	Octal registered transceiver with parity and flags (3-State)	476
74F564	Octal D-type flip-flop (3-State)	485
74F569	4-bit bidirectional binary synchronous counter (3-State)	490
74F573	Octal transparent latch (3-state) (broad side pinout of 74F373)	499
74F574	Octal D-type flip-flop (3-state) (broad side pinout of 74F374)	499
74F579	8-bit bidirectional binary counter (3-State)	507
74F595	8-bit shift register with output latches (3-State)	516

* *Discontinued part. Please see the Discontinued Products List.*

Section 2
FAST TTL Logic Devices

FAST TTL Logic Series

Section 2 – FAST TTL Logic Devices (continued)

74F597	8-bit shift register with input storage registers	523
74F598	8-bit shift register with input storage registers (3-State)	530
74F620	Octal bus transceiver, inverting (3-state)	540
74F623	Octal bus transceiver, non-inverting (3-state)	540
74F621	Octal bus transceiver, non-inverting (open collector)	547
74F640	Octal bus transceiver, inverting (3-State)	552
74F641	Octal bus transceiver with common output enable, non-inverting (open collector)	557
* 74F642	Octal bus transceiver with common output enable, inverting (open collector)	557
* 74F646	Octal transceiver/register, non-inverting (3-state)	563
74F646A	Octal transceiver/register, non-inverting (3-state)	563
* 74F648	Octal transceiver/register, inverting (3-state)	563
74F648A	Octal transceiver/register, inverting (3-state)	563
74F647	Octal transceivers/registers, non–inverting open-collector	563
74F649	Octal transceivers/registers, non–inverting open-collector	574
* 74F651	Octal transceivers/registers, inverting (3-state)	581
74F651A	Octal transceivers/registers, inverting (3-state)	581
* 74F652	Octal transceivers/registers, non-inverting (3-state)	581
74F652A	Octal transceivers/registers, non-inverting (3-state)	581
* 74F655A	Octal buffer/driver with parity, inverting (3-state)	592
74F656A	Octal buffer/driver with parity, non-inverting (3-state)	592
74F657	Octal transceiver with 8-bit parity generator/checker	599
74F670	4 x 4 register file (3-State)	606
74F676	16-bit serial/parallel-in, serial-out shift register (3-State)	613
74F711A	Quint 2-to-1 data selector multiplexer (3-state)	618
74F711–1	Quint 2-to-1 data selector multiplexer with 30Ω series termination resistors (3-state)	618
74F712A	Quint 3-to-1 data selector multiplexer	618
74F712–1	Quint 3-to-1 data selector multiplexer with 30Ω series termination resistors	618
74F723A	Quint 3-to-1 data selector multiplexer (3-state)	627
74F723–1	Quint 3-to-1 data selector multiplexer with 30Ω series termination resistors (3-state)	627
74F725A	Quad 4-to-1 data selector multiplexer	627
74F725–1	Quad 4-to-1 data selector multiplexer with 30Ω series termination resistors	627
74F756	Octal inverter buffer (open collector 74F240)	636
74F757	Octal buffer (open collector 74F241)	636
74F760	Octal buffer (open collector 74F244)	636
74F776	Pi–bus transceiver	643
74F777	Triple bidirectional latched bus transceiver (3–State + Open Collector)	651
74F779	8-bit bidirectional binary counter (3-State)	658
74F786	4-bit asynchronous bus arbiter	665
74F804	Hex 2-input NAND drivers	672
74F1804	Hex 2-input NAND drivers (center power pin 74F804)	672
74F805	Hex 2-input NOR drivers	676
74F1805	Hex 2-input NOR drivers (center power pin 74F805)	676
74F808	Hex 2-input AND drivers	680
74F1808	Hex 2-input AND drivers (center power pin 74F808)	680
74F821	10-bit interface register, non-inverting (3-state)	684
74F822	10-bit interface register, inverting (3-state)	684
74F823	9-bit interface register, non-inverting (3-state)	684
74F824	9-bit interface register, inverting (3-state)	684
74F825	8-bit interface register, non-inverting (3-state)	684
74F826	8-bit interface register, inverting (3-state)	684
74F827	10-bit buffer/line-driver, non-inverting (3-state)	697
74F828	10-bit buffer/line-driver, inverting (3-state)	697
74F832	Hex 2-input OR drivers	704

** Discontinued part. Please see the Discontinued Products List.*

Section 2
FAST TTL Logic Devices

FAST TTL Logic Series

Section 2 – FAST TTL Logic Devices (continued)

74F1832	Hex 2-input OR drivers (center power pin 74F832)	704
74F841	10-bit bus interface latch, non-inverting (3-state)	708
74F842	10-bit bus interface latch, inverting (3-state)	708
74F843	9-bit bus interface latch, non-inverting (3-state)	708
* 74F844	9-bit bus interface latch, inverting (3-state)	708
74F845	8-bit bus interface latch, non-inverting (3-state)	708
74F846	8-bit bus interface latch, inverting (3-state)	708
* 74F861	9-bit bus transceiver, non-inverting (3-state)	722
* 74F862	9-bit bus transceiver, inverting (3-state)	722
74F863	9-bit bus transceiver, non-inverting (3-state)	722
* 74F864	9-bit bus transceiver, inverting (3-state)	722
74F1240	Octal inverter buffer (3-state) (light load 74F240)	730
* 74F1241	Octal buffer (3-state) (light load 74F241)	730
74F1244	Octal buffer (3-State)	736
74F1245	Octal transceiver (3-State)	740
74F1604	Latch	745
74F1763	Intelligent DRAM controller (IDC)	750
74F1779	8-bit bidirectional binary counter (3-State)	762
74F2240	Octal inverter buffer with 30Ω equivalent output termination (3-state)	769
74F2241	Octal buffer with 30Ω equivalent output termination (3-state)	769
74F2244	Octal buffer with 30Ω equivalent output termination (3-State)	774
74F2245	Octal transceiver with 30Ω equivalent output termination (3-State)	778
74F2373	Octal transparent latch with 30Ω equivalent output termination (3-State)	783
74F2952	Octal registered transceiver, non-inverting (3–state)	788
74F2953	Octal registered transceiver, inverting (3–state)	788
74F3037	Quad 2-input NAND 30Ω driver	796
74F3038	Quad 2-input NAND 30Ω line driver (open collector)	800
74F3040	Dual 4-input NAND 30Ω line driver	804
74F3893	Quad Futurebus backplane transceiver	808
74F5074	Synchronizing dual D-type flip-flop/clock driver	814
74F5300	Fiber optic LED driver	821
74F5302	Fiber optic dual LED/clock driver	827
* 74F30240	Octal 30Ω line-driver with enable, inverting (open collector)	833
74F30244	Octal 30Ω line-driver with enable, non-inverting (open collector)	833
74F50109	Synchronizing dual J–K positive edge-triggered flip-flop with metastable immune characteristics	839
74F50728	Synchronizing cascaded dual positive edge-triggered D-type flip-flop	846
74F50729	Synchronizing dual D-type flip-flop with edge-triggered set and reset and metastable immune characteristics	853

** Discontinued part. Please see the Discontinued Products List.*

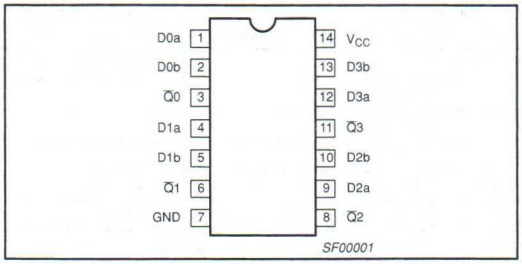
Quad 2-input NAND gate — 74F00

FEATURE

- Industrial temperature range available (–40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F00	3.4ns	4.4mA

PIN CONFIGURATION



ORDERING INFORMATION

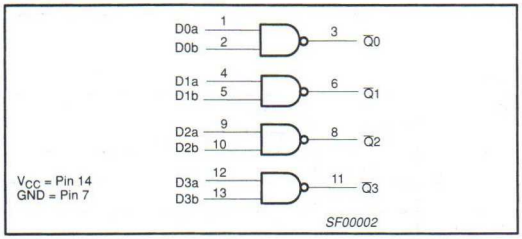
DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
14-pin plastic DIP	N74F00N	I74F00N	SOT27-1
14-pin plastic SO	N74F00D	I74F00D	SOT108-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}$n	Data output	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

LOGIC DIAGRAM

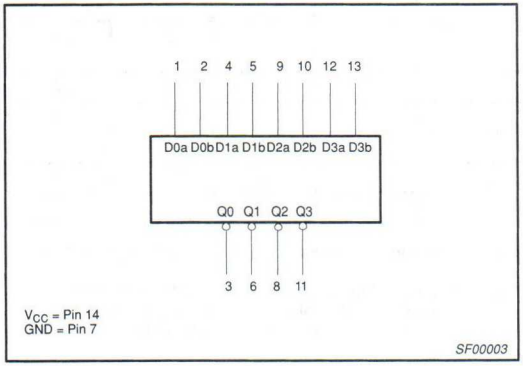


FUNCTION TABLE

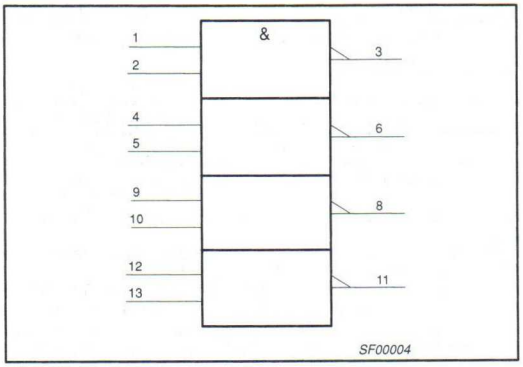
INPUTS		OUTPUT
Dna	Dnb	$\overline{Q}$n
L	L	H
L	H	H
H	L	H
H	H	L

NOTES:
H = High voltage level
L = Low voltage level

LOGIC SYMBOL



IEC/IEEE SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High-level output current				–1	mA
I_{OL}	Low-level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OI} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		1.9	2.8	mA
		I_{CCL}	V_{CC} = MAX	V_{IN} = 4.5V		6.8	10.2	mA

NOTES:

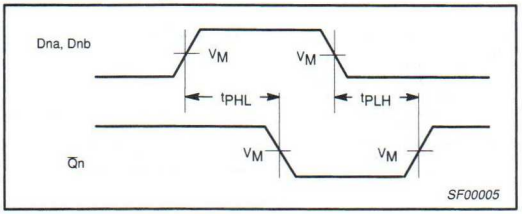
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		V_{CC} = +5.0V ± 10% T_{amb} = –40°C to +85°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to $\overline{Q}$n	Waveform 1	2.4 2.0	3.7 3.2	5.0 4.3	2.4 2.0	6.0 5.3	2.0 1.5	6.5 6.0	ns

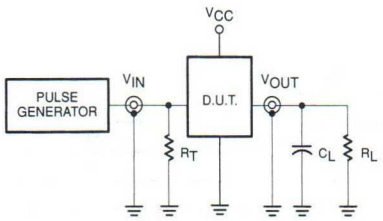
AC WAVEFORMS

For all waveforms, V_M = 1.5V.

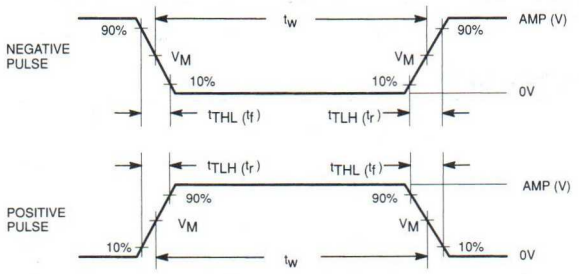


Waveform 1. Propagation delay for inverting outputs

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor;
see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

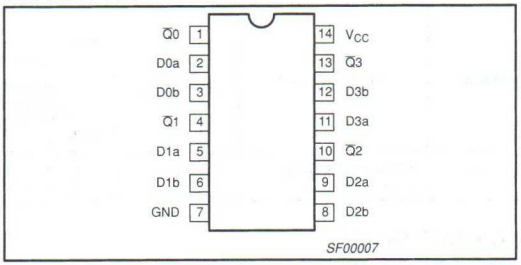
Quad 2-input NOR gate | 74F02

FEATURE

- Industrial temperature range available (–40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F02	3.4ns	4.4mA

PIN CONFIGURATION



ORDERING INFORMATION

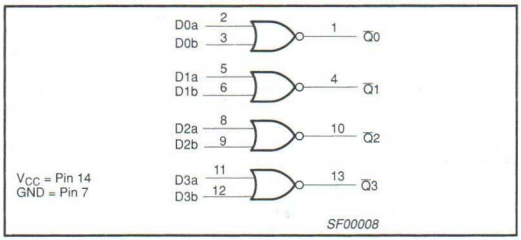
DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
14-pin plastic DIP	N74F02N	I74F02N	SOT27-1
14-pin plastic SO	N74F02D	I74F02D	SOT108-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Q}n$	Data output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.

LOGIC DIAGRAM

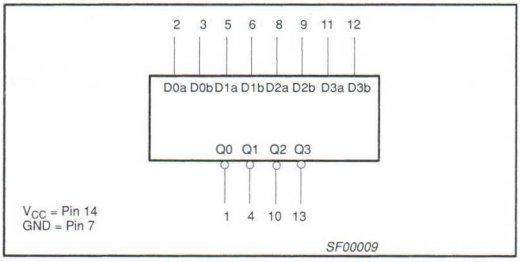


FUNCTION TABLE

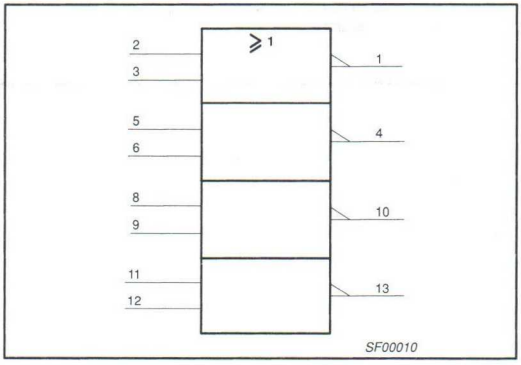
INPUTS		OUTPUT
Dna	Dnb	$\overline{Q}n$
L	L	H
L	H	L
H	L	L
H	H	L

NOTES:
1 H = High voltage level
2 L = Low voltage level

LOGIC SYMBOL



IEC/IEEE SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	−40 to +85	°C
T_{stg}	Storage temperature range		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{Ik}	Input clamp current				−18	mA
I_{OH}	High-level output current				−1	mA
I_{OL}	Low-level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	−40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OI} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)[4]	I_{CCH}	V_{CC} = MAX			3.0	5.6	mA
		I_{CCL}	V_{CC} = MAX			7.0	13.0	mA

NOTES:

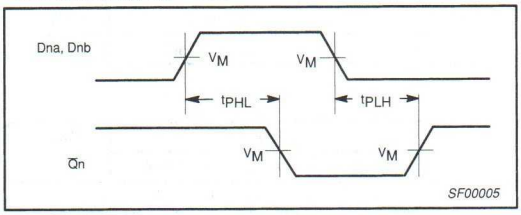
1 For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2 All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3 Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4 I_{CC} is measured with outputs open.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		V_{CC} = +5.0V ± 10% T_{amb} = –40°C to +85°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to $\overline{Q}$n	Waveform 1	2.5 2.0	4.4 3.2	5.5 4.3	2.5 2.0	6.5 5.3	2.5 1.5	7.0 6.0	ns

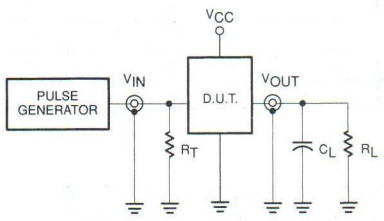
AC WAVEFORMS

For all waveforms, V_M = 1.5V.

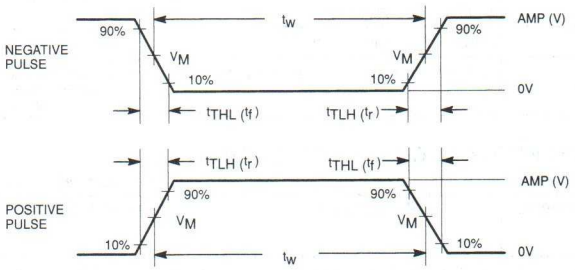


Waveform 1. Propagation delay for inverting outputs

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor;
see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

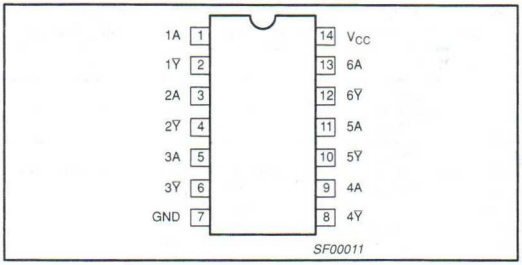
Hex inverter | 74F04

FEATURE

- Industrial temperature range available (–40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F04	3.5ns	6.9mA

PIN CONFIGURATION



ORDERING INFORMATION

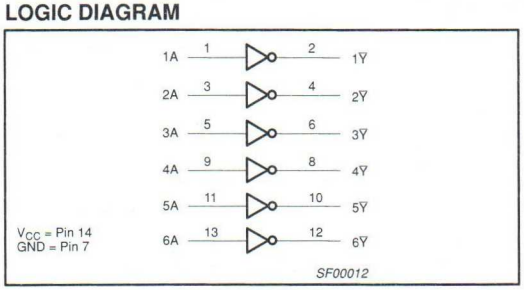
DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
14-pin plastic DIP	N74F04N	I74F04N	SOT27-1
14-pin plastic SO	N74F04D	I74F04D	SOT108-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
nA	Data inputs	1.0/1.0	20μA/0.6mA
nȲ	Data output	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.

LOGIC DIAGRAM

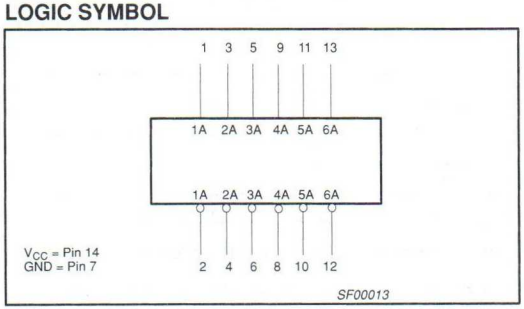


FUNCTION TABLE

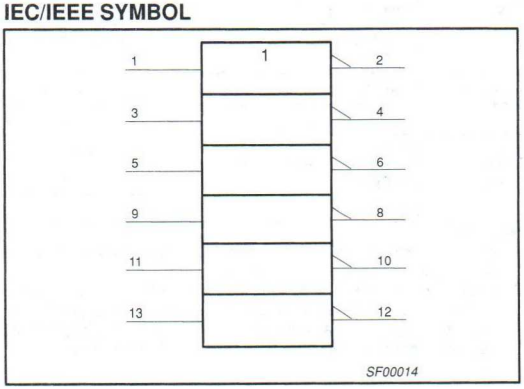
INPUTS	OUTPUT
A	Ȳ
L	H
H	L

NOTES:
H = High voltage level
L = Low voltage level

LOGIC SYMBOL



IEC/IEEE SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current				–1	mA
I_{OL}	Low-level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OI} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		2.8	4.2	mA
		I_{CCL}	V_{CC} = MAX	V_{IN} = 4.5V		10.2	15.3	mA

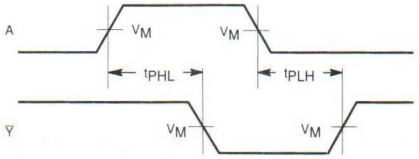
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		V_{CC} = +5.0V ± 10% T_{amb} = –40°C to +85°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay A to $\overline{Y}$	Waveform 1	2.4 1.5	3.7 3.2	5.0 4.3	2.4 1.5	6.0 5.3	1.5 1.1	8.0 6.5	ns

AC WAVEFORMS

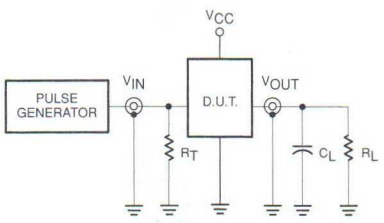


SF00015

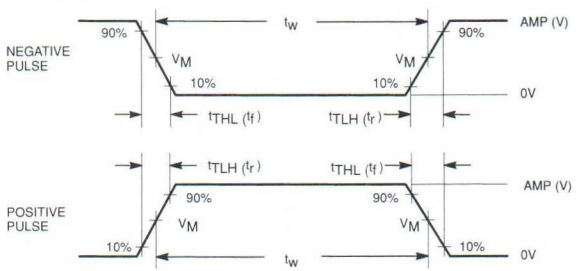
Waveform 1. Propagation delay for inverting outputs

NOTE:
For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor;
see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Hex inverter/buffer drivers (open-collector)

74F06, 74F06A, 74F07, 74F07A

FEATURES OF 74F06, 74F07

- Open Collector output drive 64mA
- High speed
- 12V output termination voltage
- Symmetrical propagation delays

FEATURES OF 74F06A, 74F07A

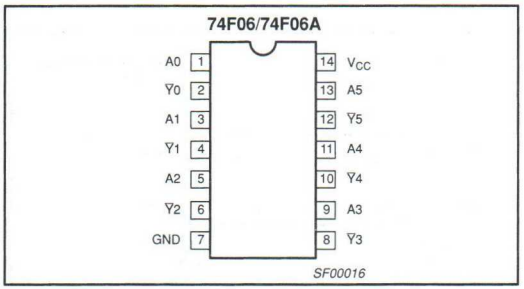
- Open Collector output drive 48mA
- High speed
- 30V output termination voltage
- Replaces 74F06 and 74F07
- Improved performance upgrade for 74F06 and 74F07
- Reduced I_{OH} leakage @ 30V

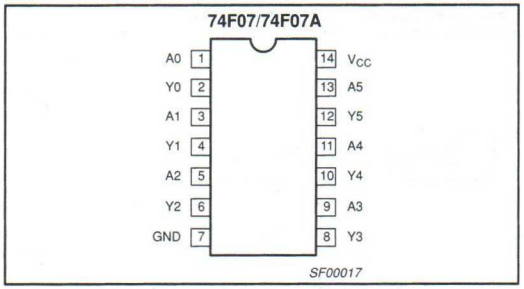
TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F06	3.5ns	30mA
74F06A	9.0ns	30mA
74F07	4.5ns	32mA
74F07A	10.0ns	32mA

ORDERING INFORMATION

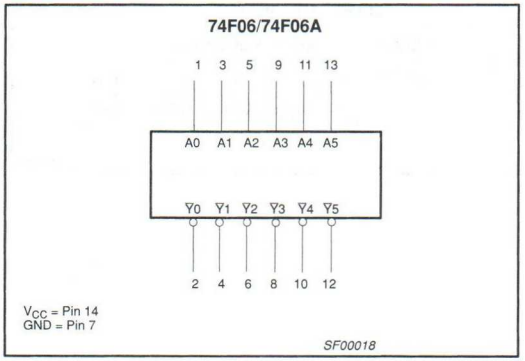
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
14-pin plastic Dual In-line Package	N74F06N, N74F06AN	SOT27–1
14-pin plastic Small Outline	N74F07D, N74F07AD	SOT108–1

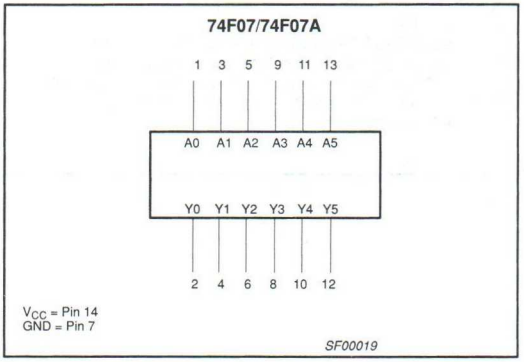
PIN CONFIGURATIONS



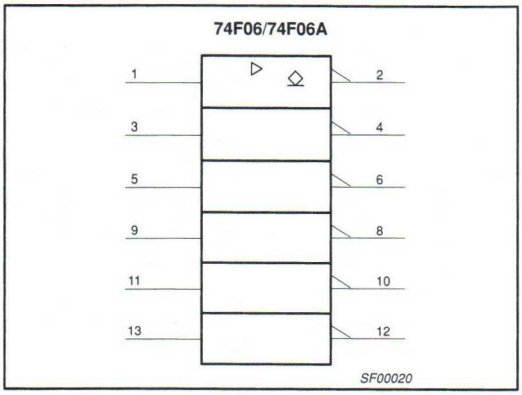


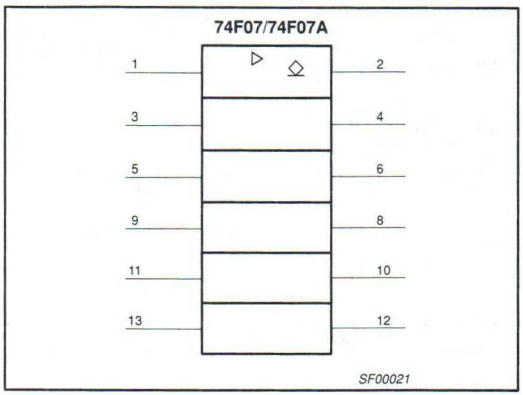
LOGIC SYMBOLS



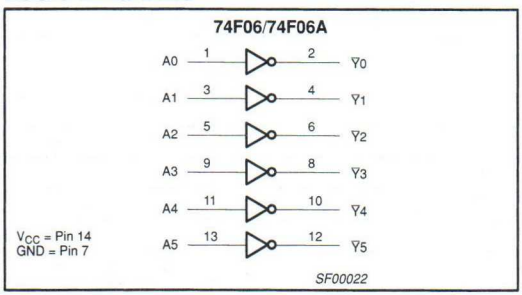


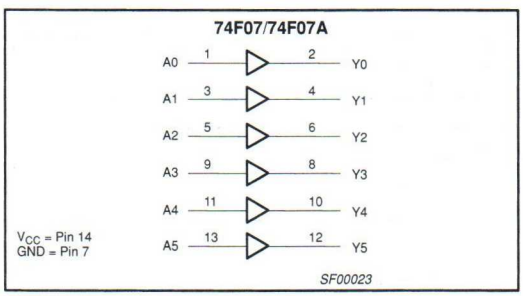
IEC/IEEE SYMBOLS





LOGIC DIAGRAMS





INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
An	Data inputs ('F06, 'F07)	1.0/1.0	20μA/0.6mA
An	Data inputs ('F06A, 'F07A)	1.0/0.7	20μA/0.4mA
$\overline{Y}n$	Data outputs ('F06)	OC/106.7	OC/64mA
$\overline{Y}n$	Data outputs ('F06A)	OC/80	OC/48mA
Yn	Data outputs ('F07)	OC/106.7	OC/64mA
Yn	Data outputs ('F07A)	OC/80	OC/48mA

NOTES:
1. One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.
2. OC = Open Collector

FUNCTION TABLE

INPUTS	OUTPUTS	
	'F06, 'F06A	'F07, 'F07A
An	$\overline{Y}n$	Yn
L	H	L
H	L	H

NOTES:
1. H = High voltage level
2. L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	'F06, 'F07	–0.5 to 12	V
		'F06A, 'F07A	–0.5 to 30	V
I_{OUT}	Current applied to output in Low output state	'F06, 'F07	128	mA
		'F06A, 'F07A	96	mA
T_{amb}	Operating free air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
V_{OH}	High-level output voltage	'F06, 'F07			12	V
		'F06A, 'F07A			30	V
I_{OL}	Low-level output current	'F06, 'F07			64	mA
		'F06A, 'F07A			48	mA
T_{amb}	Operating free air temperature range		0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
I_{OH}	High-level output current	'F06, 'F07	V_{CC} = MIN, V_{IL} = MAX, V_{OH} = MAX, V_{IH} = MIN					250	µA
		'F06A, 'F07A						100	µA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = MAX	±10% V_{CC}		0.30	0.50	V
			V_{IH} = MIN		±5% V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	'F06, 'F07	V_{CC} = MAX, V_I = 0.5V					–0.6	mA
		'F06A, 'F07A						–0.4	mA
I_{CC}	Supply current (total)	74F06, 74F06A	I_{CCH}	V_{CC} = MAX			5.0	8.0	mA
			I_{CCL}				30	43	mA
		74F07, 74F07A	I_{CCH}				10	14	mA
			I_{CCL}				32	45	mA

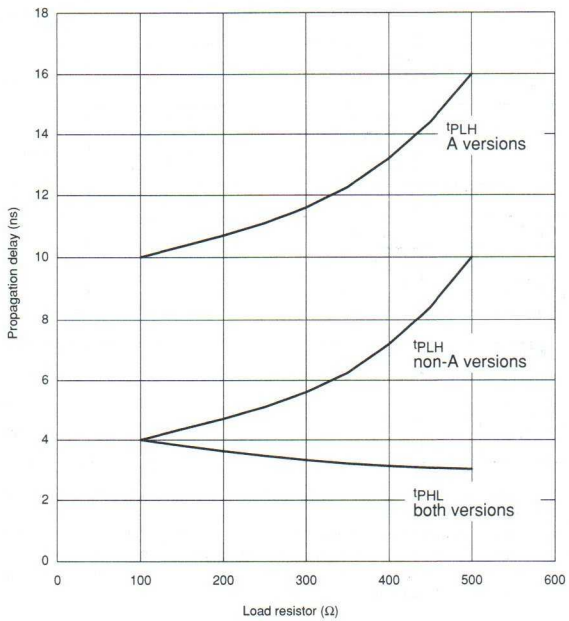
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

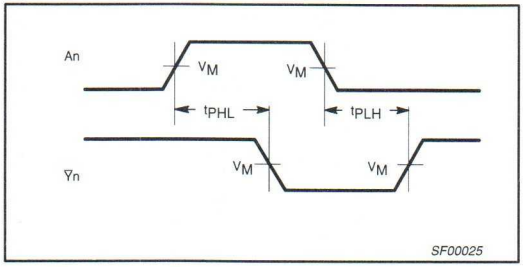
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 100Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 100Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to $\overline{Y}$n	'F06	Waveform 1	2.0 1.5	3.5 3.0	6.0 5.5	1.5 1.0	6.5 6.0	ns
		'F06A		5.0 2.0	9.0 4.0	11.0 6.0	4.0 2.0	15.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay An to Yn	'F07	Waveform 2	2.0 3.0	4.0 5.0	6.0 7.0	2.0 2.5	6.5 7.5	ns
		'F07A		6.0 5.0	10.5 7.5	13.0 10.0	5.0 4.0	17.0 13.0	ns

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS

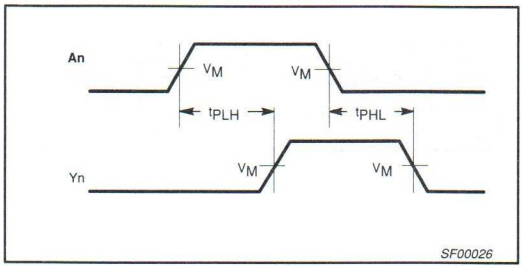


NOTE:
When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers does not exceed the I_{OL} maximum specification.

AC WAVEFORMS



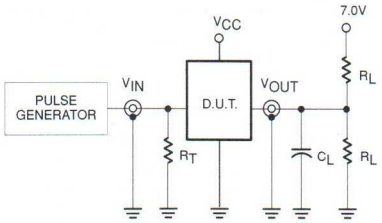
Waveform 1. Propagation delay for inverting outputs



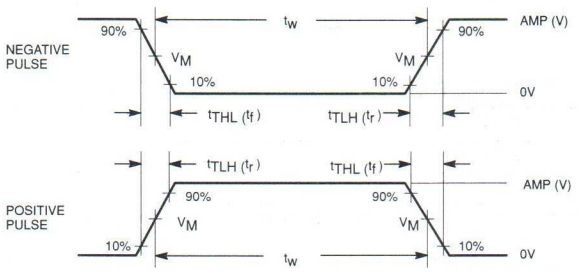
Waveform 2. Propagation delay for non-inverting outputs

NOTE:
For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs



Input Pulse Definition

DEFINITIONS:

R_L = Load resistor;
see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

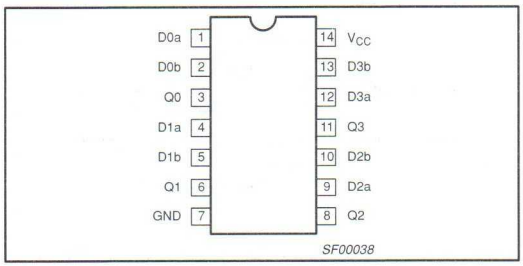
SF00027

Quad 2-input AND gate — 74F08

- 74F08 Available for industrial range (–40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F08	4.1ns	7.1mA

PIN CONFIGURATION



ORDERING INFORMATION

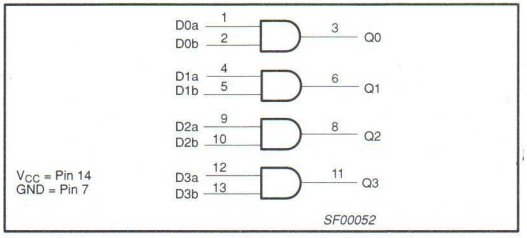
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5.0V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5.0V ±10%, T_{amb} = –40°C to +85°C	PKG DWG #
14-pin plastic DIP	N74F08N	I74F08N	SOT27-1
14-pin plastic SO	N74F08D	I74F08D	SOT108-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb	Data inputs	1.0/1.0	20μA/0.6mA
Qn	Data output	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

LOGIC DIAGRAM

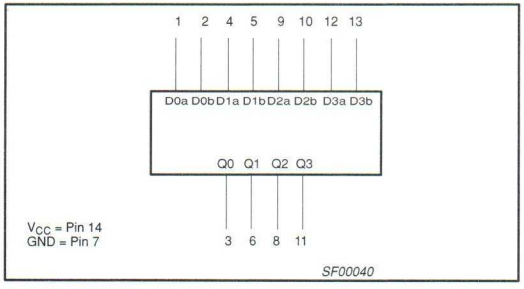


FUNCTION TABLE

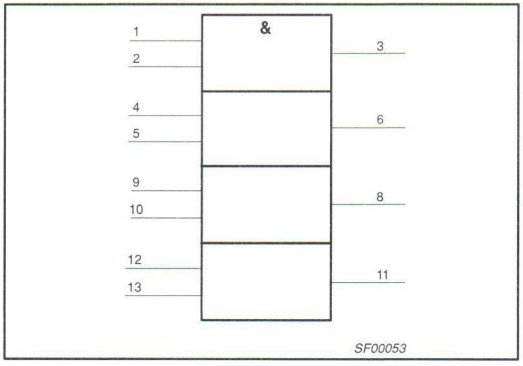
INPUTS		OUTPUT
Dna	Dnb	Qn
L	L	L
L	H	L
H	L	L
H	H	H

NOTES:
H = High voltage level
L = Low voltage level

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state		40	mA
T_{amb}	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{Ih}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current				–1	mA
I_{OL}	Low-level output current				20	mA
T_{amb}	Operating free-air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OI} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = 4.5V		5.5	8.3	mA
		I_{CCL}	V_{CC} = MAX	V_{IN} = GND		8.6	12.9	mA

NOTES:

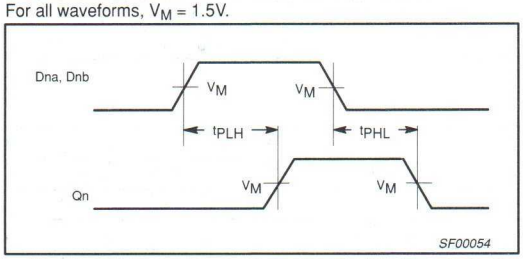
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to Qn	Waveform 1	3.0 2.5	4.2 4.0	5.6 5.3	3.0 2.5	6.6 6.3	2.5 2.5	6.6 6.3	ns

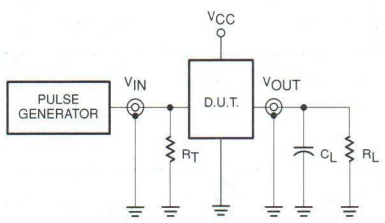
AC WAVEFORMS

For all waveforms, V_M = 1.5V.

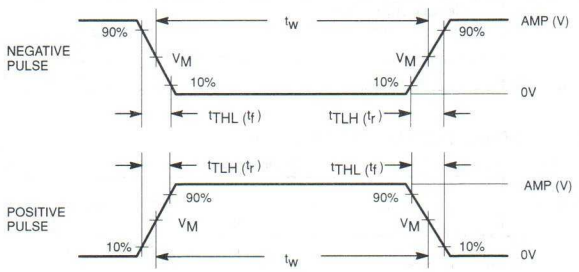


Waveform 1. Propagation Delay for Non-Inverting Outputs

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor;
see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

74F10 Triple 3-input NAND gate
74F11 Triple 3-input AND gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F10	3.5ns	3.3mA
74F11	4.2ns	5.3mA

ORDERING INFORMATION

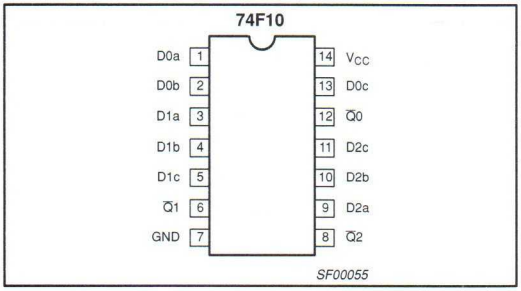
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
14-pin plastic DIP	N74F10N, N74F11N	SOT27-1
14-pin plastic SO	N74F10D, N74F11D	SOT108-1

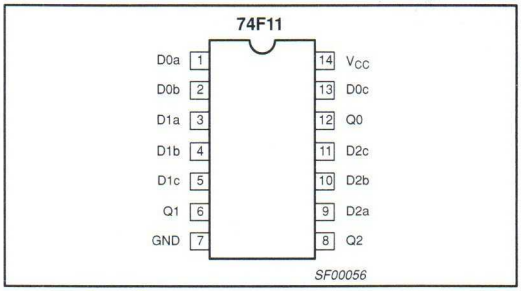
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb, Dnc	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Q}$n	Data output (74F10)	50/33	1.0mA/20mA
Qn	Data output (74F11)	50/33	1.0mA/20mA

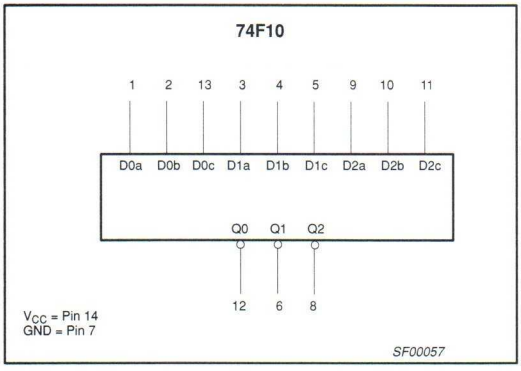
NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

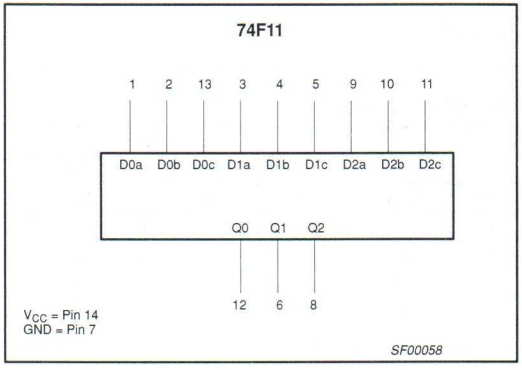
PIN CONFIGURATIONS



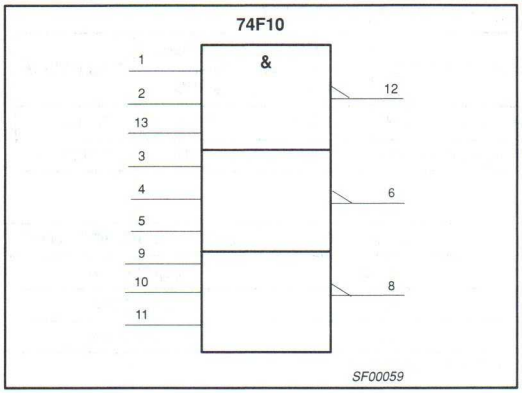


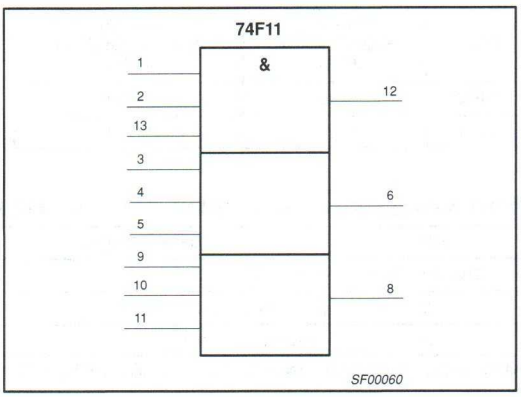
LOGIC SYMBOLS



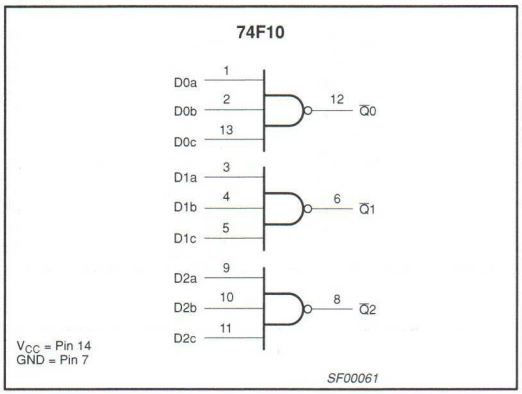


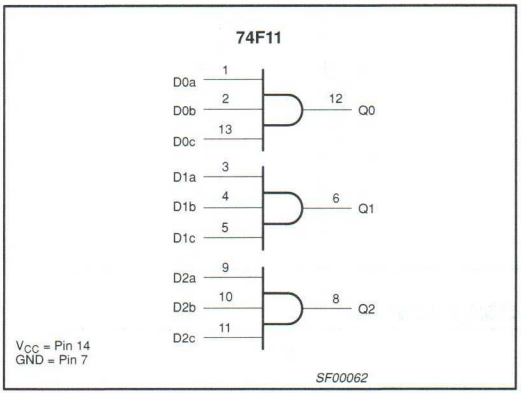
IEC/IEEE SYMBOLS





LOGIC DIAGRAMS





FUNCTION TABLE

INPUTS			OUTPUTS	
			74F10	74F11
Dna	Dnb	Dnc	$\overline{Q}n$	Qn
L	L	L	H	L
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	L	H

NOTES:
1. H = High voltage level
2. L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
				V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
				V_{IH} = MIN, I_{OI} = MAX	±5%V_{CC}		0.35	0.50	
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	74F10	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		1.8	2.1	mA
			I_{CCL}		V_{IN} = 4.5V		6.0	7.7	
		74F11	I_{CCH}	V_{CC} = MAX	V_{IN} = 4.5V		4.7	6.2	mA
			I_{CCL}		V_{IN} = GND		7.2	9.7	

NOTES:

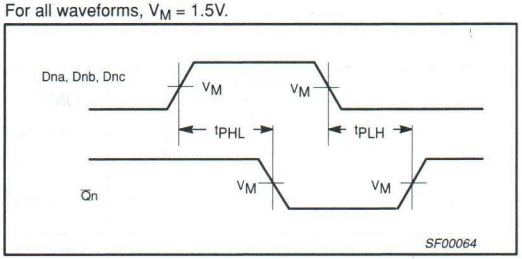
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

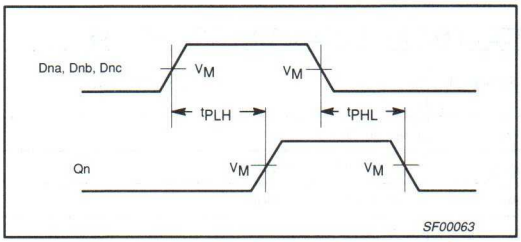
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb, Dnc to $\overline{Q}n$	74F10	Waveform 1	2.4 1.5	3.7 3.2	5.0 4.3	2.4 1.5	6.0 5.3	ns
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb, Dnc to Qn	74F11	Waveform 2	3.0 2.5	4.2 4.1	5.6 5.5	3.0 2.5	6.6 6.5	ns

AC WAVEFORMS

For all waveforms, V_M = 1.5V.

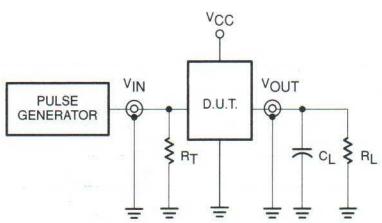


Waveform 1. Propagation Delay for Inverting Outputs (74F10)

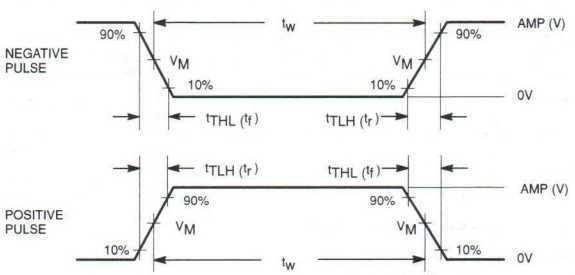


Waveform 2. Propagation Delay for Non-Inverting Outputs (74F11)

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

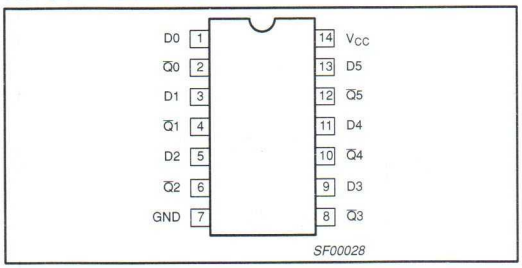
Hex inverter Schmitt trigger | 74F14

FEATURE

- Industrial temperature range available (–40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F14	5.0ns	18mA

PIN CONFIGURATION



DESCRIPTION

The 74F14 contains six logic inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter free output signals. In addition, they have greater noise margin than conventional inverters. Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive-going and negative-going input threshold (typically 800mV) is determined internally by resistor ratios and is insensitive to temperature and supply voltage variations.

ORDERING INFORMATION

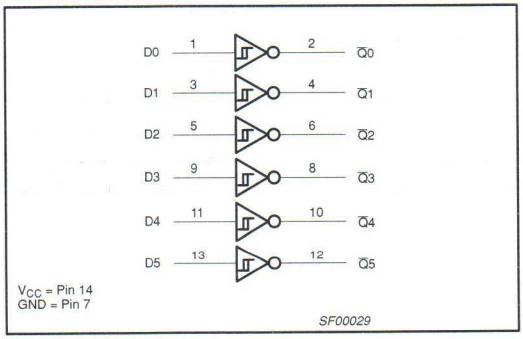
DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
14-pin plastic DIP	N74F14N	I74F14N	SOT27-1
14-pin plastic SO	N74F14D	I74F14D	SOT108-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dn	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}n$	Data output	50/33	1.0mA/20mA

NOTE:
1 One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

LOGIC DIAGRAM

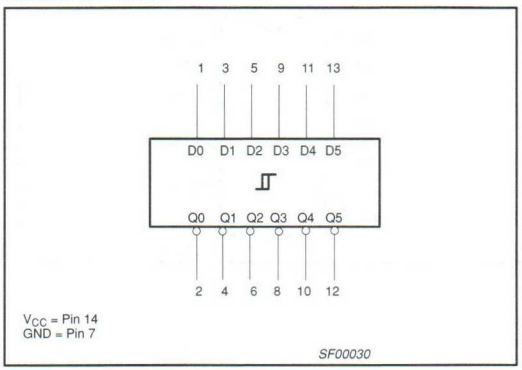


FUNCTION TABLE

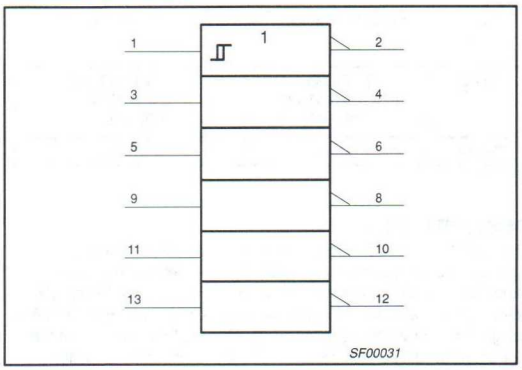
INPUTS	OUTPUT
Dn	$\overline{Q}n$
L	H
H	L

NOTES:
H = High voltage level
L = Low voltage level

LOGIC SYMBOL



IEC/IEEE SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		40	mA
T_{amb}	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High-level output current				–1	mA
I_{OL}	Low-level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{T+}	Positive-going threshold		V_{CC} = 5.0V		1.4	1.7	2.0	V
V_{T-}	Negative-going threshold		V_{CC} = 5.0V		0.7	0.9	1.1	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = 5.0V		0.4	0.8		V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_I = V_{T-MIN},	±10%V_{CC}	2.5			V
			I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_I = V_{T+MAX},	±10%V_{CC}		0.30	0.50	V
			I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_{T+}	Input current at positive-going threshold		V_{CC} = 5.0V, V_I = V_{T+}			0		µA
I_{T-}	Input current at negative-going threshold		V_{CC} = 5.0V, V_I = V_{T-}			–175		µA
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		13	22	mA
		I_{CCL}	V_{CC} = MAX	V_{IN} = 4.5V		23	32	mA

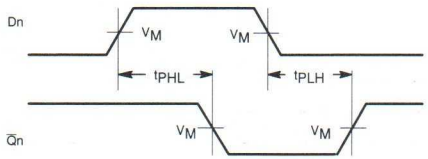
NOTES:

1 For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2 All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3 Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		V_{CC} = +5.0V ± 10% T_{amb} = –40°C to +85°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to $\overline{Q}$n	Waveform 1	4.0 3.5	6.5 5.0	8.5 6.5	4.0 3.5	9.5 7.0	3.0 3.5	10.5 9.0	ns

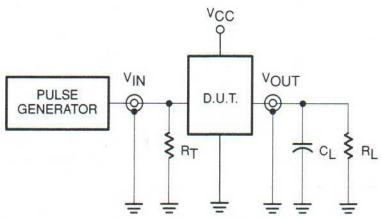
AC WAVEFORMS



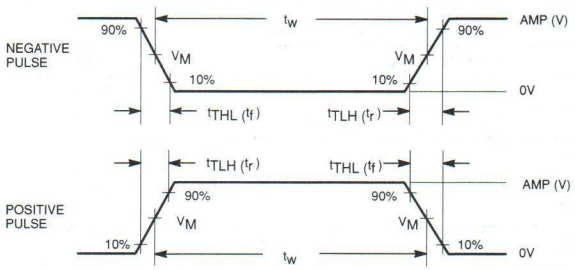
Waveform 1. Propagation delay for inverting outputs

NOTE:
For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor;
see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

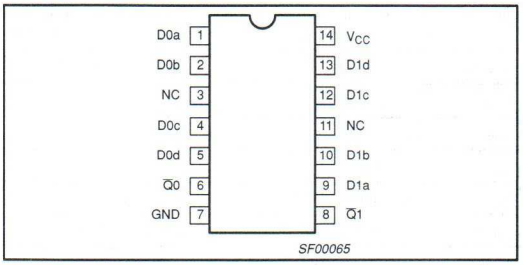
Dual 4-input NAND gate | 74F20

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F20	3.5ns	2.2mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
14-pin plastic DIP	N74F20N	SOT27-1
14-pin plastic SO	N74F20D	SOT108-1

PIN CONFIGURATION

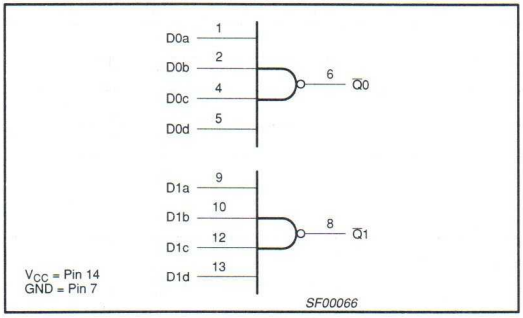


INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb, Dnc, Dnd	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}0$, $\overline{Q}1$	Data outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

LOGIC DIAGRAM

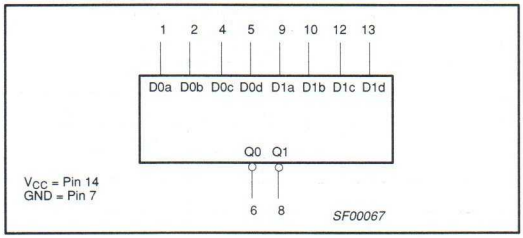


FUNCTION TABLE

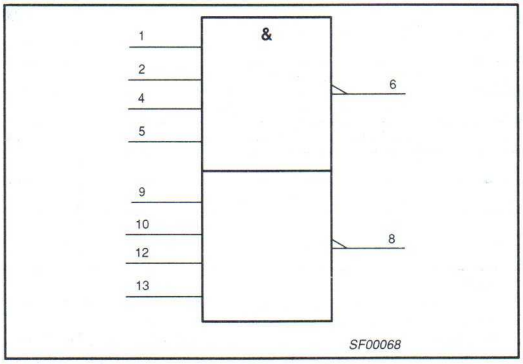
INPUTS				OUTPUT
Dna	Dnb	Dnc	Dnd	$\overline{Q}n$
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

LOGIC SYMBOL



IEC/IEEE SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		0.9	1.4	mA
		I_{CCL}		V_{IN} = 4.5V		3.4	5.1	

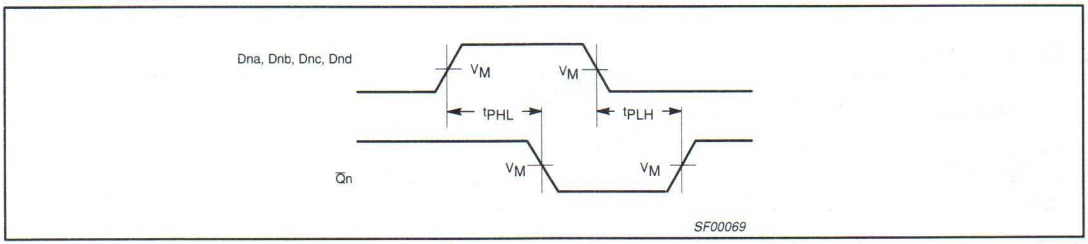
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb, Dnc, Dnd to $\overline{Q}$n	Waveform 1	2.4 2.0	3.7 3.2	5.0 4.3	2.4 2.0	6.0 5.3	ns

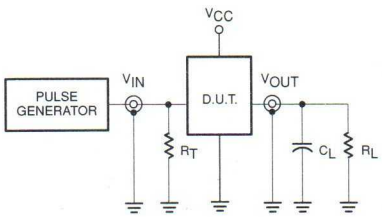
AC WAVEFORMS



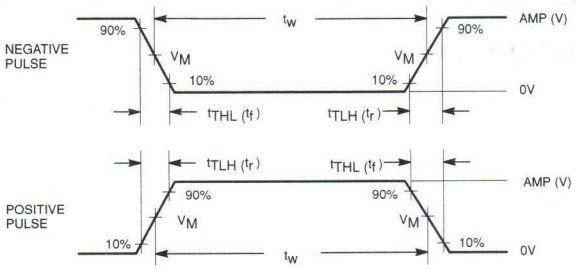
Waveform 1. Propagation Delay for Inverting Outputs

NOTE:
For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor;
see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

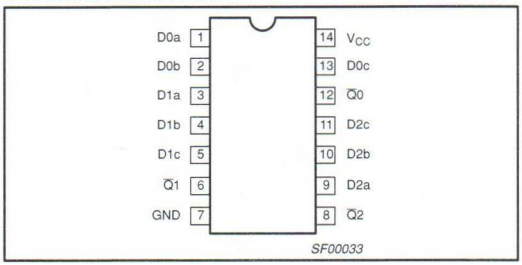
Triple 3-input NOR gate | 74F27

FEATURE

- Industrial temperature range available (–40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F27	3.0ns	6.5mA

PIN CONFIGURATION



ORDERING INFORMATION

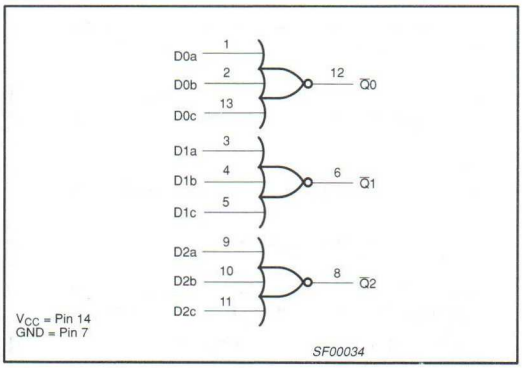
DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
14-pin plastic DIP	N74F27N	I74F27N	SOT27-1
14-pin plastic SO	N74F27D	I74F27D	SOT108-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb, Dnc	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}$n	Data output	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

LOGIC DIAGRAM

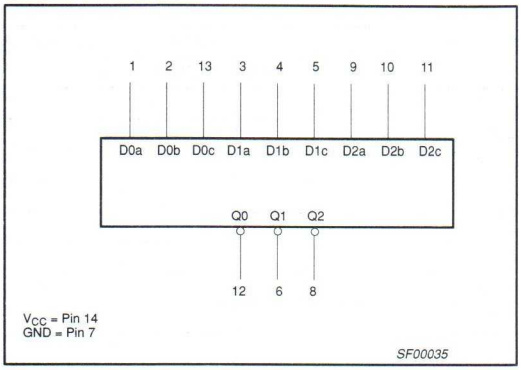


FUNCTION TABLE

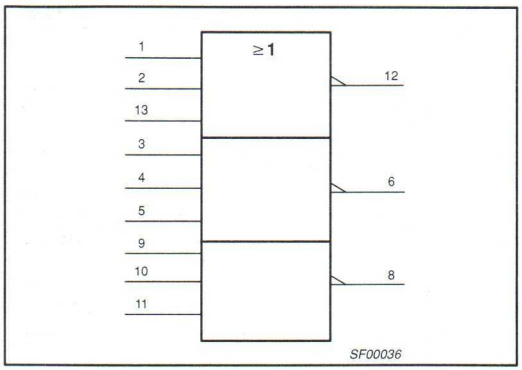
INPUTS			OUTPUT
Dna	Dnb	Dnc	$\overline{Q}$n
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

NOTES:
H = High voltage level
L = Low voltage level

LOGIC SYMBOL



IEC/IEEE SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current				–1	mA
I_{OL}	Low–level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OI} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		4.0	5.5	mA
		I_{CCL}	V_{CC} = MAX	V_{IN} = 4.5V		8.5	12.0	mA

NOTES:

1 For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

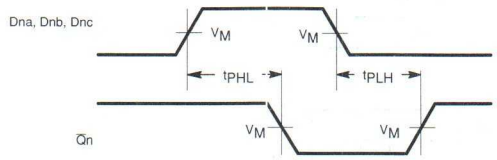
2 All typical values are at V_{CC} = 5V, T_{amb} = 25°C.

3 Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		V_{CC} = +5.0V ± 10% T_{amb} = –40°C to +85°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb, Dnc to $\overline{Q}$n	Waveform 1	2.0 1.0	3.5 2.5	5.0 4.5	1.5 1.0	5.5 4.5	1.0 1.0	7.0 5.5	ns

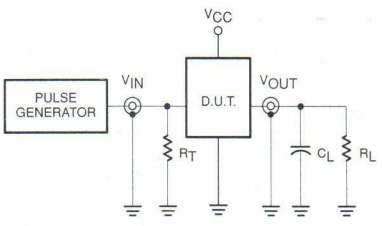
AC WAVEFORMS



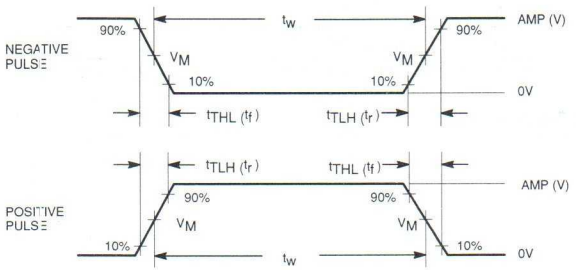
Waveform 1. Propagation delay for inverting outputs

NOTE:
For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor;
see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

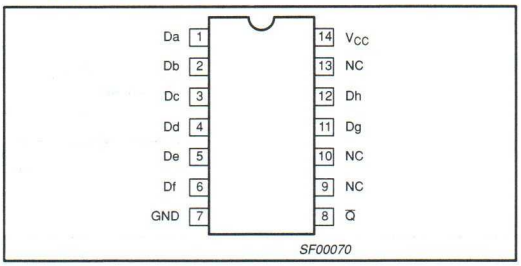
SF00006

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F30	3.2ns	1.7mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
14-pin plastic DIP	N74F30N	SOT27-1
14-pin plastic SO	N74F30D	SOT108-1

PIN CONFIGURATION

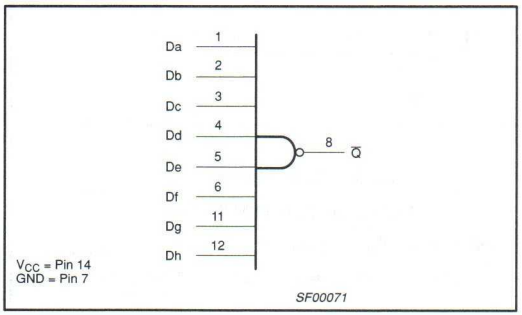


INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dn	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Q}$	Data output	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

LOGIC DIAGRAM

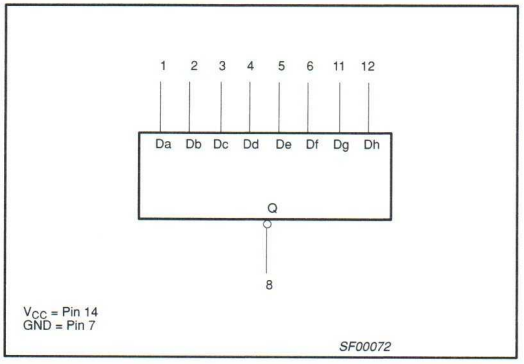


FUNCTION TABLE

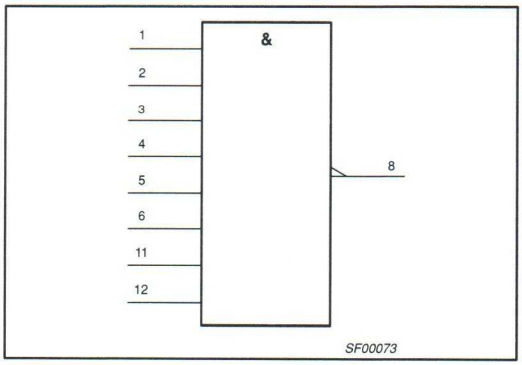
INPUTS								OUTPUT
Dna	Dnb	Dnc	Dnd	Dne	Dnf	Dng	Dnh	$\overline{Q}$n
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

NOTES:
1. H = High voltage level
2. L = Low voltage level
3. X = Don't care

LOGIC SYMBOL



IEC/IEEE SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		0.6	1.5	mA
		I_{CCL}		V_{IN} = 4.5V		2.8	4.0	

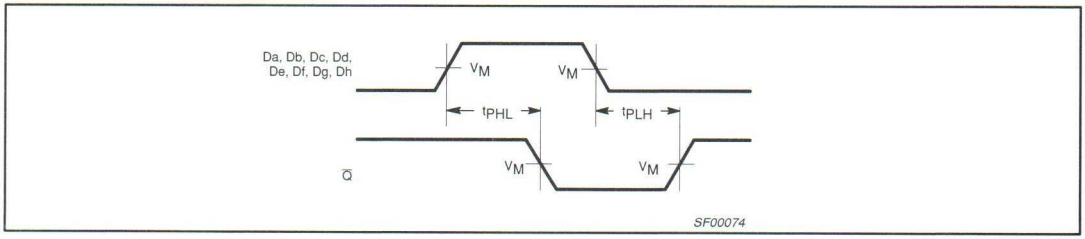
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Da, Db, Dc, Dd, De, Df, Dg, Dh to $\overline{Q}$	Waveform 1	1.5 1.0	3.5 3.0	5.0 4.5	1.5 1.0	5.5 5.0	ns

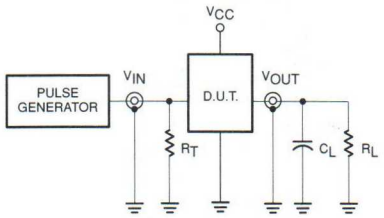
AC WAVEFORMS



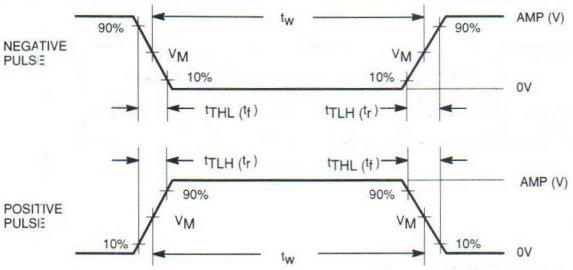
Waveform 1. Propagation Delay for Inverting Outputs

NOTE:
For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

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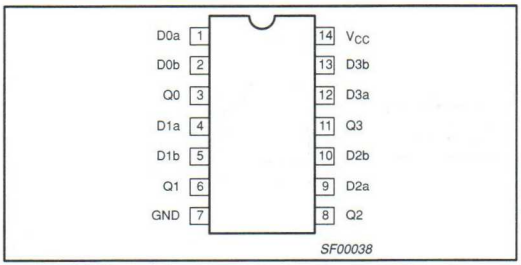
Quad 2-input OR gate | 74F32

FEATURE

- Industrial temperature range available (–40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F32	4.1ns	8.2mA

PIN CONFIGURATION



ORDERING INFORMATION

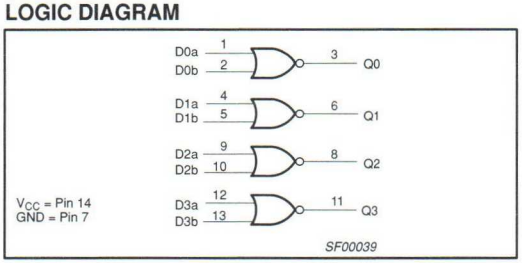
DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
14-pin plastic DIP	N74F32N	I74F32N	SOT27-1
14-pin plastic SO	N74F32D	I74F32D	SOT108–1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb	Data inputs	1.0/1.0	20µA/0.6mA
Qn	Data output	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

LOGIC DIAGRAM

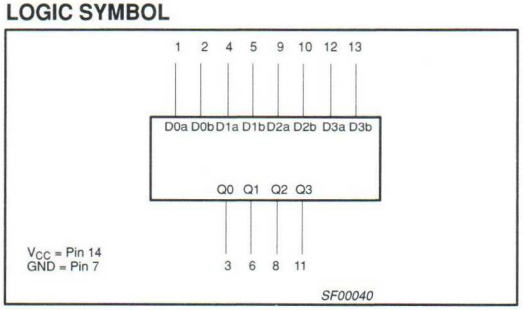


FUNCTION TABLE

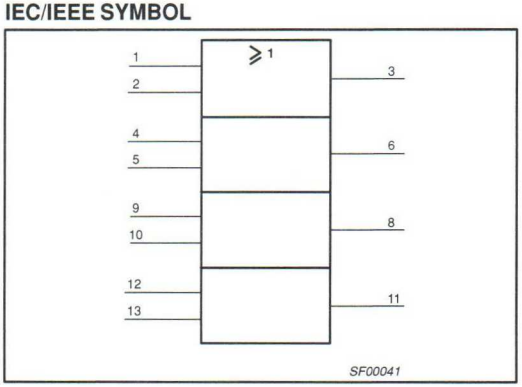
INPUTS		OUTPUT
Dna	Dnb	Qn
L	L	L
L	H	H
H	L	H
H	H	H

NOTES:
1 H = High voltage level
2 L = Low voltage level

LOGIC SYMBOL



IEC/IEEE SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High-level output current				–1	mA
I_{OL}	Low-level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OI} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = 4.5V		6.1	9.2	mA
		I_{CCL}	V_{CC} = MAX	V_{IN} = GND		10.3	15.5	mA

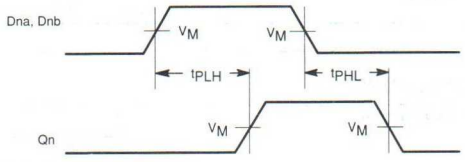
NOTES:

1 For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2 All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3 Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		V_{CC} = +5.0V ± 10% T_{amb} = –40°C to +85°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to Qn	Waveform 1	3.0 3.0	4.2 4.0	5.6 5.3	3.0 3.0	6.6 6.3	3.0 3.0	6.6 6.3	ns

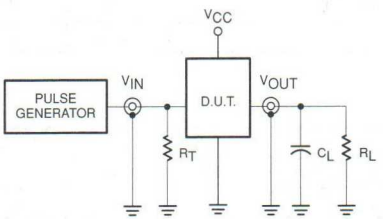
AC WAVEFORMS



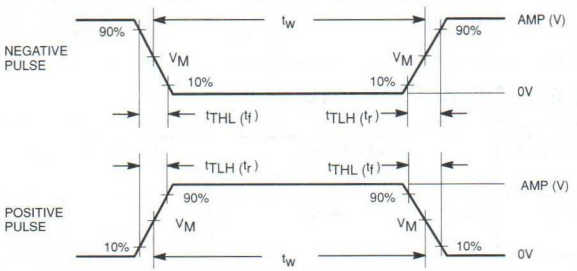
Waveform 1. Propagation delay for inverting outputs

NOTE:
For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor;
see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

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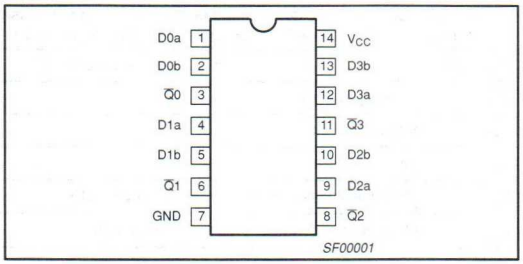
Quad 2-input NAND buffer 74F37

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F37	3.5ns	13mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
14-pin plastic DIP	N74F37N	SOT27-1
14-pin plastic SO	N74F37D	SOT108-1

PIN CONFIGURATION

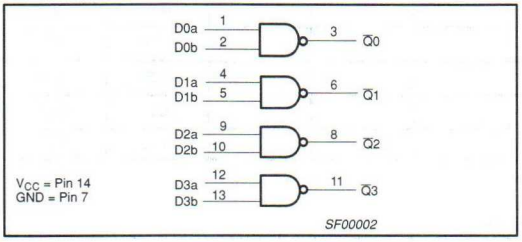


INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb	Data inputs	1.0/2.0	20μA/1.2mA
$\overline{Q}$n	Data outputs	750/106.6	15mA/64mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

LOGIC DIAGRAM

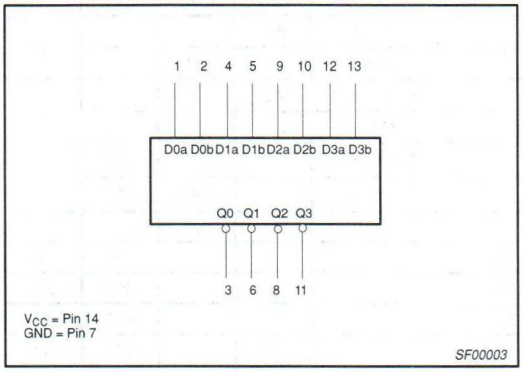


FUNCTION TABLE

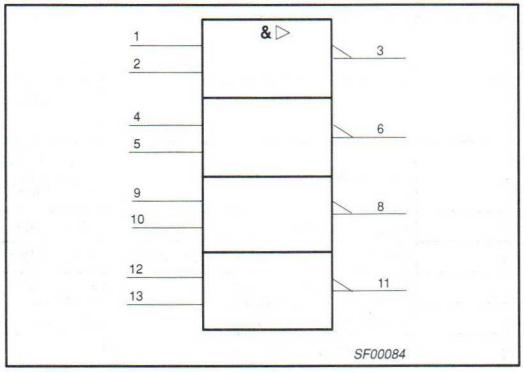
INPUTS		OUTPUT
Dna	Dnb	$\overline{Q}$n
L	L	H
L	H	H
H	L	H
H	H	L

NOTES:
1. H = High voltage level
2. L = Low voltage level

LOGIC SYMBOL



IEC/IEEE SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–15	mA
I_{OL}	Low-level output current			64	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		
				I_{OH} = –15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					–1.2	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			–100		–225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX		V_{IN} = GND		3.0	6.0	mA
		I_{CCL}			V_{IN} = 4.5V		23	33	

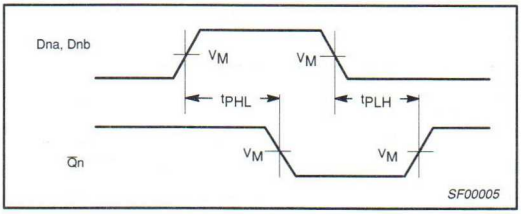
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to $\overline{Q}$n	Waveform 1	2.5 1.5	3.5 2.5	5.5 4.5	2.0 1.5	6.5 5.0	ns

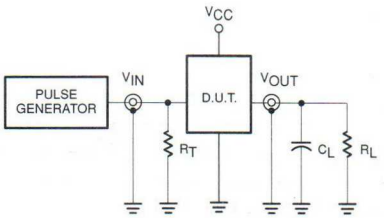
AC WAVEFORMS



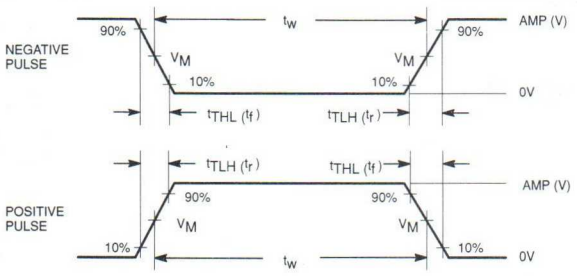
Waveform 1. Propagation Delay for Inverting Outputs

NOTE:
For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:

R_L = Load resistor;
see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SF00006

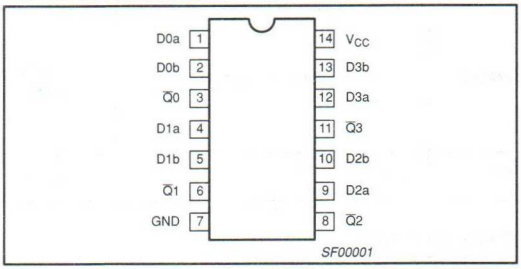
Quad 2-input NAND buffer (open collector) 74F38

FEATURE

- Industrial temperature range available (–40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F38	7.0ns	13mA

PIN CONFIGURATION



ORDERING INFORMATION

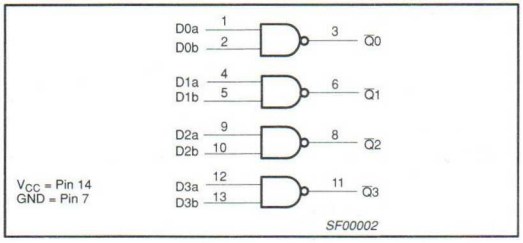
DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
14-pin plastic DIP	N74F38N	I74F38N	SOT27-1
14-pin plastic SO	N74F38D	I74F38D	SOT108-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb	Data inputs	1.0/2.0	20μA/1.2mA
$\overline{Q}$n	Data output	OC/106.7	OC/64mA

NOTES:
1 One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.
2 OC = open collector

LOGIC DIAGRAM

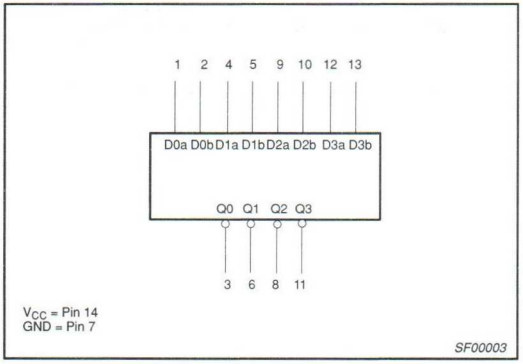


FUNCTION TABLE

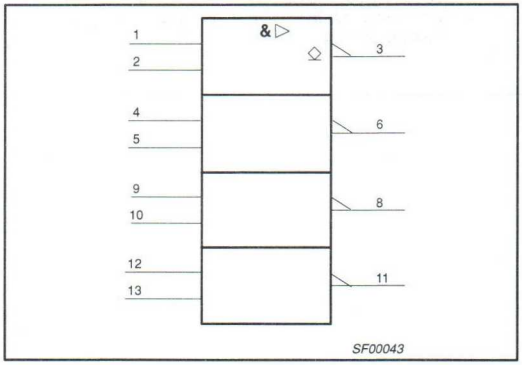
INPUTS		OUTPUT
Dna	Dnb	$\overline{Q}$n
L	L	H
L	H	H
H	L	H
H	H	L

NOTES:
H = High voltage level
L = Low voltage level

LOGIC SYMBOL



IEC/IEEE SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		128	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
V_{OH}	High-level output voltage				4.5	V
I_{OL}	Low-level output current				64	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

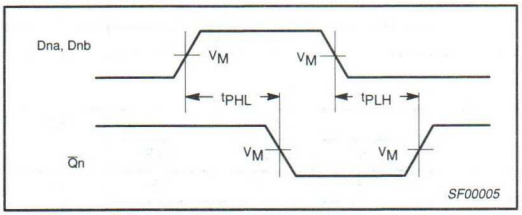
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX				250	µA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}			0.55	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-1.2	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		4.0	7.0	mA
		I_{CCL}	V_{CC} = MAX	V_{IN} = 4.5V		22	30	mA

NOTES:
1 For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2 All typical values are at V_{CC} = 5V, T_{amb} = 25°C.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		V_{CC} = +5.0V ± 10% T_{amb} = –40°C to +85°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to $\overline{Q}$n	Waveform 1	7.5 1.5	10.0 3.0	12.5 5.0	7.5 1.5	13.0 5.5	7.5 1.5	14.5 6.0	ns

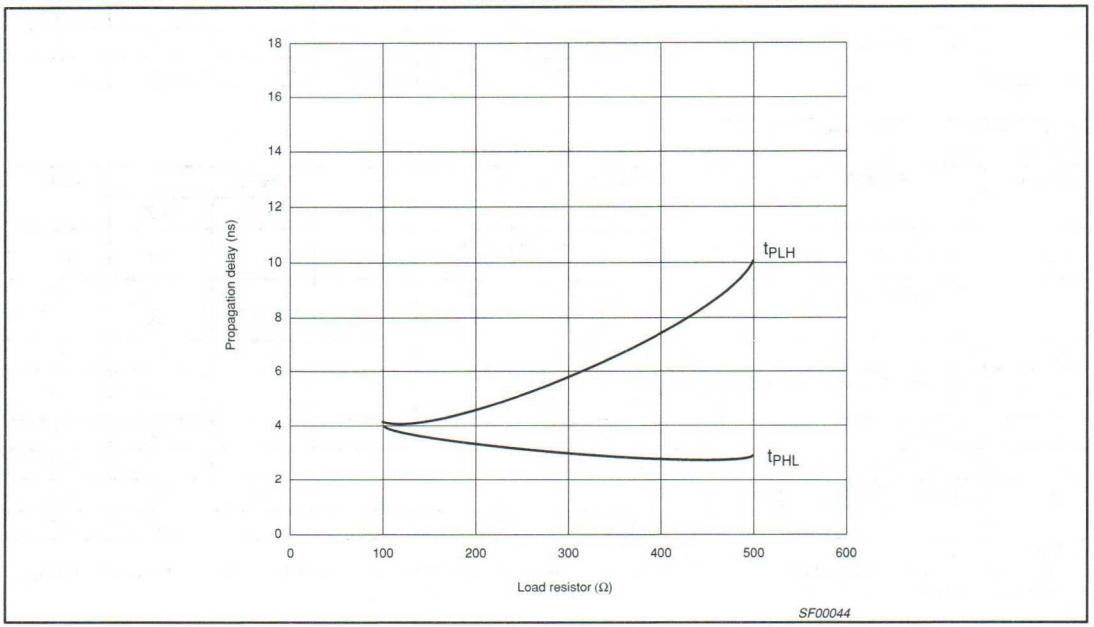
AC WAVEFORMS



Waveform 1. Propagation delay for inverting outputs

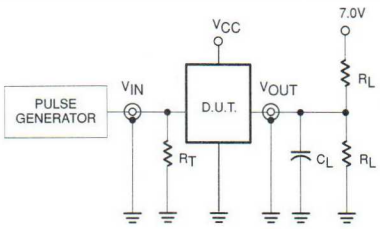
NOTE:
For all waveforms, V_M = 1.5V.

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS

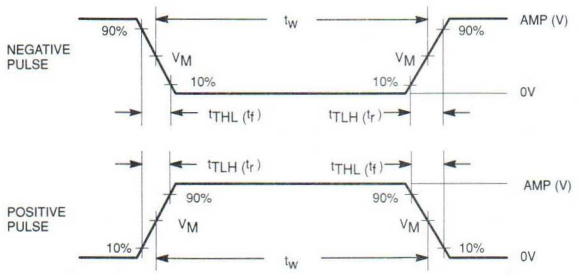


NOTE:
1 When using open collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers does not exceed the I_{OL} minimum specification.

TEST CIRCUIT AND WAVEFORM



Test Circuit for Open Collector Outputs



Input Pulse Definition

DEFINITIONS:

R_L = Load resistor;
see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00027

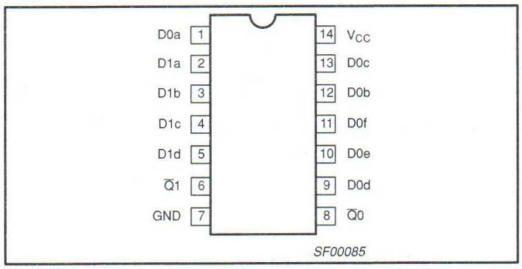
Dual 2-wide 2-input, 2-wide 3-input AND-OR-invert gate — 74F51

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F51	3.0ns	3.5mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
14-pin plastic DIP	N74F51N	SOT27-1
14-pin plastic SO	N74F51D	SOT108-1

PIN CONFIGURATION

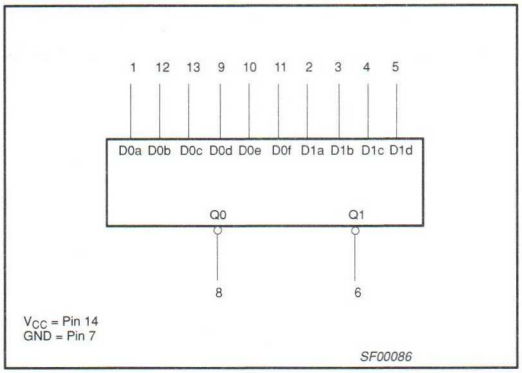


INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

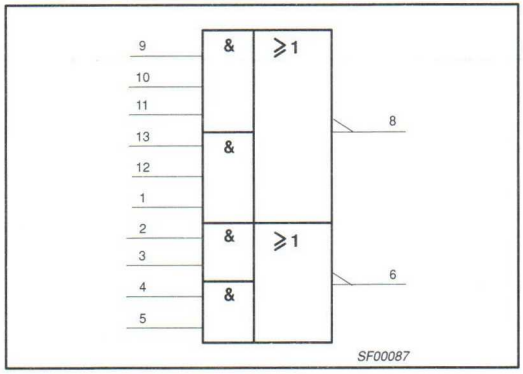
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb, Dnc, Dnd, Dne, Dnf	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}$0, $\overline{Q}$1	Data outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

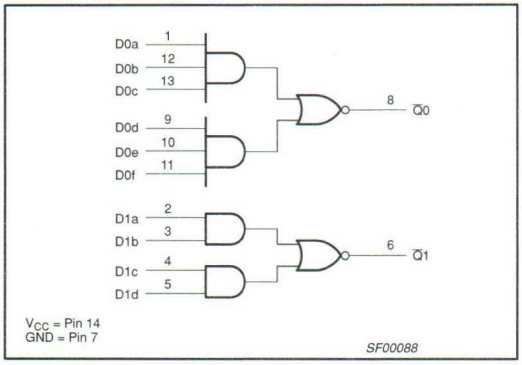
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE FOR 3-INPUT GATES

INPUTS						OUTPUT
D0a	D0b	D0c	D0d	D0e	D0f	$\overline{Q}$0
H	H	H	X	X	X	L
X	X	X	H	H	H	L
All other combinations						H

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION TABLE FOR 2-INPUT GATES

INPUTS				OUTPUT
D1a	D1b	D1c	D1d	$\overline{Q}$1
H	H	X	X	L
X	X	H	H	L
All other combinations				H

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		1.8	3.0	mA
		I_{CCL}		V_{IN} = 4.5V		5.5	7.5	mA

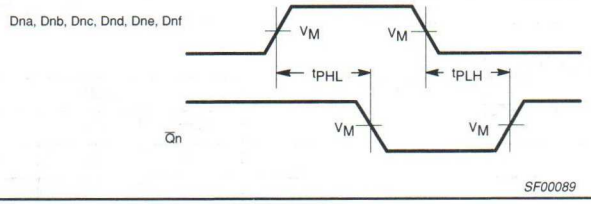
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb, Dnc, Dnd, Dne, Dnf to $\overline{Q}$n	Waveform 1	2.0 1.0	3.5 2.5	5.5 4.0	1.5 1.0	6.5 4.5	ns

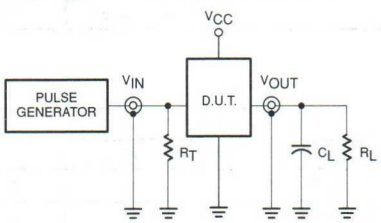
AC WAVEFORMS



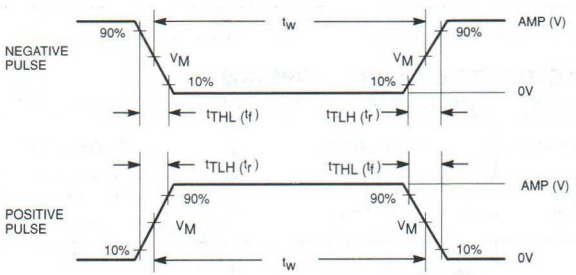
Waveform 1. Propagation Delay for Inverting Outputs

NOTE:
For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor;
see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

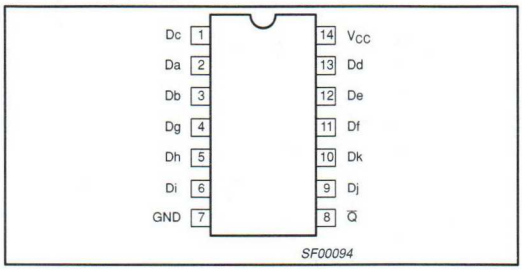
4-2-3-2-input AND-OR-invert gate 74F64

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F64	4.0ns	2.5mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG. DWG. #
14-pin plastic DIP	N74F64N	SOT27-1
14-pin plastic SO	N74F64D	SOT108-1

PIN CONFIGURATION

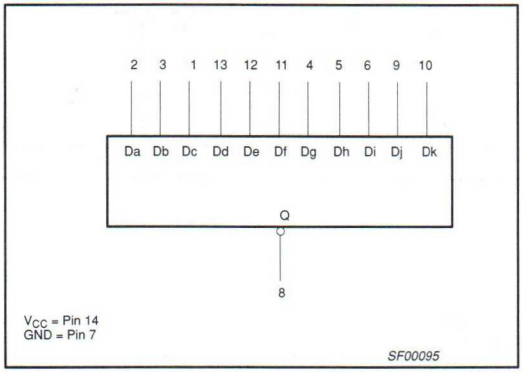


INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

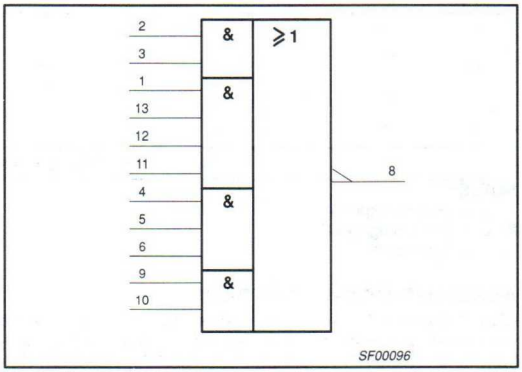
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dn	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}$	Data output	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

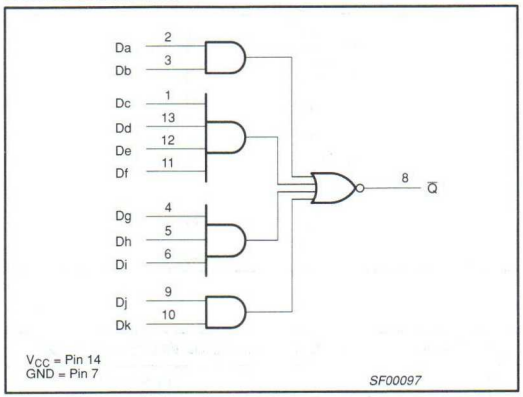
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS											OUTPUT
Da	Db	Dc	Dd	De	Df	Dg	Dh	Di	Dj	Dk	$\overline{Q}$
H	H	X	X	X	X	X	X	X	X	X	L
X	X	H	H	H	H	X	X	X	X	X	L
X	X	X	X	X	X	H	H	H	X	X	L
X	X	X	X	X	X	X	X	X	H	H	L
All other combinations											H

NOTES:
1. H = High voltage level
2. L = Low voltage level
3. X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		1.9	2.8	mA
		I_{CCL}		V_{IN} = 4.5V		3.1	4.7	mA

NOTES:

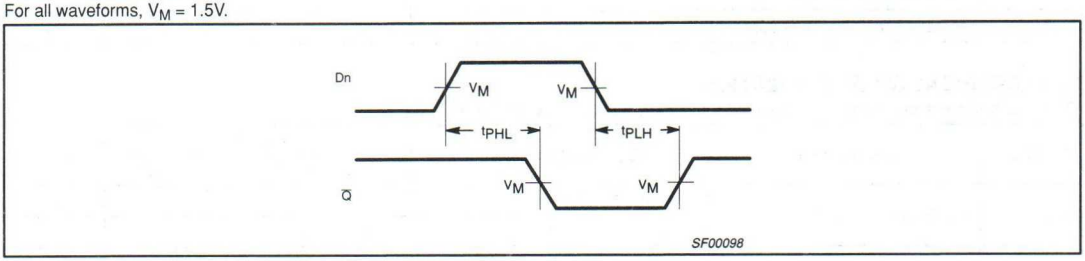
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to $\overline{Q}$	Waveform 1	2.5 2.0	4.6 3.2	6.0 4.5	2.5 2.0	7.0 5.5	ns

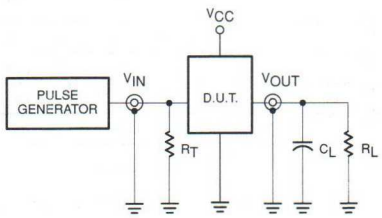
AC WAVEFORMS

For all waveforms, V_M = 1.5V.

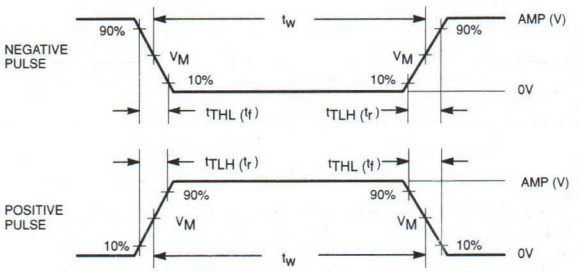


Waveform 1. Propagation Delay for Inverting Outputs

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Dual D-type flip-flop 74F74

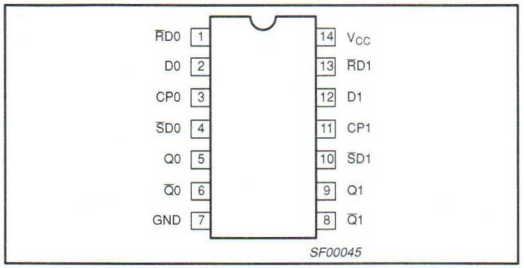
FEATURE

- Industrial temperature range available (–40°C to +85°C)

DESCRIPTION

The 74F74 is a dual positive edge-triggered D-type flip-flop featuring individual data, clock, set, and reset inputs; also true and complementary outputs. Set ($\overline{SD}$) and reset ($\overline{RD}$) are asynchronous active low inputs and operate independently of the clock input. When set and reset are inactive (high), data at the D input is transferred to the Q and $\overline{Q}$ outputs on the low-to-high transition of the clock. Data must be stable just one setup time prior to the low-to-high transition of the clock for predictable operation. Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the D input may be changed without affecting the levels of the output.

PIN CONFIGURATION



TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F74	125MHz	11.5mA

ORDERING INFORMATION

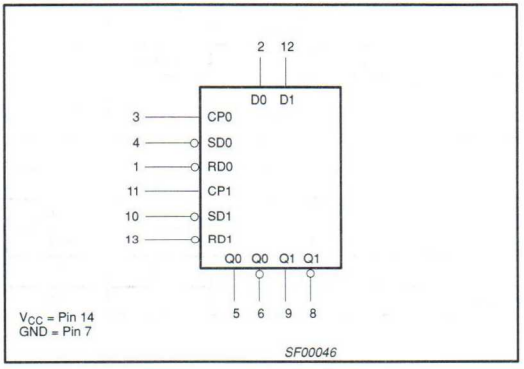
DESCRIPTION	ORDER CODE		PKG. DWG. #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
14-pin plastic DIP	N74F74N	I74F74N	SOT27-1
14-pin plastic SO	N74F74D	I74F74D	SOT108-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

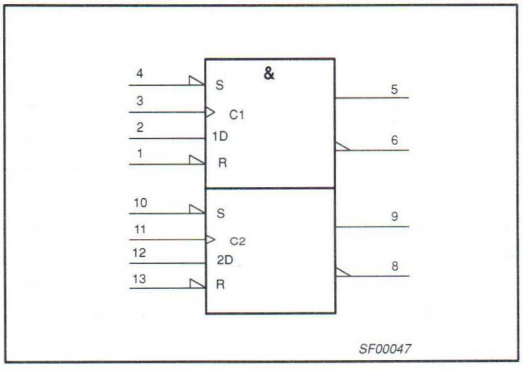
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0, D1	Data inputs	1.0/1.0	20µA/0.6mA
CP0, CP1	Clock inputs (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{SD}0$, $\overline{SD}1$	Set inputs (active low)	1.0/3.0	20µA/1.8mA
$\overline{RD}0$, $\overline{RD}1$	Reset inputs (active low)	1.0/3.0	20µA/1.8mA
Q0, Q1, $\overline{Q}0$, $\overline{Q}1$	Data outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

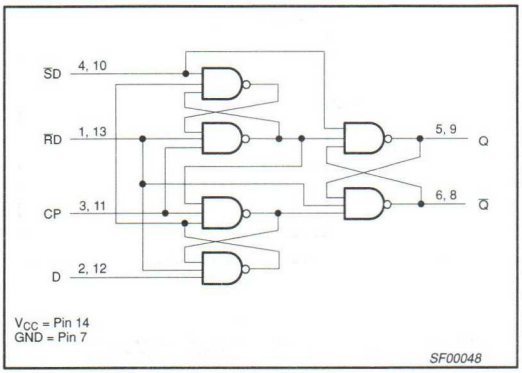
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$	
L	H	X	X	H	L	Asynchronous set
H	L	X	X	L	H	Asynchronous reset
L	L	X	X	H	H	Undetermined*
H	H	↑	h	H	L	Load "1"
H	H	↑	l	L	H	Load "0"
H	H	↕	X	NC	NC	Hold

NOTES:
H = High voltage level
h = High voltage level one setup time prior to low-to-high clock transition
L = Low voltage level
l = Low voltage level one setup time prior to low-to-high clock transition
NC = No change from the previous setup
X = Don't care
↑ = Low-to-high clock transition
↕ = Not low-to-high clock transition
* = This setup is unstable and will change when either set or reset return to the high level.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High-level output current				–1	mA
I_{OL}	Low-level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	Dn, CPn	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
		$\overline{SD}$n, $\overline{RD}$n	V_{CC} = MAX, V_I = 0.5V					-1.8	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total) [4]		V_{CC} = MAX				11.5	16	mA

NOTES:

1 For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2 All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3 Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4 Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs high in turn.

AC ELECTRICAL CHARACTERISTICS

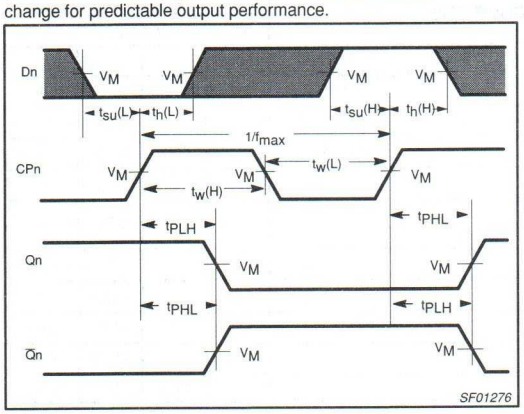
SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		V_{CC} = +5.0V ± 10% T_{amb} = –40°C to +85°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	100	125		100		90		MHz
t_{PLH} t_{PHL}	Propagation delay CPn to Qn or $\overline{Q}$n	Waveform 1	3.8 4.4	5.3 6.2	6.8 8.0	3.8 4.4	7.8 9.2	3.8 4.4	8.5 9.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SD}$n, $\overline{RD}$n to Qn or $\overline{Q}$n	Waveform 2	3.2 3.5	4.6 7.0	6.1 9.0	3.2 3.5	7.1 10.5	3.2 2.5	7.5 10.5	ns

AC SETUP REQUIREMENTS

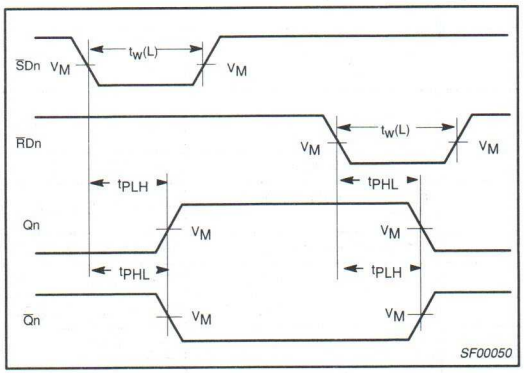
SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		V_{CC} = +5.0V ± 10% T_{amb} = –40°C to +85°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low Dn to CPn	Waveform 1	2.0 3.0			2.0 3.0		2.0 3.0		ns
t_h (H) t_h (L)	Hold time, high or low Dn to CPn	Waveform 1	1.0 1.0			1.0 1.0		1.0 1.0		ns
t_w (H) t_w (L)	CPn pulse width, high or low	Waveform 1	4.0 5.0			4.0 5.0		4.0 5.0		ns
t_w (L)	$\overline{SD}$n, $\overline{RD}$n pulse width, low	Waveform 2	4.0			4.0		4.0		ns
t_{rec}	Recovery time $\overline{SD}$n, $\overline{RD}$n to CPn	Waveform 3	2.0			2.0		2.0		ns

AC WAVEFORMS

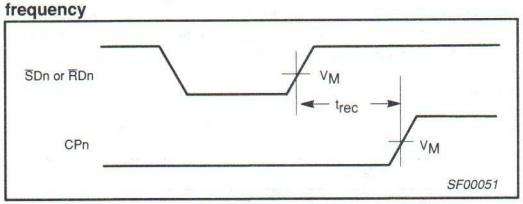
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation delay for data to output, data setup time and hold times, and clock width, and maximum clock frequency

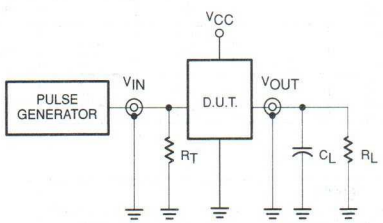


Waveform 2. Propagation delay for set and reset to output, set and reset pulse width

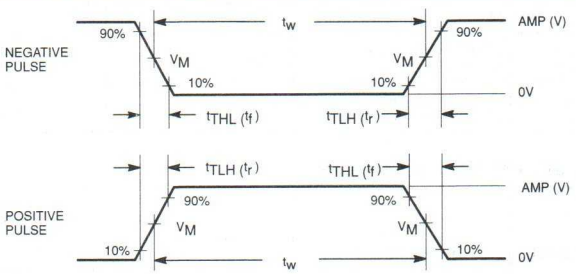


Waveform 3. Recovery time for set or reset to clock

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SF00006

4-bit magnitude comparator | 74F85

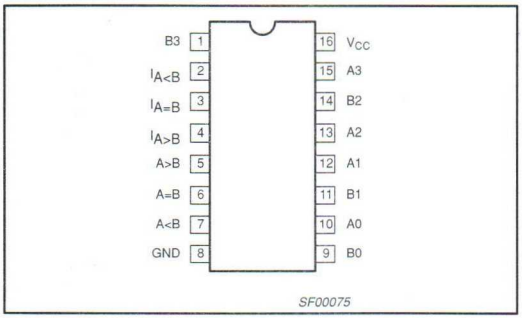
FEATURES

- High-impedance NPN base inputs for reduced loading (20μA in High and Low states)
- Magnitude comparison of any binary words
- Serial or parallel expansion without extra gating

DESCRIPTION

The 74F85 is a 4-bit magnitude comparator that can be expanded to almost any length. It compares two 4-bit binary, BCD, or other monotonic codes and presents the three possible magnitude results at the outputs. The 4-bit inputs are weighted (A0–A3) and (B0–B3) where A3 and B3 are the most significant bits. The operation of the 74F85 is described in the Function Table, showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme. In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed-forward conditions that exist in the parallel expansion scheme. The expansion inputs $I_{A>B}$, and $I_{A=B}$ and $I_{A<B}$ are the least significant bit positions. When used for series expansion, the A>B, A=B and A<B outputs of the lease significant word are connected to the corresponding $I_{A>B}$, $I_{A=B}$ and $I_{A<B}$ inputs of the next higher stage. Stages can be added in this manner to any length, but a propagation delay penalty of about 15ns is added with each additional stage. For proper operation, the expansion inputs of the least significant word should be tied as follows: $I_{A>B}$ = Low, $I_{A=B}$ = High, and $I_{A<B}$ = Low.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F85	7.0ns	40mA

ORDERING INFORMATION

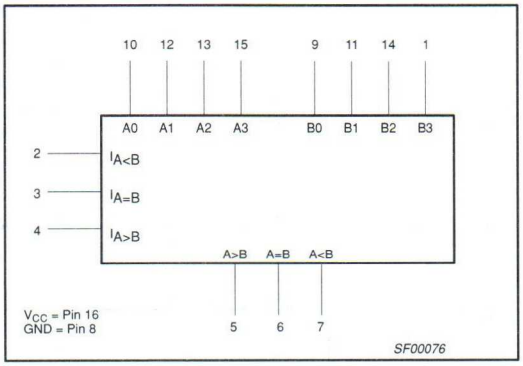
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
16-pin plastic DIP	N74F85N	SOT38-4
16-pin plastic SO	N74F85D	SOT162-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

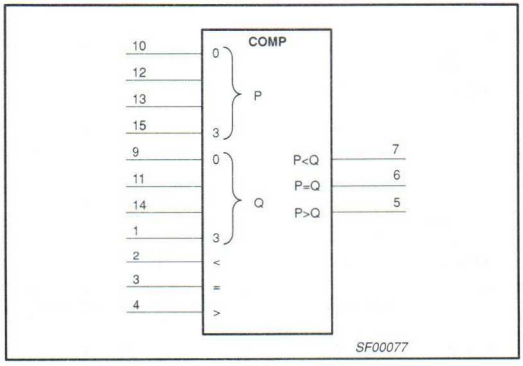
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0–A3	Comparing inputs	1.0/0.033	20μA/20μA
B0–B3	Comparing inputs	1.0/0.033	20μA/20μA
$I_{A<B}$, $I_{A=B}$, $I_{A>B}$	Expansion inputs (active High)	1.0/0.033	20μA/20μA
A<B, A=B, A>B	Data outputs (active High)	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

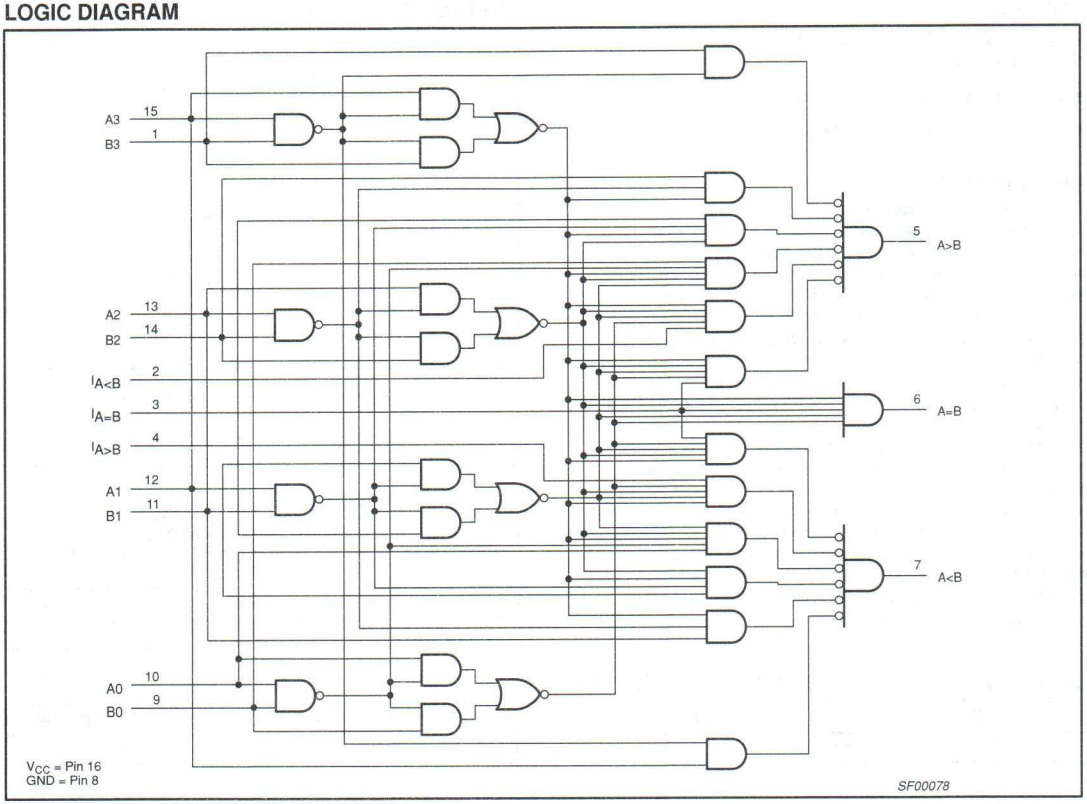
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

COMPARING INPUTS				EXPANSION INPUTS			OUTPUTS		
A3,B3	**A2,B2**	**A1,B1**	**A0,B0**	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	**A>B**	**A<B**	**A=B**
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

APPLICATION

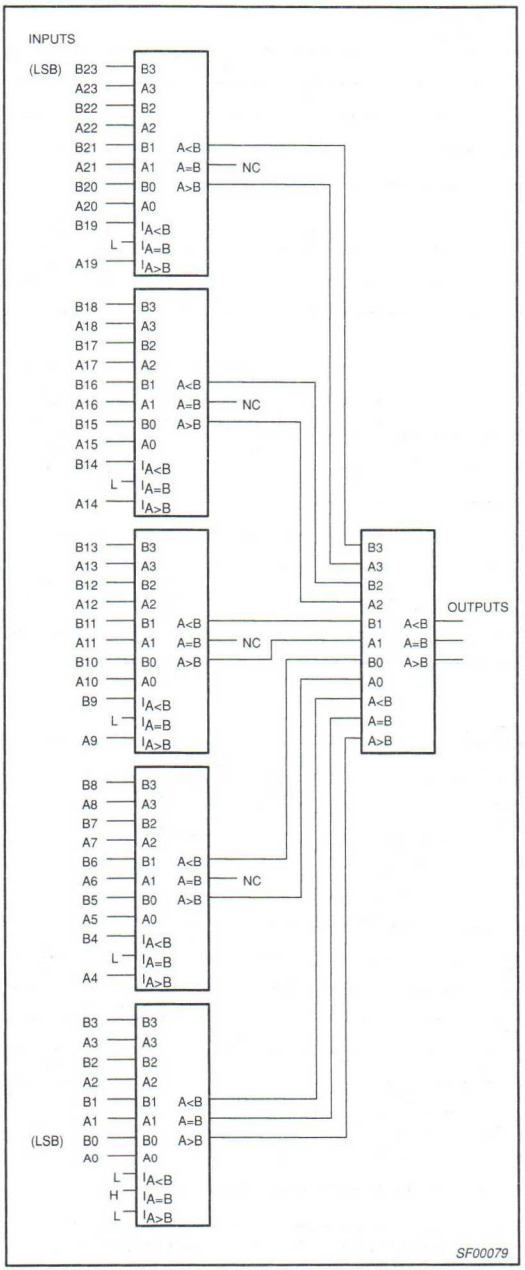


Figure 1. Comparison of Two 24-Bit Words

The parallel expansion scheme shown in Figure 1 demonstrates the most efficient general use of these comparators. The expansion inputs can be used as a fifth input bit position except on the least significant device, which must be connected as in the serial scheme. The expansion inputs used by labeling $I_{A>B}$ as an "A" input, $I_{A<B}$ as a "B" input and setting $I_{A=B}$ = Low. The 74F85 can be used as a 5-bit comparator only when the outputs are used to drive the (A0–A3) and (B0–B3) inputs of another 74F85 device. The parallel technique can be expanded to any number of bits as shown in Table 1.

Table 1.

WORD LENGTH	NUMBER OF PACKAGES	TYPICAL SPEEDS 74F
1–4 bits	1	12ns
5–24 bits	2–6	22ns
25–120 bits	8–31	34ns

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–20	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		36	50	mA
		I_{CCL}		An = Bn = $I_{A=B}$ = GND, $I_{A>B}$ = $I_{A<B}$ = 4.5V		40	54	

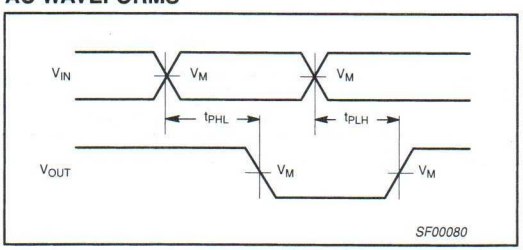
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay A or B to A<B, A>B	Waveform 1 3 logic levels	6.0 7.0	8.5 9.5	11.0 14.0	5.5 6.5	13.0 15.5	ns
t_{PLH} t_{PHL}	Propagation delay A or B to A=B	Waveform 1 4 logic levels	6.5 7.0	9.0 9.5	11.5 14.0	6.0 6.5	14.0 14.5	ns
t_{PLH} t_{PHL}	Propagation delay $I_{A<B}$ and $I_{A=B}$ to A>B	Waveform 1 1 logic level	3.0 3.0	5.0 6.0	7.5 9.0	2.5 2.5	9.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $I_{A=B}$ to A=B	Waveform 1 2 logic levels	2.5 3.5	4.5 7.5	7.0 10.0	2.0 2.5	9.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $I_{A>B}$ and $I_{A=B}$ to A<B	Waveform 1 1 logic level	3.0 3.0	5.0 6.0	8.0 9.0	3.0 2.0	9.5 9.5	ns

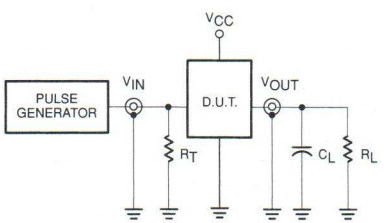
AC WAVEFORMS



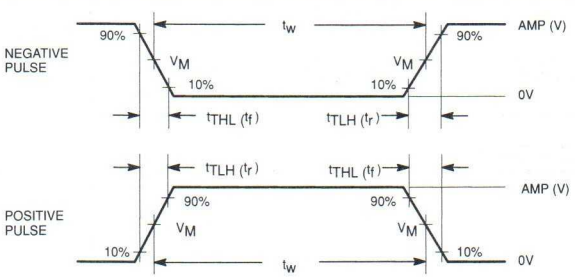
Waveform 1. Propagation Delay Input to Output

NOTE:
For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor;
see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

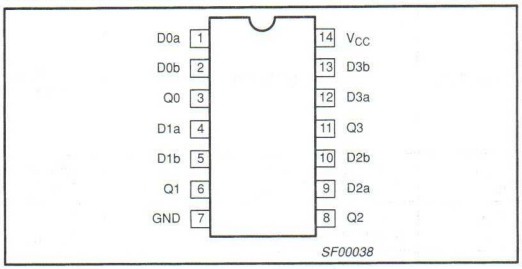
Quad 2-input Exclusive-OR gate | 74F86

FEATURE

- Industrial temperature range available (–40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F86	4.3ns	16.5mA

PIN CONFIGURATION



ORDERING INFORMATION

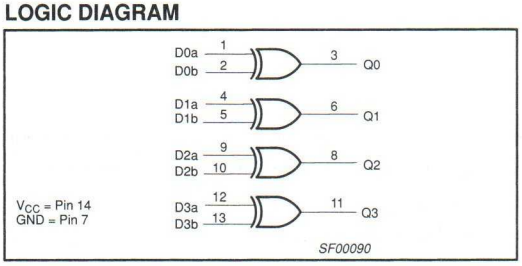
DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
14-pin plastic DIP	N74F86N	I74F86N	SOT27-1
14-pin plastic SO	N74F86D	I74F86D	SOT108-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb	Data inputs	1.0/1.0	20μA/0.6mA
Qn	Data output	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

LOGIC DIAGRAM

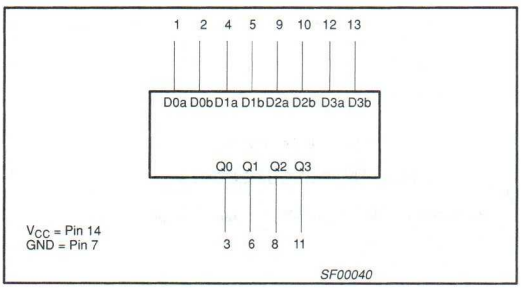


FUNCTION TABLE

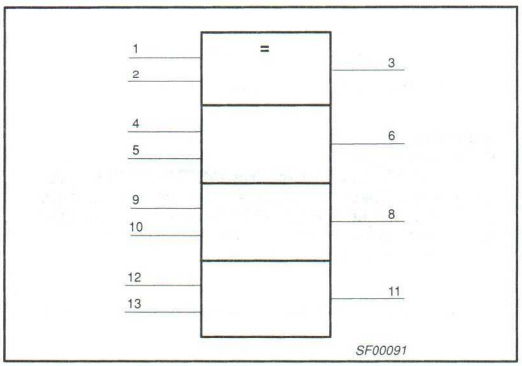
INPUTS		OUTPUT
Dna	Dnb	Qn
L	L	L
L	H	H
H	L	H
H	H	L

NOTES:
H = High voltage level
L = Low voltage level

LOGIC SYMBOL



IEC/IEEE SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state		40	mA
T_{amb}	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current				–1	mA
I_{OL}	Low-level output current				20	mA
T_{amb}	Operating free-air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	D0a = GND, D0b = 4.5V		15	23	mA
		I_{CCL}	V_{CC} = MAX	V_{IN} = 4.5V		18	28	mA

NOTES:

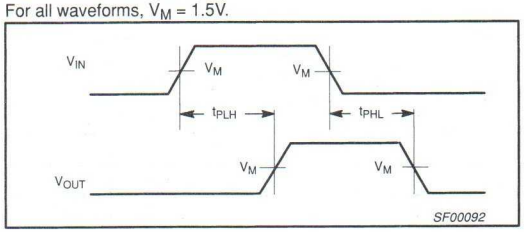
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

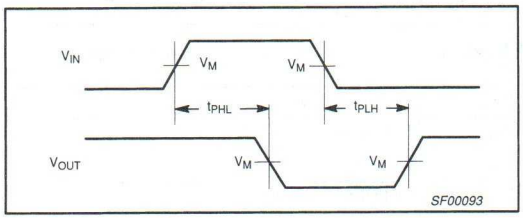
SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF R_L = 500Ω		V_{CC} = +5.0V ± 10% T_{amb} = –40°C to +85°C C_L = 50pF R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna or Dnb to Qn (other input Low)	Waveform 1	3.0 3.0	4.0 4.2	5.5 5.5	3.0 3.0	6.5 6.5	3.0 2.5	7.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay Dna or Dnb to Qn (other input High)	Waveform 2	3.5 3.0	5.3 4.7	7.0 6.5	3.5 3.0	8.0 7.5	3.5 3.0	10.0 8.0	ns

AC WAVEFORMS

For all waveforms, V_M = 1.5V.

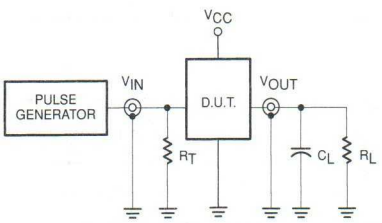


Waveform 1. Propagation Delay for Non-Inverting Outputs

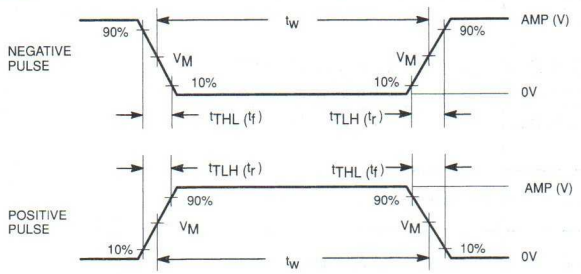


Waveform 2. Propagation Delay for Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor;
see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Postive J-$\overline{K}$ positive edge-triggered flip-flops | 74F109

FEATURE

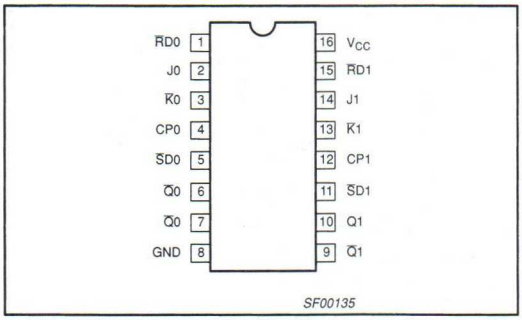
- Industrial temperature range available (–40°C to +85°C)

DESCRIPTION

The 74F109 is a dual positive edge-triggered JK-type flip-flop featuring individual J, $\overline{K}$, clock, set, and reset inputs; also true and complementary outputs. Set ($\overline{SD}$) and reset ($\overline{RD}$) are asynchronous active low inputs and operate independently of the clock (CP) input. The J and $\overline{K}$ are edge-triggered inputs which control the state changes of the flip-flops as described in the function table. Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. The J and $\overline{K}$ inputs must be stable just one setup time prior to the low-to-high transition of the clock for predictable operation. The J$\overline{K}$ design allows operation as a D flip-flop by tying J and $\overline{K}$ inputs together. Although the clock input is level sensitive, the positive transition of the clock pulse between the 0.8V and 2.0V levels should be equal to or less than the clock to output delay time for reliable operation.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F109	125MHz	12.3mA

PIN CONFIGURATION



ORDERING INFORMATION

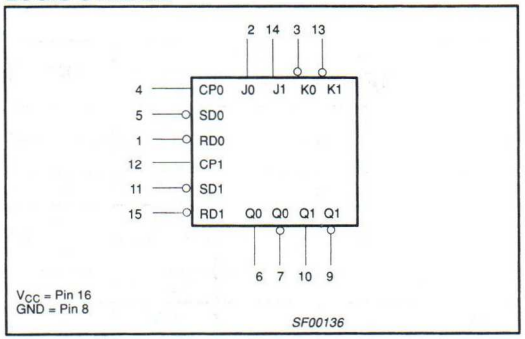
DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
16-pin plastic DIP	N74F109N	I74F109N	SOT38-4
16-pin plastic SO	N74F109D	I74F109D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

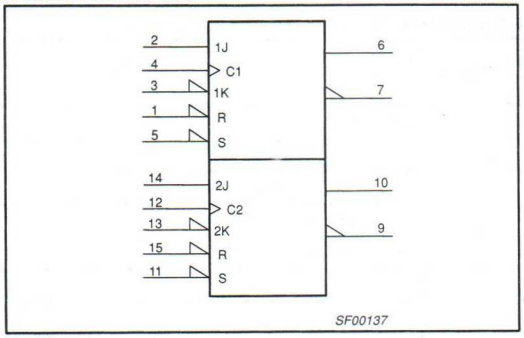
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J0, J1	J inputs	1.0/1.0	20µA/0.6mA
$\overline{K}$0, $\overline{K}$1	K inputs	1.0/1.0	20µA/0.6mA
CP0, CP1	Clock inputs (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{SD}$0, $\overline{SD}$1	Set inputs (active Low)	1.0/3.0	20µA/1.8mA
$\overline{RD}$0, $\overline{RD}$1	Reset inputs (active Low)	1.0/3.0	20µA/1.8mA
Q0, Q1, $\overline{Q}$0, $\overline{Q}$1	Data outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

LOGIC SYMBOL

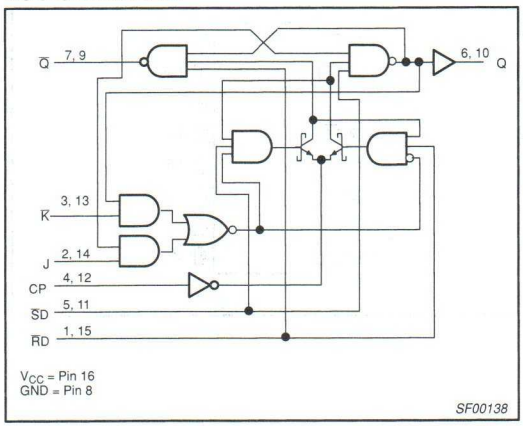


IEC/IEEE SYMBOL



Postive J-$\overline{K}$ positive edge-triggered flip-flops 74F109

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS		OPERATING MODE
$\overline{SD}$	$\overline{RD}$	CP	J	$\overline{K}$	Q	$\overline{Q}$	
L	H	X	X	X	H	L	Asynchronous set
H	L	X	X	X	L	H	Asynchronous reset
L	L	X	X	X	H	H	Undetermined*
H	H	↕	X	X	q	$\overline{q}$	Hold
H	H	↑	h	l	$\overline{q}$	q	Toggle
H	H	↑	h	h	H	L	Load "1" (set)
H	H	↑	l	l	L	H	Load "0" (reset)
H	H	↑	l	h	q	$\overline{q}$	Hold 'no change"

NOTES:
H = High-voltage level
h = High-voltage level one setup time prior to low-to-high clock transition
L = Low-voltage level
l = Low-voltage level one setup time prior to low-to-high clock transition
q = Lower case indicate the state of the referenced output prior to the low-to-high clock transition
X = Don't care
↑ = Low-to-high clock transition
↕ = Not low-to-high clock transition
* = Both outputs will be high if both $\overline{SD}$ and $\overline{RD}$ go low simultaneously

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state		40	mA
T_{amb}	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IN}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current				–1	mA
I_{OL}	Low-level output current				20	mA
T_{amb}	Operating free-air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	J, $\overline{K}$, CPn	V_{CC} = MAX, V_I = 0.5V					–0.6	mA
		$\overline{SD}$n, $\overline{RD}$n	V_{CC} = MAX, V_I = 0.5V					–1.8	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		–150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX				12.3	17	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs high in turn.

AC ELECTRICAL CHARACTERISTICS

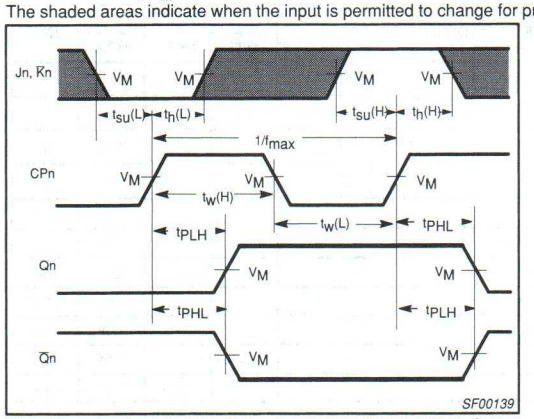
SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF R_L = 500Ω		V_{CC} = +5.0V ± 10% T_{amb} = –40°C to +85°C C_L = 50pF R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	90	125		90		90		MHz
t_{PLH} t_{PHL}	Propagation delay CPn to Qn or $\overline{Q}$n	Waveform 1	3.8 4.4	5.3 6.2	7.0 8.0	3.8 4.4	8.0 9.2	3.8 4.4	9.0 9.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SD}$n, $\overline{RD}$ to Qn or $\overline{Q}$n	Waveform 2, 3	3.2 3.5	5.2 7.0	7.0 9.0	3.2 3.5	8.0 10.5	2.8 3.5	9.0 10.5	ns

AC SETUP REQUIREMENTS

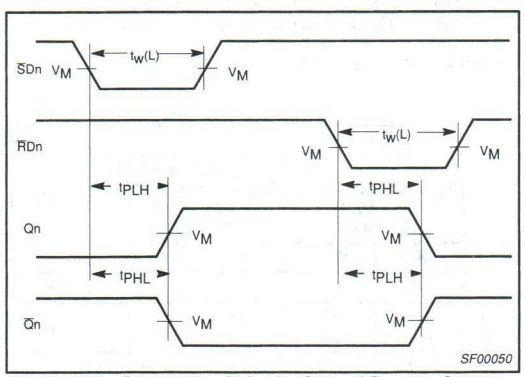
SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF R_L = 500Ω		V_{CC} = +5.0V ± 10% T_{amb} = –40°C to +85°C C_L = 50pF R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{su} (H) t_{su}(L)	Setup time, high or low Dn to CPn	Waveform 1	3.0 3.0			3.0 3.0		3.0 3.0		ns
t_h (H) t_h (L)	Hold time, high or low Dn to CPn	Waveform 1	1.0 1.0			1.0 1.0		1.0 1.0		ns
t_w (H) t_w (L)	CP pulse width, high or low	Waveform 1	4.0 5.0			4.0 5.0		4.0 5.0		ns
t_w (L)	$\overline{SD}$n or $\overline{RD}$n pulse width, low	Waveform 2	4.0			4.0		4.0		ns
t_{rec}	Recovery time $\overline{SD}$n or $\overline{RD}$n to CP	Waveform 3	2.0			2.0		2.0		ns

AC WAVEFORMS

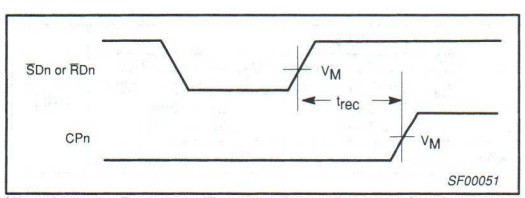
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay for Data to Output, Data Setup Time and Hold Times, and Clock Width,and Maximum Clock Frequency

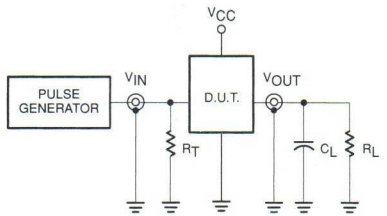


Waveform 2. Propagation Delay for Set and Reset to Output, Set and Reset Pulse Width

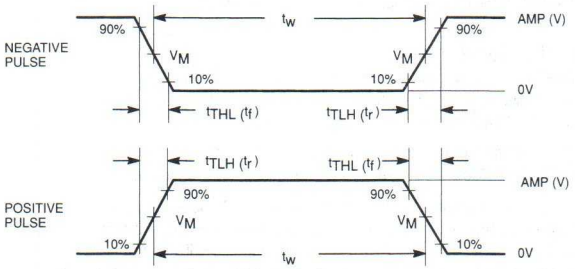


Waveform 3. Recovery Timer for Set or Reset to Clock

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Dual J-K negative edge-triggered flip-flop | 74F112

FEATURE

- Industrial temperature range available (–40°C to +85°C)

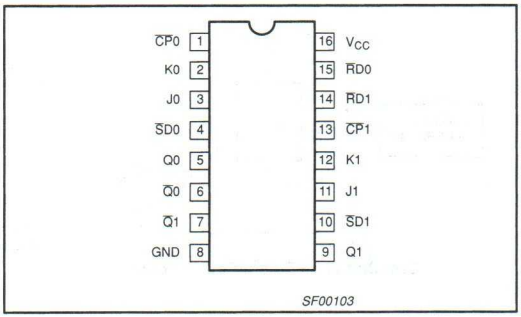
DESCRIPTION

The 74F112, Dual Negative Edge-Triggered JK-Type Flip-Flop, feature individual J, K, Clock ($\overline{CP}n$), Set ($\overline{SD}$) and Reset ($\overline{RD}$) inputs, true (Qn) and complementary ($\overline{Q}n$) outputs.

The $\overline{SD}$ and $\overline{RD}$ inputs, when Low, set or reset the outputs as shown in the Function Table, regardless of the level at the other inputs.

A High level on the clock ($\overline{CP}n$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}n$ is High and flip-flop will perform according to the Function Table as long as minimum setup and hold times are observed. Output changes are initiated by the High-to-Low transition of the $\overline{CP}n$.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F112	100MHz	15mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
16-pin plastic DIP	N74F112N	I74F112N	SOT38-4
16-pin plastic SO	N74F112D	I74F112D	SOT109-1

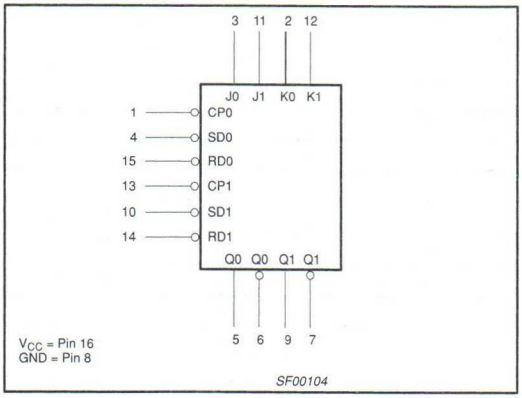
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J0, J1	J inputs	1.0/1.0	20μA/0.6mA
K0, K1	K inputs	1.0/1.0	20μA/0.6mA
$\overline{SD}0$, $\overline{SD}1$	Set inputs (active Low)	1.0/5.0	20μA/3.0mA
$\overline{RD}0$, $\overline{RD}1$	Reset inputs (active Low)	1.0/5.0	20μA/3.0mA
$\overline{CP}0$, $\overline{CP}1$	Clock Pulse input (active falling edge)	1.0/4.0	20μA/2.4mA
Q0, $\overline{Q}0$; Q1, $\overline{Q}1$	Data outputs	50/33	1.0mA/20mA

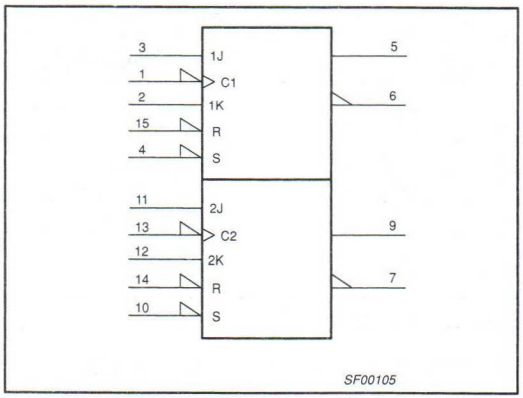
NOTE:
One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

Dual J-K negative edge-triggered flip-flop 74F112

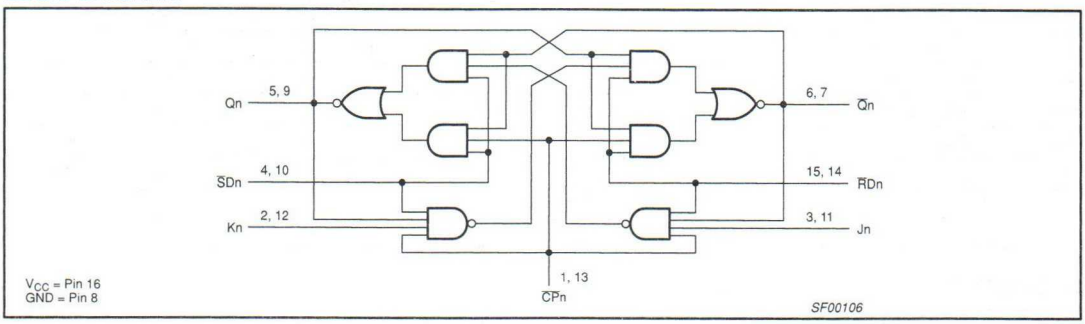
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS		OPERATING MODE
$\overline{SD}$	$\overline{RD}$	$\overline{CP}$	J	K	Q	$\overline{Q}$	
L	H	X	X	X	H	L	Asynchronous Set
H	L	X	X	X	L	H	Asynchronous Reset
L	L	X	X	X	H*	H*	Undetermined *
H	H	↓	h	h	$\overline{q}$	q	Toggle
H	H	↓	l	h	L	H	Load "0" (Reset)
H	H	↓	h	l	H	L	Load "1" (Set)
H	H	↓	l	l	q	$\overline{q}$	Hold "no change"
H	H	H	X	X	Q	$\overline{Q}$	Hold "no change"

H = High voltage level
h = High voltage level one setup time prior to High-to-Low clock transition
L = Low voltage level
l = Low voltage level one setup time prior to High-to-Low clock transition
q = Lower case letters indicate the state of the reference output prior to the High-to-Low clock transition
X = Don't care
↓ = High-to-Low clock transition
* = Both outputs will be High while both $\overline{SD}$ and $\overline{RD}$ are Low, but the output states are unpredictable if $\overline{SD}$ and $\overline{RD}$ go High simultaneously.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state		40	mA
T_{amb}	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current				–1	mA
I_{OL}	Low-level output current				20	mA
T_{amb}	Operating free-air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	Jn, Kn	V_{CC} = MAX, V_I = 0.5V				–0.6	mA
		$\overline{CP}$n					–2.4	mA
		$\overline{S}$Dn, $\overline{R}$Dn					–3.0	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)[4]		V_{CC} = MAX			15	21	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, with the Q and $\overline{Q}$ outputs High in turn.

AC ELECTRICAL CHARACTERISTICS

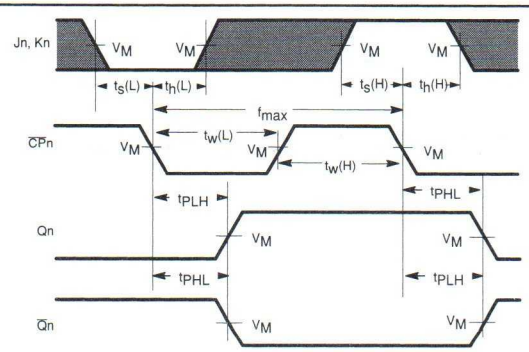
SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF R_L = 500Ω		V_{CC} = +5.0V ± 10% T_{amb} = –40°C to +85°C C_L = 50pF R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	85	100		80		80		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Qn or $\overline{Q}$n	Waveform 1	2.0 2.0	5.0 5.0	6.5 6.5	2.0 2.0	7.5 7.5	2.0 2.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}$Dn, $\overline{R}$D to Qn or $\overline{Q}$n	Waveform 2,3	2.0 2.0	4.5 4.5	6.5 6.5	2.0 2.0	7.5 7.5	1.5 1.5	7.5 7.5	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF R_L = 500Ω		V_{CC} = +5.0V ± 10% T_{amb} = –40°C to +85°C C_L = 50pF R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_S(H) t_S((L)	Setup time, High or Low Jn, Kn to $\overline{CP}$	Waveform 1	4.0 3.5			5.0 4.0		5.0 4.0		ns
t_h(H) t_h(L)	Hold time, High or Low Jn, Kn to $\overline{CP}$	Waveform 1	0.0 0.0			0.0 0.0		0.0 0.0		ns
t_W(H) t_W(L)	$\overline{CP}$ Pulse width High or Low	Waveform 1	4.5 4.5			5.0 5.0		5.0 5.0		ns
t_W(L)	$\overline{S}$Dn, $\overline{R}$D Pulse width Low	Waveform 2,3	4.5			5.0		5.0		ns
t_{REC}	Recovery time $\overline{S}$Dn, $\overline{R}$D to $\overline{CP}$	Waveform 2,3	4.5			5.0		5.0		ns

AC WAVEFORMS

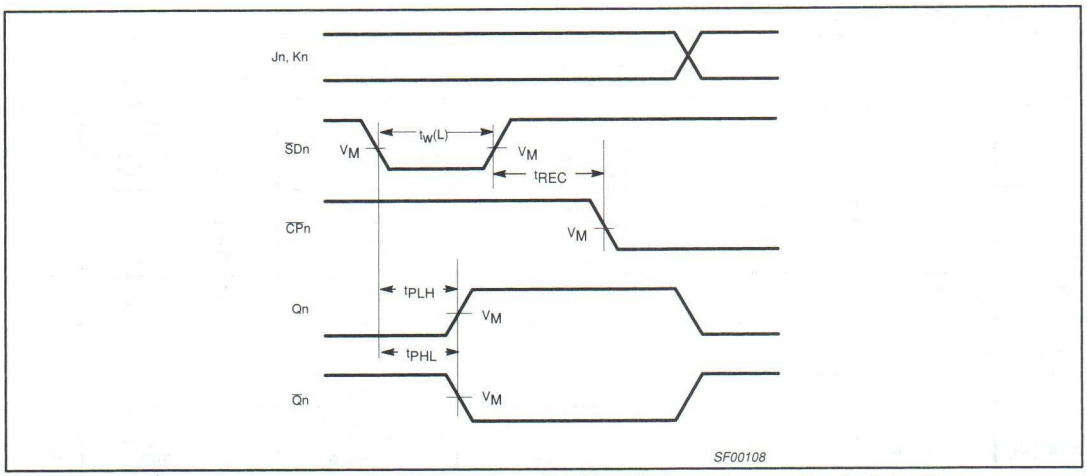
For all waveforms, V_M = 1.5V.



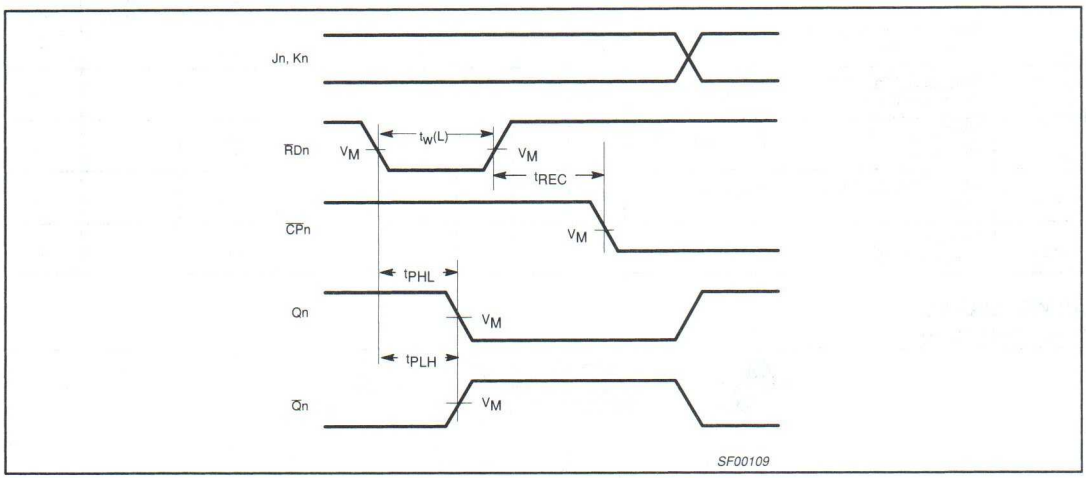
SF00107

The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 1. Propagation Delay for Data to Output, Data Setup Time and Hold Times, and Clock Pulse Width

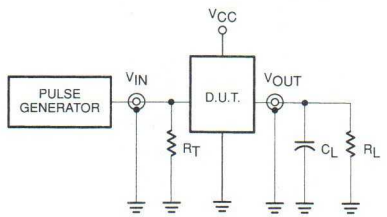


Waveform 2. Propagation Delay for Set to Output, Set Pulse Width, and Recovery Time for Set to Clock

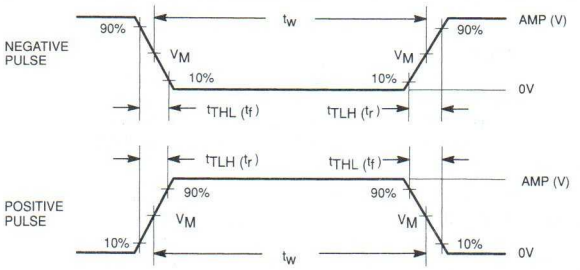


Waveform 3. Propagation Delay for Reset to Output, Reset Pulse Width, and Recovery Time for Reset to Clock

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Dual J-K negative edge-triggered flip-flops without reset

74F113

FEATURE

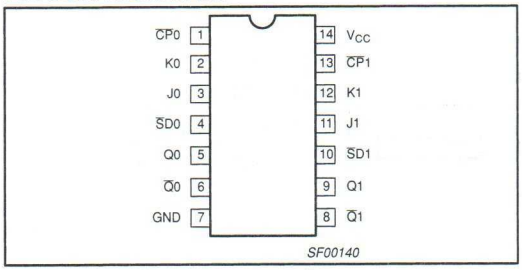
- Industrial temperature range available (–40°C to +85°C)

DESCRIPTION

The 74F113, dual negative edge-triggered JK-type flip-flop, features individual J, K, clock ($\overline{CP}$), set ($\overline{SD}$) inputs, true and complementary outputs. The asynchronous $\overline{SD}$ input, when low, forces the outputs to the steady state levels as shown in the function table regardless of the level at the other inputs.

A high level on the clock ($\overline{CP}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is high and flip-flop will perform according to the function table as long as minimum setup and hold times are observed. Output changes are initiated by the high-to-low transition of the $\overline{CP}$.

PIN CONFIGURATION



TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F113	100MHz	15mA

ORDERING INFORMATION

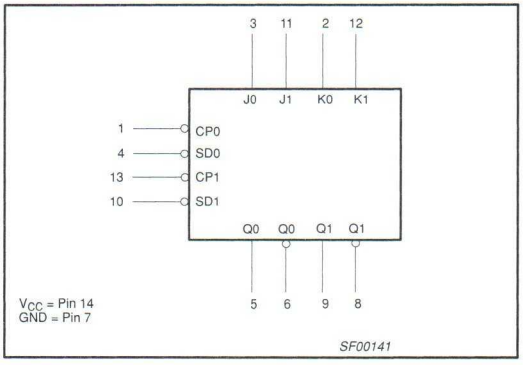
DESCRIPTION	ORDER CODE		PKG. DWG. #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
14-pin plastic DIP	N74F113N	I74F113N	SOT27–1
14-pin plastic SO	N74F113D	I74F113D	SOT108–1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

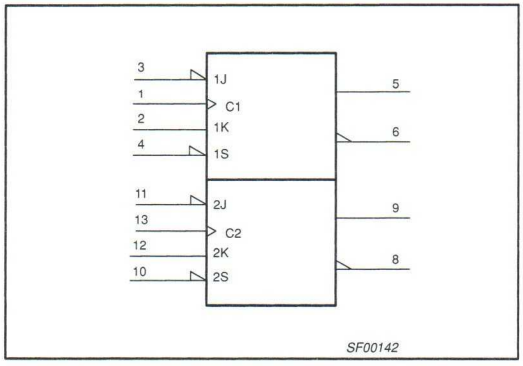
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J0, J1	J inputs	1.0/1.0	20µA/0.6mA
K0, K1	K inputs	1.0/1.0	20µA/0.6mA
$\overline{CP}0$, $\overline{CP}1$	Clock inputs (active falling edge)	1.0/4.0	20µA/2.4mA
$\overline{SD}0$, $\overline{SD}1$	Set inputs (active low)	1.0/5.0	20µA/3.0mA
Q0, Q1, $\overline{Q}0$, $\overline{Q}1$	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

LOGIC SYMBOL



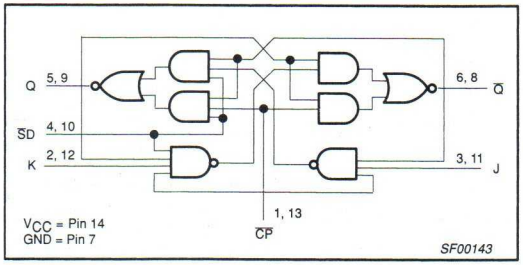
IEC/IEEE SYMBOL



Dual J-K negative edge-triggered flip-flops without reset

74F113

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{SD}$	$\overline{CP}$	J	K	Q	$\overline{Q}$	
L	X	X	X	H	L	Asynchronous set
H	↓	h	h	$\overline{q}$	q	Toggle
H	↓	h	l	H	L	Load "1" (set)
H	↓	l	h	L	H	Load "0" (reset)
H	↓	l	l	q	$\overline{q}$	Hold 'no change"

NOTES:
H = High-voltage level
h = High-voltage level one setup time prior to high-to-low clock transition
L = Low-voltage level
l = Low-voltage level one setup time prior to high-to-low clock transition
q = Lower case indicate the state of the referenced output prior to the high-to-low clock transition
X = Don't care
↓ = high-to-low clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state		40	mA
T_{amb}	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current				–1	mA
I_{OL}	Low-level output current				20	mA
T_{amb}	Operating free-air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	Jn, Kn	V_{CC} = MAX, V_I = 0.5V					–0.6	mA
		$\overline{CP}$n						–2.4	mA
		$\overline{SD}$n						–3.0	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		–150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX				15	21	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs high in turn.

AC ELECTRICAL CHARACTERISTICS

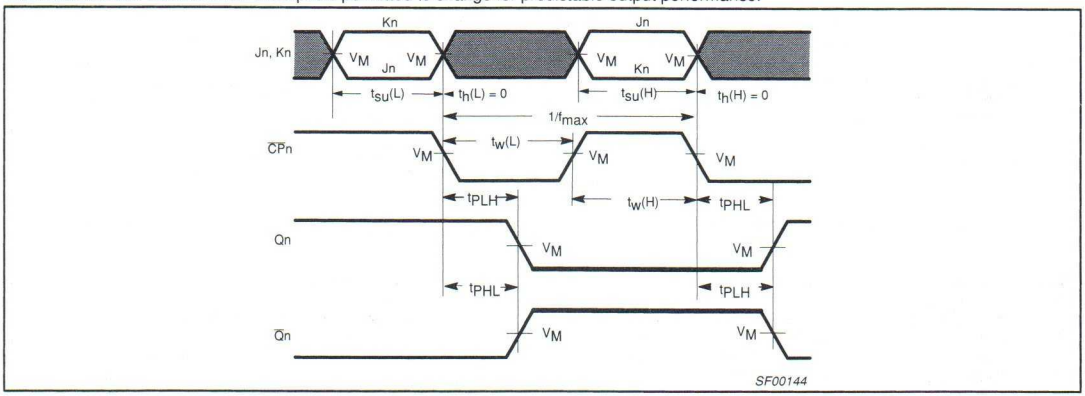
SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF R_L = 500Ω		V_{CC} = +5.0V ± 10% T_{amb} = –40°C to +85°C C_L = 50pF R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	85	100		80		80		ns
t_{PLH} t_{PHL}	Propagation delay CPn to Qn or $\overline{Q}$n	Waveform 1	2.0 2.0	4.0 4.0	6.0 6.0	2.0 2.0	7.0 7.0	2.0 2.0	7.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SD}$n, to Qn or $\overline{Q}$n	Waveform 2	2.0 2.0	4.5 4.5	6.5 6.5	2.0 2.0	7.5 7.5	2.0 2.0	8.0 7.5	ns

AC SETUP REQUIREMENTS

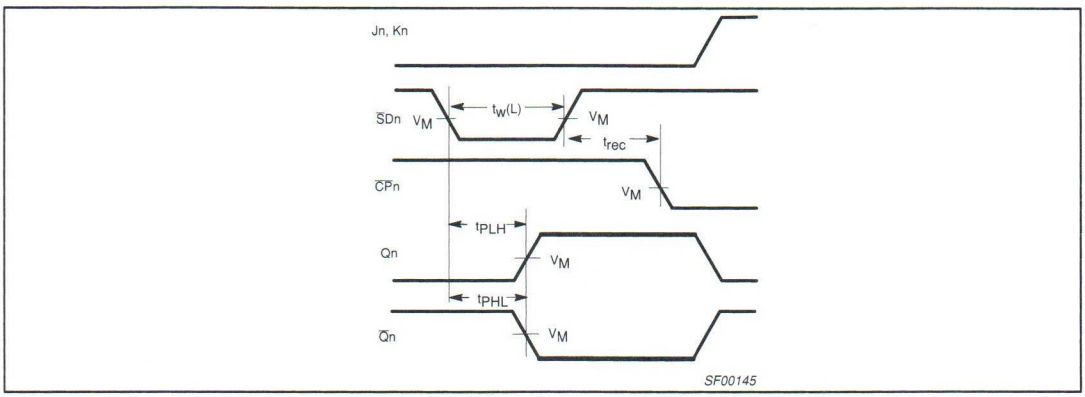
SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF R_L = 500Ω		V_{CC} = +5.0V ± 10% T_{amb} = –40°C to +85°C C_L = 50pF R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{su} (H) t_{su}(L)	Setup time, high or low Jn, Kn to $\overline{CP}$n	Waveform 1	4.0 3.5			5.0 4.0		5.0 4.5		ns
t_h (H) t_h (L)	Hold time, high or low Jn, Kn to $\overline{CP}$n	Waveform 1	0.0 0.0			0.0 0.0		0.0 0.0		ns
t_w (H) t_w (L)	$\overline{CP}$ pulse width, high or low	Waveform 1	4.5 4.5			5.0 5.0		5.0 5.0		ns
t_w (L)	$\overline{SD}$n pulse width, low	Waveform 2	4.5			5.0		5.0		ns
t_{rec}	Recovery time $\overline{SD}$n to CPn	Waveform 2	4.5			5.0		5.0		ns

AC WAVEFORMS

For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

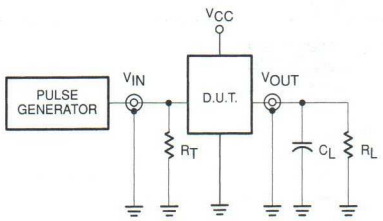


Waveform 1. Propagation Delay for Data to Output, Data Setup Time and Hold Times, and Clock Width, and Maximum Clock Frequency

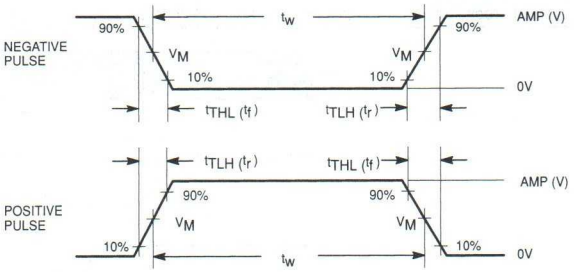


Waveform 2. Propagation Delay for Set to Output, Set Pulse Width, and Recovery Time for Set to Clock

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Quad buffers (3-State) 74F125, 74F126

FEATURE

- High impedance NPN base inputs for reduced loading (20μA in High and Low states)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F125	5.0ns	23mA
74F126	5.0ns	26mA

ORDERING INFORMATION

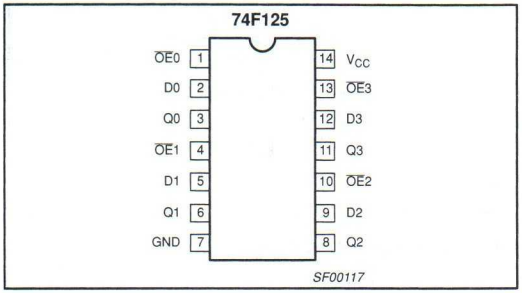
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
14-pin plastic DIP	N74F125N, N74F126N	SOT27-1
14-pin plastic SO	N74F125D, N74F126D	SOT108-1

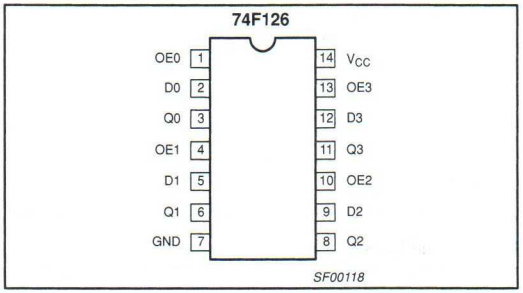
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0–D3	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE0}$–$\overline{OE3}$	Output Enable inputs (active Low), 74F125	1.0/0.033	20μA/20μA
OE0–OE3	Output Enable inputs (active High), 74F126	1.0/0.033	20μA/20μA
Q0–Q3	Data outputs	750/106.7	15mA/64mA

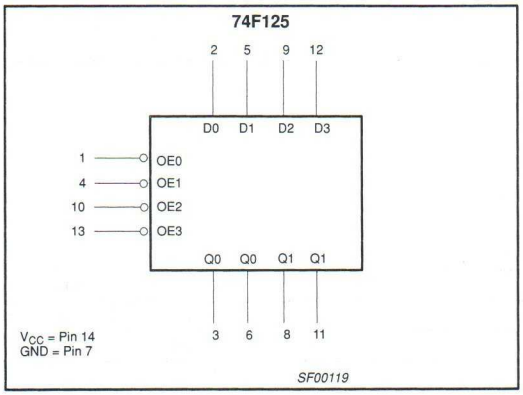
NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

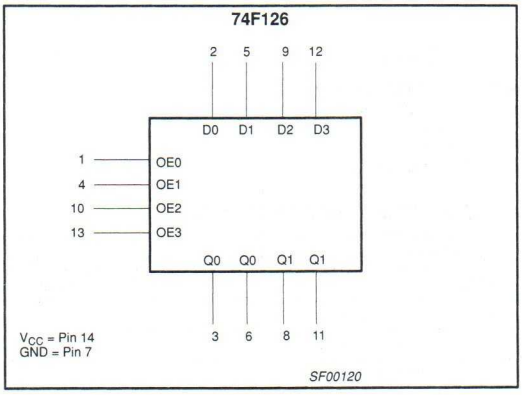
PIN CONFIGURATIONS



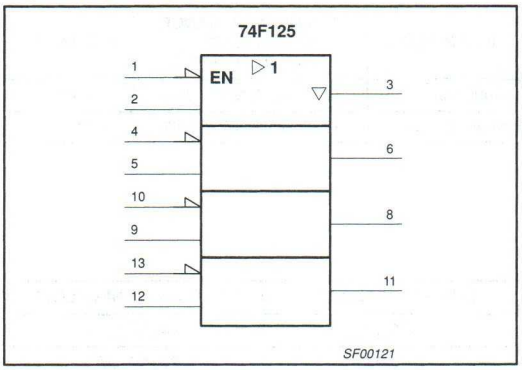


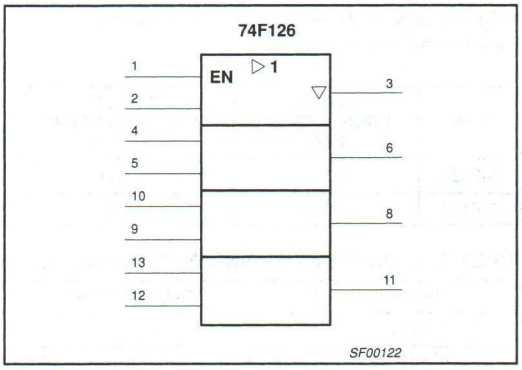
LOGIC SYMBOLS



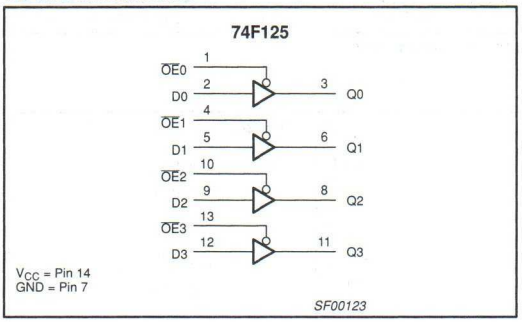


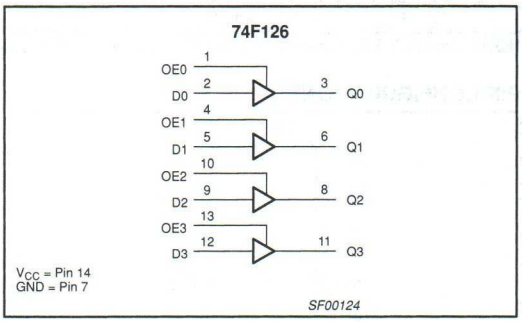
IEC/IEEE SYMBOLS





LOGIC DIAGRAMS





FUNCTION TABLE, 74F125

I NPUTS		OUTPUT
$\overline{OE}n$	Dn	Qn
L	L	L
L	H	H
H	X	Z

FUNCTION TABLE, 74F126

I NPUTS		OUTPUT
OEn	Dn	Qn
H	L	L
H	H	H
L	X	Z

NOTES TO THE FUNCTION TABLES:
H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–15	mA
I_{OL}	Low-level output current			64	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=–3mA	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.3		V
			I_{OH}=–15mA	±10%V_{CC}	2.0			V
				±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}= MAX	±10%V_{CC}			0.55	V
				±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low-level voltage applied	V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX			–100		–225	mA
I_{CC}	Supply current (total)	74F125	I_{CCH}	V_{CC} = MAX	$\overline{OE}$n = GND, Dn = 4.5V		17	24	mA
			I_{CCL}		$\overline{OE}$n = Dn = GND		28	40	mA
			I_{CCZ}		$\overline{OE}$n = Dn = 4.5V		25	35	mA
		74F126	I_{CCH}	V_{CC} = MAX	OEn = Dn = 4.5V		20	30	mA
			I_{CCL}		OEn = 4.5V, Dn = GND		32	48	mA
			I_{CCZ}		OEn = GND, Dn = 4.5V		26	39	mA

NOTES:

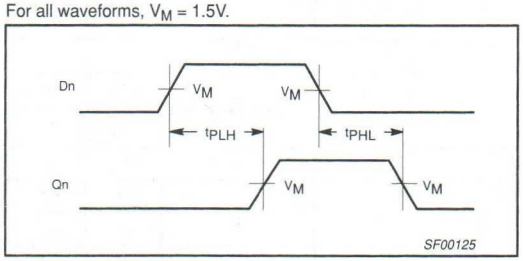
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

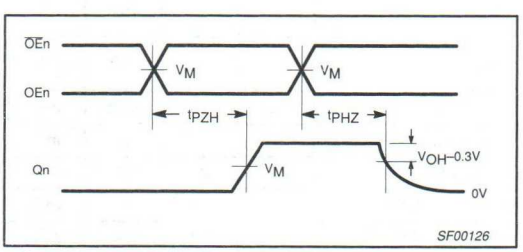
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	74F125	Waveform 1	2.0 3.0	4.0 5.5	6.0 7.5	2.0 3.0	6.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 2 Waveform 3	3.5 4.0	5.5 6.0	7.5 8.0	3.5 4.0	8.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 2 Waveform 3	1.5 1.5	3.5 3.5	5.0 5.5	1.5 1.5	6.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	74F126	Waveform 1	2.0 3.0	4.0 5.5	6.5 8.0	2.0 3.0	7.0 8.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 2 Waveform 3	4.0 4.0	6.0 6.0	7.5 8.0	3.5 3.5	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 2 Waveform 3	2.0 3.0	4.5 5.5	6.5 7.5	2.0 3.0	7.5 8.0	ns

AC WAVEFORMS

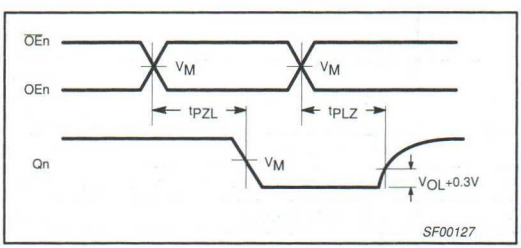
For all waveforms, V_M = 1.5V.



Waveform 1. Propagation Delay for Input to Output

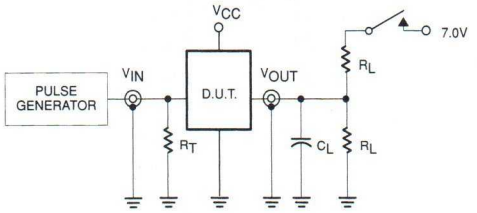


Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level

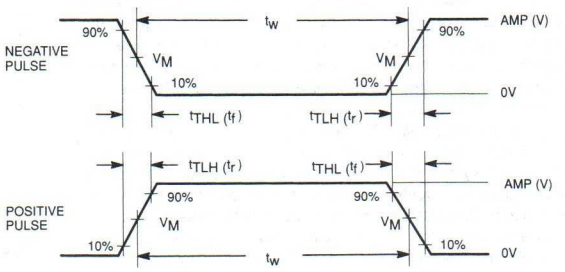


Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

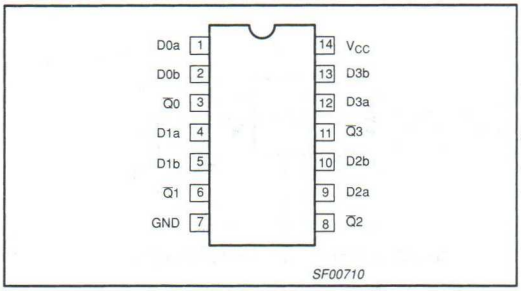
SF00128

Quad 2-input NAND Schmitt trigger | 74F132

DESCRIPTION

The 74F132 contains four 2-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates. Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Scmitt trigger uses positive feedback to effectively speed-up slow input transitions and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800mV) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as three inputs remain at a more positive voltage than V_{T+MAX}, the gate will respond in the transition of the other input as shown in Waveform 1.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F132	6.3ns	13mA

ORDERING INFORMATION

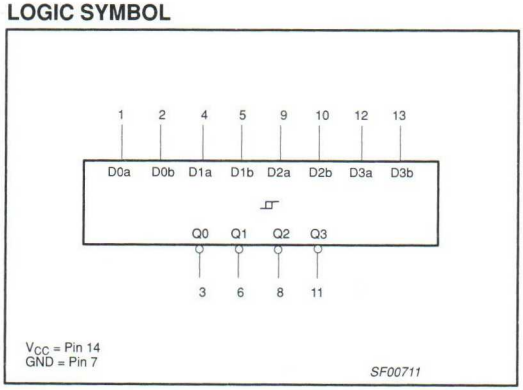
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
14-pin plastic DIP	N74F132N	SOT27-1
14-pin plastic SO	N74F132D	SOT108-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

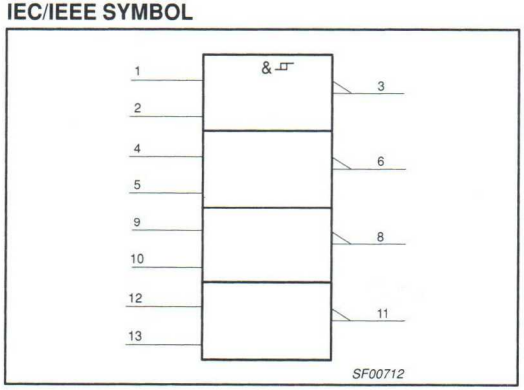
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}$n	Data output	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

LOGIC SYMBOL

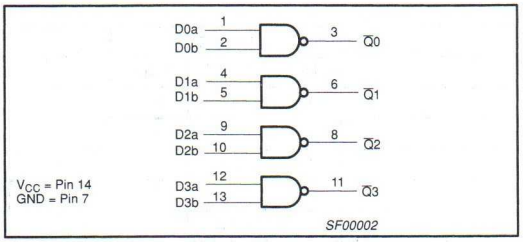


IEC/IEEE SYMBOL



Quad 2-input NAND Schmitt trigger 74F132

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUT
Dna	Dnb	$\overline{Q}$n
L	L	H
L	H	H
H	L	H
H	H	L

NOTES:
H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{T+}	Positive-going threshold		V_{CC} = 5.0V		1.5	1.7	2.0	V
V_{T-}	Negative-going threshold–		V_{CC} = 5.0V		0.7	0.9	1.1	V
† V_T	Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = 5.0V		0.4	0.8		V
V_{OH}	High-level output voltage		V_{CC} = MIN,	±10%V_{CC}	2.5			V
			V_I=V_{T-MAX}, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN,	±10%V_{CC}		0.30	0.50	V
			V_I=V_{T+MAX}, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_{T+}	Input current at positive-going threshold		V_{CC} = 5.0V, V_I=V_{T+}			0		µA
I_{T-}	Input current at negative-going threshold		V_{CC} = 5.0V, V_I=V_{T-}			–350		µA
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN}= GND		8.5	12.0	mA
		I_{CCL}		V_{IN} = 4.5V		13.0	19.5	

NOTES:

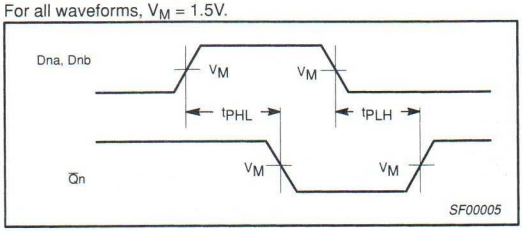
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to $\overline{Q}$n	Waveform 1	3.5 4.5	5.5 6.0	7.0 8.5	3.0 4.5	8.5 9.0	ns

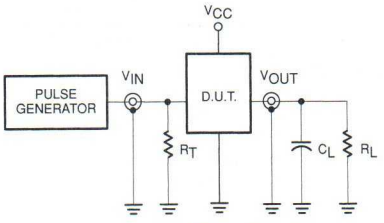
AC WAVEFORMS

For all waveforms, V_M = 1.5V.

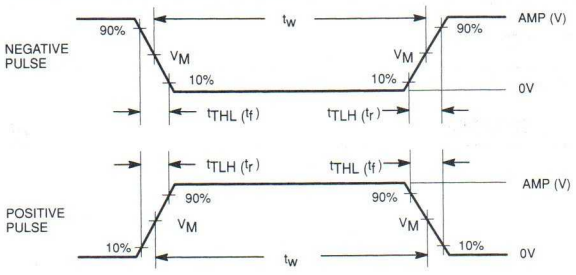


Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

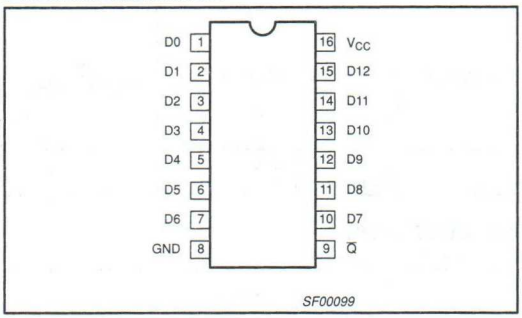
13-input NAND gate | 74F133

FEATURE

- Industrial temperature range available (–40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F133	4.0ns	2.0mA

PIN CONFIGURATION



ORDERING INFORMATION

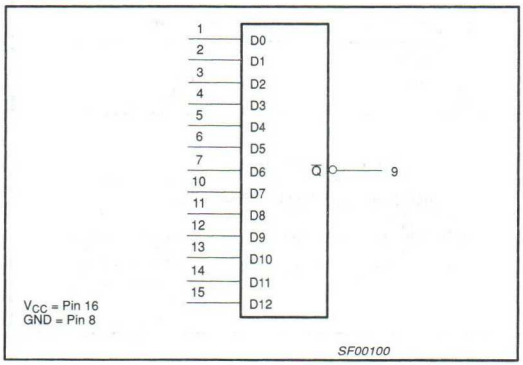
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	PKG DWG #
16-pin plastic DIP	N74F133N	I74F133N	SOT38-4
16-pin plastic SO	N74F133D	I74F133D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

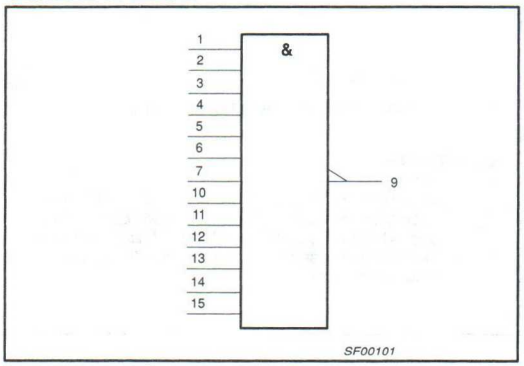
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0–D12	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Q}$	Data output	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

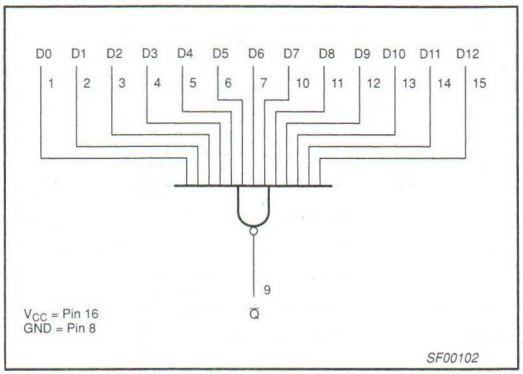
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS													OUTPUT
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	$\overline{Q}$
H	H	H	H	H	H	H	H	H	H	H	H	H	L
Any one input = L													H

NOTES:
H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state		40	mA
T_{amb}	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current				–1	mA
I_{OL}	Low-level output current				20	mA
T_{amb}	Operating free-air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			1.0	2.0	mA
		I_{CCL}				2.5	4.0	

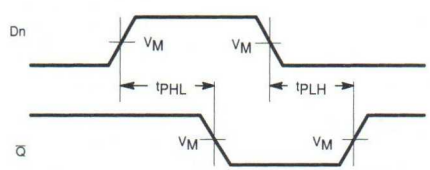
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS: V_{CC} = +5.0V, T_{amb} = +25°C, C_L = 50pF, R_L = 500Ω			LIMITS: V_{CC} = +5.0V ± 10%, T_{amb} = 0°C to +70°C, C_L = 50pF, R_L = 500Ω		LIMITS: V_{CC} = +5.0V ± 10%, T_{amb} = –40°C to +85°C, C_L = 50pF, R_L = 500Ω		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to $\overline{Q}$	Waveform 1	2.0 2.5	4.0 4.5	7.0 7.5	1.5 2.0	7.5 8.0	1.5 2.0	7.5 8.0	ns

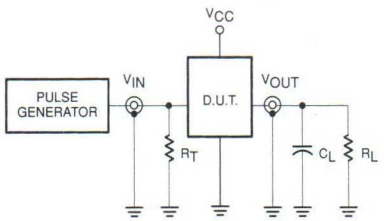
AC WAVEFORMS



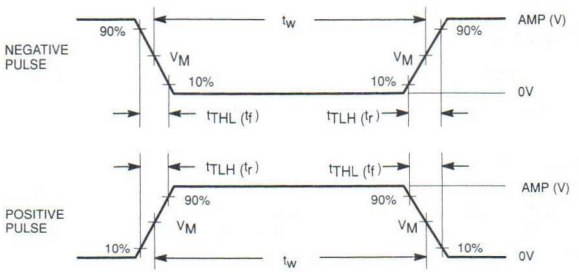
Waveform 1. Propagation Delay for Data to Outputs

NOTE:
For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

1-of-8 decoder/demultiplexer | 74F138

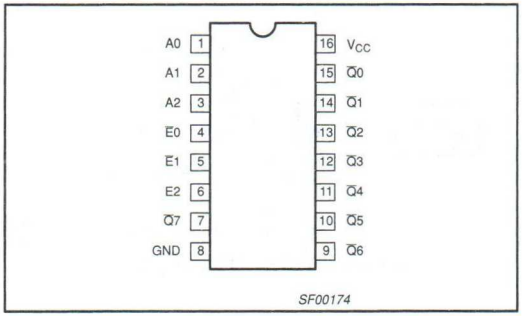
FEATURE

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Industrial temperature range available (–40°C to +85°C)

DESCRIPTION

The 74F138 decoder accepts three binary weighted inputs (A0, A1, A2) and when enabled, provides eight mutually exclusive, active low outputs ($\overline{Q}0 - \overline{Q}7$). The device features three enable inputs; two active low ($\overline{E}0$, $\overline{E}1$) and one active high (E2). Every output will be high unless $\overline{E}0$ and $\overline{E}1$ are low and E2 is high. This multiple enable function allows easy parallel expansion of the device to 1-of-32 (5 lines to 32 lines) decoder with just four 74F138s and one inverter (see Figure 1). The device can be used as an eight output demultiplexer by using one of the active low enable inputs as the data input and the remaining enable inputs as strobes. Enable inputs not used must be permanently tied to their appropriate active high or active low state.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F138	5.8ns	13mA

ORDERING INFORMATION

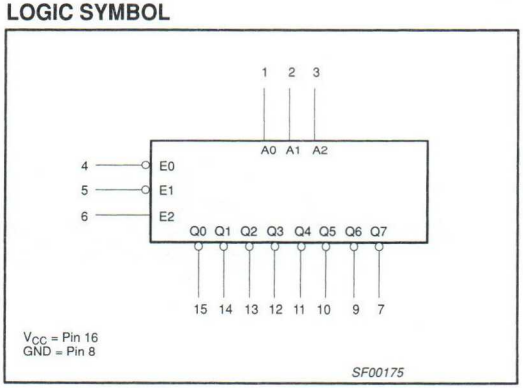
DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
16-pin plastic DIP	N74F138N	I74F138N	SOT38-4
16-pin plastic SO	N74F138D	I74F138D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

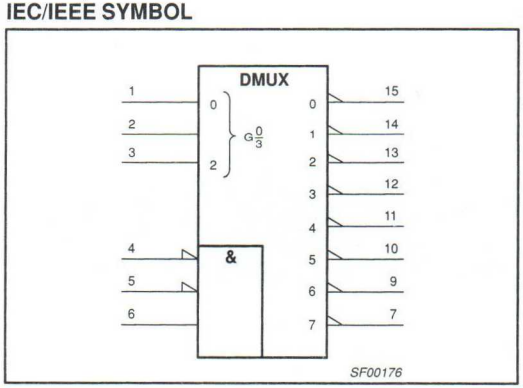
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A2	Address inputs	1.0/1.0	20µA/0.6mA
$\overline{E}0$, $\overline{E}1$	Enable inputs (active Low)	1.0/1.0	20µA/0.6mA
E2	Enable input (active High)	1.0/1.0	20µA/0.6mA
$\overline{Q}0 - \overline{Q}7$	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

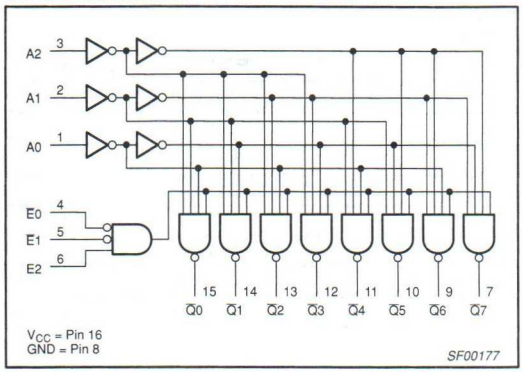
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E0}$	$\overline{E1}$	E2	A0	A1	A2	$\overline{Q0}$	$\overline{Q1}$	$\overline{Q2}$	$\overline{Q3}$	$\overline{Q4}$	$\overline{Q5}$	$\overline{Q6}$	$\overline{Q7}$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

APPLICATION

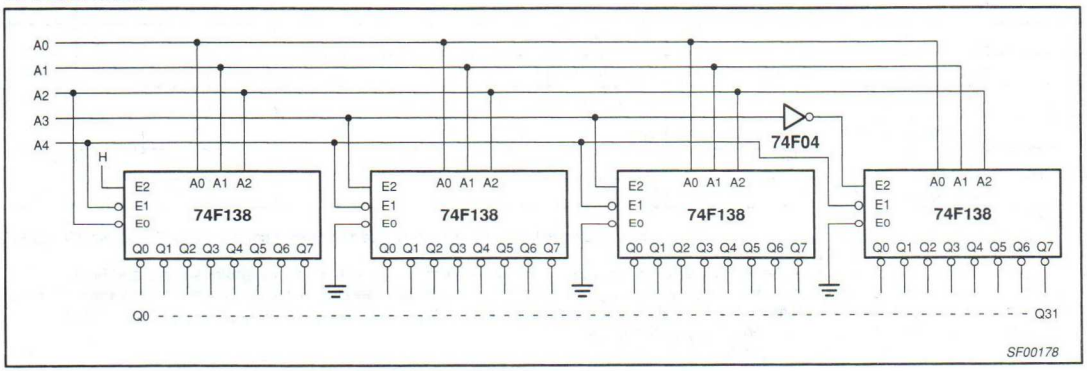


Figure 1. Expansion of 1-of-8 Decoding

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state		40	mA
T_{amb}	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current				–1	mA
I_{OL}	Low-level output current				20	mA
T_{amb}	Operating free-air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
				±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					–0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			–60		–150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				13	20	mA

NOTES:

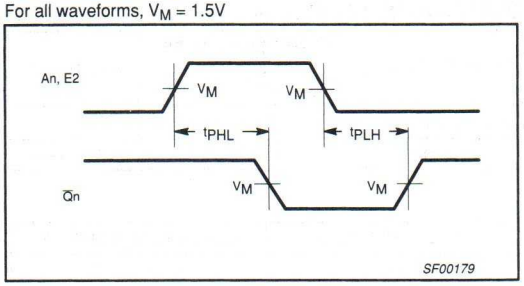
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC}, outputs must be open, V_{IN} on all inputs = 4.5V.

AC ELECTRICAL CHARACTERISTICS

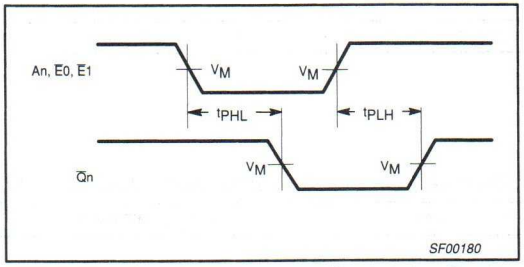
SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF R_L = 500Ω		V_{CC} = +5.0V ± 10% T_{amb} = –40°C to +85°C C_L = 50pF R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to $\overline{Qn}$	Waveform 1, 2	3.5 4.0	5.6 6.1	7.0 8.0	3.5 4.0	8.0 9.0	3.0 3.5	8.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay E0 or $\overline{E1}$ to $\overline{Qn}$	Waveform 2	3.5 3.0	6.4 5.3	7.0 7.0	3.5 3.0	8.0 7.5	3.0 3.0	8.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay E2 to $\overline{Qn}$	Waveform 1	4.0 3.5	6.2 5.6	8.0 7.5	4.0 3.5	9.0 8.5	4.0 3.5	9.5 8.5	ns

AC WAVEFORMS

For all waveforms, V_M = 1.5V

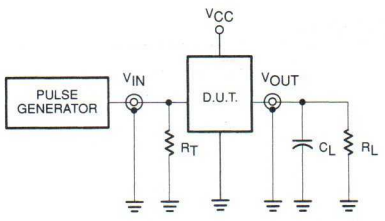


Waveform 1. Propagation Delay for Inverting Outputs

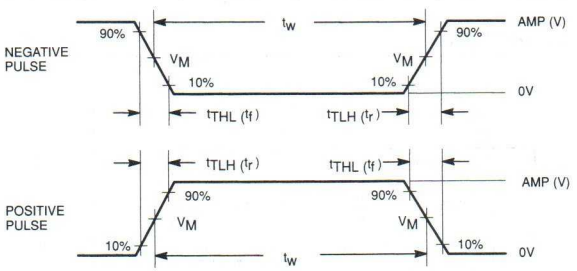


Waveform 2. Propagation Delay for Non-Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor;
see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

1-of-4 decoder/demultiplexer | 74F139

FEATURES

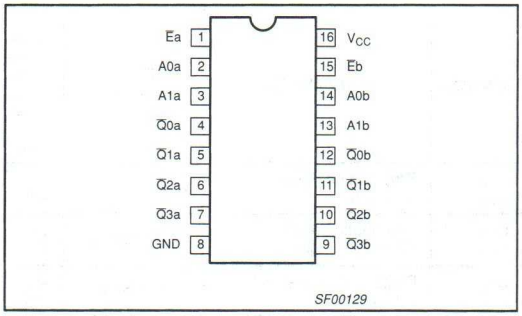
- Demultiplexing capability
- Two independent 1-of-4 decoders
- Multifunction capability

DESCRIPTION

The 74F139 is a high speed, dual 1-of-4 decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs (A0n, A1n) and providing four mutually exclusive active-Low outputs ($\overline{Q}0n$–$\overline{Q}3n$). Each decoder has an active-Low Enable ($\overline{E}$). When $\overline{E}$ is High, every output is forced High. The Enable can be used as the Data input for a 1-of-4 demultiplexer application.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F139	5.3ns	13mA

PIN CONFIGURATION



ORDERING INFORMATION

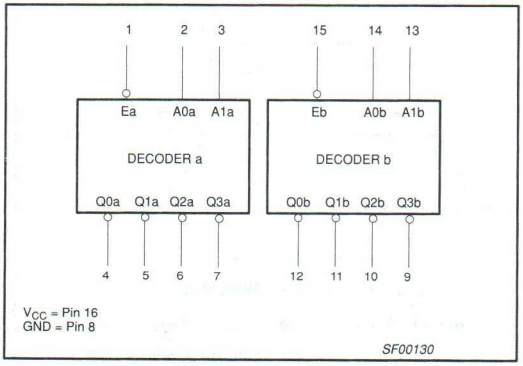
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
16-pin plastic DIP	N74F139N	SOT38-4
16-pin plastic SO	N74F139D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

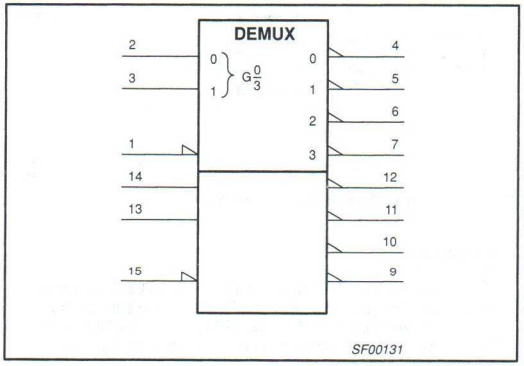
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ana, Anb	Address inputs	1.0/1.0	20μA/0.6mA
$\overline{E}$a, $\overline{E}$b	Enable inputs (active Low)	1.0/1.0	20μA/0.6mA
$\overline{Q}$0n–$\overline{Q}$3n	Data outputs (active Low)	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

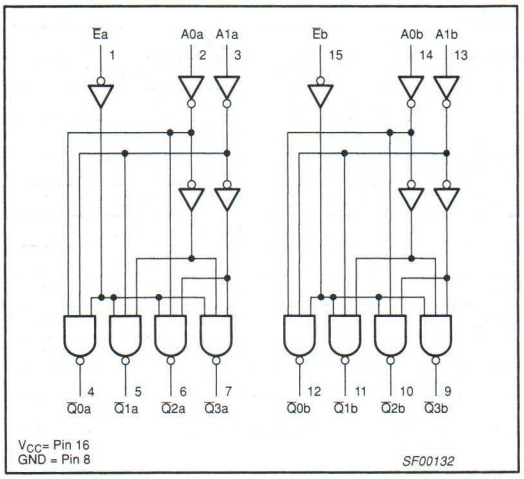
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A0	A1	$\overline{Q}0$	$\overline{Q}1$	$\overline{Q}2$	$\overline{Q}3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{ILL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			13	20	mA

NOTES:

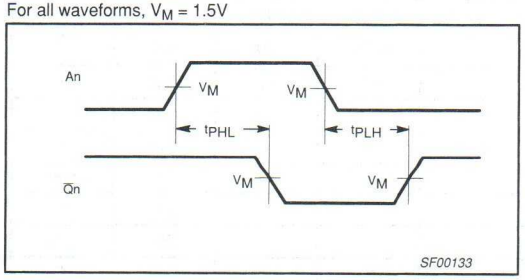
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

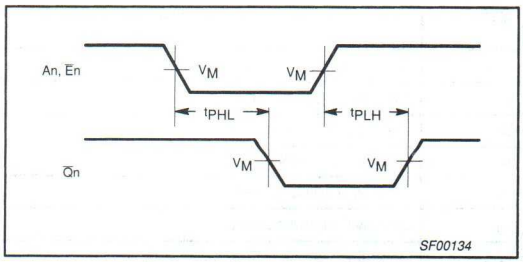
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay A0 ir A1 to $\overline{Q}$na, $\overline{Q}$nb	Waveform 1, 2	3.5 4.0	5.3 6.1	7.0 8.0	3.0 4.0	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$n to $\overline{Q}$na, $\overline{Q}$nb	Waveform 2	3.5 3.0	5.4 4.7	7.0 6.5	3.5 3.0	8.0 7.5	ns

AC WAVEFORMS

For all waveforms, V_M = 1.5V

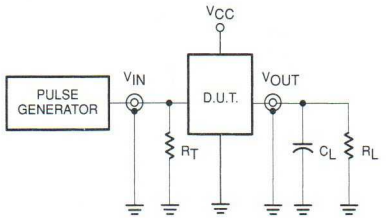


Waveform 1. Propagation Delay for Inverting Outputs

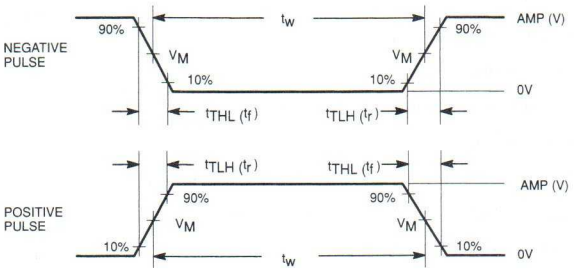


Waveform 2. Propagation Delay for Non-Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

8-input priority encoder | 74F148

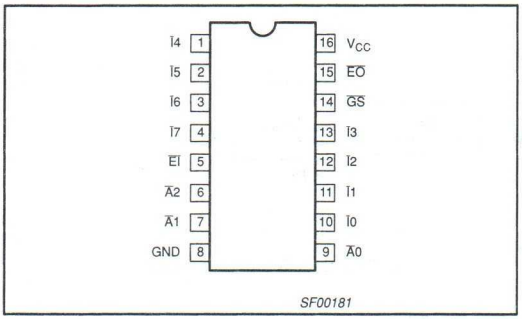
FEATURES

- Code conversions
- Multi-channel D/A converter
- Decimal-to-BCD converter
- Cascading for priority encoding of "N" bits
- Input enable capability
- Priority encoding-automatic selection of highest priority input line
- Output enable-active Low when all inputs are High
- Group signal output-active when any input is Low

DESCRIPTION

The 74F148 8-input priority encoder accepts data from eight active-Low inputs and provides a binary representation on the three active-Low outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line $\overline{I}7$ having the highest priority. A High on the Enable Input ($\overline{EI}$) will force all outputs to the inactive (High) state and allow new data to settle without producing erroneous information at the outputs. A Group Signal ($\overline{GS}$) output and an Enable Output ($\overline{EO}$) are provided with the three data outputs. The $\overline{GS}$ is active-Low when any input is Low: this indicates when any input is active. The $\overline{EO}$ is active-Low when all inputs are High. Using the Enable Output along with the Enable Input allows priority encoding of N input signals. Both $\overline{EO}$ and $\overline{GS}$ are active-High when the Enable Input is High.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F148	6.0ns	23mA

ORDERING INFORMATION

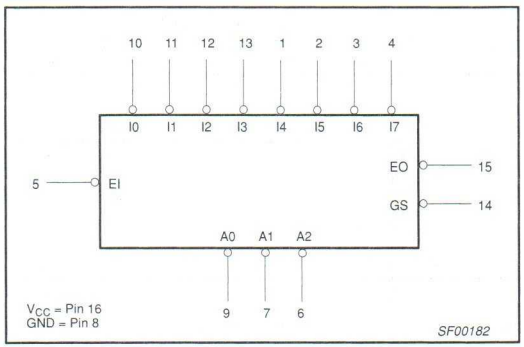
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
16-pin plastic DIP	N74F148N	SOT38-4
16-pin plastic SO	N74F148D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

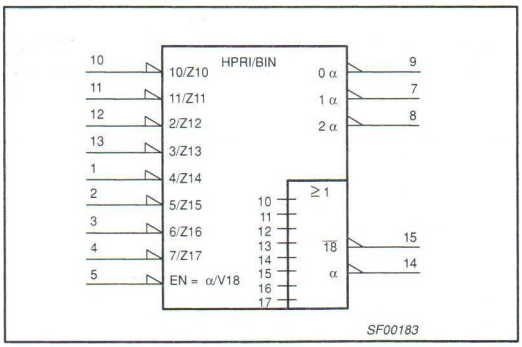
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{I}1 - \overline{I}7$	Priority inputs (active Low)	1.0/2.0	20µA/1.2mA
$\overline{I}0$	Priority input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{EI}$	Enable input (active Low)	1.0/2.0	20µA/1.2mA
$\overline{EO}$	Enable output (active Low)	50/33	1.0mA/20mA
$\overline{GS}$	Group select output (active Low)	50/33	1.0mA/20mA
$\overline{A}0 - \overline{A}2$	Address outputs (active Low)	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

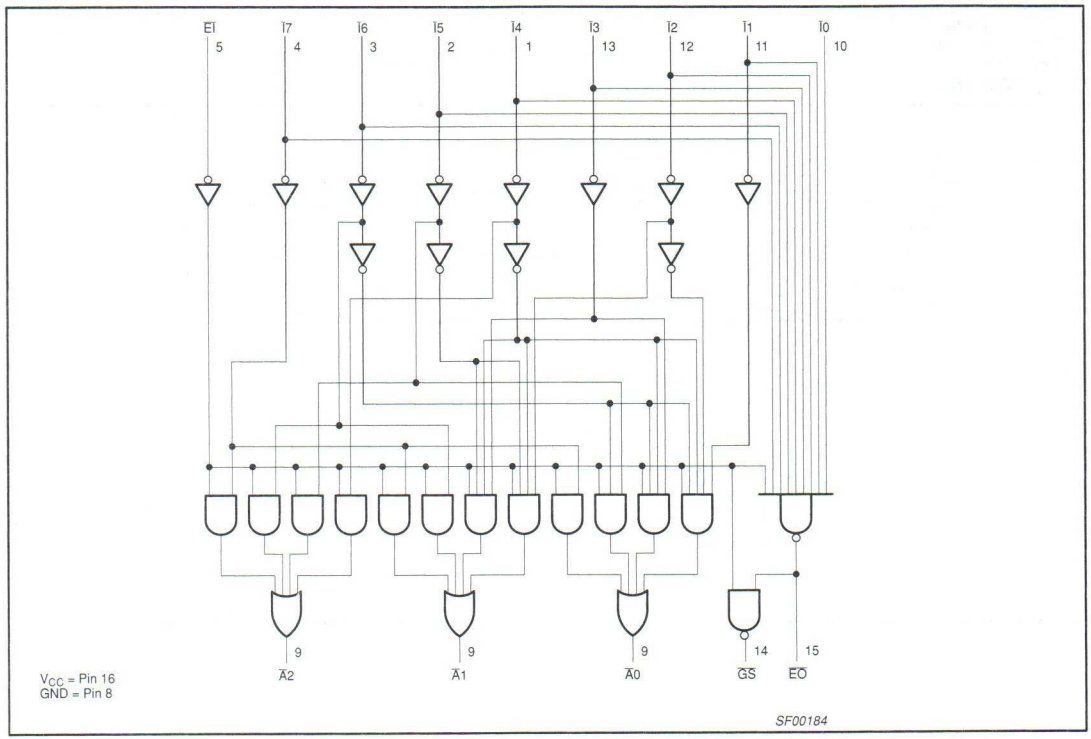
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM

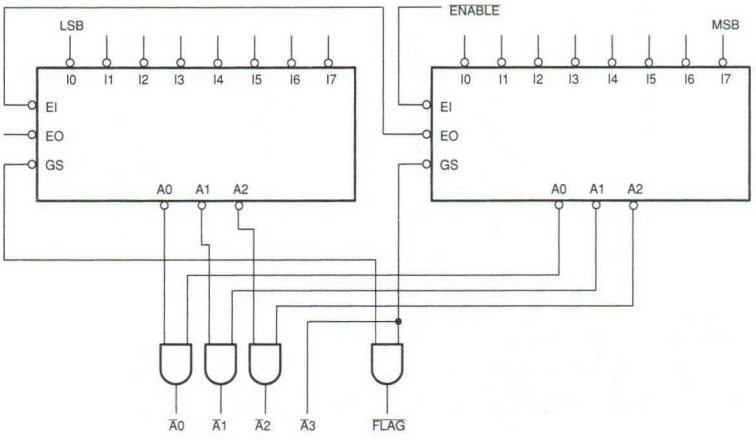


FUNCTION TABLE

INPUTS									OUTPUTS				
$\overline{EI}$	$\overline{I0}$	$\overline{I1}$	$\overline{I2}$	$\overline{I3}$	$\overline{I4}$	$\overline{I5}$	$\overline{I6}$	$\overline{I7}$	$\overline{GS}$	$\overline{A0}$	$\overline{A1}$	$\overline{A2}$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = High voltage level
L = Low voltage level
X = Don't care

APPLICATION



16-Input Priority Encoder

SF00185

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	$\overline{I0}$	V_{CC} = MAX, V_I = 0.5V				−0.6	mA
		$\overline{I1} - \overline{I7}$, $\overline{EI}$					−1.2	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)[4]		V_{CC} = MAX			23	35	mA

NOTES:

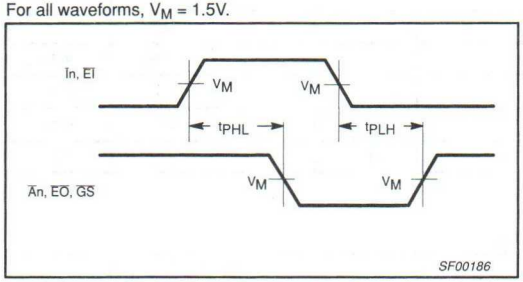
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. To measure I_{CC}, outputs must be open, V_{IN} on all inputs = 4.5V.

AC ELECTRICAL CHARACTERISTICS

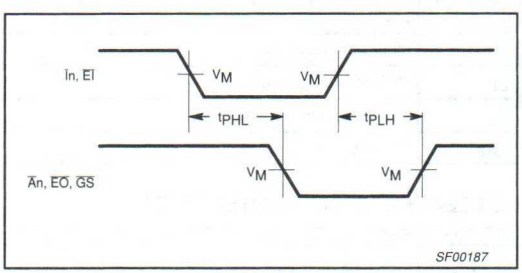
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay $\overline{In}$ to $\overline{An}$	Waveform 2	3.5 3.5	6.0 6.0	9.0 9.0	3.5 3.5	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{In}$ to $\overline{EO}$	Waveform 1	1.5 1.5	3.0 2.5	6.5 6.5	1.5 1.5	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{In}$ to $\overline{GS}$	Waveform 2	2.0 2.0	4.0 4.0	8.0 8.0	2.0 2.0	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{EI}$ to $\overline{An}$	Waveform 2	3.5 3.0	6.0 5.5	8.5 8.0	3.5 3.0	9.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{EI}$ to $\overline{GS}$	Waveform 2	2.5 3.0	4.5 5.5	7.0 7.5	2.5 3.0	8.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{EI}$ to $\overline{EO}$	Waveform 2	3.0 3.5	5.0 5.0	7.0 7.5	3.0 3.5	8.0 9.0	ns

AC WAVEFORMS

For all waveforms, V_M = 1.5V.

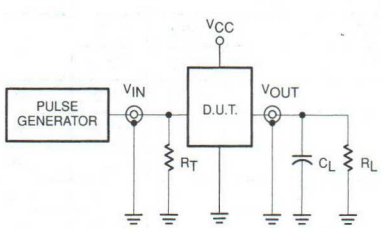


Waveform 1. For Inverting Outputs

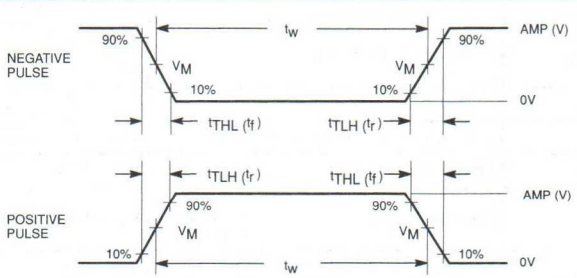


Waveform 2. For Non-Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

8-input multiplexer 74F151A

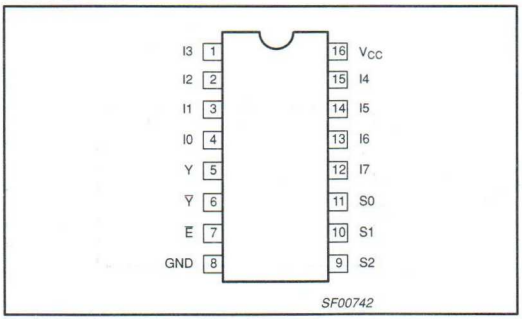
FEATURES

- High speed 8-to-1 multiplexing
- On chip decoding
- Multifunction capability
- Complementary outputs

DESCRIPTION

The 74F151A is a logic implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select (S0, S1, S2) inputs. True (Y) and complementary ($\overline{Y}$) outputs are both provided. The Enable input ($\overline{E}$) is active Low. When $\overline{E}$ is High, the $\overline{Y}$ output is High and the Y output is Low, regardless of all other inputs. In one package the 74F151A provides the ability to select from eight sources of data or control information. The device can provide any logic function of four variables and the negation with correct manipulation.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F151A	4.5ns	17mA

ORDERING INFORMATION

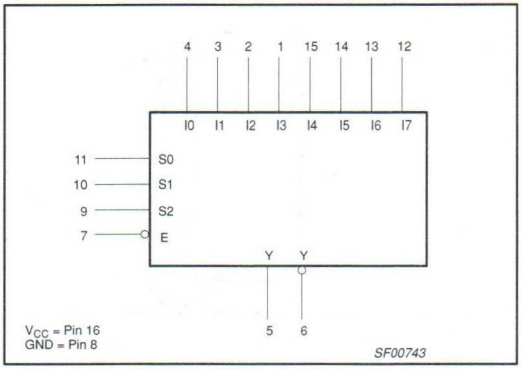
DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
16-pin plastic DIP	N74F151AN	SOT38-4
16-pin plastic SO	N74F151AD	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

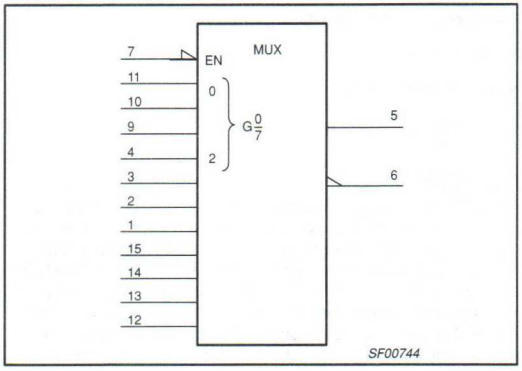
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I0–I7	Data inputs	1.0/1.0	20μA/0.6mA
S0–S2	Select inputs	1.0/1.0	20μA/0.6mA
$\overline{E}$	Enable input (active High)	1.0/1.0	20μA/0.6mA
Y, $\overline{Y}$	Data outputs	150/33	3mA/20mA

NOTE:
One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

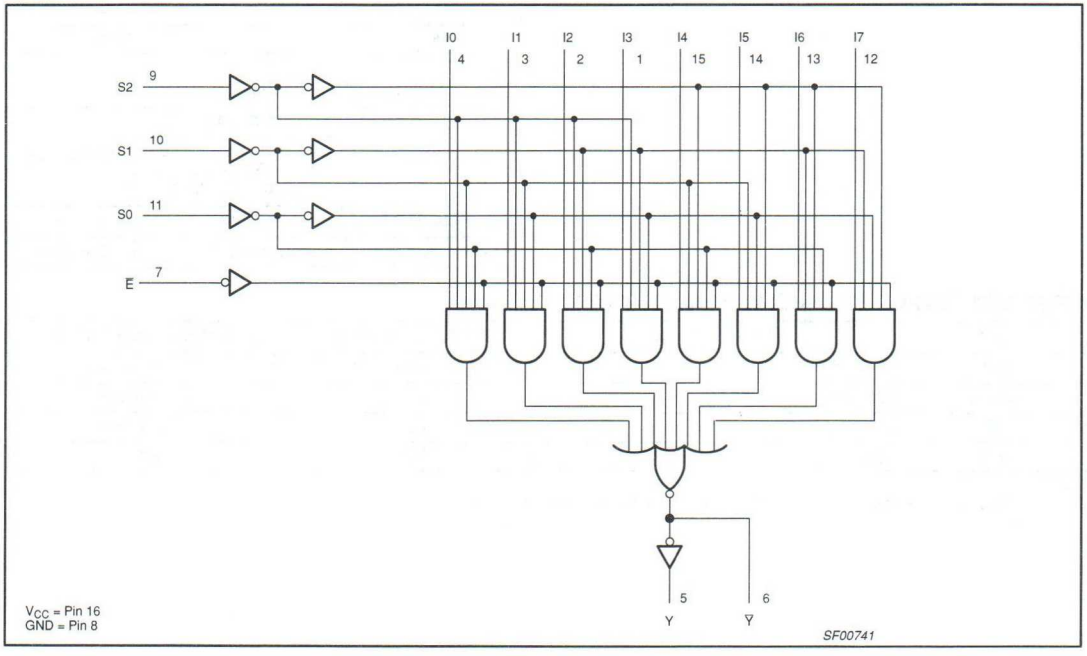
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
S2	S1	S0	$\overline{E}$	Y	$\overline{Y}$
X	X	X	H	L	H
L	L	L	L	I0	$\overline{I0}$
L	L	H	L	I1	$\overline{I1}$
L	H	L	L	I2	$\overline{I2}$
L	H	H	L	I3	$\overline{I3}$
H	L	L	L	I4	$\overline{I4}$
H	L	H	L	I5	$\overline{I5}$
H	H	L	L	I6	$\overline{I6}$
H	H	H	L	I7	$\overline{I7}$

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
				±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			18	25	mA
		I_{CCL}				17	25	mA

NOTES:

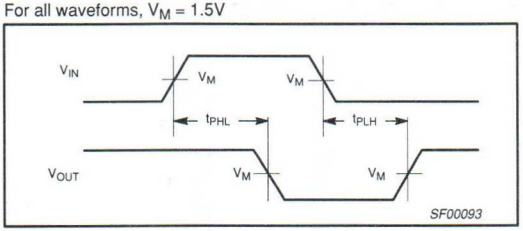
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

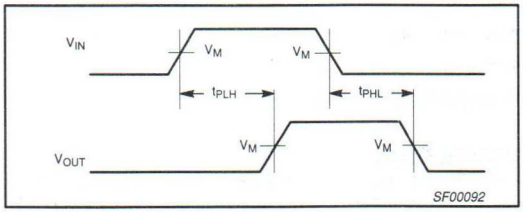
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay In to Y	Waveform 1	2.5 2.5	4.5 4.5	7.0 7.0	2.5 2.5	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay In to $\overline{Y}$	Waveform 2	2.0 1.0	4.0 2.0	7.0 4.5	2.0 1.0	7.5 5.0	ns
t_{PLH} t_{PHL}	Propagation delay Sn to Y	Waveform 1, 2	4.5 4.0	6.5 6.0	10.0 8.5	4.0 3.5	11.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay Sn to $\overline{Y}$	Waveform 1, 2	3.5 2.5	5.5 4.5	8.5 7.0	3.0 2.0	9.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Y	Waveform 1	4.0 3.0	6.5 5.0	9.0 7.0	3.5 3.0	9.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{Y}$	Waveform 1	2.5 2.0	4.5 3.5	6.5 5.5	2.5 1.5	7.0 6.0	ns

AC WAVEFORMS

For all waveforms, V_M = 1.5V

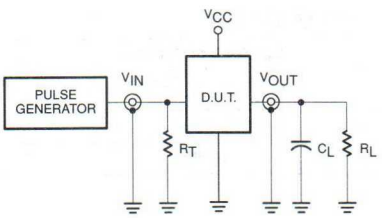


Waveform 1. For Inverting Outputs

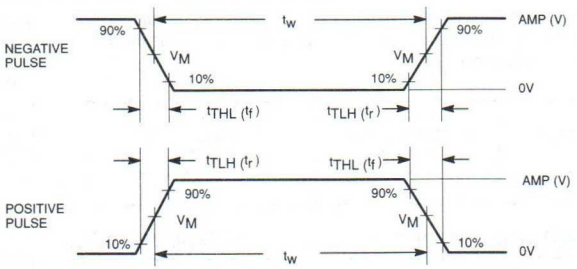


Waveform 2. For Non-Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Dual 4-line to 1-line multiplexer 74F153

FEATURES

- Non-inverting outputs
- Separate enable for each section
- Common select inputs
- See 74F253 for 3-State version

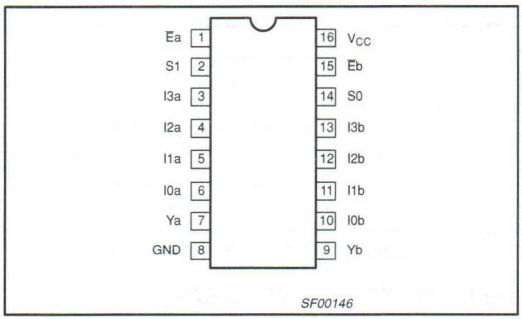
DESCRIPTION

The 74F153 is a dual 4-input multiplexer that can select 2 bits of data from up to four sources selected by common Select inputs (S0, S1). The two 4-input multiplexer circuits have individual active-Low Enables ($\overline{E}a$, $\overline{E}b$) which can be used to strobe the outputs independently. Outputs (Ya, Yb) are forced Low when the corresponding Enables ($\overline{E}a$, $\overline{E}b$) are High.

The 74F153 is the logic implementation of a 2-pole, 4-position switch where the switch is determined by the logic levels supplied to the common select inputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F153	7.0ns	12mA

PIN CONFIGURATION



ORDERING INFORMATION

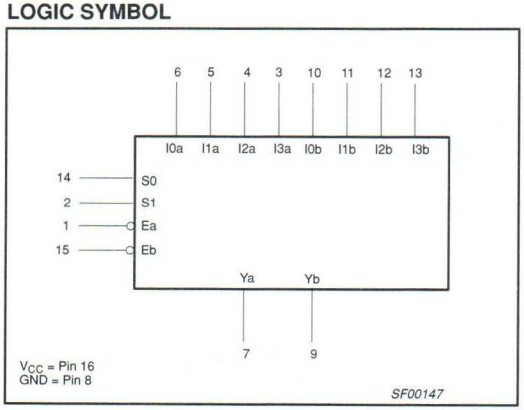
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG. DWG. #
16-pin plastic DIP	N74F153N	SOT38-4
16-pin plastic SO	N74F153D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

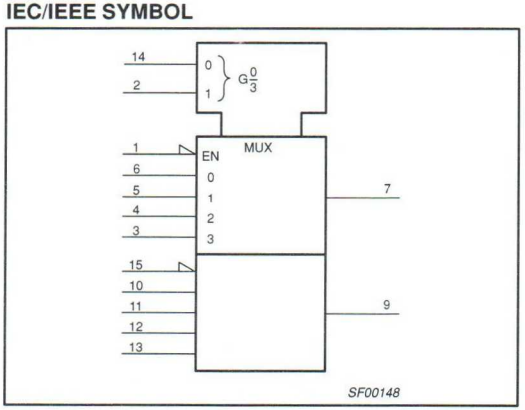
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I0a – I3a	Port A data inputs	1.0/1.0	20μA/0.6mA
I0b – I3b	Port B data inputs	1.0/1.0	20μA/0.6mA
S0, S1	Common Select inputs	1.0/1.0	20μA/0.6mA
$\overline{E}a$	Port A Enable input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{E}b$	Port B Enable input (active Low)	1.0/1.0	20μA/0.6mA
Ya, Yb	Port A, B data outputs	50/33	1.0μA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

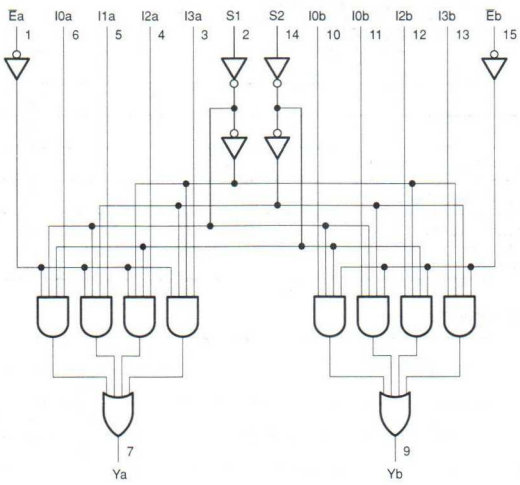
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

INPUTS							OUTPUT
S0	S1	$\overline{E}n$	I0n	I1n	I2n	I3n	Yn
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	$\overline{En}$ = GND, Sn=In=4.5V		12	20	mA
		I_{CCL}		En=Sn=In=GND		12	20	mA

NOTES:

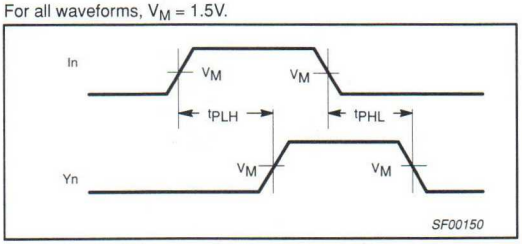
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

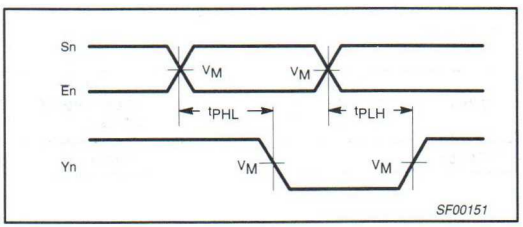
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay In to Yn	Waveform 1	3.0 3.0	4.5 5.0	7.0 7.5	2.5 2.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay Sn to Yn	Waveform 2	5.0 5.0	8.0 8.0	10.5 10.5	4.5 4.5	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{En}$ to Yn	Waveform 2	5.0 4.0	7.5 5.5	9.0 7.0	4.5 3.5	10.5 8.0	ns

AC WAVEFORMS

For all waveforms, V_M = 1.5V.

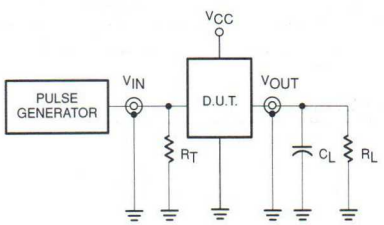


Waveform 1. Propagation Delay, Data to Output

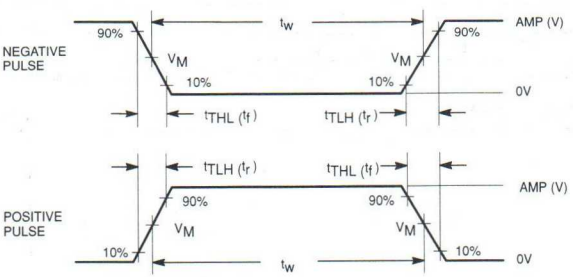


Waveform 2. Propagation Delay, Enable and Select to Output

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Decoder/demultiplexer — 74F154

FEATURES

- 16-line demultiplexing capability
- Mutually exclusive outputs
- 2-input enable gate for strobing or expansion

DESCRIPTION

The 74F154 decoder accepts four active High binary address inputs and provides 16 mutually exclusive active Low outputs. The 2-input Enable ($\overline{E}0$, $\overline{E}1$) gate can be used to strobe the decoder to eliminate the normal decoding "glitches" on the outputs, or it can be used for expansion of the decoder. The enable gate has two AND'ed inputs which must be Low to enable the outputs.

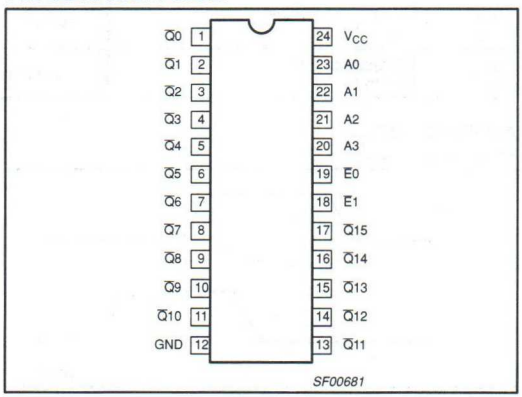
The 74F154 can be used as 1-of-16 demultiplexer by using one of the Enable inputs as the multiplexed data input. When the other Enable is Low, the addressed output will follow the state of the applied data.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F154	5.5 ns	26mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
24-pin plastic Slim DIP (300mil)	N74F154N	SOT222-1
24-pin plastic SOL	N74F154D	SOT137-1

PIN CONFIGURATION

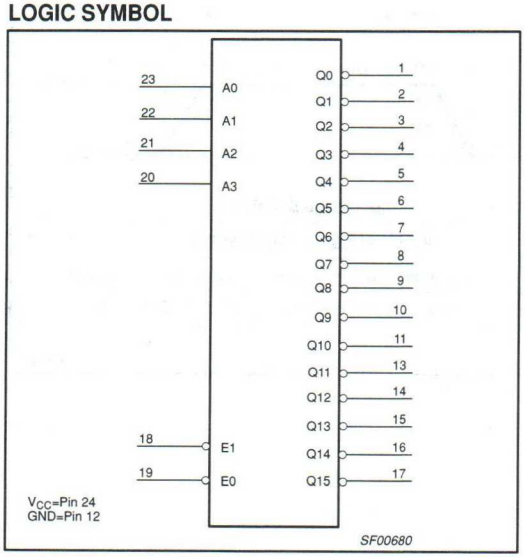


INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

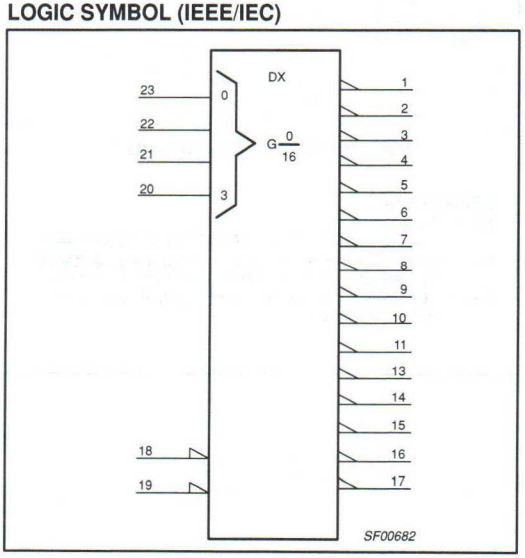
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A3	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{E}0$, $\overline{E}1$	Enable inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}0$ – $\overline{Q}15$	Data outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

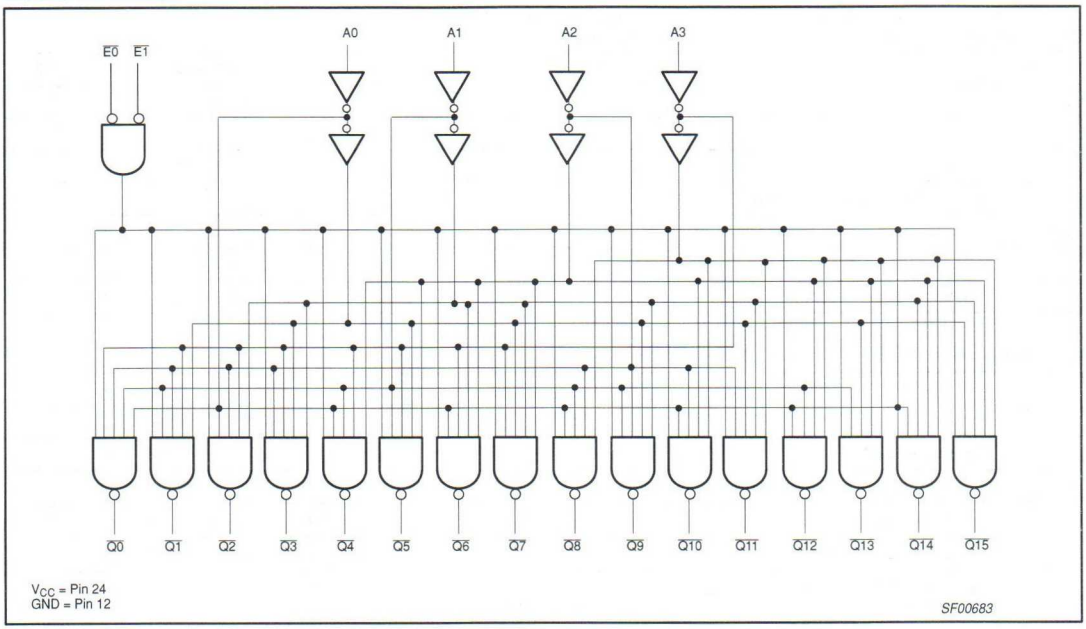
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS									OUTPUTS						
E0	E1	A0	A1	A2	A3	O0	O1	O2	O3	O4	O5	O6	O7	O8	O9	O10	O11	O12	O13	O14	O15
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			26	40	mA
		I_{CCL}	V_{CC} = MAX			35	45	mA

NOTES:

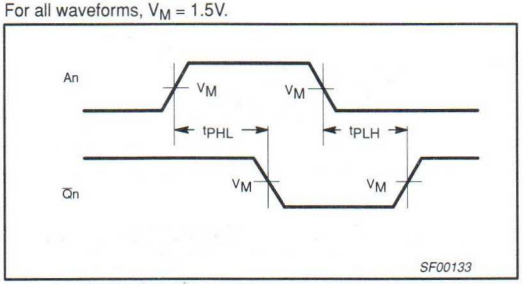
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

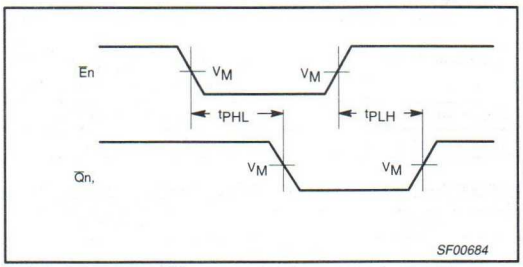
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to $\overline{Q}$n	Waveform 1	2.0 3.5	5.0 6.5	9.5 10.0	1.5 3.0	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$n to Qn	Waveform 2	2.0 4.0	4.0 6.0	7.5 9.0	1.5 3.5	8.0 9.5	ns

AC WAVEFORMS

For all waveforms, V_M = 1.5V.

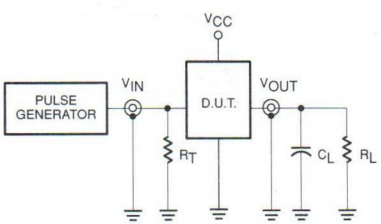


Waveform 1. Propagation Delay for Address to Output

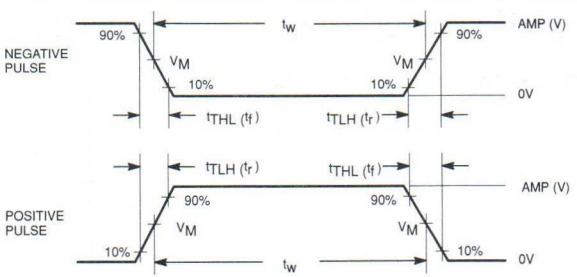


Waveform 2. Propagation Delay for Enable to Output

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Data selectors/multiplexers — 74F157A, 74F158A

74F157A: Quad 2-input data selector/multiplexer, non-inverting
74F158A: Quad 2-input data selector/multiplexer, inverting

DESCRIPTION

The 74F157A is a high speed Quad 2-Input Multiplexer which selects 4 bits of data from one of two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active when Low. When $\overline{E}$ is High, all of the outputs (Yn) are forced Low regardless of all other input conditions.

Moving data from two registers to a common output bus is a common use of the 74F157A. The state of the Select input determines the particular register from which the data comes.

The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

The 74F158A is similar, but has inverting outputs ($\overline{Y}$n).

- Industrial temperature range (–10°C to +85°C) available for 74F157A

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F157	4.6ns	15mA
74F157A	4.6ns	15mA
74F158	3.7ns	10mA
74F158A	3.7ns	10mA

ORDERING INFORMATION

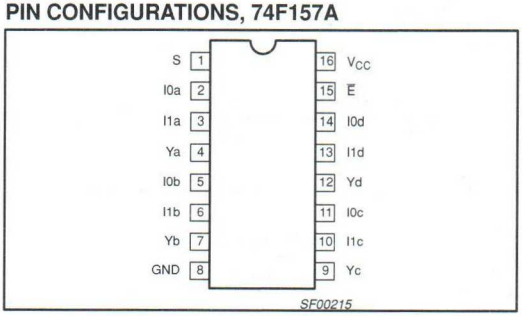
DESCRIPTION	ORDER CODE		PKG. DWG. #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
16-pin plastic DIP	N74F157AN, N174F158AN	I74F157AN	SOT38-4
16-pin plastic SO	N74F157AD, N74F158AD	I74F157AD	SOT109-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

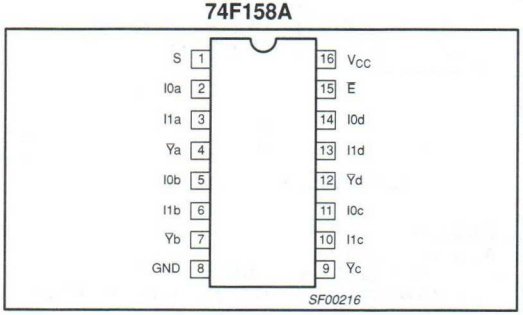
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ina, Inb, Inc, Ind	Data inputs	1.0/1.0	20µA/0.6mA
S	Select input	1.0/1.0	20µA/0.6mA
$\overline{E}$	Enable input	1.0/1.0	20µA/0.6mA
Ya–Yd	Data outputs (74F157/74F157A)	50/33	1.0mA/20mA
$\overline{Y}$a–$\overline{Y}$d	Data outputs (74F158/74F158A)	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

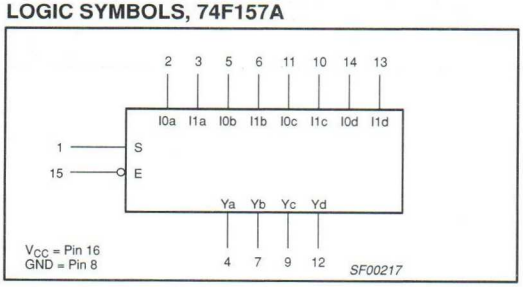
PIN CONFIGURATIONS, 74F157A



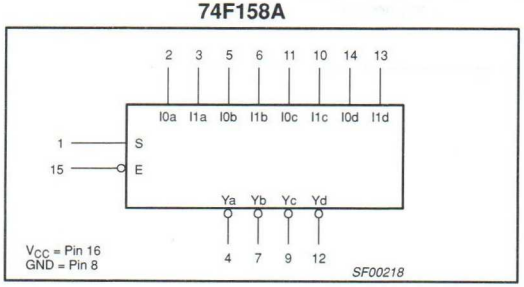
74F158A



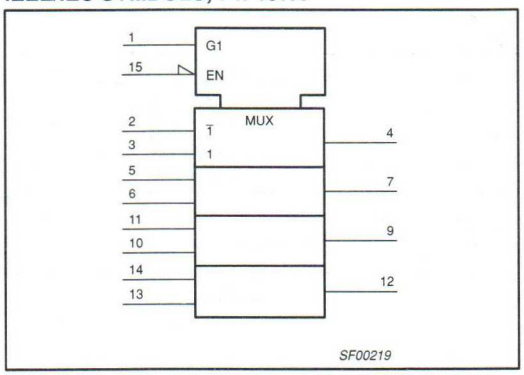
LOGIC SYMBOLS, 74F157A



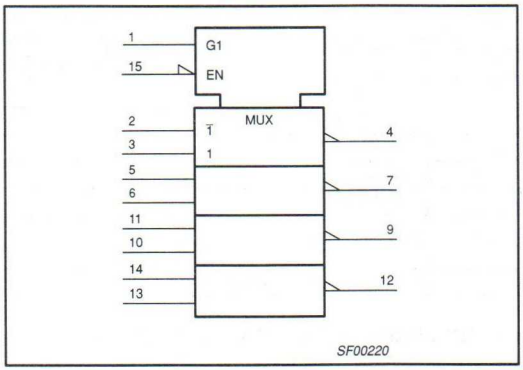
74F158A



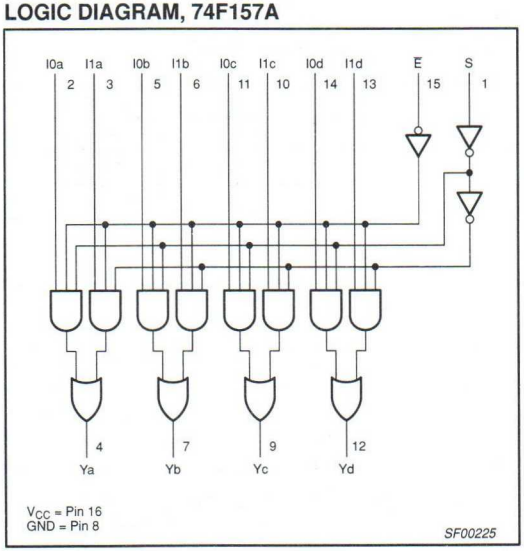
IEEE/IEC SYMBOLS, 74F157A



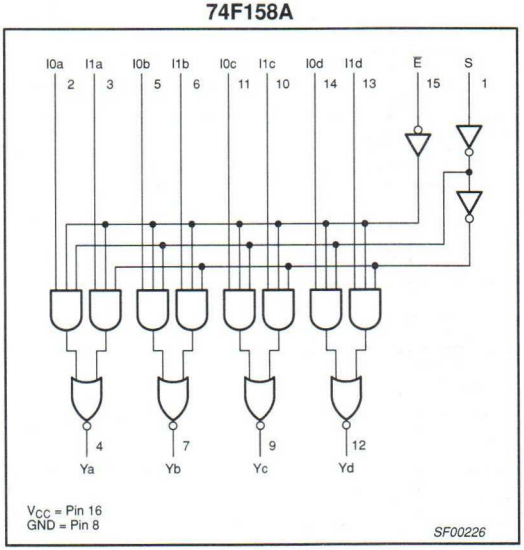
74F158A



LOGIC DIAGRAM, 74F157A



74F158A



FUNCTION TABLE, 74F157A

INPUTS				OUTPUT
E	S	I0n	I1n	Yn
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High voltage level
L = Low voltage level
X = Don't care

74F158A

INPUTS				OUTPUT
E	S	I0n	I1n	Yn
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state		40	mA
T_{amb}	Operating free-air temperature range	Commercial Range	0 to +70	°C
		Industrial Range 74F157A only	−40 to +85	
T_{stg}	Storage temperature range		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current				−1	mA
I_{OL}	Low-level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial Range	0		70	
		Industrial Range 74F157A only	−40		85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)[4]	74F157A	V_{CC} = MAX			15.0	23.0	mA
		74F158A				14.0	19.0	mA

NOTES:

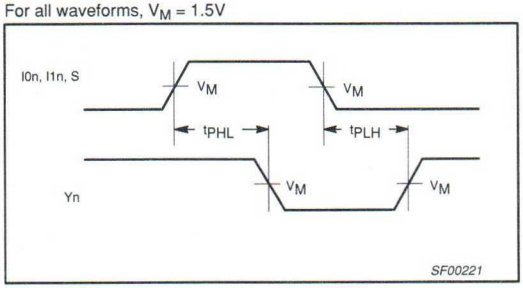
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

AC ELECTRICAL CHARACTERISTICS FOR 74F157A AND 74F158A

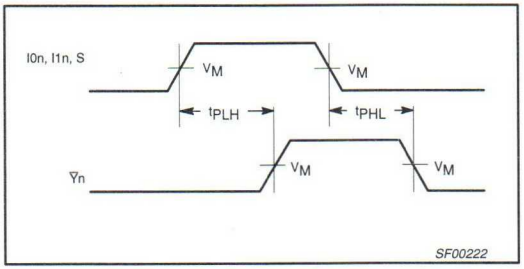
SYMBOL	PARAMETER		TEST CONDITION	LIMITS							UNIT
				V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF R_L = 500Ω		V_{CC} = +5.0V ± 10% T_{amb} = −40°C to +85°C C_L = 50pF R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay I0n, I1n to Yn	74F157A	Waveform 1	3.5 2.5	4.5 3.5	6.5 5.0	3.0 1.5	7.0 6.0	3.0 1.5	7.5 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Yn		Waveform 3	6.0 4.0	7.5 5.0	9.0 6.5	5.5 4.0	10.5 7.0	5.5 4.0	11.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay S to Yn		Waveform 1	5.5 4.5	7.5 6.0	10.0 7.5	5.0 4.0	11.0 8.5	5.0 4.0	11.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay I0n, I1n to $\overline{Y}$n	74F158A	Waveform 2	3.0 1.5	4.0 2.5	6.0 4.0	2.5 1.0	7.0 4.5	—	—	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{Y}$n		Waveform 4	4.5 5.0	5.5 6.0	7.0 7.5	4.0 5.0	7.5 8.0	—	—	ns
t_{PLH} t_{PHL}	Propagation delay S to $\overline{Y}$n		Waveform 2	4.5 4.0	6.5 5.5	8.5 7.5	4.0 3.5	9.5 8.0	—	—	ns

AC WAVEFORMS

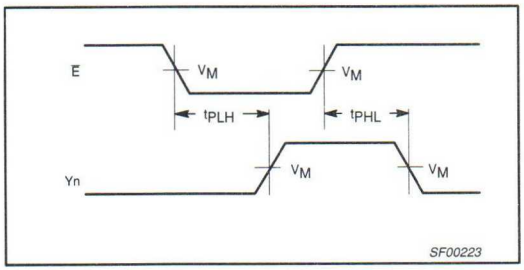
For all waveforms, V_M = 1.5V



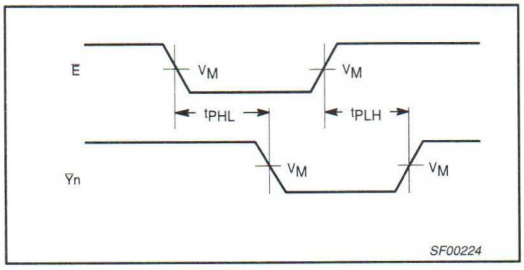
Waveform 1. Propagation Delay for Data and Select to Output



Waveform 2. Propagation Delay for Data and Select to Output

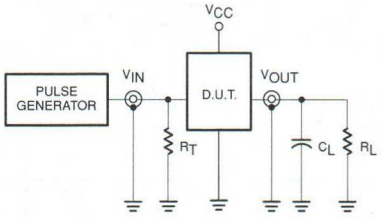


Waveform 3. Propagation Delay for Enable to Output

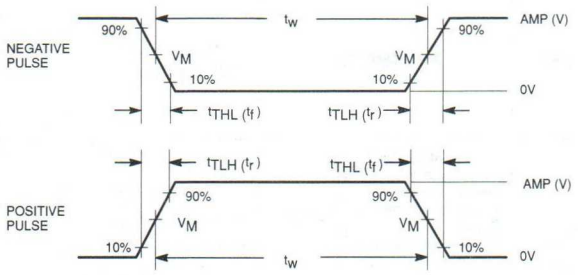


Waveform 4. Propagation Delay for Enable to Output

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

4-bit binary counters 74F161A, 74F163A

FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive edge-triggered clock
- Asynchronous Master Reset (74F161A)
- Synchronous Reset (74F163A)
- High speed synchronous expansion
- Typical count rate of 130MHz
- Industrial range (–40°C to +85°C) available

DESCRIPTION

4-bit binary counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock. The clock input is buffered.

The outputs of the counters may be preset to High or Low level. A Low level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the D0–D3 inputs to be loaded into the counter on the positive-going edge of the clock (provided that the setup and hold requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

A Low level at the Master Reset ($\overline{MR}$) input sets all the four outputs of the flip-flops (Q0 – Q3) in 74F161A to Low levels, regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function). For the 74F163A, the clear function is synchronous. A Low level at the Synchronous Reset ($\overline{SR}$) input sets all four outputs of the flip-flops (Q0 – Q3) to Low levels after the next positive-going transition on the clock (CP) input (provided that the setup and hold time requirements for $\overline{SR}$ are met). This action occurs regardless of the levels at $\overline{PE}$, CET, and CEP inputs. The synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate (see Figure 1). The carry look-ahead simplifies serial cascading of the counters. Both Count Enable (CEP and CET) inputs must be High to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a High output pulse of a duration approximately equal to the High level output of Q0. This pulse can be used to enable the next cascaded stage (see Figure 2). The TC output is subjected to decoding spikes due to internal race conditions. Therefore, it is not recommended for use as clock or asynchronous reset for flip-flops, registers, or counters.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F161A 74F163A	130MHz	46mA

ORDERING INFORMATION

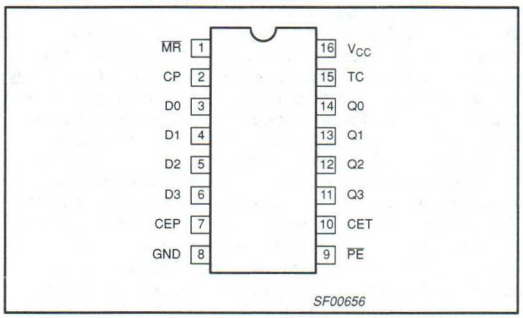
DESCRIPTION	ORDER CODE		DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
16-pin plastic DIP	N74F161AN, N74F163AN	I74F161AN, I74F163AN	SOT38-4
16-pin plastic SO	N74F161AD, N74F163AD	I74F161AD, I74F163AD	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

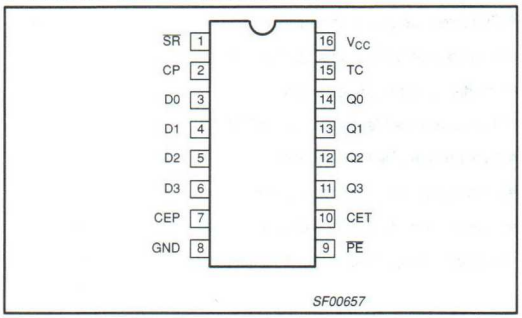
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D3	Data inputs	1.0/1.0	20µA/0.6mA
CEP	Count Enable Parallel input	1.0/1.0	20µA/0.6mA
CET	Count Enable Trickle input	1.0/2.0	20µA/1.2mA
CP	Clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/2.0	20µA/1.2mA
$\overline{MR}$	Asynchronous Master Reset input (active Low) for 74F161A	1.0/1.0	20µA/0.6mA
$\overline{SR}$	Synchronous Reset input (active Low) for 74F163A	1.0/1.0	20µA/0.6mA
TC	Terminal count output	50/33	1.0mA/20mA
Q0 – Q3	Flip-flop outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

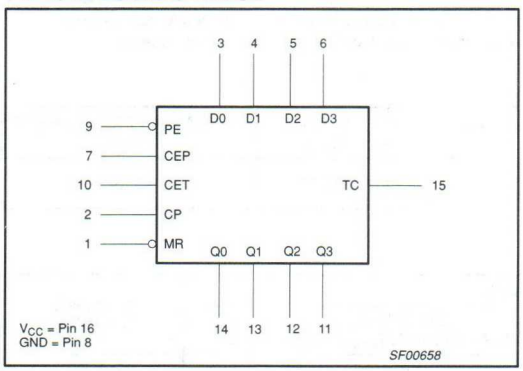
74F161A PIN CONFIGURATION



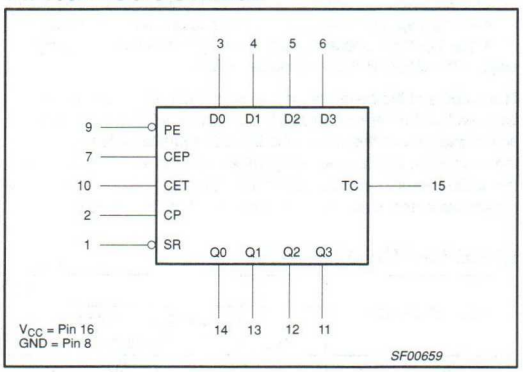
74F163A PIN CONFIGURATION



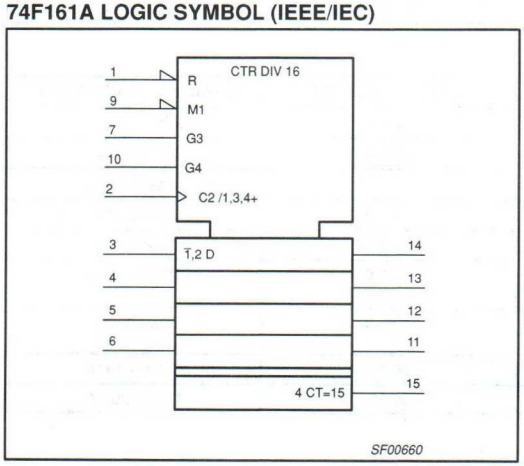
74F161A LOGIC SYMBOL



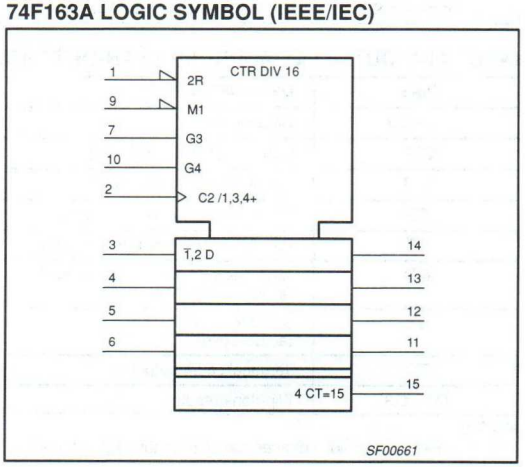
74F163A LOGIC SYMBOL



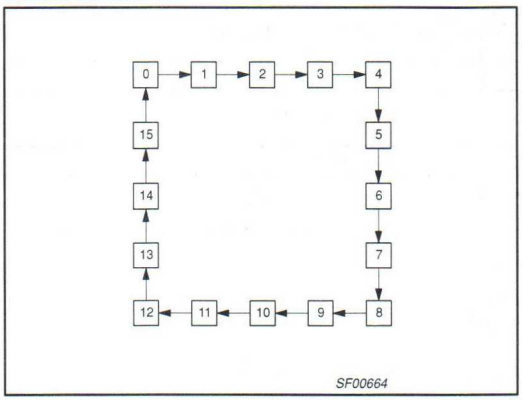
74F161A LOGIC SYMBOL (IEEE/IEC)



74F163A LOGIC SYMBOL (IEEE/IEC)



STATE DIAGRAM



APPLICATIONS

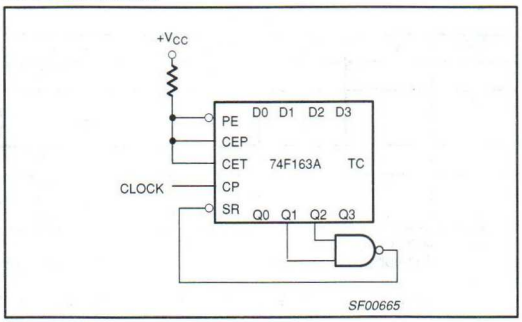


Figure 1. Maximum count modifying scheme
Terminal count = 6

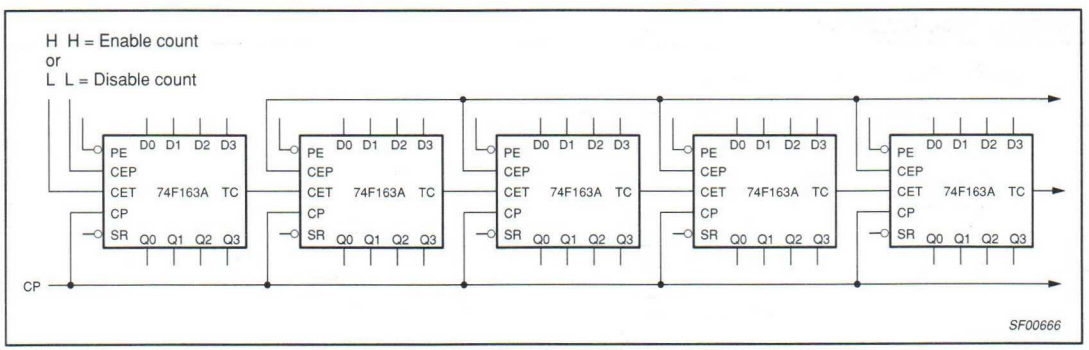


Figure 2. Synchronous multistage counting scheme

74F161A MODE SELECT – FUNCTION TABLE

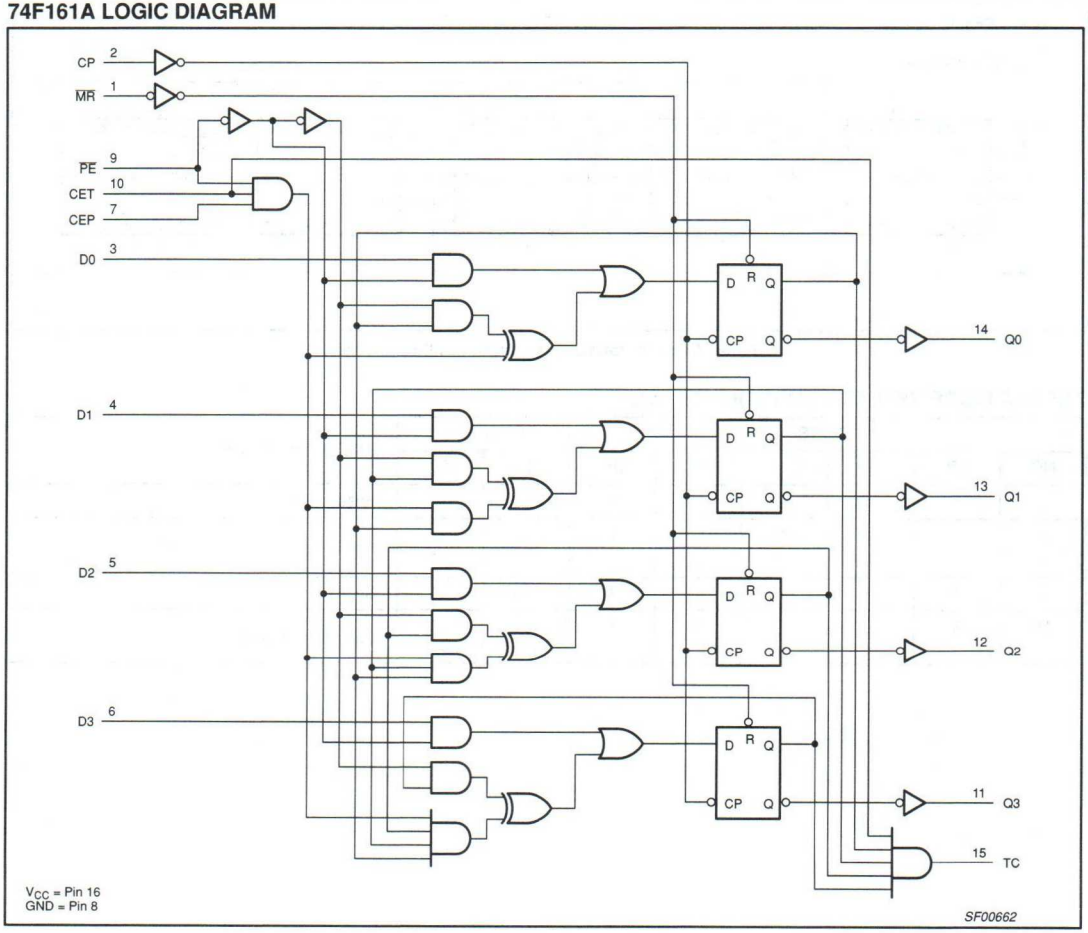
INPUTS						OUTPUTS		OPERATING MODE
$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	Dn	Qn	TC	
L	X	X	X	X	X	L	L	Reset (clear)
H	↑	X	X	l	l	L	L	Parallel load
H	↑	X	X	l	h	H	(1)	
H	↑	h	h	h	X	count	(1)	Count
H	X	l	X	h	X	q_n	(1)	Hold (do nothing)
H	X	X	l	h	X	q_n	L	

74F163A MODE SELECT – FUNCTION TABLE

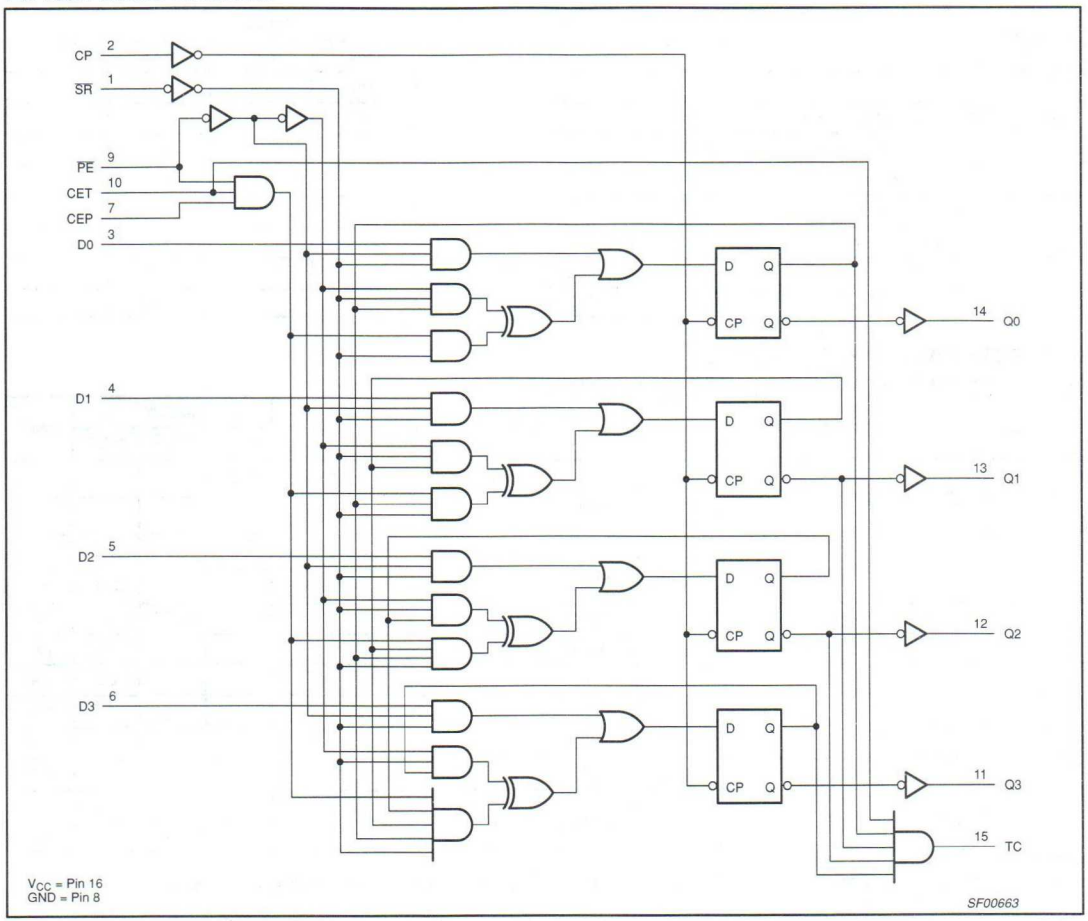
INPUTS						OUTPUTS		OPERATING MODE
$\overline{SR}$	CP	CEP	CET	$\overline{PE}$	Dn	Qn	TC	
l	↑	X	X	X	X	L	L	Reset (clear)
h	↑	X	X	l	l	L	L	Parallel load
h	↑	X	X	l	h	H	(2)	
h	↑	h	h	h	X	count	(2)	Count
h	X	l	X	h	X	q_n	(2)	Hold (do nothing)
h	X	X	l	h	X	q_n	L	

H = High voltage level
h = High voltage level one setup prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup prior to the Low-to-High clock transition
q_n = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
(1) = The TC output is High when CET is High and the counter is at Terminal Count (HHHH for 74F161A)
(2) = The TC output is High when CET is High and the counter is at Terminal Count (HHHH for 74F163A)

74F161A LOGIC DIAGRAM



74F163A LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state		40	mA
T_{amb}	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current				–1	mA
I_{OL}	Low-level output current				20	mA
T_{amb}	Operating free-air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	CET, $\overline{PE}$	V_{CC} = MAX, V_I = 0.5V					–1.2	mA
		others						–0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				42	55	mA
		I_{CCL}					49	65	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

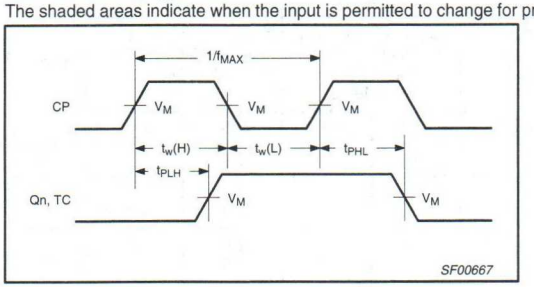
SYMBOL	PARAMETER		TEST CONDITION	LIMITS							UNIT
				T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency		Waveform 1	100	130		90		75		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn ($\overline{PE}$ = High)		Waveform 1	2.0 4.0	4.0 6.5	6.5 10.0	2.0 4.0	7.0 11.0	2.0 4.0	7.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Qn ($\overline{PE}$ = Low)		Waveform 1	2.0 3.5	4.5 5.5	6.5 8.5	2.0 3.5	7.5 9.5	2.0 3.5	7.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		Waveform 1	5.0 4.5	7.5 7.5	10.5 10.5	5.0 4.0	11.5 11.5	5.0 4.0	11.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC		Waveform 2	1.5 2.5	3.5 5.0	6.5 7.5	1.5 2.5	7.0 8.0	1.5 2.5	7.0 8.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn	'F161A	Waveform 3	6.0	8.5	12.0	5.5	13.0	5.5	13.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	'F161A	Waveform 3	5.0	8.5	10.0	5.0	11.0	5.0	11.0	ns

AC SETUP REQUIREMENTS

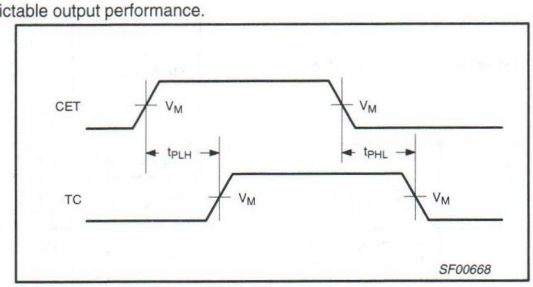
SYMBOL	PARAMETER		TEST CONDITION	LIMITS				UNIT
				T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω		T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω	T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω	
				MIN	TYP	MIN	MIN	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to CP		Waveform 6	5.0 5.0		5.0 5.0	5.0 5.0	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP		Waveform 6	0 0		0 0	0 0	ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP		Waveform 5 or 6	9.0 6.5		9.5 7.0	9.5 7.0	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP		Waveform 5 or 6	0 0		0 0	0 0	ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low CET or CEP to CP		Waveform 4	10.5 6.0		10.5 7.0	10.5 7.0	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CET or CEP to CP		Waveform 4	0 0		0 0	0 0	ns
$t_w(H)$ $t_w(L)$	CP pulse width (Load) High or Low		Waveform 1	4.0 5.0		4.0 5.5	4.0 7.0	ns
$t_w(H)$ $t_w(L)$	CP pulse width (Count) High or Low		Waveform 1	4.0 6.0		4.0 7.0	4.0 7.0	ns
$t_w(L)$	$\overline{MR}$ pulse width Low	'F161A	Waveform 3	4.5		4.5	4.5	ns
t_{REC}	Recovery time $\overline{MR}$ to CP	'F161A	Waveform 3	6.0		6.5	6.5	ns

AC WAVEFORMS

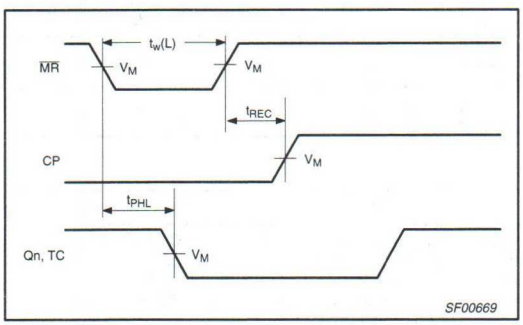
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



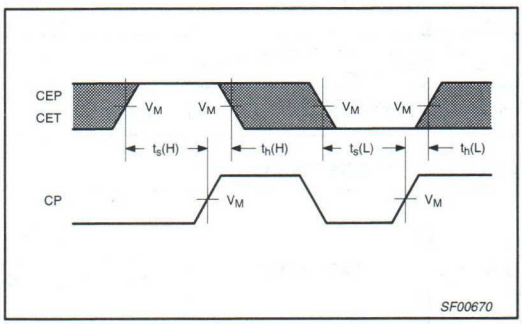
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



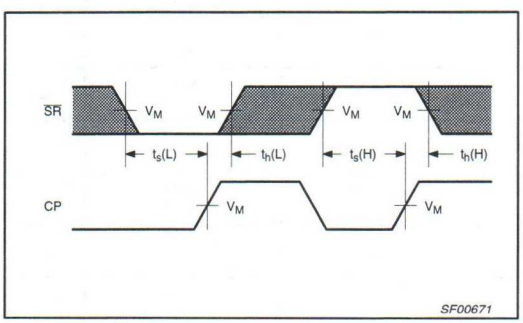
Waveform 2. Propagation Delay, CET Input to TC Output



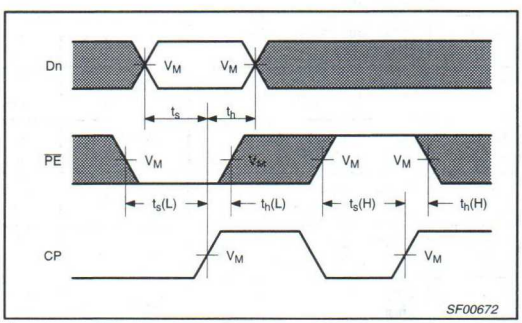
Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay, and Master Reset to Recovery Time



Waveform 4. CEP and CET Reset Setup and Hold Times

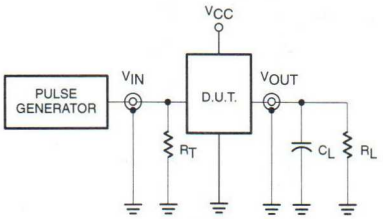


Waveform 5. Synchronous Reset Setup and Hold Times

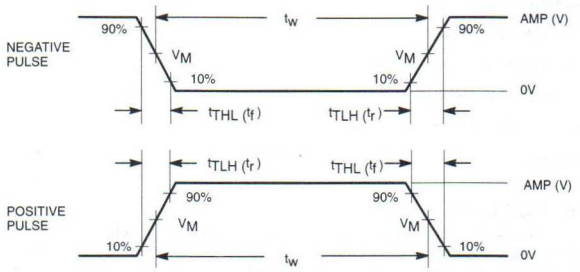


Waveform 6. Parallel Data and Parallel Enable Setup and Hold Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

8-bit serial-in parallel-out shift register | 74F164

FEATURES

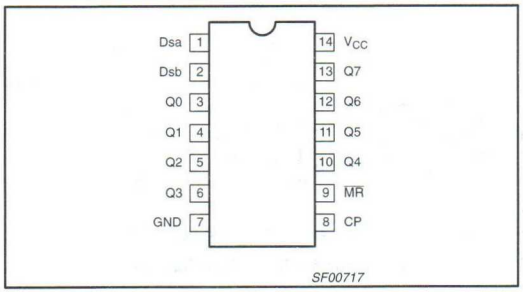
- Gated serial data inputs
- Typical shift frequency of 100MHz
- Asynchronous Master Reset
- Buffered clock and data inputs
- Fully synchronous data transfer
- Industrial temperature range available (–40°C to +85°C)

DESCRIPTION

The 74F164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered through one of two inputs (Dsa, Dsb); either input can be used as an active High enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied High.

Data shifts one place to the right on each Low-to-High transition of the clock (CP) input, and enters into Q0 the logical AND of the two data inputs (Dsa, Dsb) that existed one setup time before the rising edge. A Low level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs Low.

PIN CONFIGURATION



TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F164	100MHz	33mA

ORDERING INFORMATION

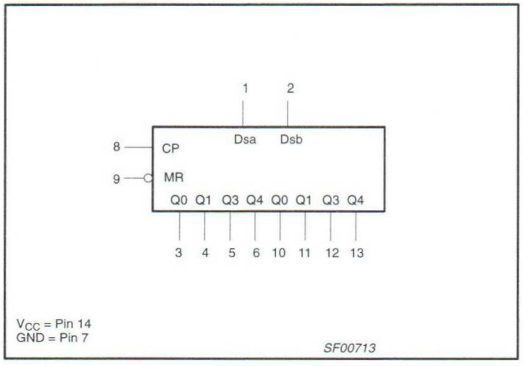
DESCRIPTION	ORDER CODE		DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
14-pin plastic DIP	74F164N	I74F164N	SOT27-1
14-pin plastic SO	74F164D	I74F164D	SOT108-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

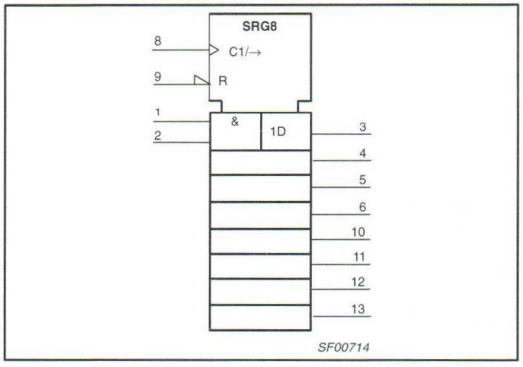
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dsa, Dsb	Data inputs	1.0/1.0	20μA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master reset input (active-Low)	1.0/1.0	20μA/0.6mA
Q0 – Q7	Data outputs	50/33	1.0mA/20mA

One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

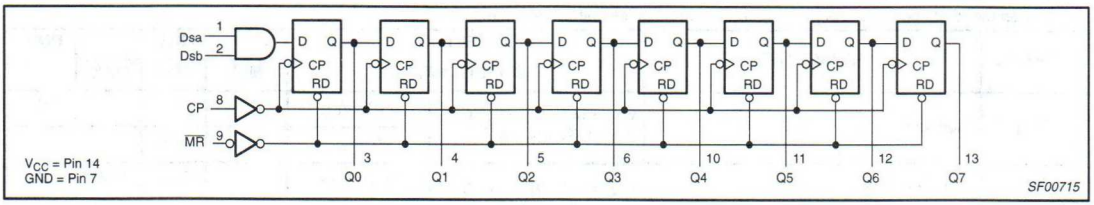
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS								OPERATING MODE
$\overline{MR}$	CP	Dsa	Dsb	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	
L	X	X	X	L	L	L	L	L	L	L	L	Reset (Clear)
H	↑	l	l	L	q0	q1	q2	q3	q4	q5	q6	Shift
H	↑	l	h	L	q0	q1	q2	q3	q4	q5	q6	
H	↑	h	l	L	q0	q1	q2	q3	q4	q5	q6	
H	↑	h	h	H	q0	q1	q2	q3	q4	q5	q6	

H = High voltage level
h = High voltage level one setup time prior to the Low-to-High clock transition.
L = Low voltage level
l = Low voltage level one setup time prior to the Low-to-High clock transition.
qn = Lower case letter indicate the state of the referenced output one setup time prior to the Low-to-High clock transition.
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state		40	mA
T_{amb}	Operating free-air temperature range	Commercial Range	0 to +70	°C
		Industrial Range	−40 to +85	
T_{stg}	Storage temperature range		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMIT			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level iput voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{Ik}	Input clamp current				−18	mA
I_{OH}	High-level output current				−1	mA
I_{OL}	Low-level output current				20	mA
T_{amb}	Operating free-air temperature range	Commercial Range	0		+70	°C
		Industrial Range	−40		+85	

DC ELECTRICAL CHARACTERISTICS

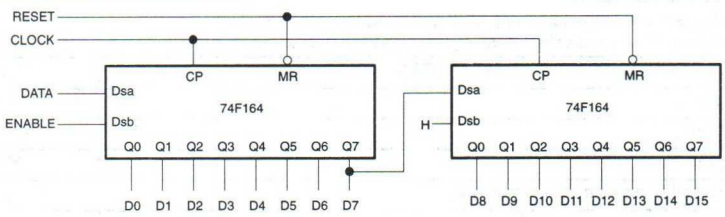
(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
			±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{ILL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		-60		–150	mA
I_{CC}	Supply current (total)4	V_{CC} = MAX			33	55	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
4. Measure I_{CC} with the serial inputs grounded, the clock input at 2.4V, and a momentary ground, then applied to Master Reset, and all outputs open.

APPLICATION



The 74F164 can be cascaded to form synchronous shift registers of longer length.
Here, two devices are combined to form a 16-bit shift register.

SF00716

AC ELECTRICAL CHARACTERISTICS

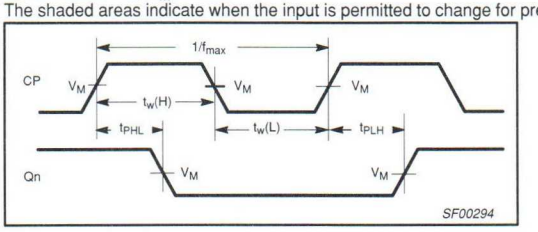
SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5V±10% C_L = 50pF R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5V±10% C_L = 50pF R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	80	100		80		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	Waveform 1	3.0 5.0	5.0 7.0	8.0 10.0	2.5 5.0	9.0 11.0	2.5 5.0	9.0 11.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn	Waveform 3	5.5	7.5	10.5	5.5	11.5	5.5	11.5	ns

AC SETUP REQUIREMENTS

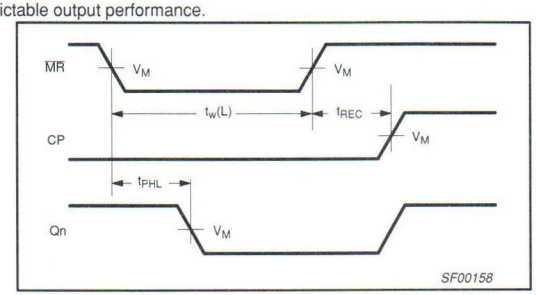
SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5V±10% C_L = 50pF R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5V±10% C_L = 50pF R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low D_n to CP	Waveform 2	7.0 7.0			7.0 7.0		7.0 7.0		ns
t_h(H) t_h(L)	Hold time, High or Low D_n to CP	Waveform 2	1.0 1.0			2.0 2.0		2.0 2.0		ns
t_w(H) t_w(L)	CP Pulse width High or Low	Waveform 1	4.0 7.0			4.0 7.0		4.0 7.0		ns
t_w(L)	$\overline{MR}$ Pulse wicth Low	Waveform 3	7.0			7.0		7.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 3	7.0			7.0		7.0		ns

AC WAVEFORMS

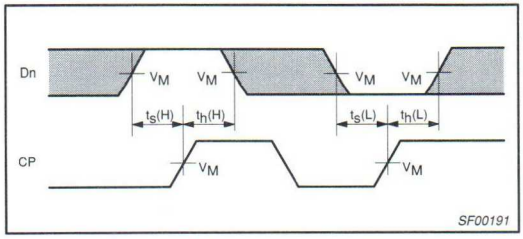
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation delay for Clock input to output, Clock Pulse width, and maximum Clock frequency

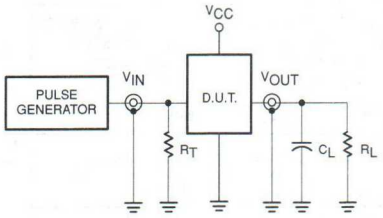


Waveform 3. Master Reset pulse width, Master Reset to output delay and Master Reset to Clock recovery time

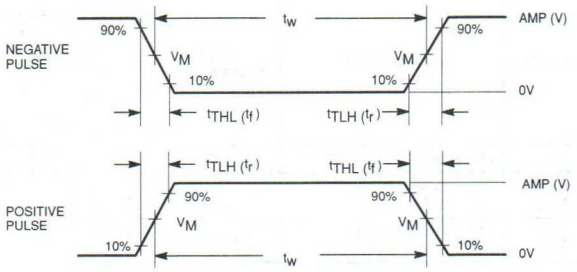


Waveform 2. Data setup and hold times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

8-bit bidirectional universal shift register 74F166

FEATURES

- High impedance NPN base inputs for reduced loading (20μA in high and low states)
- Synchronous parallel to serial applications
- Synchronous serial data input for easy expansion
- Clock enable for "do nothing" mode
- Asynchronous master reset
- Expandable to 16 bits in 8–bit increments
- Industrial temperature range available (–40°C to +85°C)

DESCRIPTION

The 74F166 is a high speed 8–bit shift register that has fully synchronous serial parallel data entry selected by an active low parallel enable ($\overline{PE}$) input. When the $\overline{PE}$ is low one setup time before the low–to–high clock transition, parallel data is entered into the register.

When $\overline{PE}$ is high, data is entered into internal bit position Q0 from serial data input (Ds), and the remaining bits are shifted one place to the right (Q0 → Q1 → Q2, etc.) with each positive going clock transition.

For expansion of the register in parallel to serial converters, the Q7 output is connected to the Ds input of the succeeding stage. The clock input is gated OR structure which allows one input to be used as an active–low clock enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The low–to–high transition of $\overline{CE}$ input should only take place while the CP is high for predictable operation. A low on the master reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a low state.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT(TOTAL)
74F166	175MHz	50mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
16–pin plastic DIP	N74F166N	I74F166N	SOT38-4
16–pin plastic SO	N74F166D	I74F166D	SOT109-1

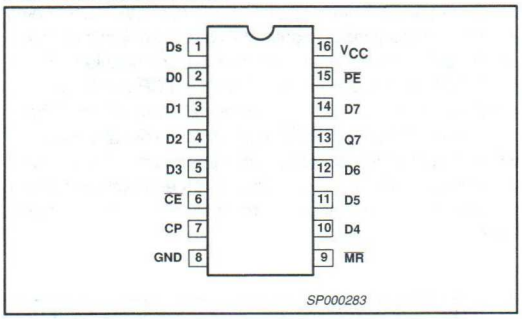
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/ LOW	LOAD VALUE HIGH/ LOW
D0 – D7	Parallel data inputs	1.0/0.033	20μA/20μA
Ds	Serial data input (shift right)	2.0/0.066	40μA/40μA
CP	Clock input (active rising edge)	1.0/0.033	20μA/20μA
$\overline{CE}$	Clock enable input (active low)	1.0/0.033	20μA/20μA
$\overline{PE}$	Parallel enable input (active low)	1.0/0.033	20μA/20μA
$\overline{MR}$	Master reset input (active low)	2.0/0.066	40μA/40μA
Q7	Data output	50/33	1.0mA/20mA

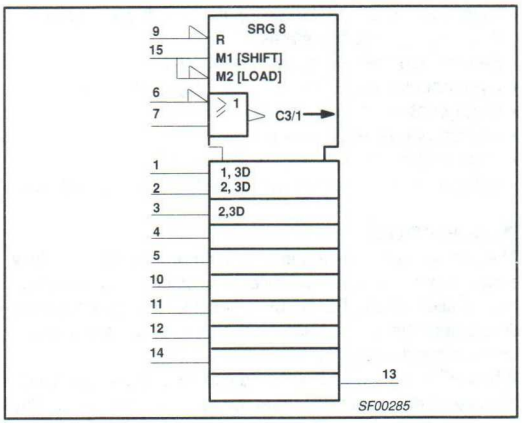
Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.

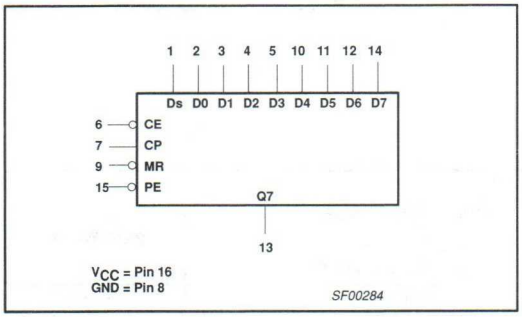
PIN CONFIGURATION



IEC/IEEE SYMBOL



LOGIC SYMBOL



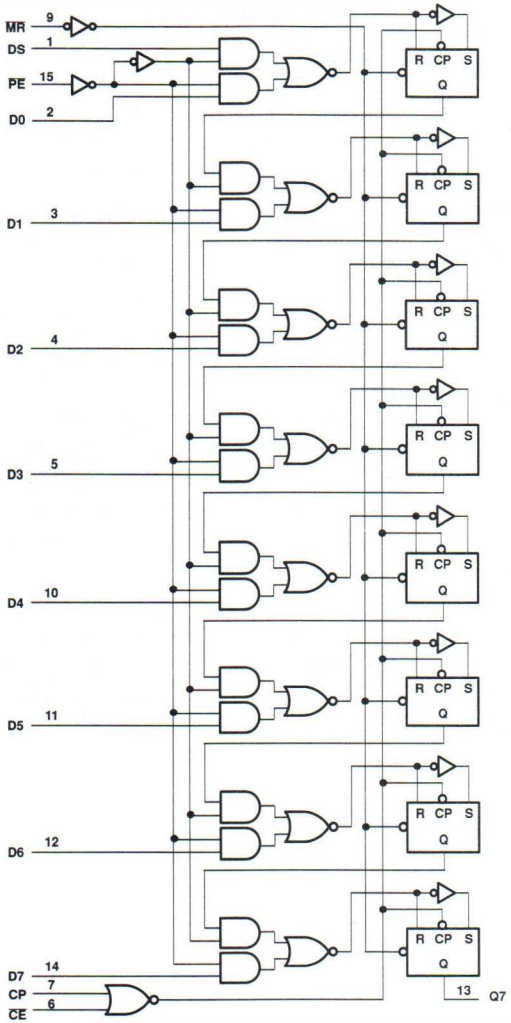
FUNCTION TABLE

INPUTS					Qn REGISTER		OUTPUT	OPERATING MODE
$\overline{PE}$	$\overline{CE}$	CP	DS	D0 –D7	Q0	Q1 – Q6	Q7	
l	l	↑	X	l – l	L	L – L	L	Parallel load
l	l	↑	X	h – h	H	H – H	H	
h	l	↑	l	X – X	L	q0 – q5	q6	Serial shift
h	l	↑	h	X – X	H	q0 – q5	q6	
X	h	X	X	X – X	qn	q1 – q6	q7	Hold (do nothing)

Notes to function table

1. H = High–voltage level
2. h = High voltage level one setup time before the low–to–high clock transition
3. L = Low–voltage level
4. l = Low voltage level one setup time before the low–to–high clock transition
5. qn = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the low–to–high clock transition
6. X = Don't care
7. ↑ = Low–to–high clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IN}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High–level output current				–1	mA
I_{OL}	Low–level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High–level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low–level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN		±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		$\overline{CE}$, CP[3]							
I_{IH}	High–level input current	others	V_{CC} = MAX, V_I = 2.7V					20	µA
		$\overline{MR}$, Ds						40	µA
		Industrial only: others						40	µA
		Industrial only: $\overline{MR}$, Ds						80	µA
I_{IL}	Low–level input current	others	V_{CC} = MAX, V_I = 0.5V					-20	µA
		$\overline{MR}$, Ds						-40	µA
I_{OS}	Short–circuit output current[4]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX, $\overline{PE}$ = $\overline{CE}$ = Dn = GND, $\overline{MR}$ = Ds = 4.5V, CP = ↑				50	70	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. When testing CP, $\overline{CE}$ must remain in high state, whereas CP must remain in high state when testing $\overline{CE}$.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

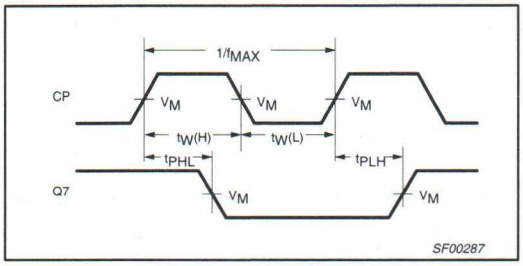
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_{amb} = +25°C; V_{CC} = +5.0V; C_L = 50pF; R_L = 500Ω			LIMITS T_{amb} = 0°C to +70°C; V_{CC} = +5.0V ± 10%; C_L = 50pF; R_L = 500Ω		LIMITS T_{amb} = –40°C to +85°C; V_{CC} = +5.0V ± 10%; C_L = 50pF; R_L = 500Ω		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	135	175		110		100		ns
t_{PLH} t_{PHL}	Propagation delay CP to Q7	Waveform 1	5.0 4.0	7.5 6.0	10.0 8.0	5.0 3.5	12.0 9.0	5.0 3.5	13.0 9.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q7	Waveform 2	4.0	6.5	8.5	4.0	9.5	4.0	9.5	ns

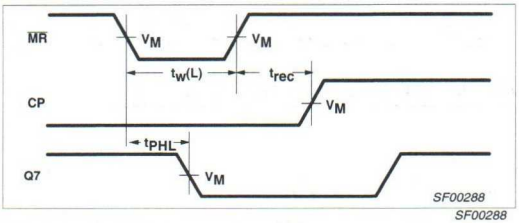
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = −40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{su} (H) t_{su}(L)	Setup time, high or low Dn, Ds to CP, $\overline{CE}$	Waveform 3	3.0 2.5			4.0 3.0		4.0 3.0		ns
t_h (H) t_h (L)	Hold time, high or low Dn, Ds to CP	Waveform 3	0.0 0.0			1.0 0.0		1.0 0.0		ns
t_h (H) t_h (L)	Hold time, high or low Dn, Ds to $\overline{CE}$	Waveform 3	1.5 0.0			2.0 0.0		2.0 0.0		ns
t_{su}(L)	Setup time, low $\overline{CE}$ to CP	Waveform 3	5.0			6.0		6.0		ns
t_h (H)	Hold time, high $\overline{CE}$ to CP	Waveform 3	0.0			0.0		0.0		ns
t_{su} (H) t_{su}(L)	Setup time, high or low $\overline{PE}$ to CP, $\overline{CE}$	Waveform 3	3.0 3.0			4.0 4.0		4.0 6.0		ns
t_h (H) t_h (L)	Hold time, high or low $\overline{PE}$ to CP	Waveform 3	0.0 0.0			0.0 0.0		0.0 0.0		ns
t_w (H) t_w (L)	CP pulse width, high or low	Waveform 1	3.0 4.5			3.5 5.0		3.5 6.0		ns
t_w (L)	$\overline{MR}$ pulse width, low	Waveform 2	4.0			4.0		4.0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 2	4.0			4.5		4.5		ns

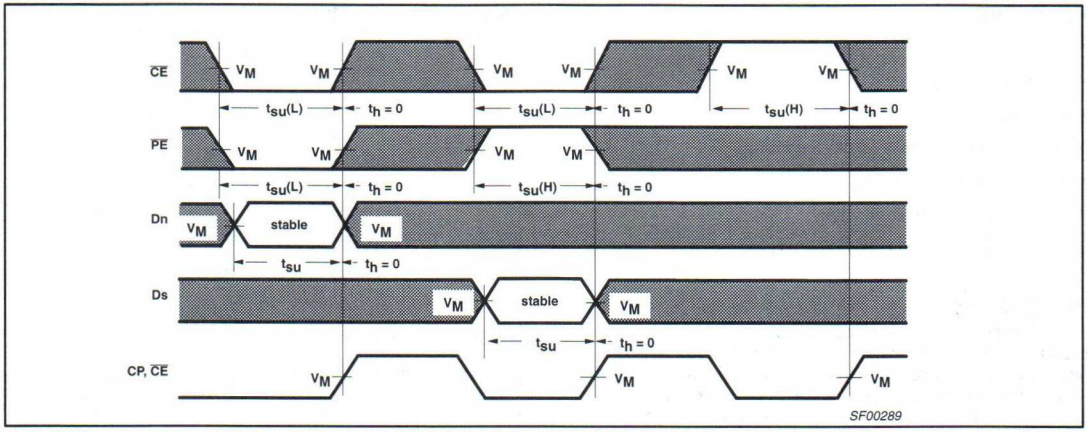
AC WAVEFORMS



Waveform 1. Propagation delay for clock input to output, clock pulse width, and maximum clock frequency



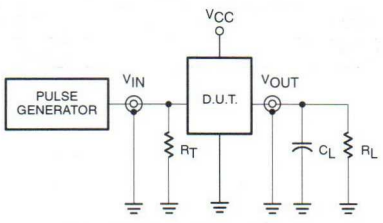
Waveform 2. Master reset pulse width, master reset to output delay and master reset to clock recovery time



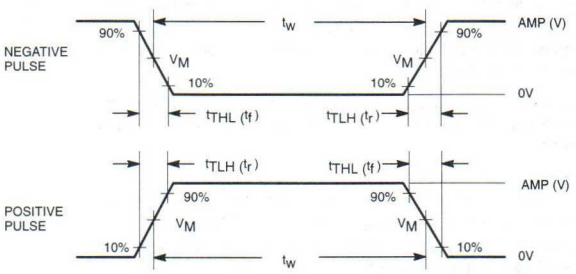
Waveform 3. Setup and hold times

Notes to AC waveforms
1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

4-bit up/down binary synchronous counter | 74F169

FEATURES

- Synchronous counting and loading
- Up/Down counting
- Modulo 16 binary counter
- Two Count Enable inputs for n-bit cascading
- Positive edge-triggered clock
- Built-in carry look-ahead capability
- Presettable for programmable operation

DESCRIPTION

The 74F169 is a 4-bit synchronous, presettable Modulo 16 up/down counter featuring an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed by the Count Enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the flip-flops on the Low-to-High transition of the clock.

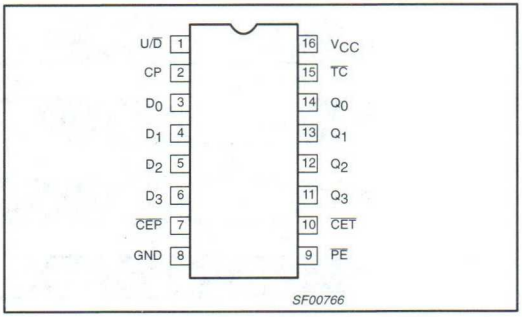
The counter is fully programmable; that is, the outputs may be preset to either level.

Presetting is synchronous with the clock and takes place regardless of the levels of the Count Enable inputs. A Low level on the Parallel Enable ($\overline{PE}$) input disables the counter and causes the data at the D_n input to be loaded into the counter on the next Low-to-High transition of the clock.

The direction of counting is controlled by the Up/Down (U/$\overline{D}$) input; a High will cause the count to increase, a Low will cause the count to decrease.

The carry look-ahead circuitry provides for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs ($\overline{CET}$, $\overline{CEP}$) and a Terminal Count ($\overline{TC}$) output. Both Count Enable inputs must be Low to count. The $\overline{CET}$ input is fed forward to enable the $\overline{TC}$ output. The $\overline{TC}$ output thus enabled will produce a Low output pulse with a duration approximately equal to the High level portion of the Q_0 output. The Low level $\overline{TC}$ pulse is used to enable successive cascaded stages.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F169	115MHz	35mA

ORDERING INFORMATION

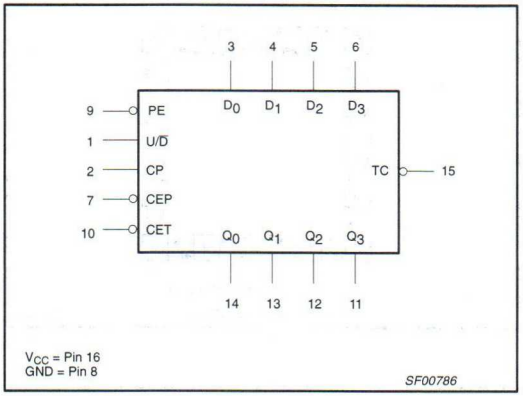
DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
16-pin plastic DIP	N74F169N	SOT38-4
16-pin plastic SO	N74F169D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

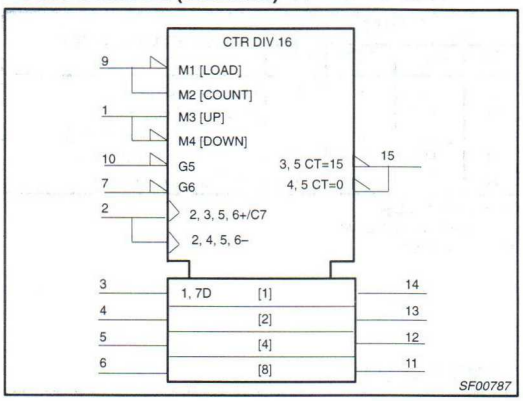
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Parallel data inputs	1.0/1.0	20µA/0.6mA
$\overline{CEP}$	Count Enable parallel input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/2.0	20µA/1.2mA
CP	Clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/1.0	20µA/0.6mA
U/$\overline{D}$	Up/Down count control input	1.0/1.0	20µA/0.6mA
Q_0 - Q_3	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{TC}$	Terminal count output (active Low)	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DESCRIPTION

The 74F169 uses edge-triggered J-K-type flip-flops and have no constraints on changing the control or data input signals in either state of the clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is Low, the data on the D_0 - D_3 inputs enter the flip-flops on the next rising edge of the Clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be Low and $\overline{PE}$ must be High; the U/$\overline{D}$ input determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally High and goes Low, provided that $\overline{CET}$ is Low, when a counter reaches zero in the Count Down mode or reaches 15 in the Count Up mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended (see logic equations below).

1) Count Enable = $\overline{CEP} \cdot \overline{CET} \cdot \overline{PE}$

2) Up: $\overline{TC} = Q_0 \cdot Q_3 \cdot (U/\overline{D}) \cdot \overline{CET}$

3) Down: $\overline{TC} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (U/\overline{D}) \cdot \overline{CET}$

MODE SELECT — FUNCTION TABLE

INPUTS						OUTPUTS		OPERATING MODE
CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	D_n	Q_n	$\overline{TC}$	
↑	X	X	X	l	l	L	(1)	Parallel load (Dn→Qn)
↑	X	X	X	X	X	H	(1)	
↑	h	l	l	h	X	Count Up	(1)	Count Up (increment)
↑	l	l	l	h	X	Count Down	(1)	Count Down (decrement)
↑	X	h	X	h	X	q_n	(1)	Hold (do nothing)
↑	X	X	X	h	X	q_n	H	

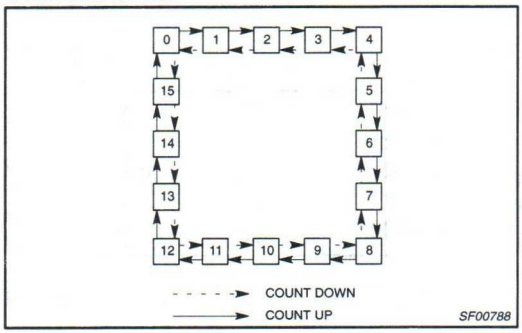
H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the Low-to-High clock transition
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
(1) = The $\overline{TC}$ is Low when $\overline{CET}$ is Low and the counter is at Terminal Count. Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL).

MODE SELECT TABLE

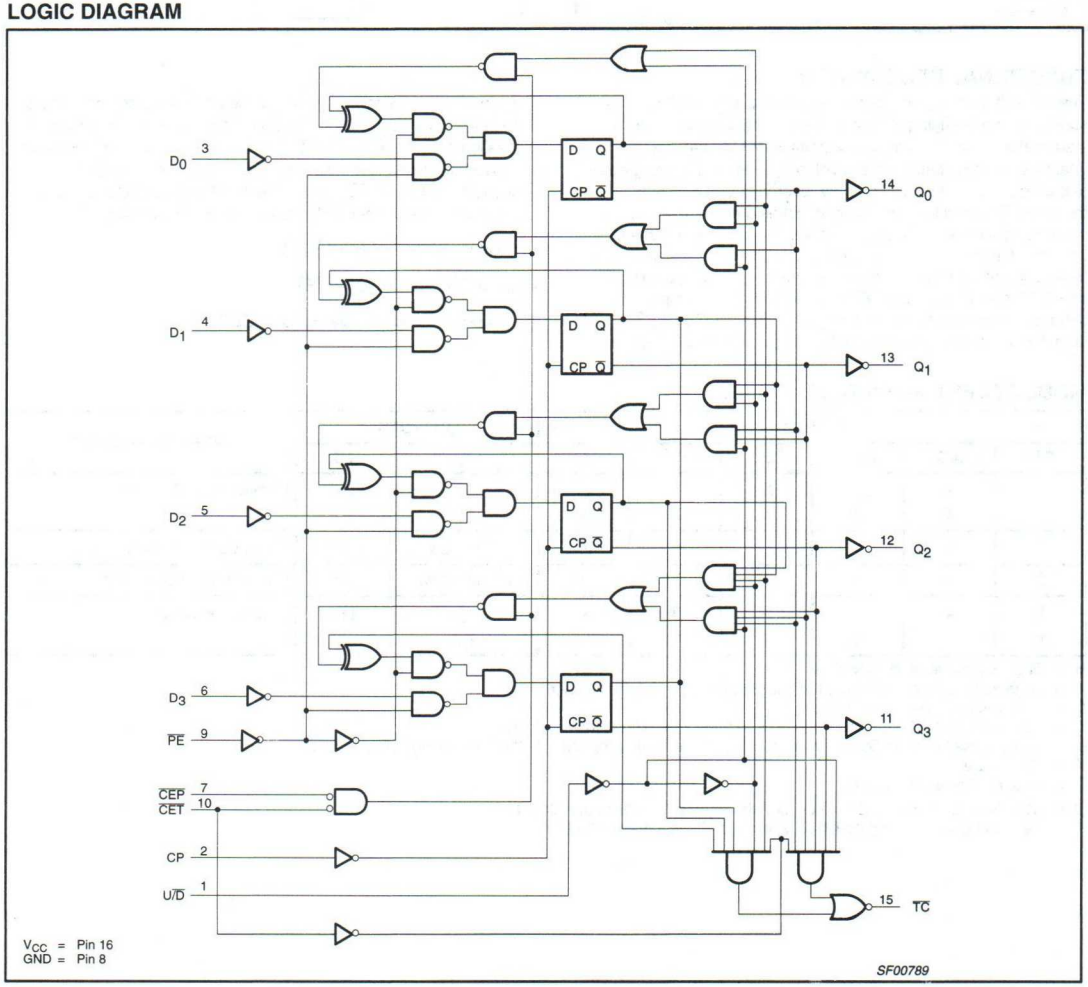
INPUTS				OPERATING MODE
$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	
L	X	X	X	Load ($D_n \rightarrow Q_n$)
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

H = High Voltage
L = Low Voltage Level
X = Don't care

STATE DIAGRAM



LOGIC DIAGRAM



APPLICATION

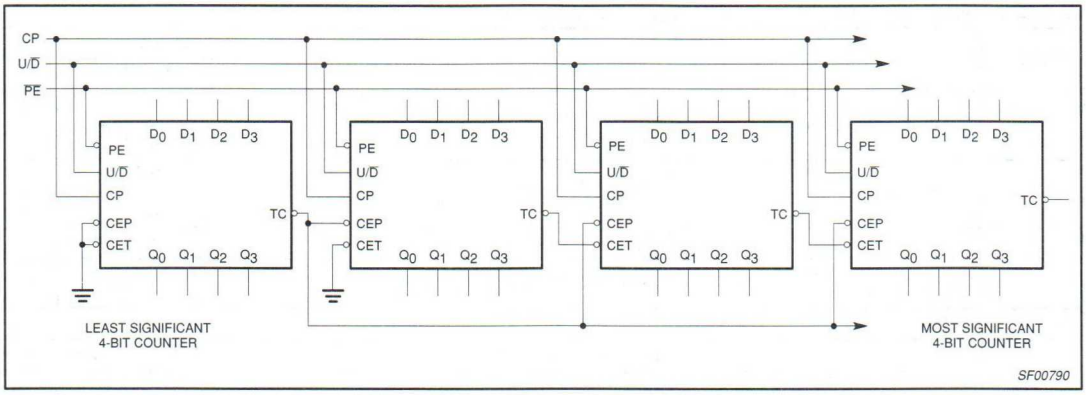


Figure 1. Synchronous Multistage Counting Scheme

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	$\overline{CET}$	V_{CC} = MAX, V_I = 0.5V				–1.2	mA
		Others	V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)[4]		V_{CC} = MAX			35	52	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured after applying a momentary 4.5V, then ground to the clock input with all other inputs grounded and all outputs open.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$, High or Low)	Waveform 1	3.0 4.0	6.5 9.0	8.5 11.5	3.0 4.0	9.5 13.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	5.5 4.0	12.0 8.5	15.5 11.0	5.5 4.0	17.0 12.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 2	2.5 2.5	4.5 6.0	6.0 8.0	2.5 2.5	7.0 9.0	ns ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	Waveform 3	3.5 4.0	8.5 8.0	15.0 10.5	3.5 4.0	15.5 12.0	ns ns

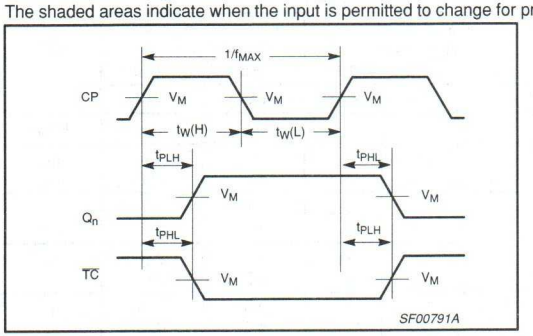
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		LIMITS		UNIT
			T_{amb}= +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω		T_{amb}= 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low D_n to CP	Waveform 4	4.0 4.0		4.5 4.5		ns ns
t_h(H) t_h(L)	Hold time, High or Low D_n to CP	Waveform 4	3.0 3.0		3.5 3.5		ns ns
t_s(H) t_s(L)	Set-up time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	5.0 5.0		5.5 5.5		ns ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	0 0		0 0		ns ns
t_s(H) t_s(L)	Set-up time, High or Low $\overline{PE}$ to CP	Waveform 4	8.0 8.0		9.0 9.0		ns ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{PE}$ to CP	Waveform 4	0 0		0 0		ns ns
t_s(H) t_s(L)	Set-up time, High or Low U/$\overline{D}$ to CP	Waveform 6	11.0 7.0		12.5 8.0		ns ns
t_h(H) t_h(L)	Hold time, High or Low U/$\overline{D}$ to CP	Waveform 6	0 0		0 0		ns ns
t_w(H) t_w(L)	CP_U or CP_D pulse width, High or Low	Waveform 1	5.0 5.0		5.5 5.5		ns ns

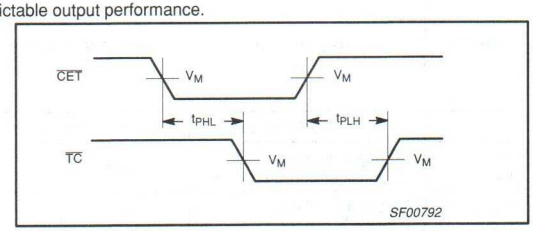
AC WAVEFORMS

For all waveforms, V_M = 1.5V

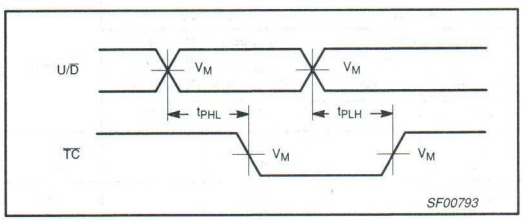
The shaded areas indicate when the input is permitted to change for predictable output performance.



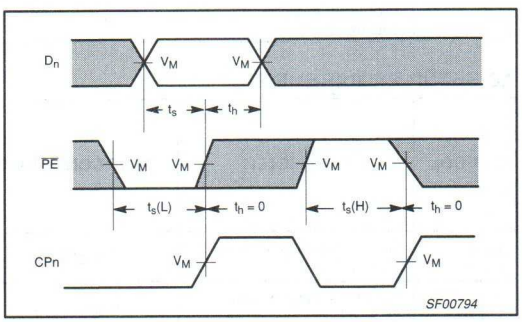
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



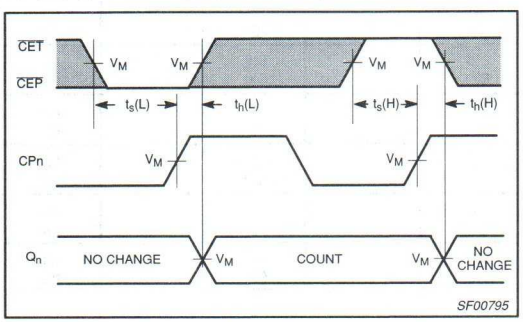
Waveform 2. Propagation Delays $\overline{CET}$ Input to Terminal Count Output



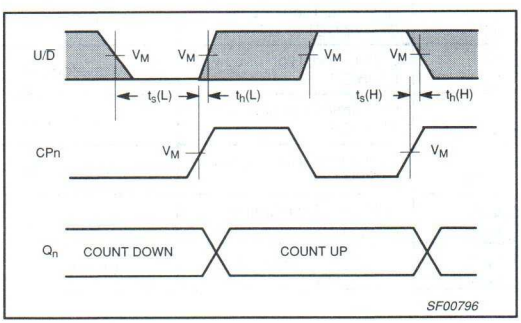
Waveform 3. Propagation Delay U/$\overline{D}$ Input to Terminal Count Output



Waveform 4. Parallel Data and Parallel Enable Setup and Hold Times

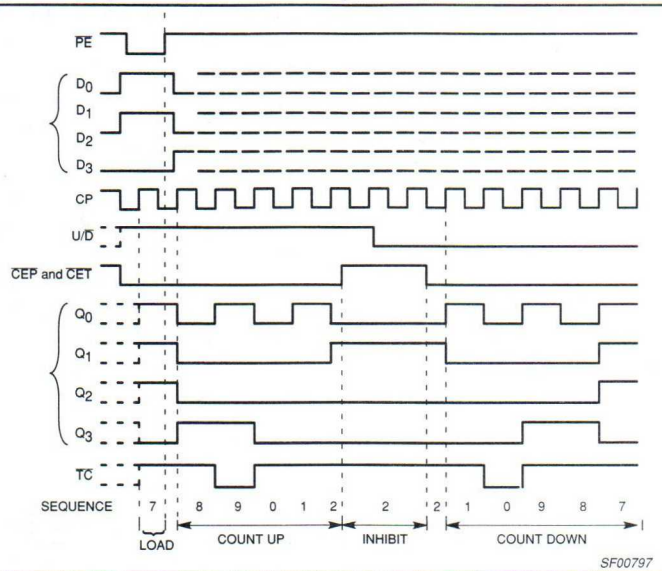


Waveform 5. Count Enable Setup and Hold Times



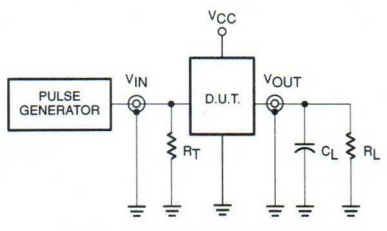
Waveform 6. Up/Down Control Setup and Hold Times

TIMING DIAGRAM (Typical Load, Count, and Inhibit Sequences)

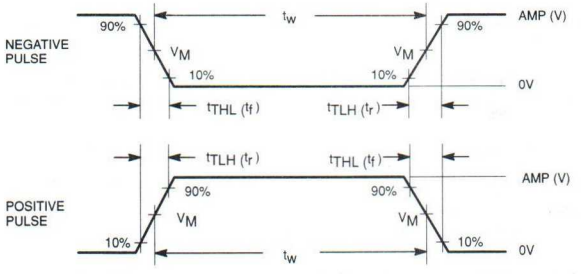


NOTES:
The operation of the 74F169 is similar to the Illustration above.
1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



DEFINITIONS:
R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Quad D-type flip–flop (3-State) 74F173

FEATURES

- Edge–triggered D–type register
- Gated clock enable for hold "do nothing" mode
- 3–state output buffers
- Gated output enable control
- Speed upgrade of N8T10 and current sink upgrade
- Controlled output edges to minimize ground bounces
- 48mA sinking capability

DESCRIPTION

The 74F173 is a high speed 4–bit parallel load register with clock enable control, 3–state buffered outputs, and master reset (MR). When the two clock enable ($\overline{E}0$ and $\overline{E}1$) inputs are low, the data on the D inputs is loaded into the register simultaneously with low–to–high clock (CP) transition. When one or both enable inputs are high one setup time before the low–to–high clock transition, the register retains the previous data.

Data inputs and clock enable inputs are fully edge–triggered and must be stable only one setup time before the low–to–high clock transition.

The master reset (MR) is an active–high asynchronous input. When the MR is high, all four flip–flops are reset (cleared) independently of any other input condition.

The 3–state output buffers are controlled by a 2–input NOR gate. When both output enable ($\overline{OE}0$ and $\overline{OE}1$) inputs are low, the data in the register is presented at the Q output.

When one or both $\overline{OE}$ inputs are high, the outputs are forced to a high impedance "off" state.

The 3–state output buffers are completely independent of the register operation; the $\overline{OE}$ transition does not affect the clock and reset operations.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F173	125MHz	23mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
16–pin plastic DIP	N74F173N	SOT38-4
16–pin plastic SO	N74F173D	SOT109-1

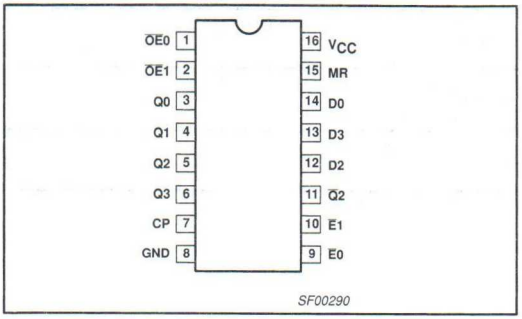
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/ LOW	LOAD VALUE HIGH/LOW
D0 – D3	Data inputs	1.0/1.0	20µA/0.6mA
CP	Clock input	1.0/1.0	20µA/0.6mA
$\overline{E}0$, $\overline{E}1$	Clock enable inputs	1.0/1.0	20µA/0.6mA
MR	Master reset input	1.0/1.0	20µA/0.6mA
$\overline{OE}0$, $\overline{OE}1$	Output enable inputs	1.0/1.0	20µA/0.6mA
Q0 – Q3	Data outputs	750/80	15mA/48mA

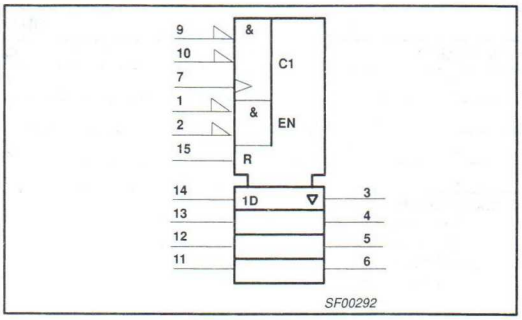
Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

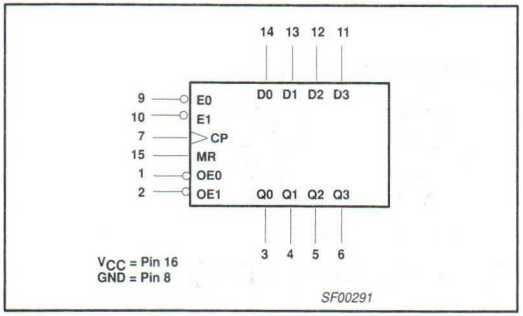
PIN CONFIGURATION



IEC/IEEE SYMBOL



LOGIC SYMBOL



FUNCTION TABLE

INPUTS					OUTPUTS	OUTPUTS
MR	CP	$\overline{E0}$	$\overline{E1}$	Dn	Qn (register)	
H	X	X	X	X	L	Reset (clear)
L	↑	l	l	l	L	Parallel load
L	↑	l	l	h	H	
L	X	h	X	X	qn	Hold (do nothing)
L	X	X	h	X	qn	

Notes to function table

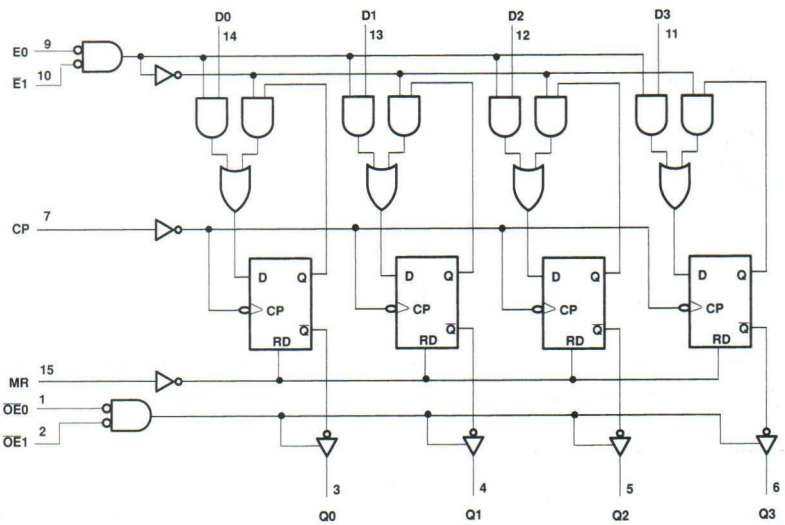
H = High–voltage level
h = High state one setup time before the low–to–high clock transition
L = Low–voltage level
l = Low state one setup time before the low–to–high clock transition
qn = Lower case letters indicate the state of the referenced input (or output) on setup time prior to the low–to–high clock transition
X = Don't care
↑ = Low–to–high clock transition

FUNCTION TABLE

INPUTS			OUTPUTS	OUTPUTS
Qn (register)	$\overline{OE0}$	$\overline{OE1}$	Qn	
L	L	L	L	Read
H	L	L	H	
X	H	X	Z	Disabled
X	X	H	Z	

Notes to function table
H = High–voltage level
L = Low–voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	96	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–15	mA
I_{OL}	Low–level output current			48	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
			V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}	2.0			V
			V_{IH} = MIN, I_{OH} = –15mA	±5%V_{CC}	2.0	3.1		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OZH}	Off–state output current, high–level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off–state output current, low–level voltage applied		V_{CC} = MAX, V_O = 0.5V				–50	µA
I_{OS}	Short–circuit output current3		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			19	26	mA
		I_{CCL}				27	37	mA
		I_{CCZ}				23	32	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

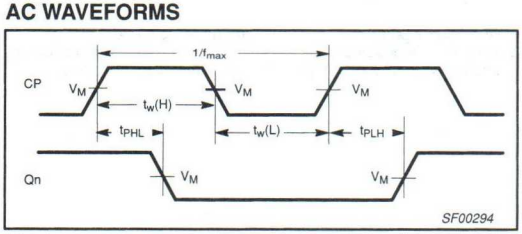
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	100	125		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	Waveform 1	4.5 6.0	6.5 8.0	9.0 10.5	4.0 5.5	10.0 11.5	ns
t_{PHL}	Propagation delay MR to Qn	Waveform 2	6.5	8.5	11.5	6.0	12.5	ns
t_{PZH} t_{PZL}	Output enable time to high or low level	Waveform 4 Waveform 5	3.5 5.5	5.0 7.0	8.0 10.0	2.5 4.5	8.5 11.0	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level	Waveform 4 Waveform 5	1.5 3.0	3.5 5.0	7.0 8.5	1.0 2.5	8.0 9.0	ns
t_{THL} t_{TLH}	Transition time 10% to 90%, 90% to 10%	Waveform 5 Waveform 4	2.0 4.0	5.0 7.5	8.0 10.0	2.0 4.0	8.5 11.0	ns

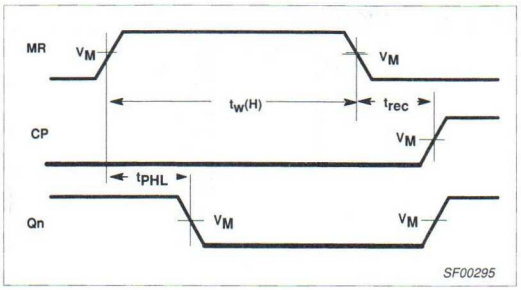
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low level Dn to CP	Waveform 3	2.5 2.5			3.0 4.0		ns
t_h (H) t_h (L)	Hold time, high or low level Dn to CP	Waveform 3	0 0			0 0		ns
t_{su} (H) t_{su} (L)	Setup time, high or low level $\overline{E}$ to CP	Waveform 3	4.5 7.5			5.0 8.5		ns
t_h (H) t_h (L)	Hold time, high or low level $\overline{E}$ to CP	Waveform 3	0 0			0 0		ns
t_w (H) t_w (L)	CP Pulse width, high or low	Waveform 1	3.0 6.0			3.0 6.0		ns
t_w (H)	MR Pulse width, high	Waveform 2	3.5			3.5		ns
t_{rec}	Recovery time, MR to CP	Waveform 2	4.5			5.5		ns

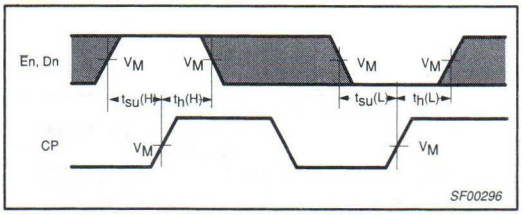
AC WAVEFORMS



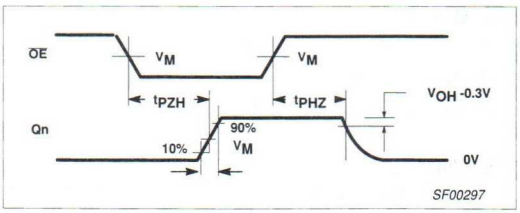
Waveform 1. Propagation delay for clock input to output, clock pulse widths, and maximum clock frequency



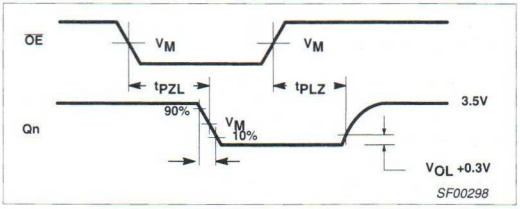
Waveform 2. Master reset pulse width, master reset to output delay and master reset to clock recovery time



Waveform 3. Data and enable setup time and hold times



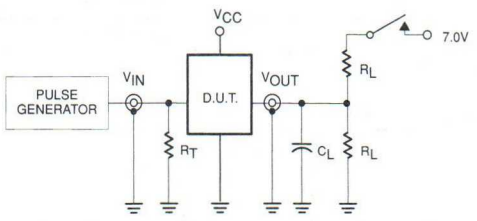
Waveform 4. 3-state output enable time to high level, output disable time from high level and transition time to high level



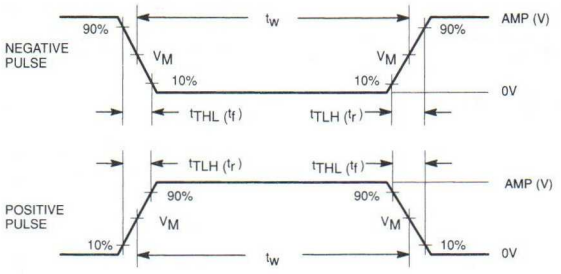
Waveform 5. 3-state output enable time to low level, output disable time from low level and transition time to low level

Notes to AC waveforms
1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

Hex D flip-flop | 74F174

FEATURES

- Six edge-triggered D-type flip-flops
- Buffered common Clock
- Buffered, asynchronous Master Reset

DESCRIPTION

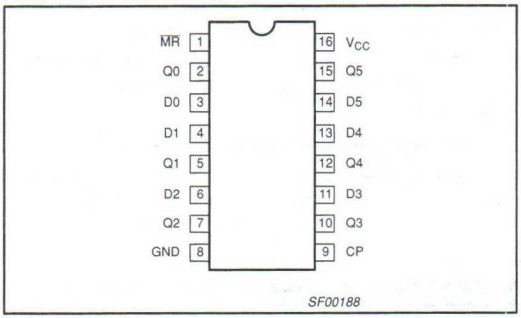
The 74F174 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

All Q outputs will be forced Low independent of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where true outputs only are required, and the Clock and Master Reset are common to all storage elements.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F174	100MHz	35mA

PIN CONFIGURATION



ORDERING INFORMATION

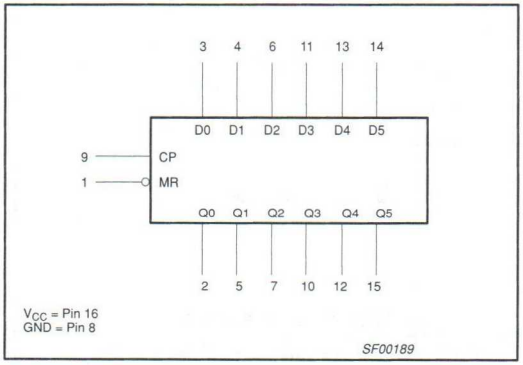
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
16-pin plastic DIP	N74F174N	SOT38-4
16-pin plastic SO	N74F174D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

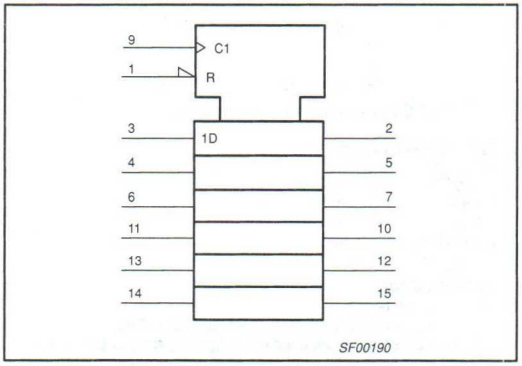
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0–D5	Data inputs	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (active-Low)	1.0/1.0	20µA/0.6mA
Q0–Q5	Outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

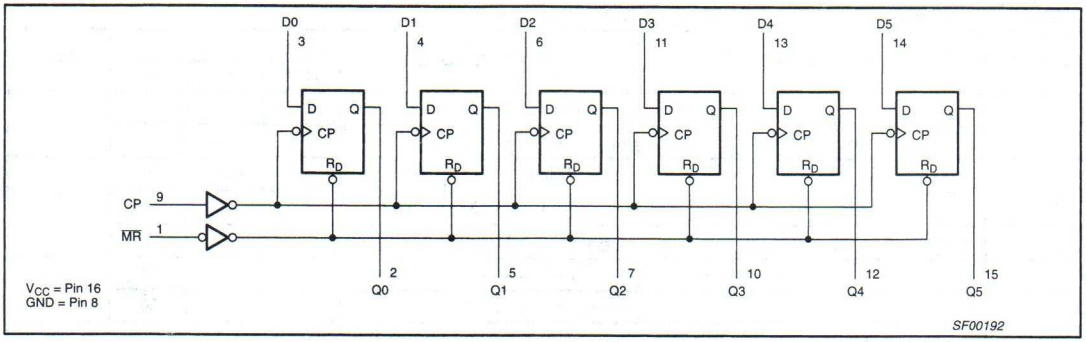
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{MR}$	CP	D	Qn	
L	X	X	L	Reset (clear)
H	↑	h	H	Load "1"
H	↑	l	L	Load "0"

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High Clock transition
h = High voltage level one set-up time prior to the Low-to-High Clock transition.
l = Low voltage level one set-up time prior to the Low-to-High Clock transition.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX, Dn = $\overline{MR}$ = 4.5V, CP = ↑			35	45	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

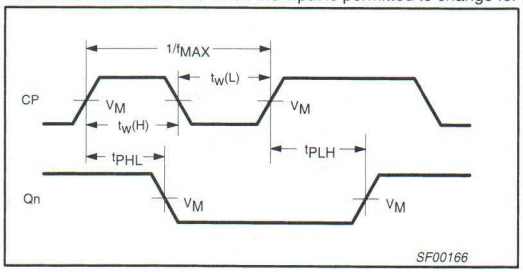
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	80	100		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	Waveform 1	3.5 4.5	5.5 6.0	8.0 10.0	3.5 4.5	9.0 11.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn	Waveform 2	5.0	8.5	14.0	5.0	15.0	ns

AC SETUP REQUIREMENTS

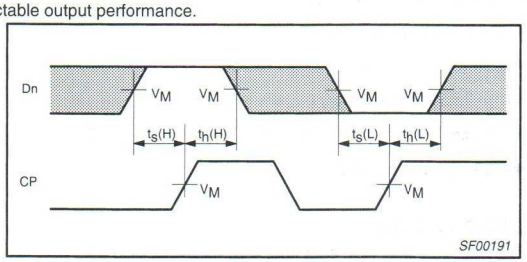
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_S(H)$ $t_S(L)$	Setup time, High or Low Dn to CP	Waveform 3	4.0 4.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP	Waveform 3	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.0 6.0			4.0 6.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 2	5.0			5.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP	Waveform 2	5.0			5.0		ns

AC WAVEFORMS

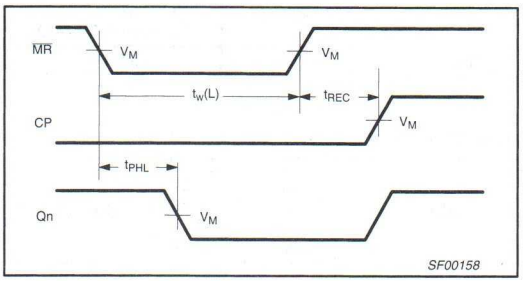
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

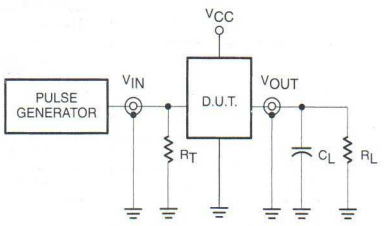


Waveform 3. Data Setup and Hold Times

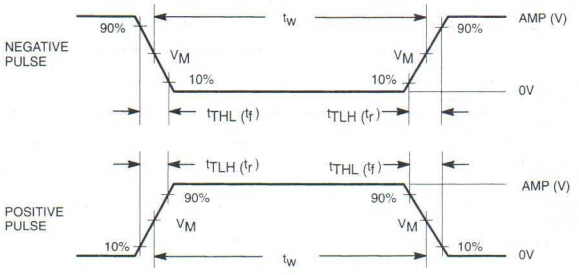


Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock recovery Time

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor;
see AC ELECTRICAL CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance;
see AC ELECTRICAL CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Quad D flip-flop | 74F175A

FEATURES

- Four edge-triggered D-type flip-flops
- Buffered common clock
- Buffered asynchronous Master Reset
- True and complementary outputs
- Industrial temperature range available (–40°C to +85°C)
- PNP light loading inputs

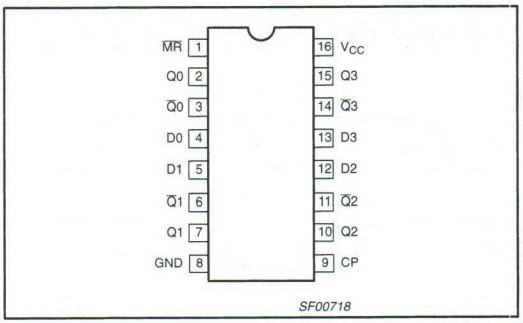
DESCRIPTION

The 74F175A is a quad, edge-triggered D-type flip-flop with individual D inputs and both Q and $\overline{Q}$ outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

All Q outputs will be forced Low independently of clock or data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where both true and complementary outputs are required, and the CP and $\overline{MR}$ are common to all storage elements.

PIN CONFIGURATION



TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F175A	160MHz	22mA

ORDERING INFORMATION

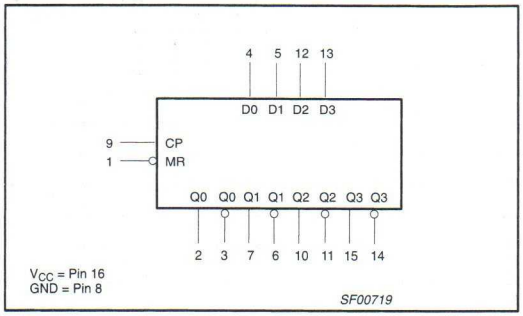
DESCRIPTION	ORDER CODE	PKG. DWG. #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
16-pin plastic DIP	74F175AN	SOT38-4
16-pin plastic SO	74F175AD	SOT109-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

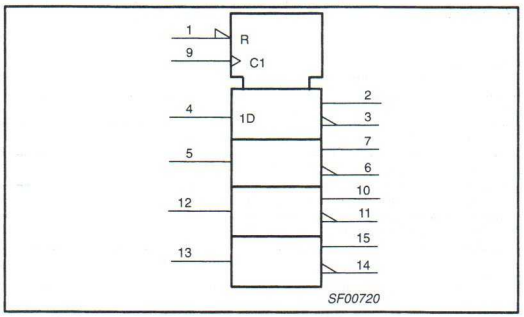
PINS	DESCRIPTION		74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D3	Data inputs	74F175A	1.0/0.033	20μA/20μA
$\overline{MR}$	Master reset input (active–Low)	74F175A	1.0/0.033	20μA/20μA
CP	Clock input (active rising edge)	74F175A	1.0/0.033	20μA/20μA
Q0–Q3	True outputs		50/33	1.0mA/20mA
$\overline{Q0}$–$\overline{Q3}$	Complementary outputs		50/33	1.0mA/20mA

NOTE:
One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

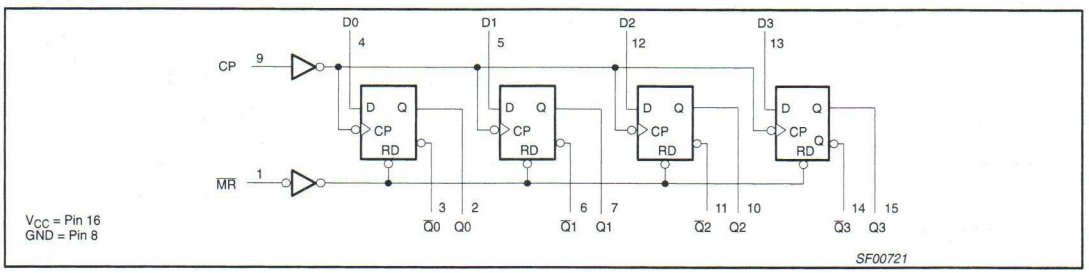
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS		OPERATING MODE
$\overline{MR}$	CP	Dn	Q_n	$\overline{Q}_n$	
L	X	X	L	H	Reset (clear)
H	↑	h	H	L	Load "1"
H	↑	l	L	H	Load "0"

H = High voltage level
h = High state must be present one setup time before the Low-to-High clock transition
L = Low voltage level
l = Low state must be present one setup time before the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	−40 to +85	°C
T_{stg}	Storage temperature range		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current				–1	mA
I_{OL}	Low-level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC}= MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.30	0.5	V
			±5%V_{CC}		0.30	0.5	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V	74F175A			–20	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	74F175A		22	31	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS FOR 74F175A

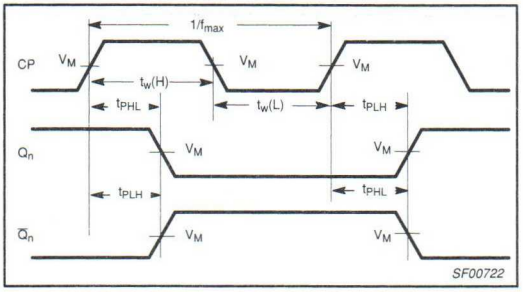
SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = 25°C, V_{CC} = +5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	140	160		125		110		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn or $\overline{Qn}$	Waveform 1	3.0 4.5	4.0 6.0	6.5 8.5	2.5 4.0	7.5 9.0	2.5 4.0	8.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to Qn	Waveform 3	4.5	6.5	9.0	4.5	10.0	4.5	11.0	ns
t_{PHL} t_{PHL}	Propagation delay $\overline{MR}$ to $\overline{Qn}$	Waveform 3	4.5	6.0	8.0	4.0	9.0	4.0	10.0	ns

AC SETUP REQUIREMENTS FOR 74F175A

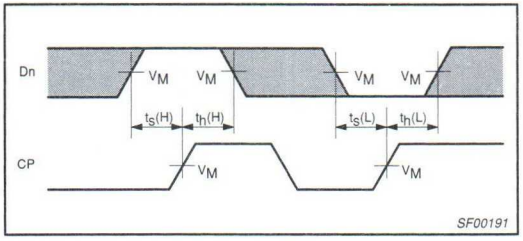
SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = 25°C, V_{CC} = +5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		T_{amb} = −40°C to +85°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to CP	Waveform 2	3.0 3.0			3.5 3.5		4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP	Waveform 2	0.0 0.0			0.0 0.0		0.0 0.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width High or Low	Waveform 1	3.0 4.0			3.5 5.0		4.0 5.5		ns
$t_w(L)$	$\overline{MR}$ Pulse width Low	Waveform 3	3.5			3.5		4.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 3	4.0			4.5		5.0		ns

AC WAVEFORMS

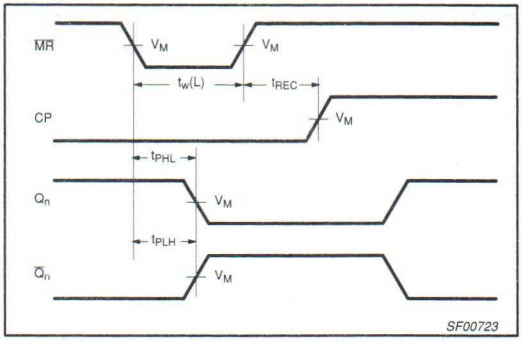
For all waveforms, V_M = 1.3V.



Waveform 1. Propagation delay for clock input to output, clock pulse width, and maximum clock frequency

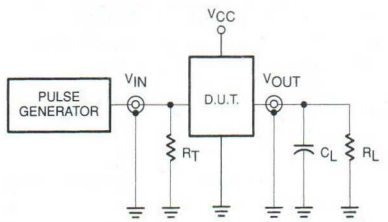


Waveform 2. Data setup time and hold times

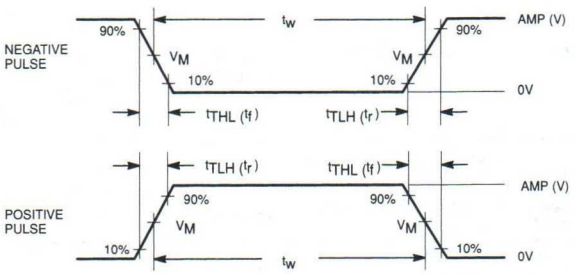


Waveform 3. Master Reset pulse width, Master Reset to output delay and Master Reset to Clock recovery time

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

64-bit TTL bipolar RAM, inverting (3-State) 74F189A

FEATURES

- High speed performance
- Replaces 74F189
- Address access time: 8ns max vs 28ns for 74F189
- Power dissipation: 4.3mW/bit
- Schottky clamp TTL
- One chip enable
- Inverting outputs (for non-inverting outputs see 74F219A)
- 3-State outputs
- 74F189A in 150 mil wide SO is preferred options for new designs

DESCRIPTION

The 74F189A is a high speed, 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on chip. The outputs are in high impedance state whenever the chip enable ($\overline{CE}$) is high. The outputs are active only in the READ mode ($\overline{WE}$ = high) and the output data is the complement of the stored data.

TYPE	TYPICAL ACCESS TIME	TYPICAL SUPPLY CURRENT (TOTAL)
74F189A	5.0ns	55mA

ORDERING INFORMATION

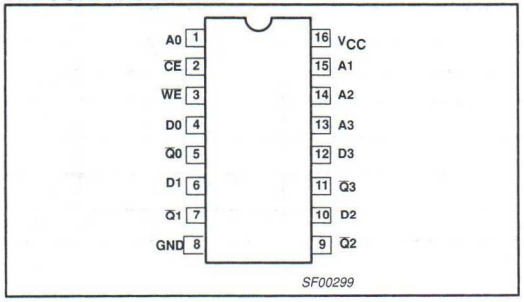
DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
16-pin plastic Dual In-line Package	N74F189AN	SOT38-4
16-pin plastic Small Outline (150mil)	N74F189AD	SOT109-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

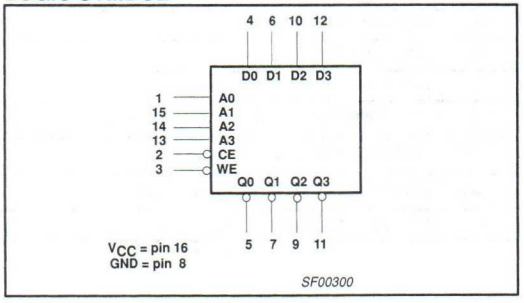
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D3	Data inputs	1.0/1.0	20μA/0.6mA
A0 – A3	Address inputs	1.0/1.0	20μA/0.6mA
$\overline{CE}$	Chip enable input (active low)	1.0/2.0	20μA/1.2mA
$\overline{WE}$	Write enable input (active low)	1.0/2.0	20μA/1.2mA
$\overline{Q}0$ – $\overline{Q}3$	Data outputs	150/40	3mA/24mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.

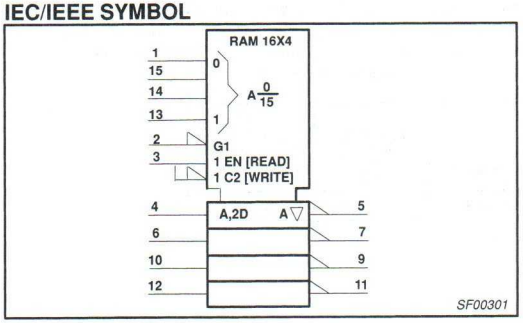
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL

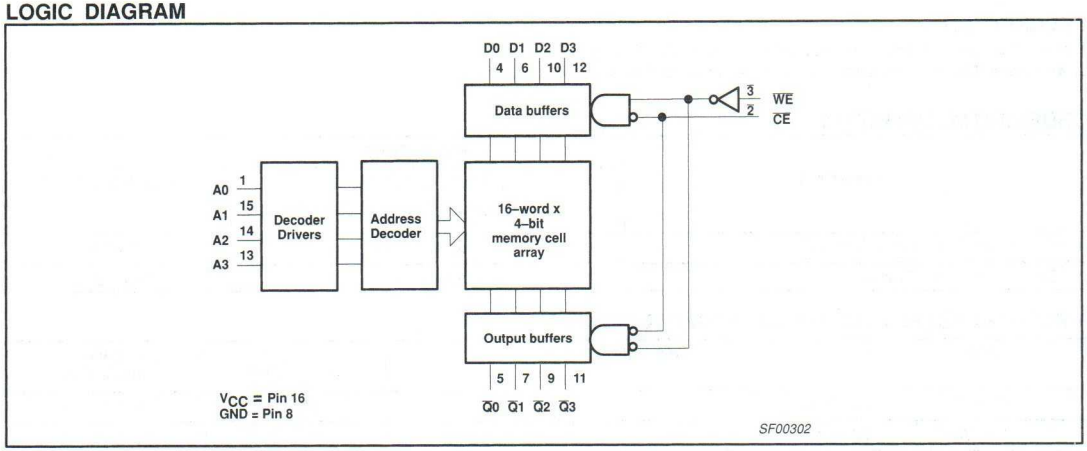


FUNCTION TABLE

INPUTS			OUTPUT	OPERATING MODE
$\overline{CE}$	$\overline{WE}$	Dn	$\overline{Q}_n$	
L	H	X	Complement of stored data	Read
L	L	L	High impedance	Write "0"
H	L	H	High impedance	Write "1"
H	X	X	High impedance	Disable input

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	48	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–3	mA
I_{OL}	Low–level output current			24	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	$\pm10\%V_{CC}$	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	$\pm5\%V_{CC}$	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	$\pm10\%V_{CC}$		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	$\pm5\%V_{CC}$		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current	others	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		$\overline{CE}$, $\overline{WE}$					-1.2	mA
I_{OZH}	Offset output current, high–level voltage applied		V_{CC} = MAX, V_I = 2.7V				50	µA
I_{OZL}	Offset output current, low–level voltage applied		V_{CC} = MAX, V_I = 0.5V				–50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX, $\overline{CE}$ = $\overline{WE}$ = GND			55	80	mA
C_{IN}	Input capacitance		V_{CC} = 5V, V_{IN} = 2.0V			4		pF
C_{OUT}	Output capacitance		V_{CC} = 5V, V_{OUT} = 2.0V			7		pF

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

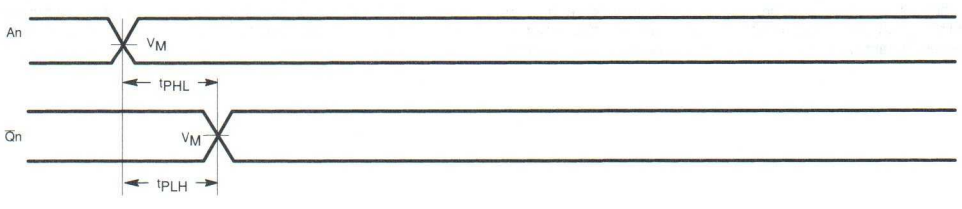
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Access time	Propagation delay An to $\overline{Q}$n	Waveform 1	2.5 2.0	5.0 4.5	8.0 8.0	2.5 2.0	8.0 8.0	ns
t_{PZH} t_{PZL}		Enable time $\overline{CE}$ to $\overline{Q}$n	Waveform 2	2.0 2.0	3.5 4.0	6.0 7.0	1.5 2.0	7.0 7.5	ns
t_{PHZ} t_{PLZ}	Disable time $\overline{CE}$ to $\overline{Q}$n		Waveform 3	2.5 1.5	4.5 3.0	7.0 5.5	2.0 1.5	8.0 6.0	ns
t_{PZH} t_{PZL}	Write recovery time	Enable time $\overline{WE}$ to $\overline{Q}$n	Waveform 4	2.0 2.5	4.0 4.5	6.5 7.5	2.0 2.5	7.0 8.0	ns
t_{PHZ} t_{PLZ}	Disable time $\overline{WE}$ to $\overline{Q}$n		Waveform 4	3.5 1.5	5.5 3.5	8.5 6.5	3.0 1.5	9.0 7.0	ns

AC SETUP REQUIREMENT

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low An to $\overline{WE}$	Waveform 4	4.5 4.5			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low An to $\overline{WE}$	Waveform 4	0 0			0 0		ns
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low Dn to $\overline{WE}$	Waveform 4	7.5 6.5			9.0 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low Dn to $\overline{WE}$	Waveform 4	0 0			0 0		ns
$t_{su}(L)$	Setup time, low $\overline{CE}$ (falling edge) to $\overline{WE}$ (falling edge)	Waveform 4	0			0		ns
$t_h(L)$	Hold time, low $\overline{WE}$ (falling edge) to $\overline{WE}$ (rising edge)	Waveform 4	6.5			7.5		ns
$t_w(L)$	Pulse width, low $\overline{WE}$	Waveform 4	7.0			8.0		ns

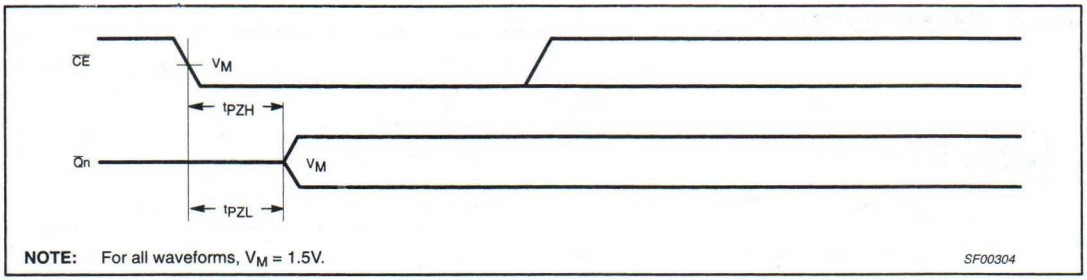
AC WAVEFORMS FOR READ CYCLES



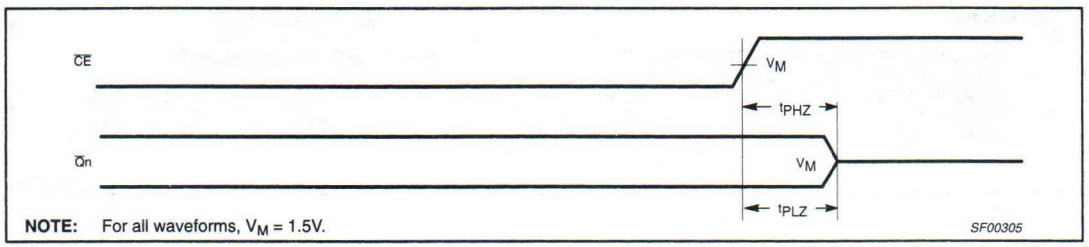
NOTE: For all waveforms, V_M = 1.5V.

SF00303

Waveform 1. Read cycle, address access time

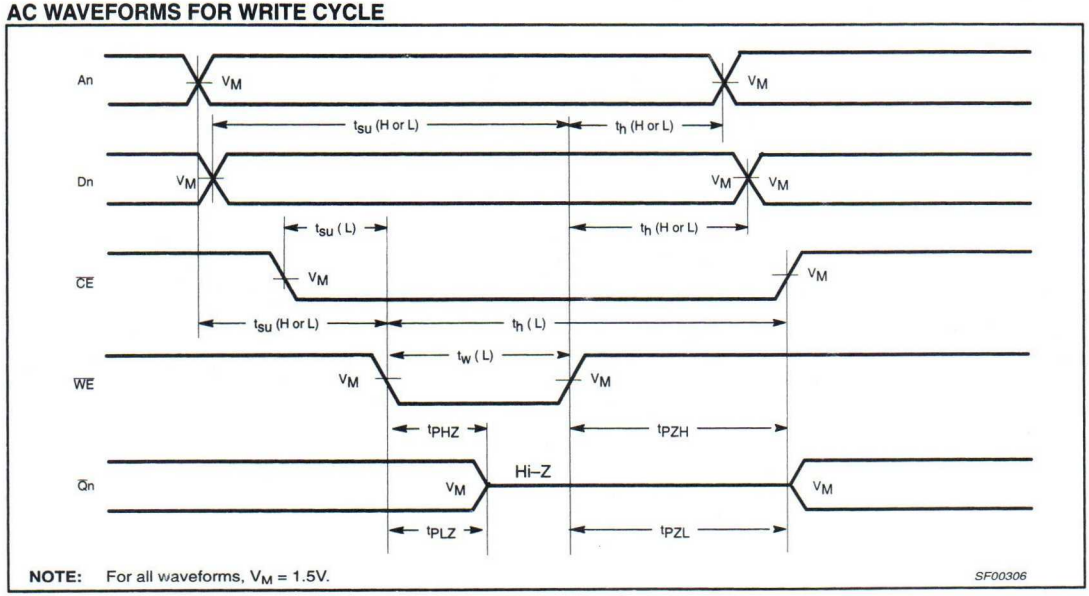


Waveform 2. Read cycle, chip enable access time



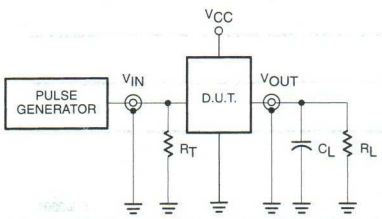
Waveform 3. Read cycle, chip disable time

AC WAVEFORMS FOR WRITE CYCLE

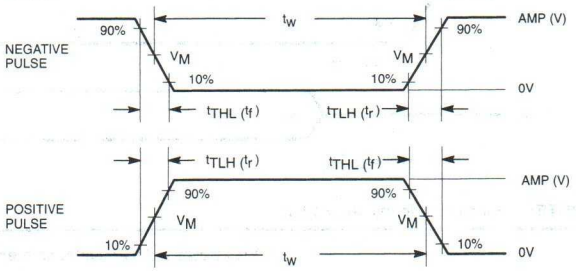


Waveform 4. Write cycle

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Up/Down binary counter with reset and ripple clock | 74F191

FEATURES

- High speed –125MHz typical f_{MAX}
- Synchronous, reversible counting
- 4-Bit binary
- Asynchronous parallel load capability
- Cascadable without external logic
- Single up/down control input

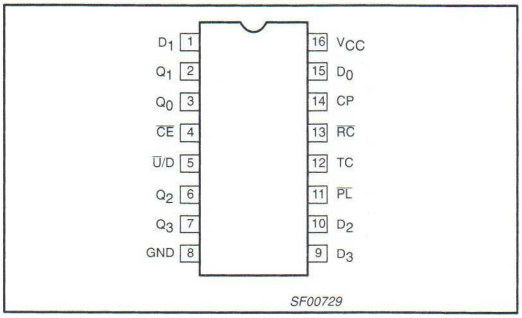
DESCRIPTION

The 74F191 is a 4-bit binary counter. It contains four edge-triggered master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operations.

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel data inputs (D_0 - D_3) is loaded into the counter and appears on the outputs when the Parallel Load ($\overline{PL}$) input is Low. This operation overrides the counting function. Counting is inhibited by a High level on the count enable ($\overline{CE}$) input. When $\overline{CE}$ is Low, internal state changes are initiated. Overflow/underflow indications are provided by two types of outputs, the Terminal Count (TC) and Ripple Clock ($\overline{RC}$).

The TC output is normally Low and goes High when: 1) the count reaches zero in the countdown mode or 2) reaches "15" in the count up mode. The TC output will remain High until a state change occurs, either by counting or presetting, or until $\overline{U}$/D is changed. TC output should not be used as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the $\overline{RC}$ output. When TC is High and $\overline{CE}$ is Low, the $\overline{RC}$ follows the clock pulse. The $\overline{RC}$ output essentially duplicates the Low clock pulse width, although delayed in time by two gate delays.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F191	125MHz	40mA

ORDERING INFORMATION

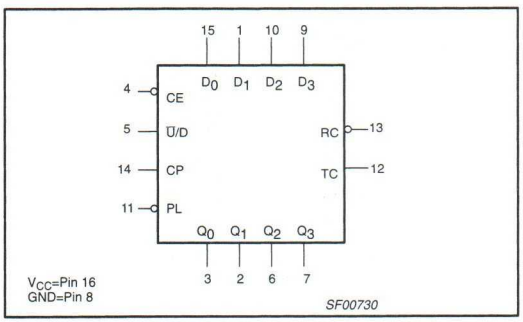
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
16-pin plastic DIP	N74F191N	SOT38-4
16-pin plastic SO	N74F191D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

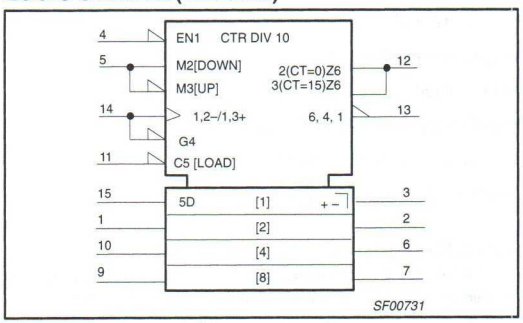
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{CE}$	Count enable input (active Low)	1.0/3.0	20µA/1.8mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{PL}$	Asynchronous parallel load control input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{U}$/D	Up/down count control input	1.0/1.0	20µA/0.6mA
Q_0 - Q_3	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{RC}$	Ripple clock output (active low)	50/33	1.0mA/20mA
TC	Terminal count output	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

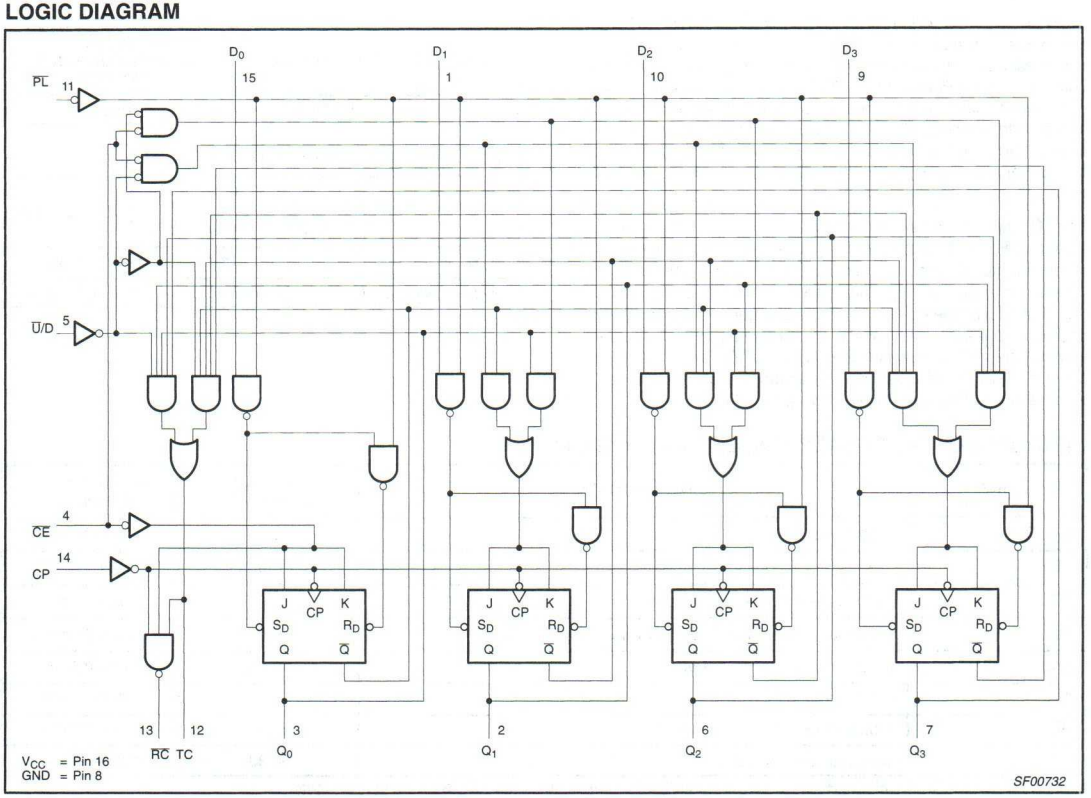
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
$\overline{PL}$	$\overline{U}/D$	$\overline{CE}$	CP	D_n	Q_n	
L L	X X	X X	X X	L H	L H	Parallel load
H	L	I	↑	X	Count up	Count up
H	H	I	↑	X	Count down	Count down
H	X	H	X	X	No change	Hold (do nothing)

TC AND $\overline{RC}$ FUNCTION TABLE

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}/D$	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	⊔	H	H	H	H	H	⊔
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊔	L	L	L	L	H	⊔

H = High voltage level steady state
L = Low voltage level steady state
X = Don't care
⊔ = Low pulse
↑ = Low-to-High clock transition
I = Low voltage level one set-up time prior to the Low-to-High clock transition

APPLICATIONS

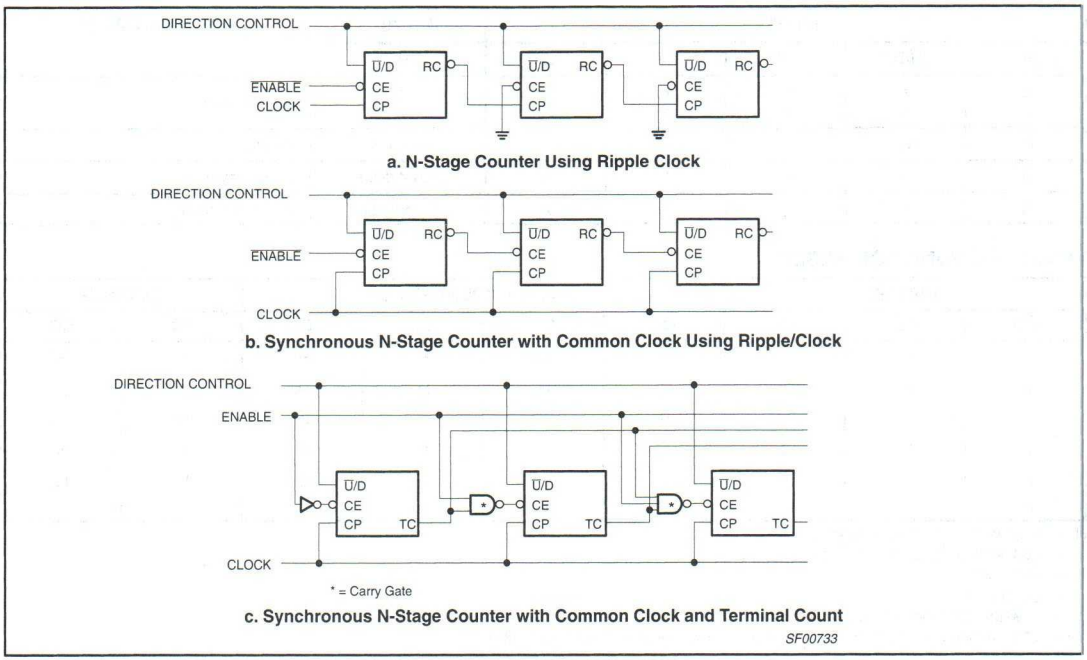


Figure 2.

The 74F191 simplifies the design of multi-stage counters, as indicated in Figure 1, each $\overline{RC}$ output is used as the clock input for the next higher stage. When the clock source has a limited drive capability this configuration is particularly advantageous, since the clock source drives only the first stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a High signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse as indicated in the Mode Select Table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This is a disadvantage of the configuration in some applications.

Figure 1b shows a method of causing state changes to occur simultaneously in all stages. The $\overline{RC}$ output signals propagate in ripple fashion and all clock inputs are driven in parallel. The Low state duration of the clock in this configuration must be long enough to allow the negative-going edge of the $\overline{RC}$ signal to ripple through to the last stage before the clock goes High. Since the $\overline{RC}$ output of any package goes High shortly after its clock input goes High, there is no such restriction on the High state duration of the clock.

In Figure 1c, the configuration shown avoids ripple delays and their associated restrictions. The combined TC signals from all the preceding stages forms the $\overline{CE}$ input signal for a given stage. An enable signal must also be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own $\overline{CE}$, therefore, the simple inhibit scheme of Figure 1a and 1b does not apply.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min	±10%V_{CC}		0.30	0.50	V
				±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	$\overline{CE}$	V_{CC} = Max, V_I = 0.5V				−1.8	mA
		Others					−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max		−60		−150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = Max			40	55	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} all inputs grounded and all outputs open.

AC ELECTRICAL CHARACTERISTICS

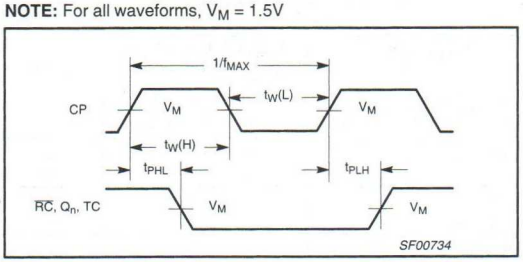
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb}= +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb}= 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency to Qn outputs	Waveform 1	100	125		90		MHz
f_{MAX}	Maximum clock frequency to $\overline{RC}$ outputs	Waveform 1	85	95		75		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	2.5 5.0	4.5 7.5	8.0 11.5	2.0 5.0	8.5 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	Waveform 1	6.5 6.0	9.0 8.0	12.5 11.0	6.0 6.0	13.0 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$	Waveform 2	2.5 3.0	4.5 5.0	7.5 7.5	2.0 2.5	8.0 8.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$	Waveform 2	2.0 3.0	4.0 5.0	7.0 7.5	2.0 3.0	7.5 8.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$	Waveform 2	8.0 4.5	11.0 7.5	16.0 10.5	8.0 4.0	17.0 11.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to TC	Waveform 4	4.0 3.0	6.5 6.0	9.5 9.5	3.0 3.0	10.5 10.0	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 3	2.0 6.5	4.0 9.0	7.0 12.0	1.5 6.5	7.5 13.0	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC	Waveform 3 Waveform 4	5.5 6.5	9.5 9.5	13.0 13.0	5.0 6.0	14.0 14.0	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$	Waveform 3 Waveform 4	6.0 6.0	14.0 11.0	18.0 13.5	6.0 6.0	19.5 15.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n	Waveform 5	4.5 5.5	6.5 8.0	9.5 11.5	4.0 5.0	10.5 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC	Waveform 5	5.5 6.0	8.5 10.5	12.0 13.5	5.5 6.0	13.0 14.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$	Waveform 5	8.5 7.5	16.0 10.0	18.5 13.0	8.5 7.0	21.0 13.5	ns ns

AC SETUP REQUIREMENTS

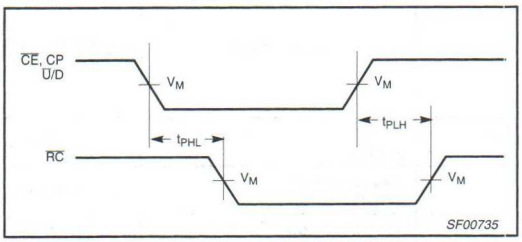
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb}= +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to $\overline{PL}$	Waveform 6	4.5 4.5			5.0 5.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{PL}$	Waveform 6	2.0 2.0			2.0 2.0		ns ns
$t_s(L)$	Setup time, Low $\overline{CE}$ to CP	Waveform 6	10.0			10.0		ns
$t_h(L)$	Hold time, Low $\overline{CE}$ to CP	Waveform 6	0			0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{U}$/D to CP	Waveform 6	12.0 12.0			12.0 12.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{U}$/D to CP	Waveform 6	0 0			0 0		ns ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	3.5 6.0			3.5 6.0		ns ns
$t_w(L)$	$\overline{PL}$ Pulse width, Low	Waveform 5	6.0			6.0		ns
t_{rec}	Recovery time, $\overline{PL}$ to CP	Waveform 5	6.0			6.0		ns

AC WAVEFORMS

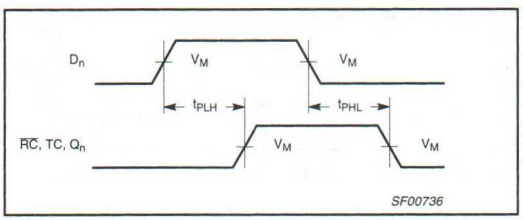
NOTE: For all waveforms, $V_M = 1.5V$



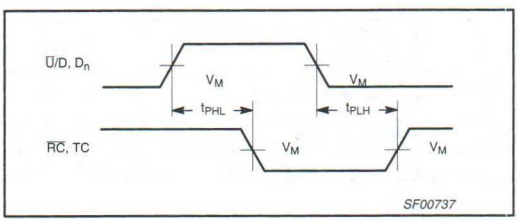
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency.



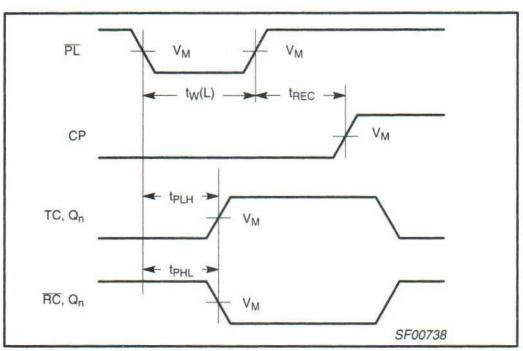
Waveform 2. Propagation Delay, Clock, Clock Enable or Up/Down to Ripple Clock Output



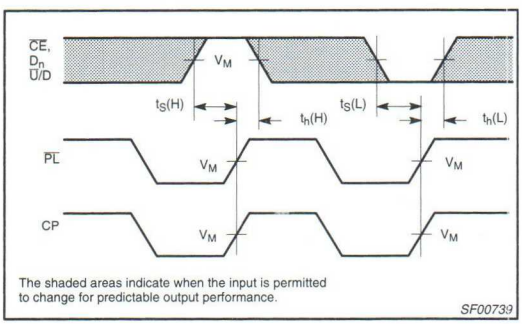
Waveform 3. Propagation Delay, Non-Inverting Path



Waveform 4. Propagation Delay, Inverting Path

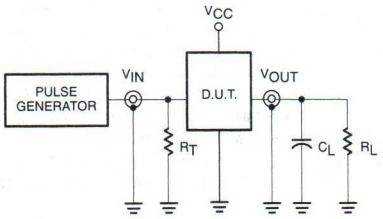


Waveform 5. Parallel Load Pulse Width, Parallel Load to Output Delay and Parallel Load to Clock Recovery Time

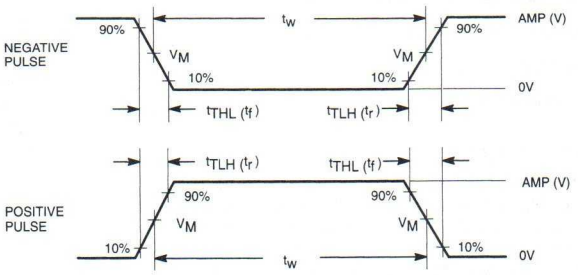


Waveform 6. Data Set Up and Hold Times

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Up/down binary counter with separate up/down clocks 74F193

FEATURES

- Synchronous reversible 4-bit counting
- Asynchronous parallel load capability
- Asynchronous reset (clear)
- Cascadable without external logic

DESCRIPTION

The 74F193 is a 4-bit synchronous up/down counter in the binary mode. Separate up/down clocks, CP_U and CP_D respectively, simplify operation. The outputs change state synchronously with the Low-to-High transition of either clock input. If the CP_U clock is pulsed while CP_D is held High, the device will count up. If CP_D clock is pulsed while CP_U is held High, the device will count down. The device can be cleared at any time by the asynchronous reset pin. It may also be loaded in parallel by activating the asynchronous parallel load pin.

Inside the device are four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, asynchronous preset, load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master, such that a Low-to-High transition on the CP_D input will decrease the count by one, while a similar transition on the CP_U input will advance the count by one.

One clock should be held High while counting with the other, because the circuit will either count by twos or not at all, depending on the state of the first JK flip-flop, which cannot toggle as long as either clock input is Low. Applications requiring reversible operation must make the reversing decision while the activating clock is High to avoid erroneous counts.

The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally High. When the circuit has reached the maximum count state of 15, the next High-to-Low transition of CP_U will cause $\overline{TC}_U$ to go Low. $\overline{TC}_U$ will stay Low until CP_U goes High again, duplicating the count up clock, although delayed by two gate delays. Likewise, the $\overline{TC}_D$ output will go Low when the circuit is in the zero state and the CP_D goes Low. The $\overline{TC}$ outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms.

Multistage counters will not be fully synchronous since there is a two-gate delay time difference added for each stage that is added.

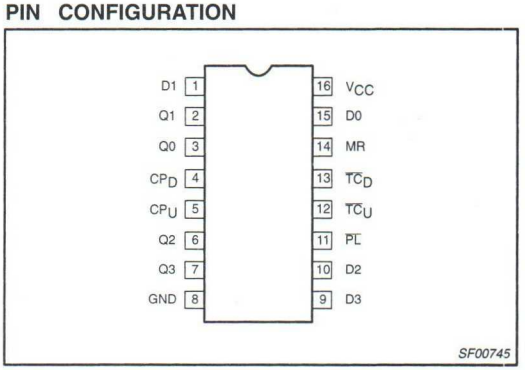
The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel Data inputs (D0 - D3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs when the Parallel Load ($\overline{PL}$) input is Low. A High level on the Master Reset (MR) input will disable the parallel load gates, override both clock inputs, and set all Q outputs Low. If one of the clock inputs is Low during and after a reset or load operation, the next Low-to-High transition of the clock will be interpreted as a legitimate signal and will be counted.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F193	125MHz	32mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
16-pin plastic DIP	N74F193N	SOT38-4
16-pin plastic SO	N74F193D	SOT109-1

PIN CONFIGURATION

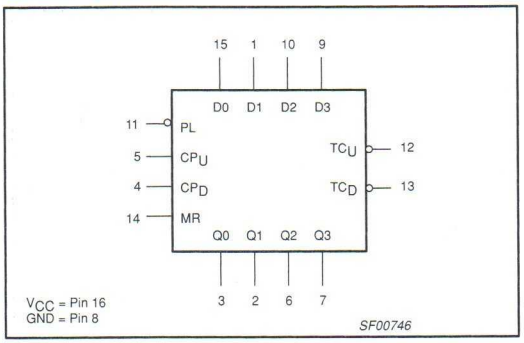


INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

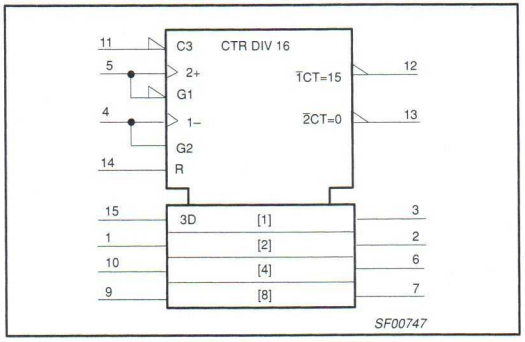
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 - D3	Data inputs	1.0/1.0	20µA/0.6mA
CP_U	Count up clock input (active rising edge)	1.0/3.0	20µA/1.8mA
CP_D	Count down clock input (active rising edge)	1.0/3.0	20µA/1.8mA
$\overline{PL}$	Asynchronous parallel load control input (active Low)	1.0/1.0	20µA/0.6mA
MR	Asynchronous master reset input	1.0/1.0	20µA/0.6mA
Q0 - Q3	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{TC}_U$	Terminal count up (carry) output (active Low)	50/33	1.0mA/20mA
$\overline{TC}_D$	Terminal count down (borrow) output (active Low)	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

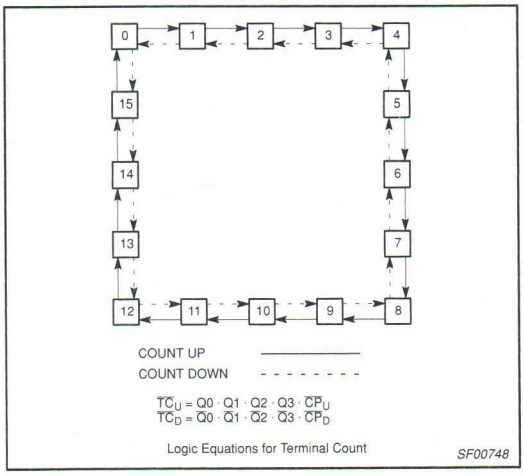
LOGIC SYMBOL



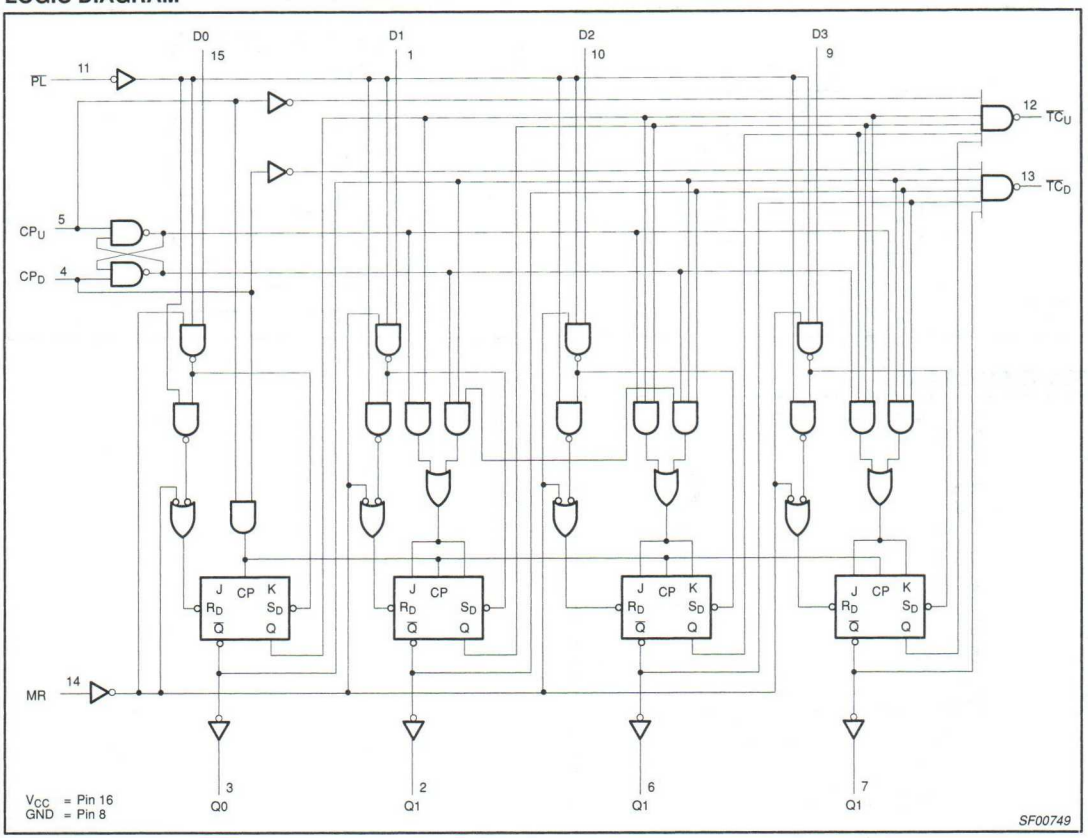
LOGIC SYMBOL (IEEE/IEC)



STATE DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS								OUTPUTS						OPERATING MODE
MR	$\overline{PL}$	CP_U	CP_D	D0	D1	D2	D3	Q0	Q1	Q2	Q3	$\overline{TC}_U$	$\overline{TC}_D$	
H	X	X	L	X	X	X	X	L	L	L	L	H	L	Reset (clear)
H	X	X	H	X	X	X	X	L	L	L	L	H	H	
L	L	X	L	L	L	L	L	L	L	L	L	H	L	Parallel load
L	L	X	H	L	L	L	L	L	L	L	L	H	H	
L	L	L	X	H	H	H	H	H	H	H	H	L	H	
L	L	H	X	H	H	H	H	H	H	H	H	H	H	
L	H	↑	H	X	X	X	X	Count up				H[1]	H	Count up
L	H	H	↑	X	X	X	X	Count down				H	H[2]	Count down

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

NOTES:
$\overline{TC}_U = \overline{CP}_U$ at terminal count up (HHHH)
$\overline{TC}_D = \overline{CP}_D$ at terminal count down (LLLL)

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	CP_U, CP_D	V_{CC} = MAX, V_I = 0.5V				−1.8	mA
		Others					−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)[4]		V_{CC} = MAX			32	50	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with parallel load and Master reset inputs grounded, all other inputs at 4.5V and all outputs open.

AC ELECTRICAL CHARACTERISTICS

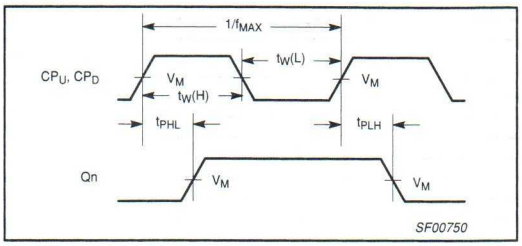
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	100	125		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP_U or CP_D to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 2	2.5 3.0	5.5 5.0	8.5 8.0	2.5 3.0	9.0 9.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CP_U or CP_D to Qn	Waveform 1	2.5 5.0	5.5 8.5	8.5 12.0	2.5 5.0	9.0 13.0	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to Qn	Waveform 4	2.0 6.0	4.0 9.5	7.0 13.5	1.5 6.0	8.0 15.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Qn	Waveform 3	4.5 5.5	6.5 8.5	10.0 12.0	4.0 5.0	11.0 13.0	ns ns
t_{PHL}	Propagation delay MR to Qn	Waveform 5	5.0	7.5	11.0	5.0	12.0	ns
t_{PLH}	Propagation delay MR to $\overline{TC}_U$	Waveform 5	6.0	8.5	12.0	5.5	13.0	ns
t_{PHL}	Propagation delay MR to $\overline{TC}_D$	Waveform 5	5.0	7.5	11.0	5.0	12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 3	6.0 6.0	9.5 9.0	13.5 12.0	6.0 6.0	15.0 13.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Dn to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 4	5.5 4.5	9.0 8.5	13.0 12.5	5.0 4.5	14.0 13.5	ns ns

AC SETUP REQUIREMENTS

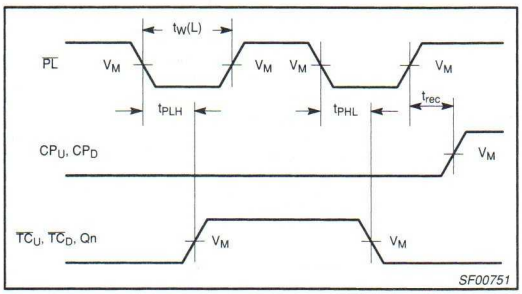
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb}= 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to $\overline{PL}$	Waveform 6	4.5 4.5			5.0 5.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to $\overline{PL}$	Waveform 6	2.0 2.0			2.0 2.0		ns ns
$t_w(L)$	$\overline{PL}$ Pulse width Low	Waveform 3	6.0			6.0		ns
$t_w(H)$ $t_w(L)$	CP_U or CP_D Pulse width High or Low	Waveform 1	3.5 5.0			3.5 5.0		ns ns
$t_w(L)$	CP_U or CP_D Pulse width Low (Change of direction)	Waveform 1	10.0			10.0		ns
$t_w(H)$	MR Pulse width High	Waveform 5	6.0			6.0		ns
t_{rec}	Recovery time, $\overline{PL}$ to CP_U or CP_D	Waveform 3	6.0			6.0		ns
t_{rec}	Recovery time MR to CP_U or CP_D	Waveform 5	4.0			4.0		ns

AC WAVEFORMS

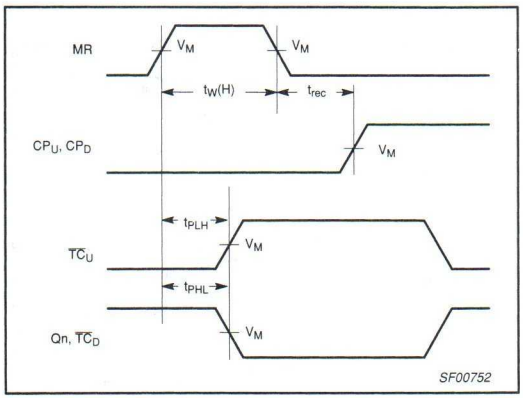
For all waveforms Vm = 1.5V



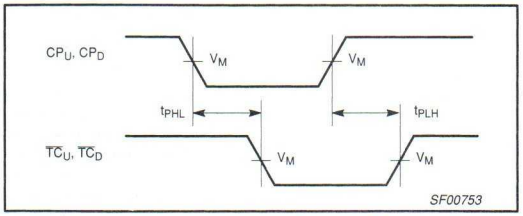
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width and Maximum Clock Frequency



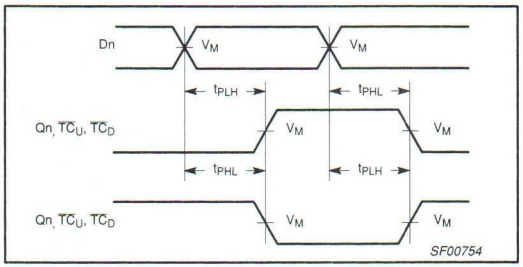
Waveform 3. Parallel Pulse Width, Parallel Load to Output Delays, and Parallel Load to Clock Recovery Time



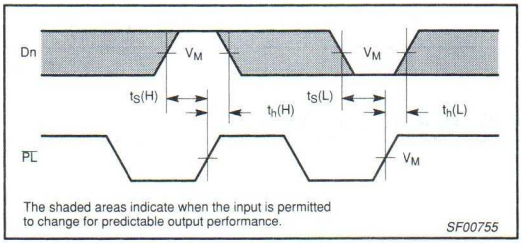
Waveform 5. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Waveform 2. Propagation Delay, Clock to Terminal Count

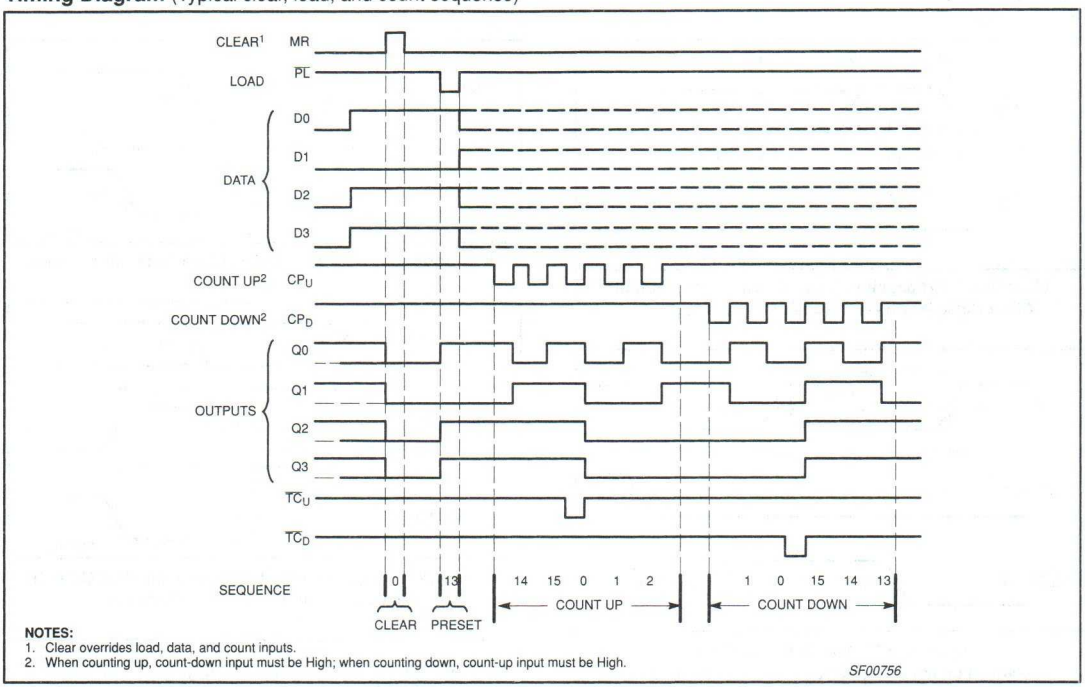


Waveform 4. Propagation Delay, Data to Flip-Flop Outputs, Terminal Count Up and Down Outputs



Waveform 6. Data Setup and Hold Times

Timing Diagram (Typical clear, load, and count sequence)

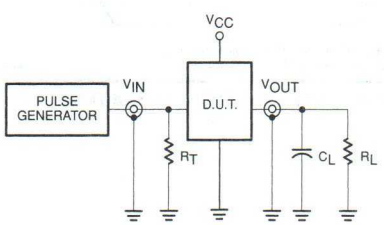


NOTES:
1. Clear overrides load, data, and count inputs.
2. When counting up, count-down input must be High; when counting down, count-up input must be High.

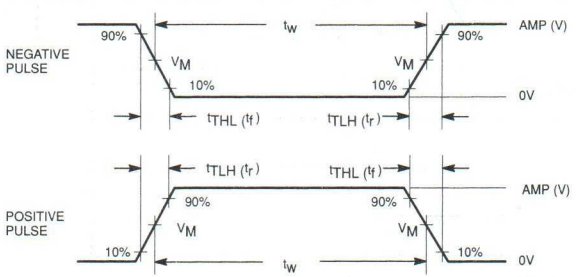
SF00756

Binary Counter

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

4-bit bidirectional universal shift register

74F194

FEATURES

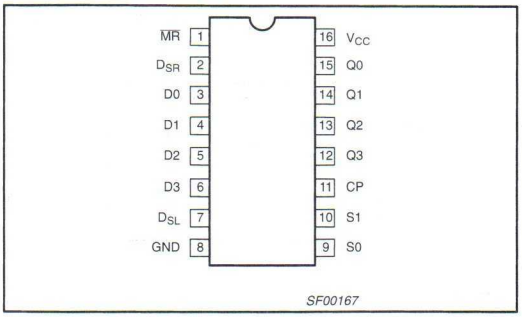
- Shift right and shift left capability
- Synchronous parallel and serial data transfer
- Easily expanded for both serial and parallel operation
- Asynchronous Master Reset
- Hold (do nothing) mode

DESCRIPTION

The functional characteristics of the 74F194 4-Bit Bidirectional Shift Register are indicated in the Logic Diagram and Function Table. The register is fully synchronous, with all operations taking place in less than 9ns (typical) for 74F, making the device especially useful for implementing very high speed CPUs, or for memory buffer registers.

The 74F194 design has special logic features which increase the range of application. The synchronous operation of the device is determined by two Mode Select inputs, S0 and S1. As shown in the Mode Select-Function Table, data can be entered and shifted from left to right (shift right, Q0→Q1, etc.), or right to left (shift left, Q3→Q2, etc.), or parallel data can be entered, loading all 4 bits of the register simultaneously. When both S0 and S1 are Low, existing data is retained in a hold (do nothing) mode. The first and last stages provide D-type Serial Data inputs (D_{SR}, D_{SL}) to allow multistage shift right or shift left data transfers without interfering with parallel load operation. Mode Select and data inputs on the 74F194 are edge-triggered, responding only to the Low-to-High transition of the Clock (CP). Therefore, the only timing restriction is that the Mode Select and selected data inputs must be stable one setup time prior to the Low-to-High transition of the clock pulse. Signals on the Mode Select, Parallel Data (D0–D3) and Serial Data (D_{SR}, D_{SL}) can change when the clock is in either state, provided only the recommended setup and hold times, with respect to the clock rising edge, are observed. The four Parallel Data inputs (D0–D3) are D-type inputs. Data appearing on (D0–D3) inputs when S0 and S1 are High is transferred to the Q0–Q3 outputs respectively, following the next Low-to-High transition of the clock. When Low, the asynchronous Master Reset ($\overline{MR}$) overrides all other input conditions and forces the Q outputs Low.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F194	150MHz	33mA

ORDERING INFORMATION

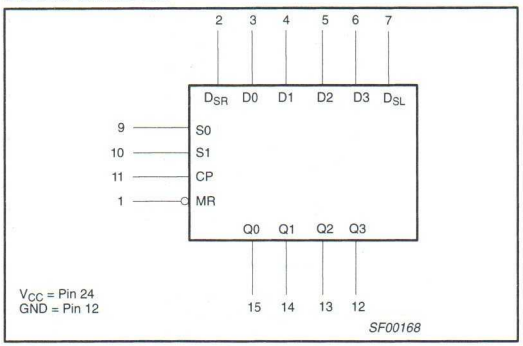
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
16-pin plastic DIP	N74F194N	SOT38-4
16-pin plastic SO	N74F194D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

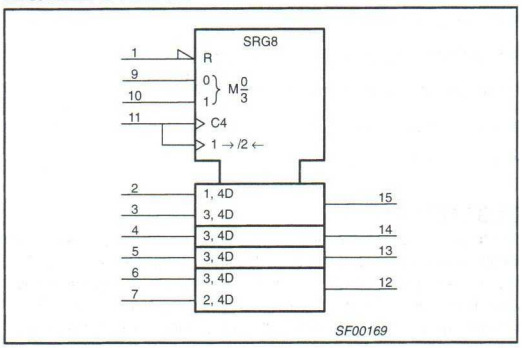
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0–D3	Parallel data inputs	1.0/1.0	20μA/0.6mA
D_{SR}	Serial data input (Shift Right)	1.0/1.0	20μA/0.6mA
D_{SL}	Serial data input (Shift Left)	1.0/1.0	20μA/0.6mA
S0, S1	Mode Select inputs	1.0/1.0	20μA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Asynchronous master Reset input (Active Low)	1.0/1.0	20μA/0.6mA
Q0–Q3	Data outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

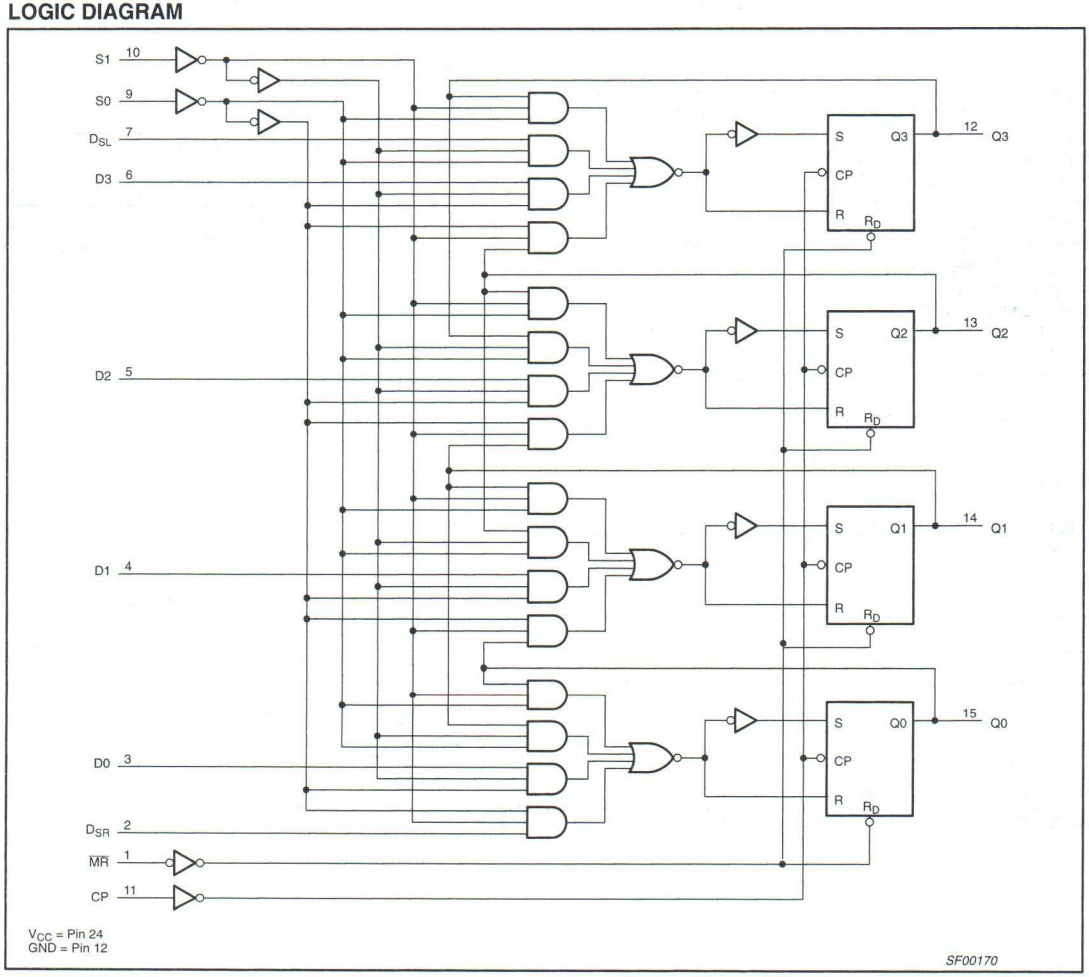
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUTS				OPERATING MODES
CP	$\overline{MR}$	S1	S0	D_{SR}	D_{SL}	Dn	Q0	Q1	Q2	Q3	
X	L	X	X	X	X	X	L	L	L	L	Reset (clear)
X	H	l	l	X	X	X	q0	q1	q2	q3	Hold (do nothing)
↑	H	h	l	X	l	X	q1	q2	q3	L	Shift left
↑	H	h	l	X	h	X	q1	q2	q3	H	
↑	H	l	h	l	X	X	L	q0	q1	q2	Shift right
↑	H	l	h	h	X	X	H	q0	q1	q2	
↑	H	h	h	X	X	dn	d0	d1	d2	d3	Parallel load

H = High voltage level
h = High voltage level one setup time prior to Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
dn(qn) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the Low-to-High clock transition.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage[3]	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OS}	Short-circuit output current[4]	V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)[5]	V_{CC} = MAX			33	46	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Output High state will change to Low stat if an external voltage of less than 0.0V is applied.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
5. With all outputs open, D_i inputs grounded and a 4.5V applied to S0, S1, MR and the serial inputs, I_{CC} is tested with a momentary ground, then 4.5V applied to CP.

AC ELECTRICAL CHARACTERISTICS

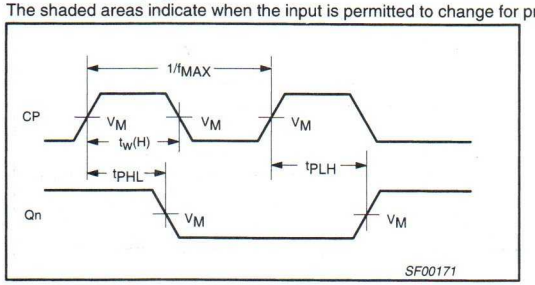
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	105	150		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	Waveform 1	3.5 3.5	5.2 5.5	7.0 7.0	3.5 3.5	8.0 8.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn	Waveform 2	4.5	8.6	12.0	4.5	14.0	ns

AC SETUP REQUIREMENTS

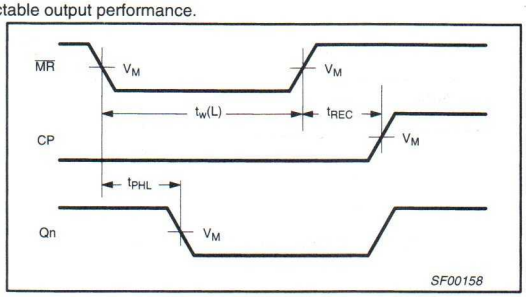
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_S(H) t_S(L)	Setup time, High or Low Dn, D_{SL}, D_{SR} to CP	Waveform 3	4.0 4.0			4.0 4.0		ns
t_h(H) t_h(L)	Hold time, High or Low Dn, D_{SL}, D_{SR} to CP	Waveform 3	0 0			1.0 1.0		ns
t_S(H) t_S(L)	Setup time, High or Low Sn to CP	Waveform 3	8.0 8.0			9.0 8.0		ns
t_h(H) t_h(L)	Hold time, High or Low Sn to CP	Waveform 3	0 0			0 0		ns
t_W(H)	CP Pulse width, High	Waveform 1	5.0			5.5		ns
t_W(L)	$\overline{MR}$ Pulse width, Low	Waveform 2	5.0			5.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP	Waveform 2	7.0			8.0		ns

AC WAVEFORMS

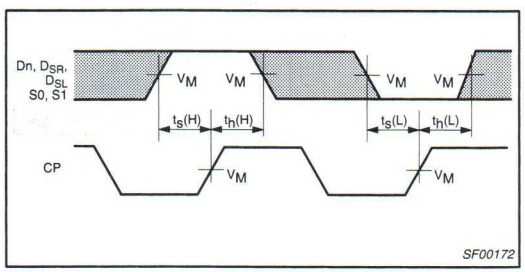
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



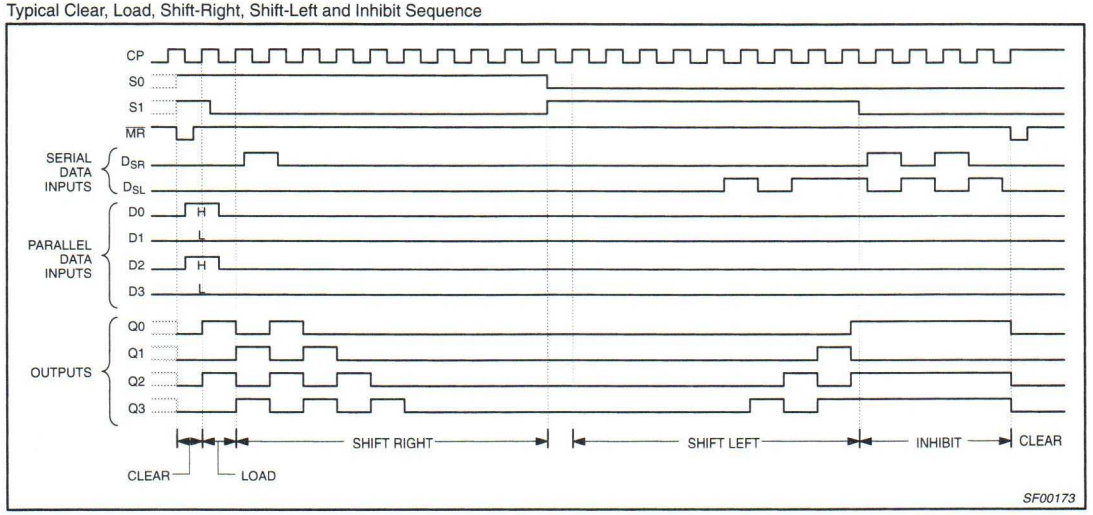
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay, and Master Reset to Clock Recovery Time



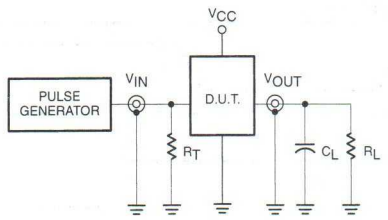
Waveform 3. Setup and Hold Times

TIMING DIAGRAM

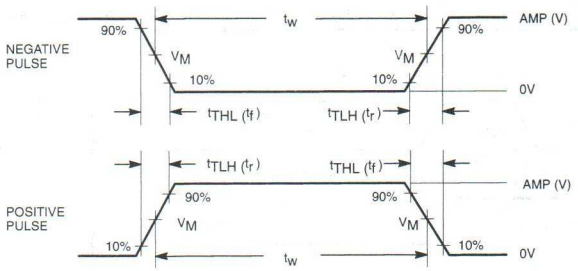
Typical Clear, Load, Shift-Right, Shift-Left and Inhibit Sequence



TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor;
see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

4-bit parallel-access shift register | 74F195A

FEATURES

- Shift right and parallel load capability
- J – $\overline{K}$ (D) inputs to first stage
- Complement output from last stage
- Asynchronous Master Reset
- Diode inputs

DESCRIPTION

The 74F195A is a 4-Bit Parallel Access Shift Register and its functional characteristics are indicated in the Logic Diagram and Function Table. This device is useful in a variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The 74F195A operates in two primary modes: shift right (Q0→Q1) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q0) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is High, and is shifted one bit in the direction Q0→Q1→Q2→Q3 following each Low-to-High clock transition.

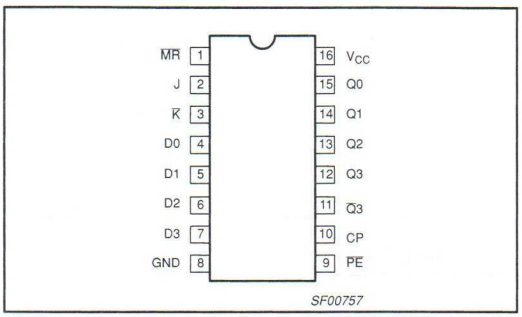
The J and $\overline{K}$ inputs provide the flexibility of the J-$\overline{K}$ type input for special applications, and by tying the two together the simple D-type input is made for general applications.

The device appears as four common clocked D flip-flops when the $\overline{PE}$ input is Low. After the Low-to-High clock transition, data on the parallel inputs (D0–D3) is transferred to the respective Q0–Q3 outputs. Shift left operation (Q3–Q2) can be achieved by tying the Qn outputs to the Dn-1 inputs and holding the $\overline{PE}$ input Low.

All parallel and serial data transfers are synchronous, occurring after each Low-to-High clock transition. The 74F195A utilizes edge-triggering, therefore there is no restriction on the activity of the J, $\overline{K}$, Dn, and $\overline{PE}$ inputs for logic operation, other than the set-up and hold time requirements.

A Low on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs Low, independent of any other input condition.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F195A	180MHz	40mA

ORDERING INFORMATION

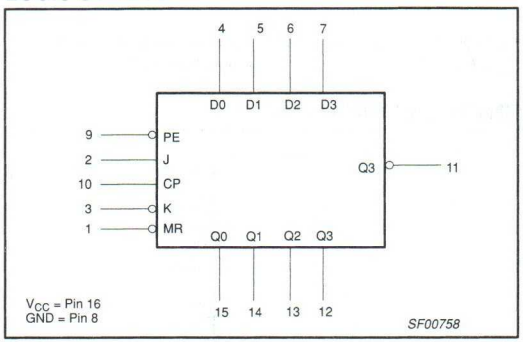
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG. DWG. #
16-pin plastic DIP	N74F195AN	SOT 38-4
16-pin plastic SO	N74F195AD	SOT 109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

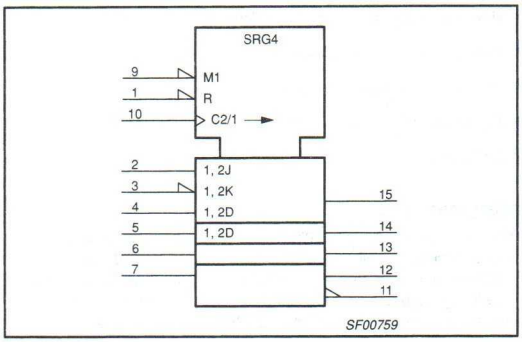
PINS	DESCRIPTION		74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0–D3	Data inputs	74F195	1.0/0.033	20μA/20μA
		74F195A	1.0/1.0	20μA/0.6mA
J, $\overline{K}$	J-K or D type serial inputs	74F195	1.0/0.033	20μA/20μA
		74F195A	1.0/1.0	20μA/0.6mA
CP	Clock Pulse input (active rising edge)	74F195	1.0/0.033	20μA/20μA
		74F195A	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master Reset input (active Low)	74F195	2.0/0.066	40μA/40μA
		74F195A	1.0/1.0	20μA/0.6mA
Q0–Q3, $\overline{Q3}$	Data outputs		50/33	1.0mA/20mA

NOTE:
One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

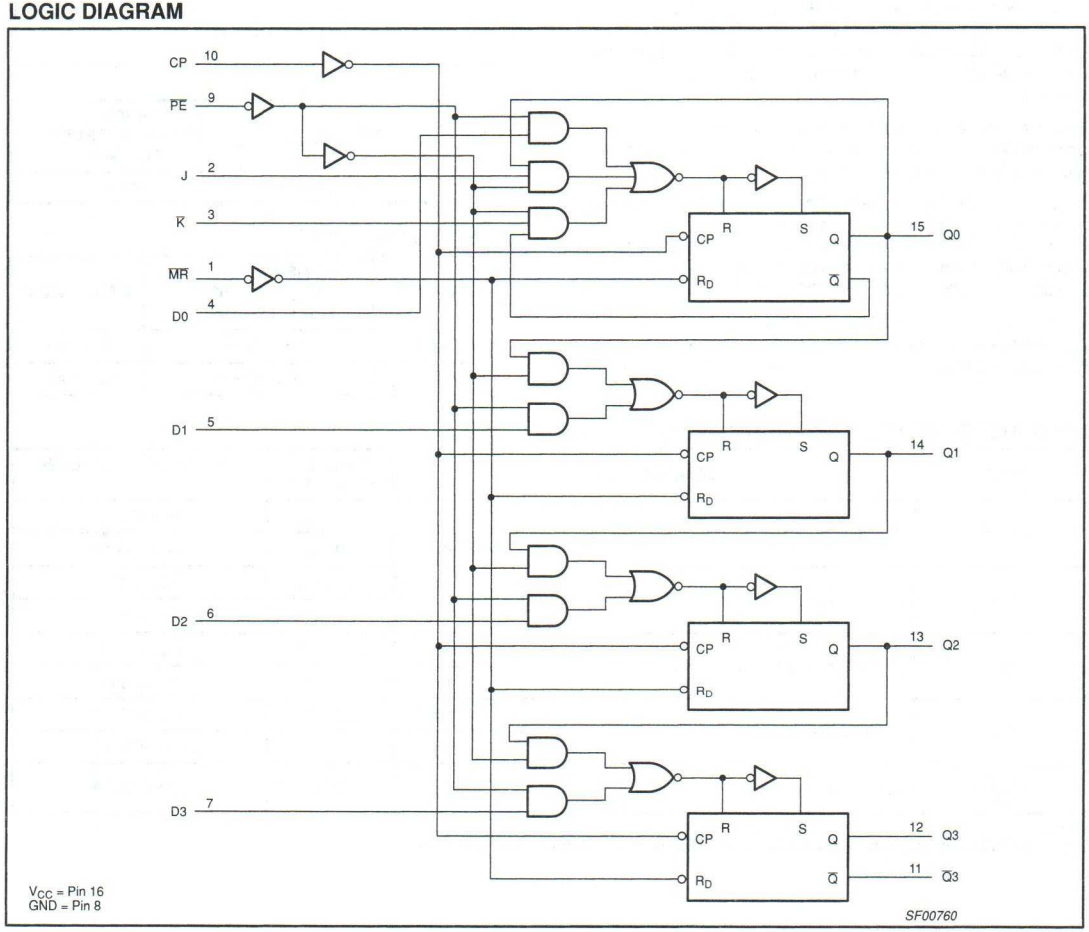
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS					OPERATING MODES
$\overline{MR}$	CP	$\overline{PE}$	J	$\overline{K}$	Dn	Q0	Q1	Q2	Q3	$\overline{Q3}$	
L	X	X	X	X	X	L	L	L	L	H	Reset (clear)
H	↑	h	h	h	X	H	q0	q1	q2	$\overline{q2}$	Shift, set First stage
H	↑	h	l	l	X	L	q0	q1	q2	$\overline{q2}$	Shift, reset First stage
H	↑	h	h	l	X	$\overline{q0}$	q0	q1	q2	$\overline{q2}$	Shift, toggle First stage
H	↑	h	l	h	X	q0	q0	q1	q2	$\overline{q2}$	Shift, retain First stage

H = High voltage level
h = High voltage level one setup time prior to Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
dn(qn) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the Low-to-High clock transition.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V	74F195A			100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V	all others			20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V	74F195A			–600	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	74F195A		40	58	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				V_{CC} = +5V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Load mode	Waveform 1	165	180		150		MHz
		Shift mode		180	190		170		
t_{PLH} t_{PHL}	Propagation delay CP to Qn		Waveform 1	3.0 2.5	5.0 4.0	9.5 7.0	2.5 2.0	10.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q3}$		Waveform 1	2.0 2.0	5.5 4.0	9.5 6.5	2.5 2.0	9.5 7.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn		Waveform 2	2.0	4.0	7.0	2.0	7.0	ns
t_{PLH}	Propagation delay $\overline{MR}$ to $\overline{Q3}$		Waveform 2	2.5	4.5	8.0	2.0	10.0	ns

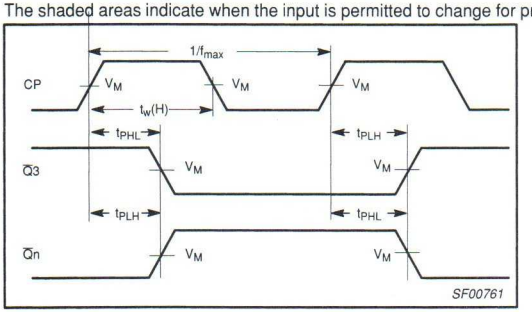
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_S(H)$ $t_S(L)$	Setup time, High or Low J, $\overline{K}$ and Dn to CP	Waveform 3	2.5 2.5			2.5 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J, $\overline{K}$ and Dn to CP	Waveform 3	0.0 1.0			0.0 1.0		ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low $\overline{PE}$ to CP	Waveform 4	2.0 2.5			2.0 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP	Waveform 4	0.0 0.0			0.0 0.0		ns
$t_W(H)$	CP Pulse width High	Waveform 1	4.5			4.5		ns
$t_W(L)$	$\overline{MR}$ Pulse width Low	Waveform 2	4.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 2	2.5			3.0		ns

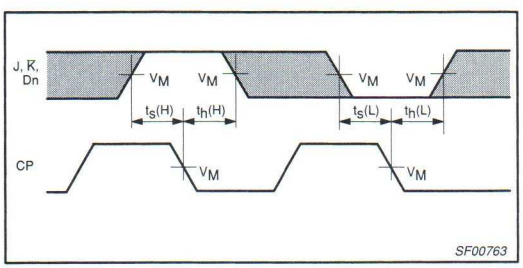
AC WAVEFORMS

For all waveforms, V_M = 1.5V.

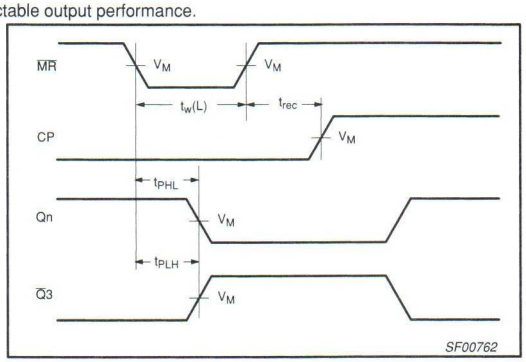
The shaded areas indicate when the input is permitted to change for predictable output performance.



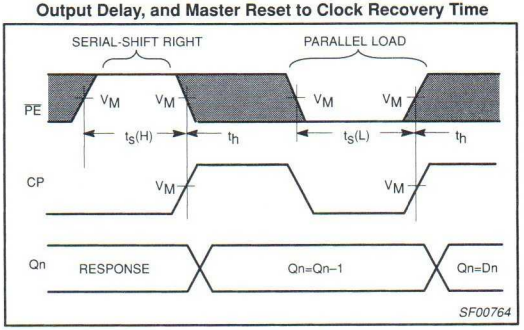
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup and Hold Times

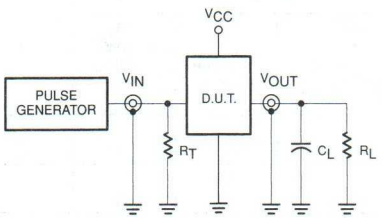


Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay, and Master Reset to Clock Recovery Time

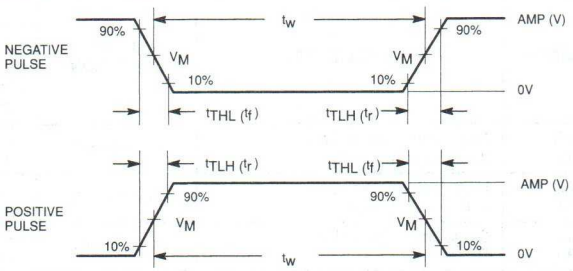


Waveform 4. Setup and Hold Times, Parallel Enable to Clock

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

8-bit bidirectional universal shift register 74F198

FEATURES

- Buffered clock and control inputs
- Shift right, shift left, and parallel load capability
- Asynchronous Master Reset

DESCRIPTION

The 74F198 Bidirectional Universal Shift Register is designed to incorporate virtually all of the features a system designer may want in a shift register. This circuit features parallel inputs and outputs, shift right and shift left serial inputs, operating mode select inputs, and direct overriding master reset input. The register has four distinct modes of operation:

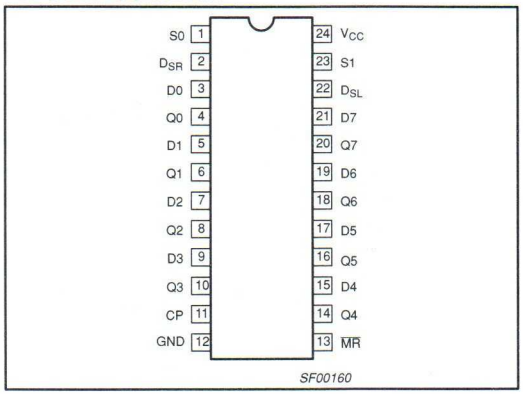
– Parallel (broadside) load
– Shift right (in the direction Q0 toward Q7)
– Shift left (in the direction Q7 toward Q0)
– Inhibit clock (do nothing).

Synchronous parallel loading is accomplished by applying the 8 bits of data and taking both mode control inputs, S0 and S1, High. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock inputs. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously, with the rising edge of the clock pulse when S0 is High and S1 is Low. Serial data for this mode is entered at the right data input (D_{SR}). When S0 is Low and S1 is High, data shifts left synchronously and new data is entered at the shift-left serial input (D_{SL}).

Clocking of the flip-flops is inhibited when both mode control inputs are Low.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F198	95MHz	73mA

ORDERING INFORMATION

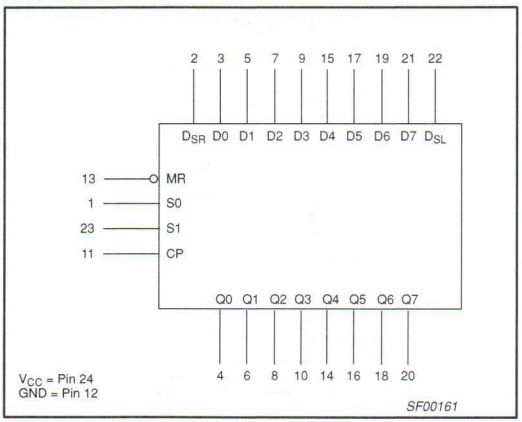
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
24-pin Plastic Slim DIP (300mil)	N74F198N	SOT222-1
24-pin Plastic SOL	N74F198D	SOT137-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

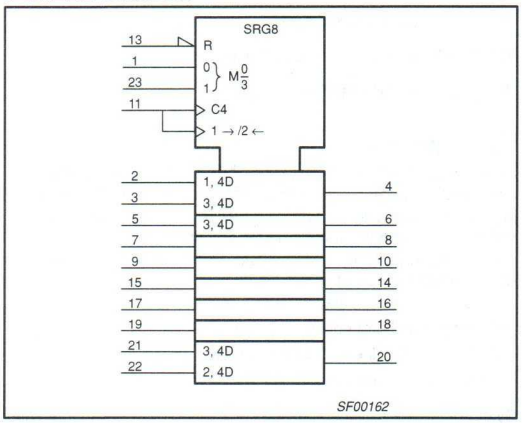
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0–D7	Parallel data inputs	1.0/1.0	20µA/0.6mA
D_{SR}	Serial data input (Shift Right)	1.0/1.0	20µA/0.6mA
D_{SL}	Serial data input (Shift Left)	1.0/1.0	20µA/0.6mA
S0–S1	Mode Select inputs	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (Active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (Active Low)	1.0/1.0	20µA/0.6mA
Q0–Q7	Data outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

LOGIC SYMBOL



IEC/IEEE SYMBOL

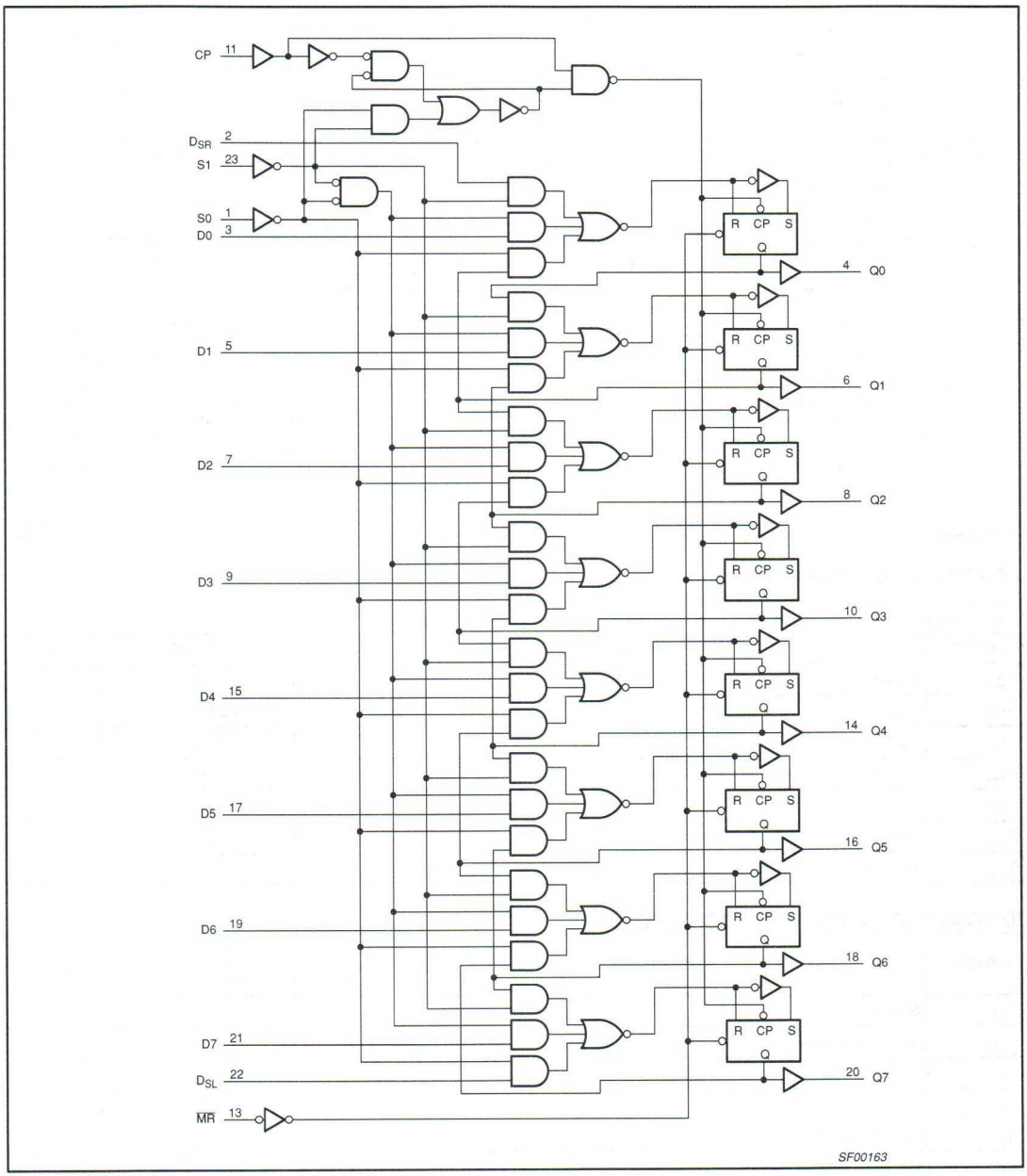


FUNCTION TABLE

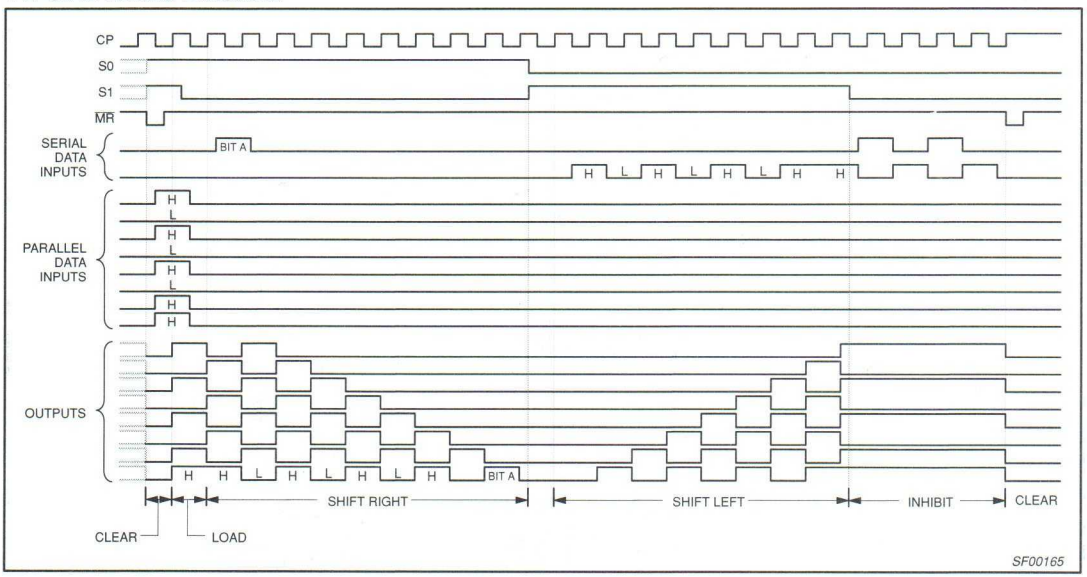
INPUTS							OUTPUTS				
MR	MODE		CP	SERIAL		PARALLEL	Q0	Q1	...	Q6	Q7
	S0	S1		LEFT	RIGHT	0...7					
L	X	X	X	X	X	X	L	L		L	L
H	X	X	L	X	X	X	Q00	Q10		Q60	Q70
H	H	H	↑	X	X	0...7	0	1		6	7
H	H	L	↑	X	H	X	H	Q0n		Q5n	Q6n
H	H	L	↑	X	L	X	L	Q0n		Q5n	Q6n
H	L	H	↑	H	X	X	Q1n	Q2n		Q7n	H
H	L	H	↑	L	X	X	Q1n	Q2n		Q7n	L
H	L	L	X	X	X	X	Q00	Q10		Q60	Q70

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High transition of designated input
0...7 = The level of steady input at inputs 0 through 7, respectively.
Q00, Q10, Q60, Q70 = The level of Q0, Q1, Q6, Q7, respectively, before the indicated steady state input conditions were established.
Q0n, Q1n, Q6n, Q7n = The level of Q0, Q1, Q6, Q7, respectively, before the most recent Low-to-High clock transition.

LOGIC DIAGRAM



TYPCIAL TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			70	100	mA
		I_{CCL}				75	110	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

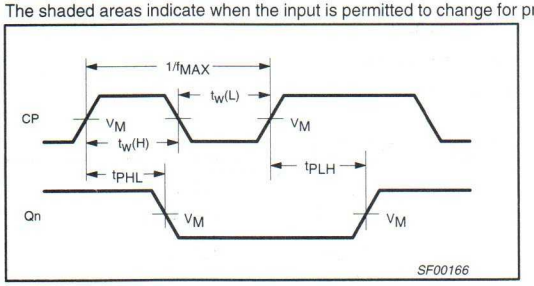
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	80	95		70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	Waveform 1	5.0 6.0	7.5 8.5	10.0 11.0	4.5 5.5	11.0 12.0	ns
t_{PHL}	Propagation delay	Waveform 3	5.0	7.5	10.0	4.5	11.0	ns

AC SETUP REQUIREMENTS

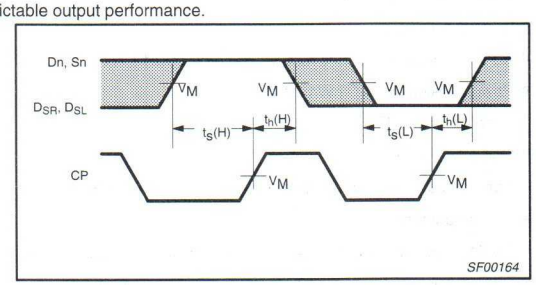
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_S(H) t_S((L)	Setup time, High or Low Dn to CP	Waveform 2	0.0 3.0			0.0 3.0		ns
t_h(H) t_h(L)	Hold time, High or Low Dn to CP	Waveform 2	0.0 3.5			1.0 4.0		ns
t_S(H) t_S(L)	Setup time, High or Low D_{SR}, D_{SL} to CP	Waveform 2	0.0 3.0			0.0 3.0		ns
t_h(H) t_h(L)	Hold time, High or Low D_{SR}, D_{SL} to CP	Waveform 2	0.0 2.5			0.0 3.0		ns
t_S(H) t_S(L)	Setup time, High or Low Sn to CP	Waveform 2	9.0 6.0			10.0 7.0		ns
t_h(H) t_h(L)	Hold time, High or Low Sn to CP	Waveform 2	0.0 0.0			0.0 0.0		ns
t_w(H) t_w(L)	CP Pulse width, High or Low	Waveform 1	5.0 5.0			6.0 6.0		ns
t_w(L)	$\overline{MR}$ Pulse width, Low	Waveform 3	5.0			5.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 3	5.0			6.0		ns

AC WAVEFORMS

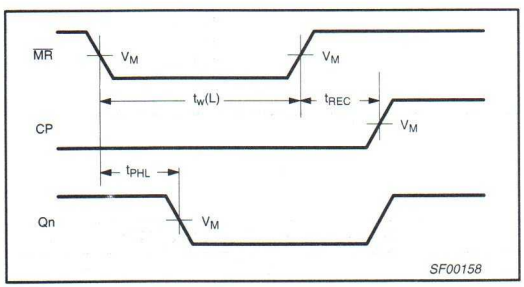
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation 'Delay, Clock Input to Output, Clock Widths, and Maximum Clock Frequency

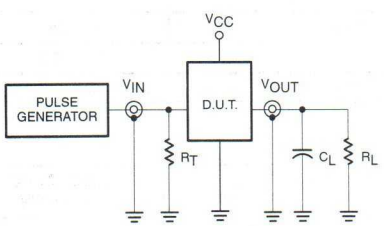


Waveform 2. Setup Time and Hold Time

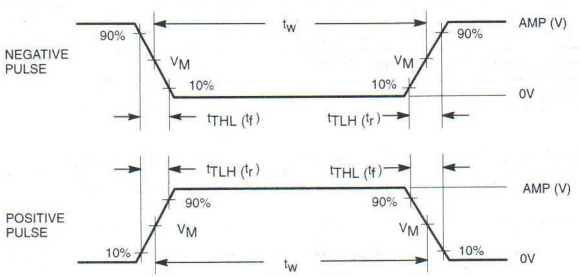


Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SF00006

64-bit TTL bipolar RAM, non-inverting (3-State) 74F219A

FEATURES

- High speed performance
- Replaces 74F219
- Address access time: 8ns max vs 28ns for 74F219
- Power dissipation: 4.3mW/bit typ
- Schottky clamp TTL
- One chip enable
- Non–Inverting outputs (for inverting outputs see 74F189A)
- 3–state outputs
- 74F219A in 150 mil wide SO is preferred options for new designs
- C3F219A in 300 mil wide SOL replaces 74F219 in existing designs

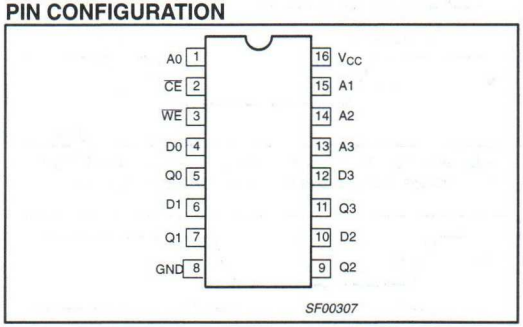
APPLICATIONS

- Scratch pad memory
- Buffer memory
- Push down stacks
- Control store

DESCRIPTION

The 74F219A is a high speed, 64–bit RAM organized as a 16–word by 4–bit array. Address inputs are buffered to minimize loading and are fully decoded on chip. The outputs are in high impedance state whenever the chip enable ($\overline{CE}$) is high. The outputs are active only in the READ mode ($\overline{WE}$ = high) and the output data is the complement of the stored data.

PIN CONFIGURATION



TYPE	TYPICAL ACCESS TIME	TYPICAL SUPPLY CURRENT(TOTAL)
74F219A	5.0ns	55mA

ORDERING INFORMATION

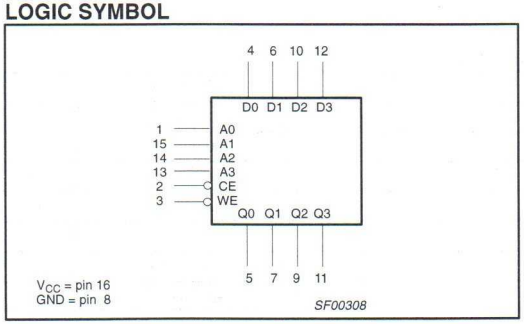
DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
16-pin plastic Dual In-line Package	N74F219AN	SOT38-4
16-pin plastic Small Outline (150mil)	N74F219AD	SOT109-1
16-pin plastic Small Outline Large (300mil)	C3F219AD	SOT162–1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

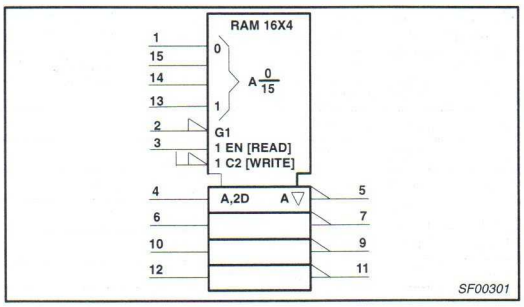
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D3	Data inputs	1.0/1.0	20µA/0.6mA
A0 – A3	Address inputs	1.0/1.0	20µA/0.6mA
$\overline{CE}$	Chip enable input (active low)	1.0/2.0	20µA/1.2mA
$\overline{WE}$	Write enable input (active low)	1.0/2.0	20µA/1.2mA
Q0 – Q3	Data outputs	150/40	3mA/24mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

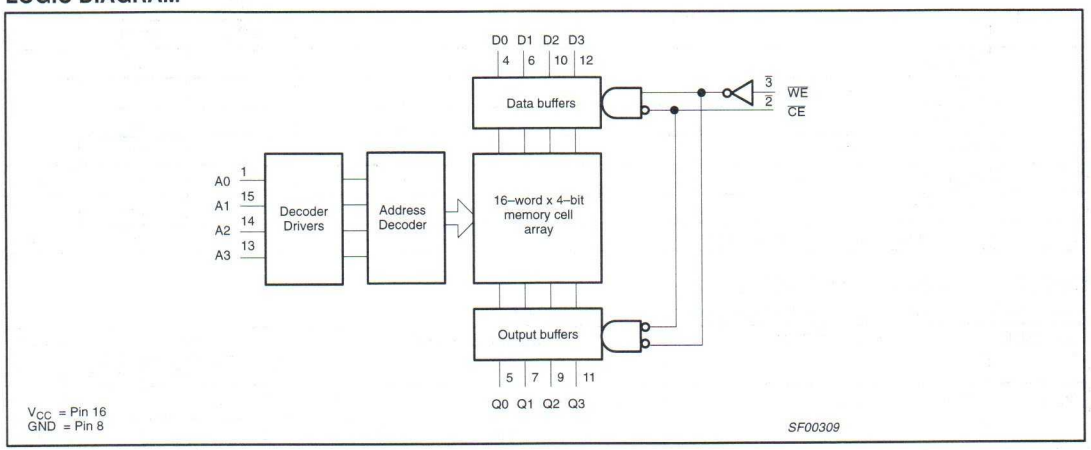
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUT	OPERATING MODE
$\overline{CE}$	$\overline{WE}$	Dn	Q_n	
L	H	X	Stored data	Read
L	L	L	High impedance	Write "0"
L	L	H	High impedance	Write "1"
H	X	X	High impedance	Disable input

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–3	mA
I_{OL}	Low–level output current			24	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current	others	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		$\overline{CE}$, $\overline{WE}$					-1.2	mA
I_{OZH}	Offset output current, high–level voltage applied		V_{CC} = MAX, V_I = 2.7V				50	µA
I_{OZL}	Offset output current, low–level voltage applied		V_{CC} = MAX, V_I = 0.5V				–50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX, $\overline{CE}$ = $\overline{WE}$ = GND			55	80	mA
C_{IN}	Input capacitance		V_{CC} = 5V, V_{IN} = 2.0V			4		pF
C_{OUT}	Output capacitance		V_{CC} = 5V, V_{OUT} = 2.0V			7		pF

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

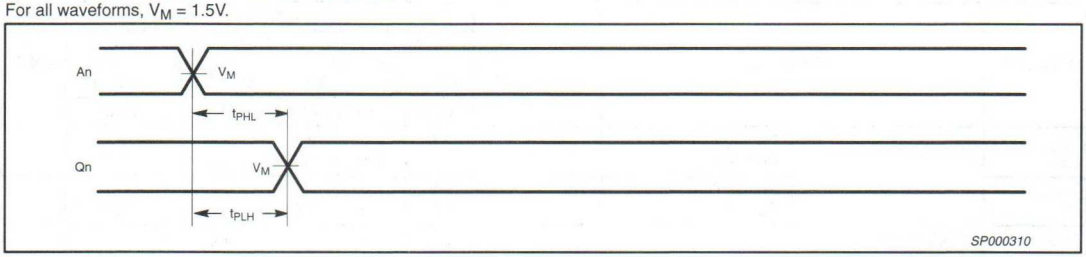
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Access time	Propagation delay An to Qn	Waveform 1	2.5 2.0	5.0 4.5	8.0 8.0	2.5 2.0	8.0 8.0	ns
t_{PZH} t_{PZL}		Enable time $\overline{CE}$ to Qn	Waveform 2	1.5 2.5	3.0 4.0	6.0 7.0	1.5 2.0	7.0 7.5	ns
t_{PHZ} t_{PLZ}	Disable time $\overline{CE}$ to Qn		Waveform 3	2.5 1.5	4.5 3.0	7.0 5.5	2.0 1.0	8.0 6.0	ns
t_{PZH} t_{PZL}	Write recovery time	Enable time $\overline{WE}$ to Qn	Waveform 4	2.0 3.0	3.5 4.5	6.5 7.5	1.5 2.5	7.0 8.0	ns
t_{PHZ} t_{PLZ}	Disable time $\overline{WE}$ to Qn		Waveform 4	3.0 1.5	5.0 3.5	8.0 6.0	2.5 1.5	9.0 7.0	ns

AC SETUP REQUIREMENT

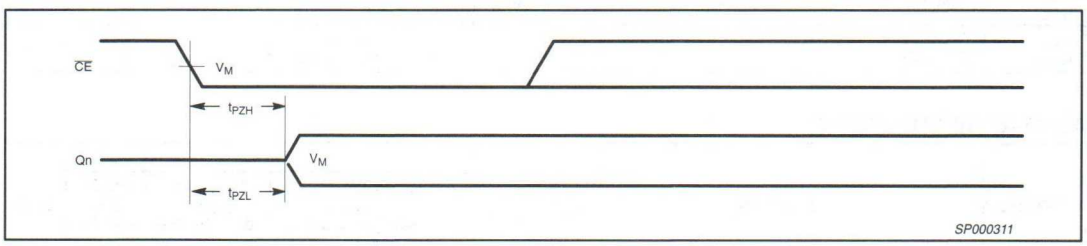
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low An to $\overline{WE}$	Waveform 4	4.5 4.5			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low An to $\overline{WE}$	Waveform 4	0 0			0 0		ns
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low Dn to $\overline{WE}$	Waveform 4	8.0 7.5			9.0 8.5		ns
$t_h(H)$ $t_h(L)$	Hold time, high or low Dn to $\overline{WE}$	Waveform 4	0 0			0 0		ns
$t_{su}(L)$	Setup time, low $\overline{CE}$ (falling edge) to $\overline{WE}$ (falling edge)	Waveform 4	0			0		ns
$t_h(L)$	Hold time, low $\overline{WE}$ (falling edge) to $\overline{WE}$ (rising edge)	Waveform 4	6.5			7.5		ns
$t_w(L)$	Pulse width, low $\overline{WE}$	Waveform 4	7.0			8.0		ns

AC WAVEFORMS FOR READ CYCLES

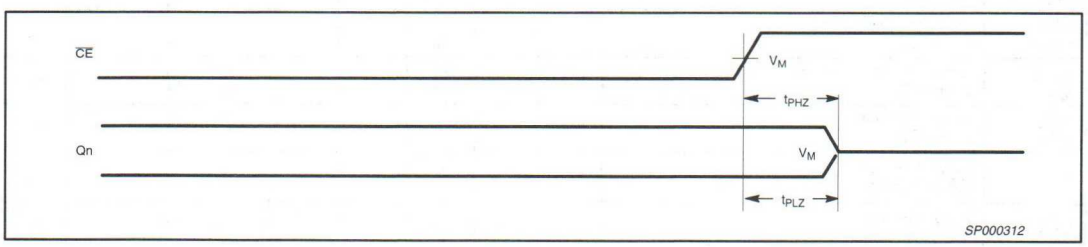
For all waveforms, V_M = 1.5V.



Waveform 1. Read cycle, address access time

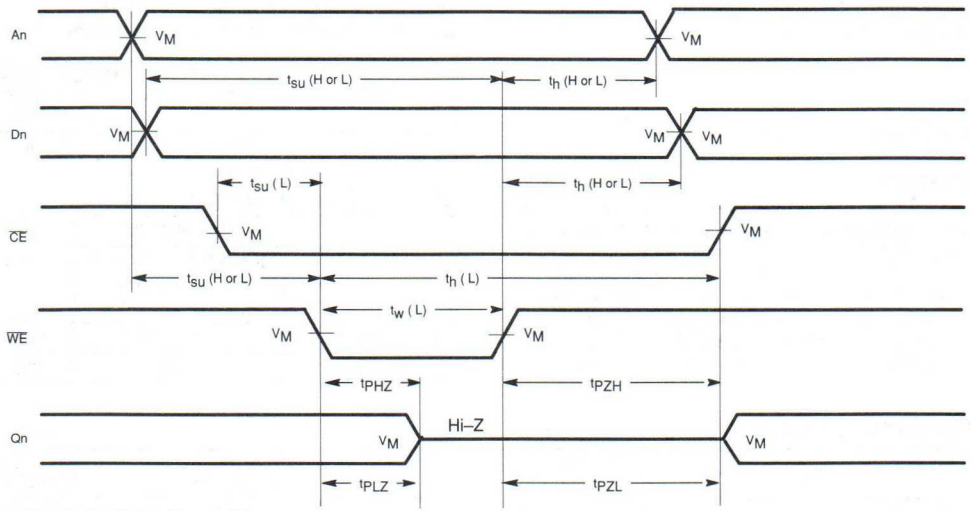


Waveform 2. Read cycle, chip enable access time



Waveform 3. Read cycle, chip disable time

AC WAVEFORMS FOR WRITE CYCLE

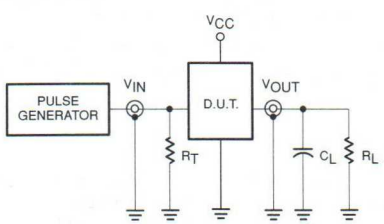


NOTE: For all waveforms, V_M = 1.5V.

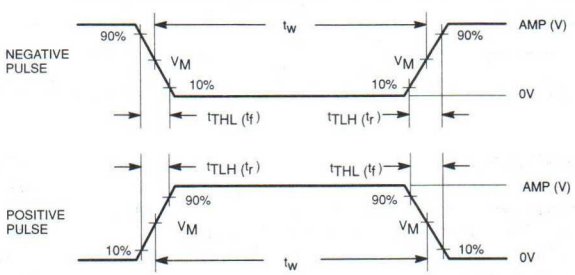
SP000313

Waveform 4. Write cycle

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

16 × 5 asynchronous FIFO (3-State) 74F225

FEATURES

- Independent synchronous inputs and outputs
- Organized as 16 words of 5 bits
- DC to 25MHz data rate
- 3–State outputs
- Cascadable in word–width and depth direction

DESCRIPTION

This 80–bit active element First–In–First–Out (FIFO) is a monolithic Schottky–clamped transistor–transistor logic (STTL) array organized as 16–words of 5–bits each. A memory system using the 'F225 can be easily expanded in multiples of 16–words of 5–bits as shown in Figure 1. The 3–State outputs controlled by a single enable input ($\overline{OE}$) make bus connection and multiplexing simple. The 'F225 processes data in a parallel format at any desired clock rate from DC to 25MHz. Status of the 'F225 is provided by three outputs, Input Ready (IR), Unload Clock Output (UNCPOUT) and Output Ready (OR). The data outputs are non–inverting with respect to the data inputs and are disabled when the $\overline{OE}$ input is High. When $\overline{OE}$ is Low, the data outputs are enabled to function as totem–pole outputs.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F225	25MHz	65mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
20–pin plastic DIP	N74F225N	SOT146-1
20–pin plastic SOL	N74F225D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
CPA, CPB	Load clock A and load clock B inputs	1.0/0.033	20µA/20µA
D0 – D4	Data inputs	1.0/0.033	20µA/20µA
$\overline{OE}$	Output enable input (active–Low)	1.0/0.033	20µA/20µA
UNCPIN	Unload clock input	1.0/0.033	20µA/20µA
$\overline{MR}$	Master reset input (active–Low)	1.0/0.033	20µA/20µA
IR	Input ready output	50/33	1.0mA/20mA
UNCPOUT	Unload clock output (active–Low)	50/33	1.0mA/20mA
Q0 – Q4	Data outputs	150/40	3.0mA/24mA
OR	Output ready output	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

RESET MODE

A High–to–Low transition on the Master Reset ($\overline{MR}$) input invalidates all data stored in the FIFO by clearing the control logic and setting OR Low. This High–to–Low transition on the $\overline{MR}$ input does not effect the data outputs but since OR is driven Low, it signifies invalid data on the outputs.

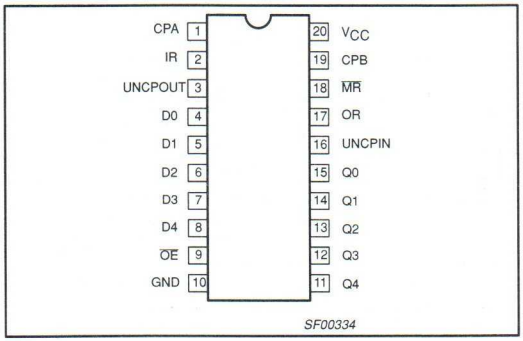
WRITE MODE

Data may be written into the array on the Low–to–High transition of either load clock (CPA or CPB) input. When writing data into the FIFO, one of the load clock inputs must be held High while the other strobes data into the FIFO. This arrangement allows either load clock to function as an inhibit for the other. Input Ready (IR) monitors the status of the last word location and signifies when the FIFO is full. This output is High whenever the FIFO is available to accept new data. The unload clock output (UNCPOUT) also monitors the last word location. This output generates a Low–logic–level pulse (synchronized to the internal clock pulse) when the last word location is vacant

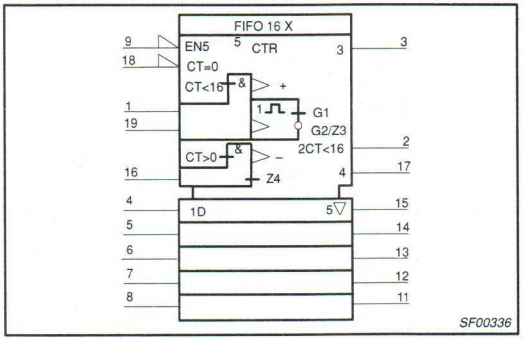
READ MODE

The Output Ready (OR) output is High when valid data is present on the data outputs. Data in the array is shifted on the Low–to–High transition of the Unload Clock Input (UNCPIN). In order for Output Ready (OR) to go High, Unload Clock Input (UNCPIN) must also be High.

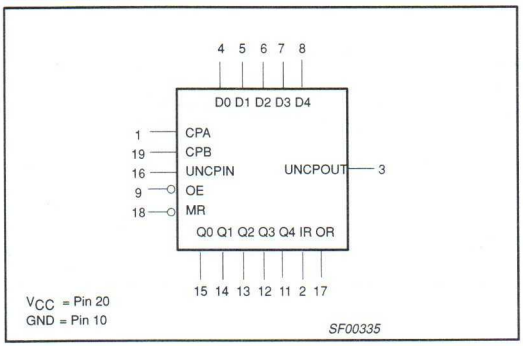
PIN CONFIGURATION



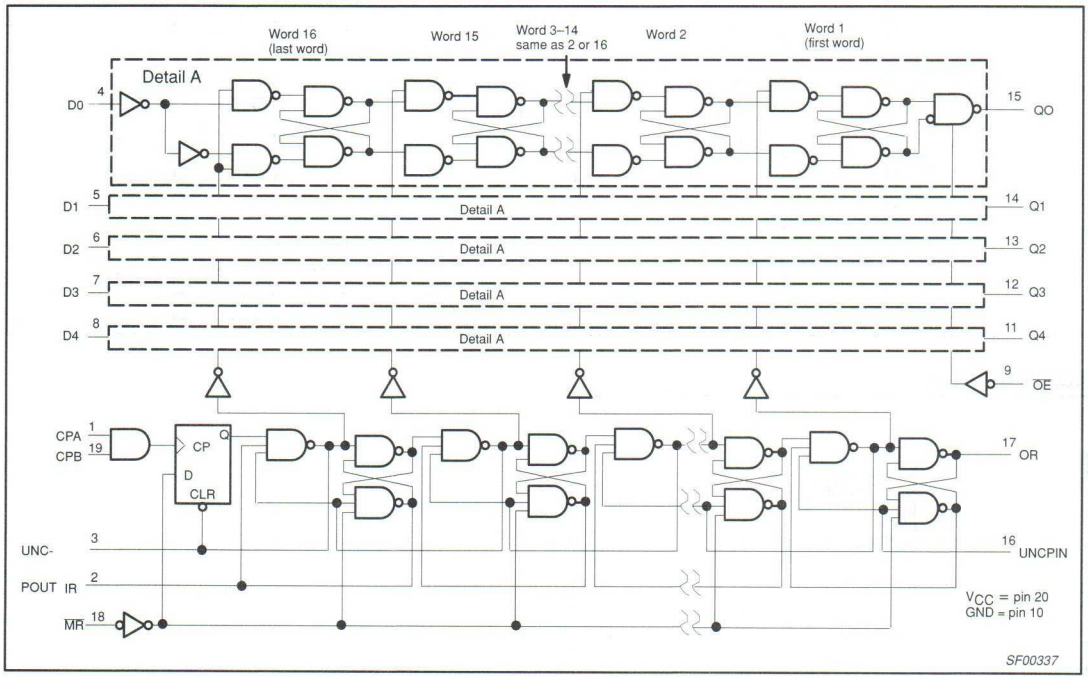
IEC/IEEE SYMBOL



LOGIC SYMBOL



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	IR, OR, UNCPOUT	40	mA
	Current applied to output in Low output state	Data outputs	48	mA
T_{amb}	Operating free air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IN}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current	IR, OR, UNCPOUT			–1	mA
		Data outputs			–3	mA
I_{OL}	Low–level output current	IR, OR, UNCPOUT			20	mA
		Data outputs			24	mA
T_{amb}	Operating free air temperature range		0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	IR, OR, UNCPOUT	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7			V
		Data outputs	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				–20	µA
I_{OZH}	Offset–output current, High–level voltage applied		V_{CC} = MAX, V_I = 2.7V				50	µA
I_{OZL}	Offset–output current, Low–level voltage applied		V_{CC} = MAX, V_I = 0.5V				–50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			65	95	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

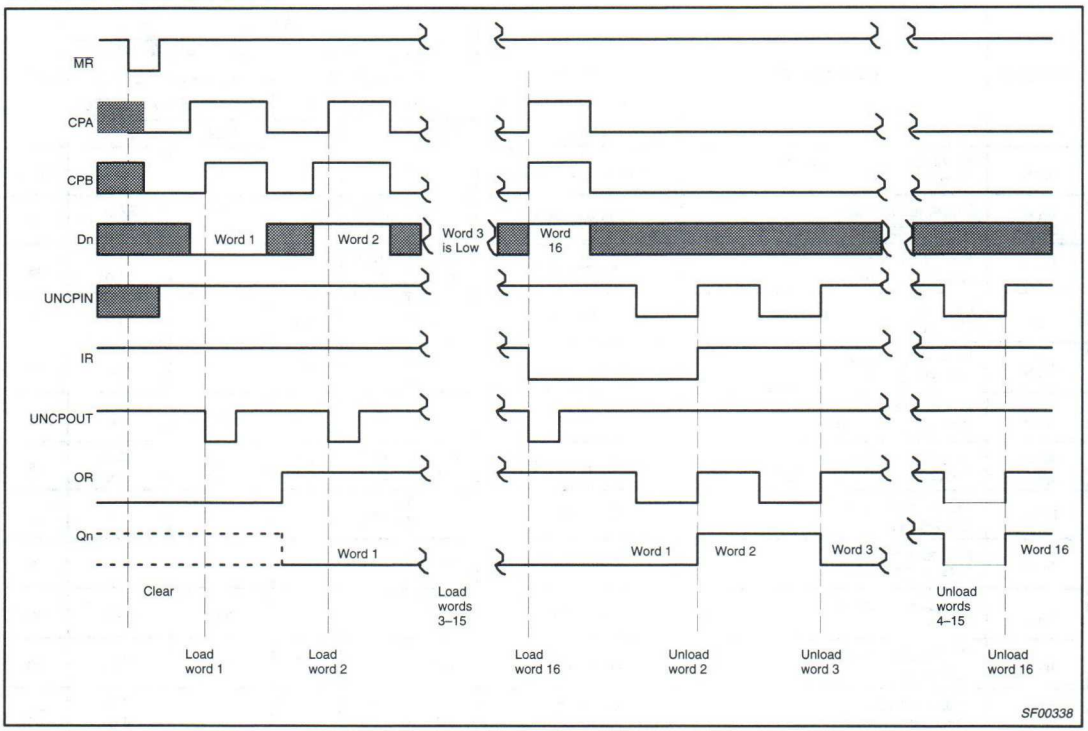
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency, Cascade mode	Waveform 2 and 3	25			25		MHz
t_{PLH} t_{PHL}	Propagation delay UNCPIN to Qn	Waveform 2	10.0 9.5	13.0 12.0	19.5 16.0	9.0 8.5	22.0 19.0	ns
t_{PLH} t_{PHL}	Propagation delay UNCPIN to OR	Waveform 2	16.0 6.0	20.0 8.5	25.0 11.0	14.0 5.0	29.0 12.0	ns
t_{SK}	Output skew Qn to OR ↑	Waveform 4	2.0		12.0	0.0	15.0	ns
t_{PLH}	Propagation delay UNCPIN to IR	Waveform 2	50	60	70	50	85	ns
t_{PLH}	Propagation delay CPA or CPB to OR	Waveform 4	55	65	75	50	90	ns
t_{PLH} t_{PHL}	Propagation delay CPA or CPB to UNCPOUT	Waveform 4	20.0 8.5	23.0 11.5	27.0 15.0	17.0 7.5	29.0 16.0	ns
$t_w(L)$	Pulse width, Low UNCPOUT	Waveform 4		12.0				ns
t_{PHL}	Propagation delay CPA or CPB to IR	Waveform 3	11.0	13.5	17.0	9.0	19.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to OR	Waveform 3	5.5	8.5	11.5	5.0	13.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to IR	Waveform 3	2.0	4.0	7.0	1.5	7.5	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	Waveform 5 Waveform 6	1.5 2.5	3.5 4.5	6.5 7.5	1.0 2.0	7.0 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	Waveform 5 Waveform 6	1.5 2.0	3.5 4.0	7.0 7.0	1.0 1.5	7.5 7.5	ns

AC SETUP REQUIREMENTS

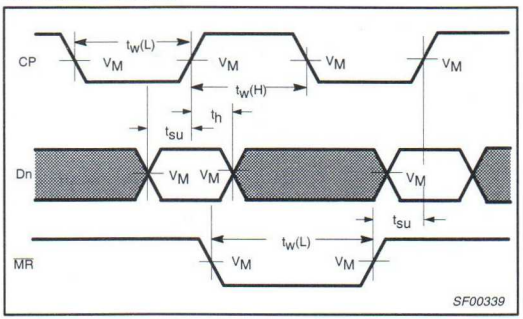
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to CPA or CPB	Waveform 1	0.0 0.0			0.0 0.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CPA or CPB	Waveform 1	14.0 12.5			16.5 14.0		ns
t_{rec}	Recovery time $\overline{MR}$ to CPA or CPB	Waveform 1	0.0			0.0		ns
$t_w(H)$ $t_w(L)$	CPA or CPB pulse width, High or Low	Waveform 1	6.5 3.0			8.5 3.5		ns
$t_w(L)$	UNCPIN pulse width, High or Low	Waveform 2	24.0 3.5			28.0 4.0		ns
$t_w(L)$	$\overline{MR}$ pulse width, Low	Waveform 1	3.5			4.5		ns

TYPICAL TIMING DIAGRAM

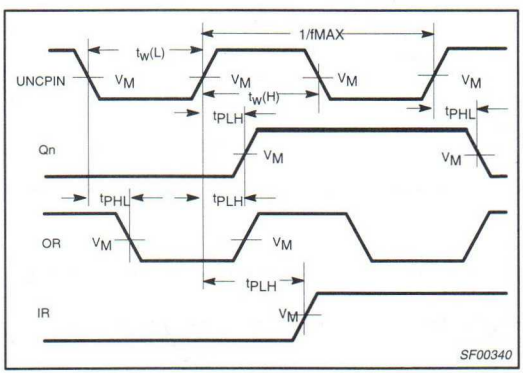


NOTE: Shaded areas Indicates irrelevant input conditions.

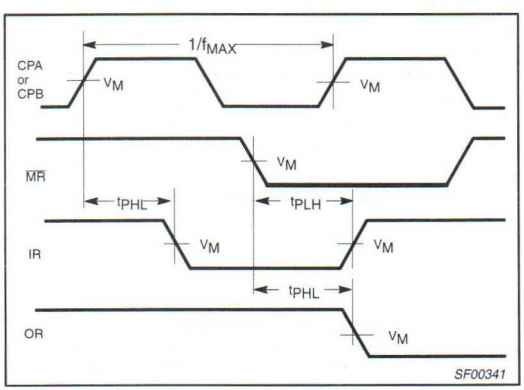
AC WAVEFORMS



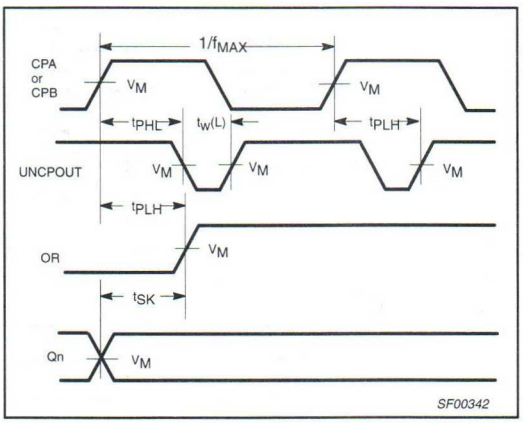
Waveform 1. $\overline{MR}$ and Clock Pulse Widths, Data Setup and Hold Times and $\overline{MR}$ to Clock Setup Time



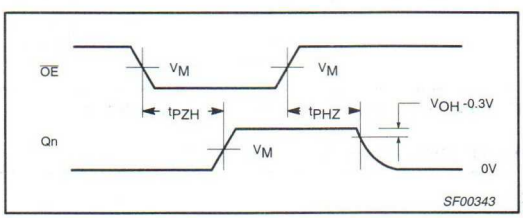
Waveform 2. UNCPIN to Output Delays



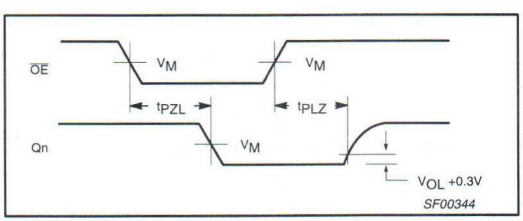
Waveform 3. CPA or CPB to IR Delay and $\overline{MR}$ to IR and OR Delay



Waveform 4. CPA or CPB to UNCPOUT and OR Delay, UNCPOUT Pulse Width and Qn to OR Skew



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTES:
1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION

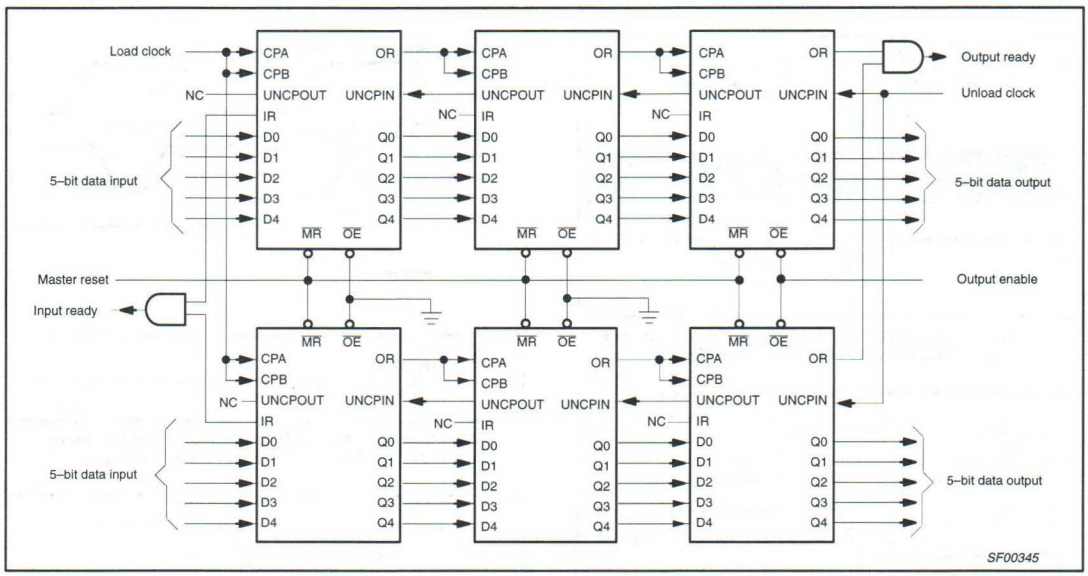
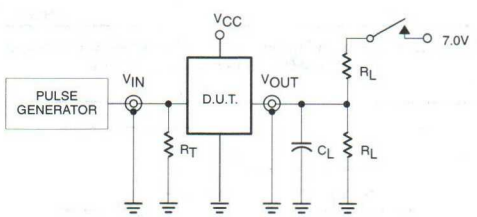
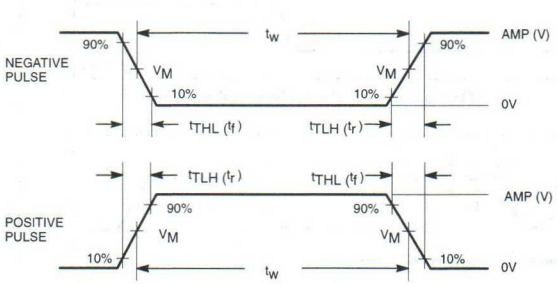


Figure 1. Expanding the 74F225 FIFO (48 words of 10 bits)

TEST CIRCUIT AND WAVEFORM



Test Circuit for Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

Buffers

74F240/74F240A/ 74F241/74F241A

FEATURES

- Octal bus interface
- 3-State buffer outputs sink 64mA
- 15mA source current
- Guaranteed output skew less than 2.0ns (74F240A/74F241A)
- Reduced ground bounce (74F240A/74F241A)
- Reduced I_{CC} (74F241A only)
- Reduced loading (74F240A I_{IL} = 100µA, 74F241A I_{IL} = 40µA)

DESCRIPTION

The 74F240 and 74F241 are octal buffers that are ideal for driving bus lines of buffer memory address registers. The outputs are all capable of sinking 64mA and sourcing up to 15mA. The device features two output enables, each controlling four of the 3–state outputs.

The 74F240A and 74F241A are functionally equivalent to their non–A counterparts. They have been designed to reduce effects of ground noise. Other advantages are noted in the features.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F240	4.3ns	37mA
74F240A	3.8ns	40mA
74F241	5.0ns	53mA
74F241A	4.5ns	32mA

ORDERING INFORMATION

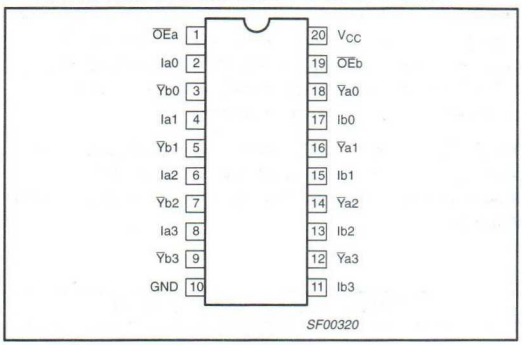
DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
20–pin plastic DIP	N74F240N, N74F240AN, N74F241N, N74F241AN	SOT146-1
20–pin plastic SOL	N74F240D, N74F240AD, N74F241D, N74F241AD	SOT163-1
20-pin plastic SSOP II	N74F240DB	SOT339-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

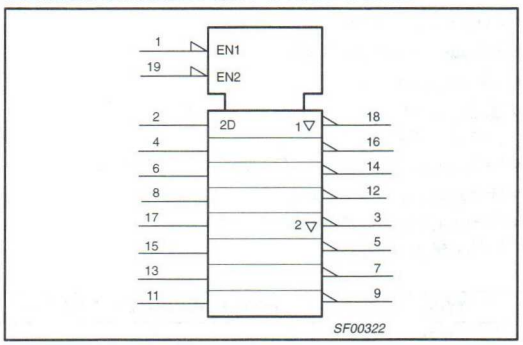
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ian, Ibn	Data inputs (74F240)	1.0/1.67	20µA/1.0mA
	Data inputs (74F240A)	1.0/0.167	20µA/100µA
	Data inputs (74F241)	1.0/2.67	20µA/1.6mA
	Data inputs (74F241A)	1.0/0.067	20µA/40µA
$\overline{OE}$a, $\overline{OE}$b	Output enable inputs (active low) (74F240)	1.0/0.33	20µA/0.2mA
	Output enable inputs (active low) (74F240A)	1.0/0.167	20µA/100µA
$\overline{OE}$a, OEb	Output enable input (74F241)	1.0/1.67	20µA/1.0mA
	Output enable input (74F241A)	1.0/0.067	20µA/40µA
Yan, Ybn	Data outputs (74F241, 74F241A)	750/106.7	15mA/64mA
$\overline{Y}$an, $\overline{Y}$bn	Data outputs (74F240, 74F240A)	750/106.7	15mA/64mA

Note to input and output loading and fan out table
One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

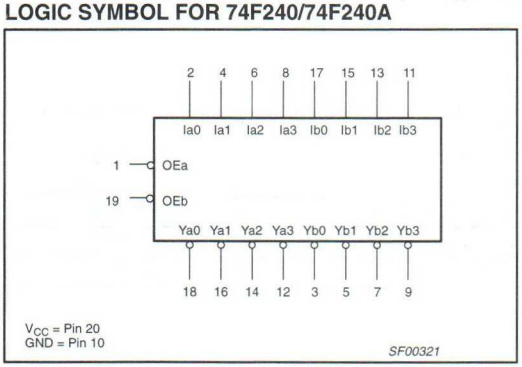
PIN CONFIGURATION FOR 74F240/74F240A



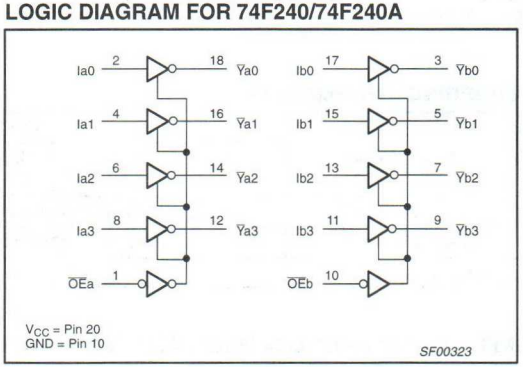
IEC/IEEE SYMBOL FOR 74F240/74F240A



LOGIC SYMBOL FOR 74F240/74F240A



LOGIC DIAGRAM FOR 74F240/74F240A



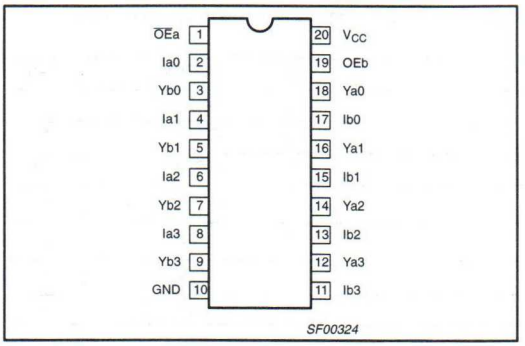
FUNCTION TABLE FOR 74F240/74F240A

INPUTS				OUTPUTS	
$\overline{OEa}$	Ia	$\overline{OEb}$	Ib	$\overline{Ya}$	$\overline{Yb}$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

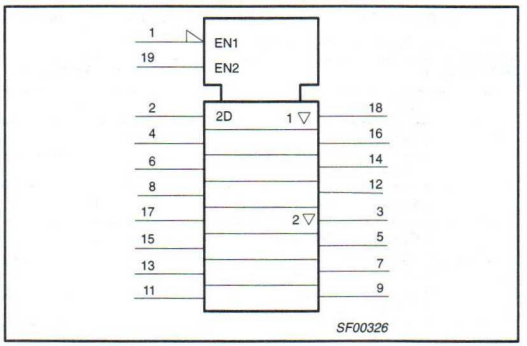
Notes to function table for 74F240/74F240A

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

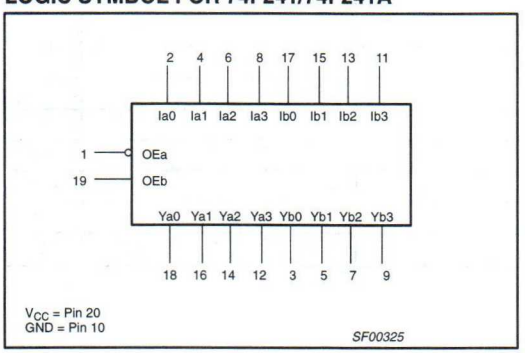
PIN CONFIGURATION FOR 74F241/74F241A



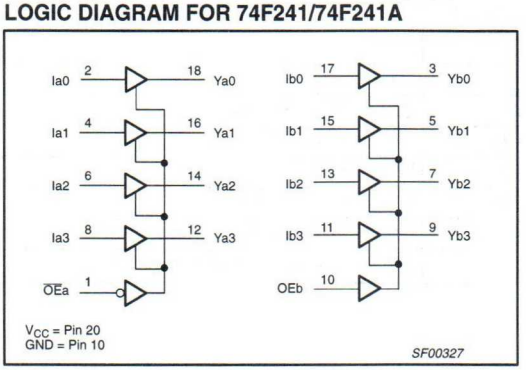
IEC/IEEE SYMBOL FOR 74F241/74F241A



LOGIC SYMBOL FOR 74F241/74F241A



LOGIC DIAGRAM FOR 74F241/74F241A



FUNCTION TABLE FOR 74F241/74F241A

INPUTS				OUTPUTS	
$\overline{OEa}$	Ia	OEb	Ib	Ya	Yb
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

Notes to function table for 74F241/74F241A

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	128	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–15	mA
I_{OL}	Low–level output current			64	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.4		V
					I_{OH} = –15mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL} = MAX	±10%V_{CC}			0.50	V
						±5%V_{CC}		0.42	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				–0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current	74F240 all inputs		V_{CC} = MAX, V_I = 0.5V					–1.0	mA
		74F240A all inputs							–100	µA
		74F241 $\overline{OE}$a, OEb							–1.0	mA
		74F241 Ian, Ibn							–1.6	mA
		74F241A all inputs							–40	µA
I_{OZH}	Off–state output current, high–level voltage applied			V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off–state output current, low–level voltage applied			V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short–circuit output current[3]			V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	74F240	I_{CCH}	V_{CC} = MAX				12	18	mA
			I_{CCL}					50	70	mA
			I_{CCZ}					35	45	mA
		74F240A	I_{CCH}					28	37	mA
			I_{CCL}					58	75	mA
			I_{CCZ}					34	50	mA
		74F241	I_{CCH}	V_{CC} = MAX				40	60	mA
			I_{CCL}					60	90	mA
			I_{CCZ}					65	90	mA
		74F241A	I_{CCH}					20	30	mA
			I_{CCL}					49	65	mA
			I_{CCZ}					26	40	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

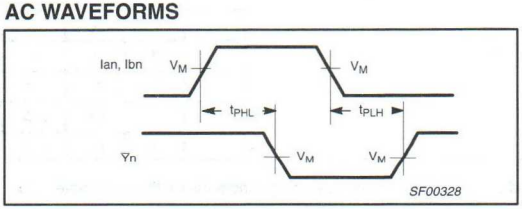
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Ian, Ibn to $\overline{Y}$n	74F240	Waveform 1	3.0 2.0	4.5 3.0	6.5 4.5	3.0 2.0	7.5 5.0	ns
t_{PZH} t_{PZL}	Output enable time to high or low level		Waveform 3 Waveform 4	3.0 4.5	5.0 6.5	7.5 8.5	3.0 4.0	9.0 10.0	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level		Waveform 3 Waveform 4	3.0 3.0	5.5 5.0	7.0 7.0	3.0 3.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay Ian, Ibn to $\overline{Y}$n	74F240A	Waveform 1	2.5 2.0	4.0 3.5	5.5 5.5	2.0 2.0	6.5 6.0	ns
t_{PZH} t_{PZL}	Output enable time to high or low level		Waveform 3 Waveform 4	2.0 3.5	4.0 5.0	6.5 7.5	2.0 3.0	7.0 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level		Waveform 3 Waveform 4	2.0 1.5	3.5 2.5	6.0 5.0	1.5 1.0	6.5 5.5	ns
$t_{sk(0)}$	Output skew[1, 2]		Waveform 5			1.5		2.0	ns
t_{PLH} t_{PHL}	Propagation delay Ian, Ibn to Yn	74F241	Waveform 2	2.5 2.5	4.0 4.0	5.2 5.2	2.5 2.5	6.2 6.5	ns
t_{PZH} t_{PZL}	Output enable time to high or low level		Waveform 3 Waveform 4	2.0 2.0	4.0 5.0	5.7 7.0	2.0 2.0	6.7 8.0	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level		Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	6.0 6.0	2.0 2.0	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay Ian, Ibn to Yn	74F241A	Waveform 2	2.5 2.5	4.5 4.5	5.8 5.8	2.5 2.5	6.5 6.5	ns
t_{PZH} t_{PZL}	Output enable time to high or low level		Waveform 3 Waveform 4	2.5 3.5	4.5 5.0	6.0 7.0	2.0 3.0	6.7 8.0	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level		Waveform 3 Waveform 4	2.0 1.5	4.0 3.5	6.0 5.5	1.5 1.0	6.5 6.0	ns
$t_{sk(0)}$	Output skew[1, 2]		Waveform 5			1.5		2.0	ns

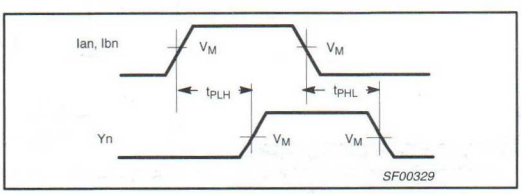
Notes to AC electrical characteristics

1. $| t_{PN}$ actual – t_{PM} actuall for any output compared to any other output where N and M are either LH or HL.
2. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

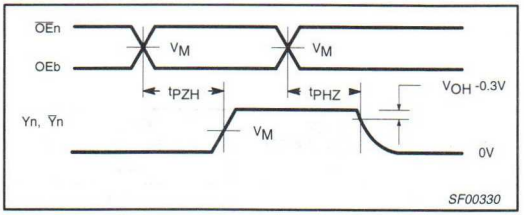
AC WAVEFORMS



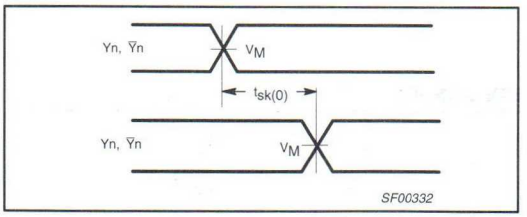
Waveform 1. Propagation delay for inverting outputs



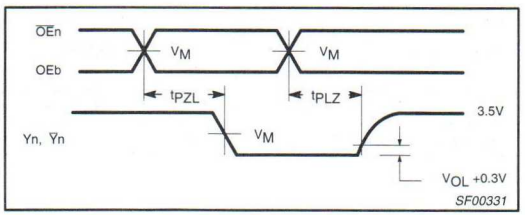
Waveform 2. Propagation delay for non–invertlng outputs



Waveform 3. 3-state output enable time to high level and output disable time from high level



Waveform 5. Output skew

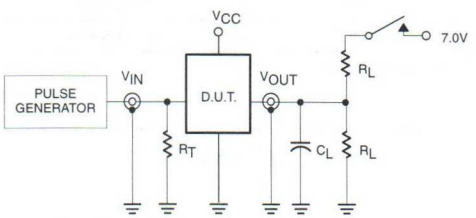


Waveform 4. 3-state output enable time to low level and output disable time from low level

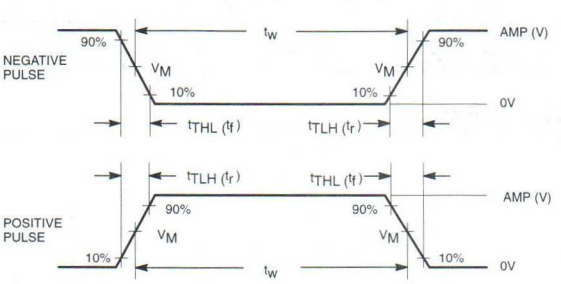
Notes to AC waveforms

1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

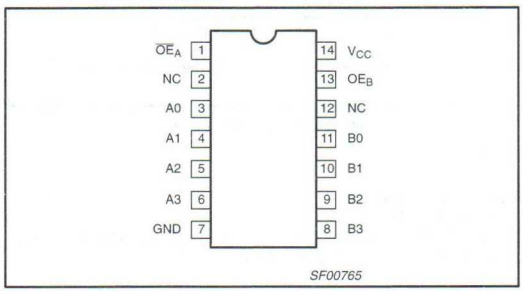
family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

Transceivers | 74F242/74F243

74F242 Quad Transceiver, Inverting (3-State)
74F243 Quad Transceiver (3-State)

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F242	4.3ns	31.2mA
74F243	4.0ns	66mA

ORDERING INFORMATION

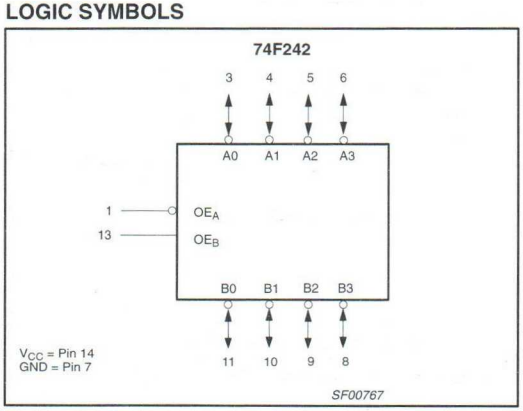
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
14-pin plastic DIP	N74F242N, N74F243N	SOT27-1
14-pin plastic SO	N74F242D, N74F243D	SOT108-1

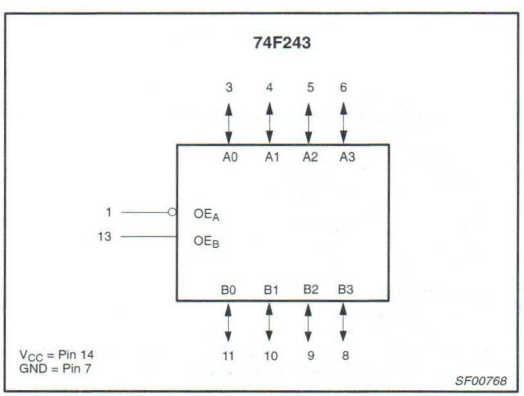
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
An, Bn	Data inputs (74F242)	3.5/1.67	70μA/1.0mA
An, Bn	Data inputs (74F243)	3.5/2.67	70μA/1.6mA
$\overline{OE}_A$	Output enable input (active Low)	1.0/1.67	20μA/1.0mA
OE_B	Output enable input	1.0/1.67	20μA/1.0mA
An, Bn	Data outputs	750/106.7	15mA/64mA

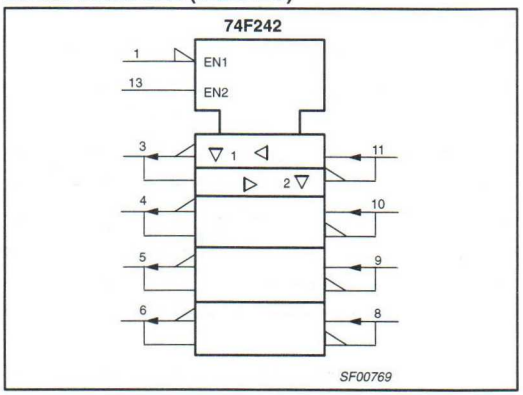
NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

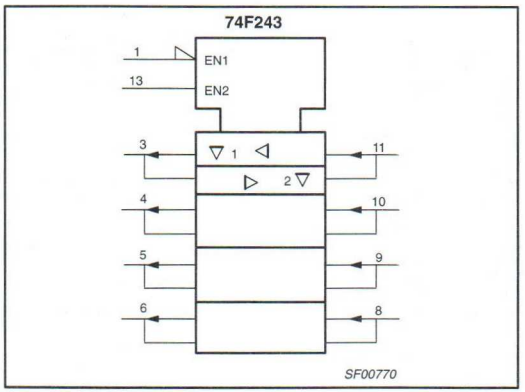
LOGIC SYMBOLS



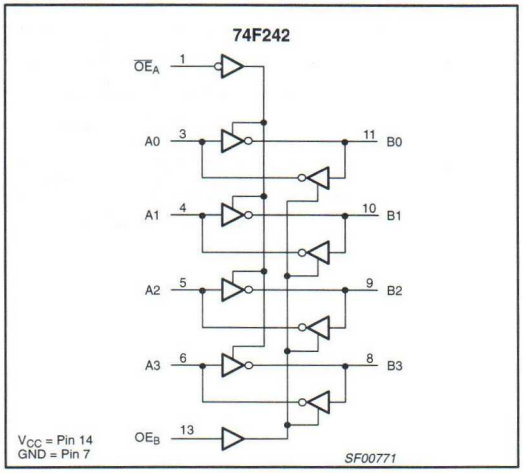


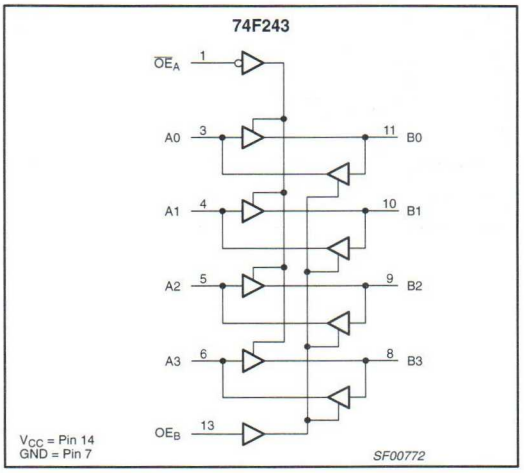
LOGIC SYMBOLS (IEEE/IEC)





LOGIC DIAGRAMS





FUNCTION TABLE, 74F242

INPUTS		OUTPUTS	
$\overline{OE}_A$	OE_B	An	Bn
L	L	INPUT	$B=\overline{A}$
H	L	Z	Z
L	H	a	a
H	H	$A=\overline{B}$	INPUT

H = High voltage level
L = Low voltage level
Z = High impedance "off" state
a = This condition is not allowed due to excessive currents

FUNCTION TABLE, 74F243

INPUTS		OUTPUTS	
$\overline{OE}_A$	OE_B	An	Bn
L	L	INPUT	B=A
H	L	Z	Z
L	H	a	a
H	H	A=B	INPUT

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.3		
				V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = –15mA	±10%V_{CC}	2.0	3.2		V
						±5%V_{CC}	2.0	3.1		
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=MAX	±10%V_{CC}			0.55	V
						±5%V_{CC}		0.42	0.55	
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	A0–A3, B0–B3		V_{CC} = MAX, V_I = 5.5V					1	mA
		$\overline{OE}_A$, OE_B		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current	OE_A, OE_B only		V_{CC} = MAX, VI = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, VI = 0.5V					–1	mA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied			V_{CC} = MAX, V_O = 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied	74F242		V_{CC} = MAX, V_O = 0.5V					–1.0	mA
		74F243							–1.6	
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			–100		–225	mA
I_{CC}	Supply current (total)	74F242	I_{CCH}	V_{CC} = MAX				22	35	mA
			I_{CCL}					40	55	mA
			I_{CCZ}					32	45	mA
		74F243	I_{CCH}	V_{CC} = MAX				64	80	mA
			I_{CCL}					64	90	mA
			I_{CCZ}					71	90	mA

NOTES:

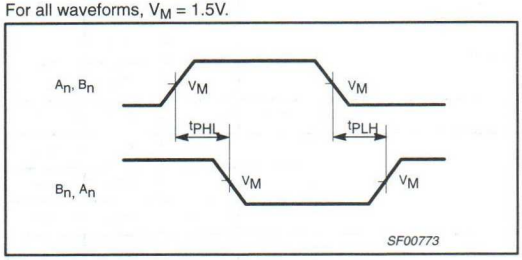
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

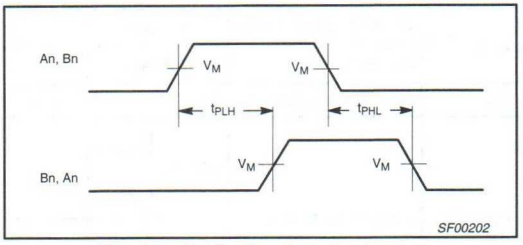
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				V_{CC} = +5V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An, Bn to Bn, An	74F242	Waveform 1	2.5 2.0	3.5 3.0	6.0 4.5	2.5 2.0	7.0 4.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	3.0 3.5	4.0 6.5	7.0 9.0	3.0 3.5	8.0 10.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 3 Waveform 4	3.5 3.5	5.5 6.0	8.5 9.5	3.5 3.5	9.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay An, Bn to Bn, An	74F243	Waveform 2	2.5 2.5	4.0 4.0	5.2 5.2	2.0 2.0	6.2 6.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	2.0 2.0	4.5 5.0	5.7 7.5	2.0 2.0	6.7 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 3 Waveform 4	2.0 2.0	4.0 4.5	6.0 6.0	2.0 2.0	7.0 7.0	ns

AC WAVEFORMS

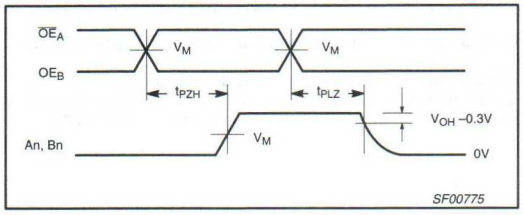
For all waveforms, V_M = 1.5V.



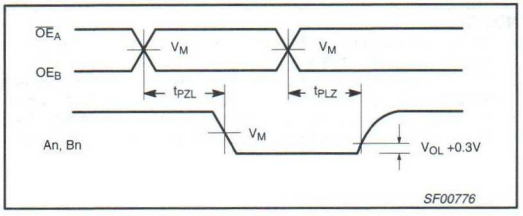
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs

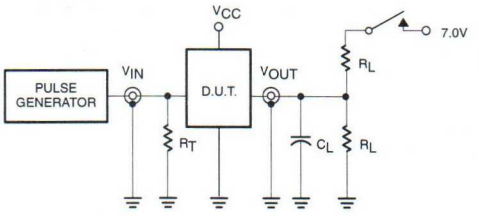


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

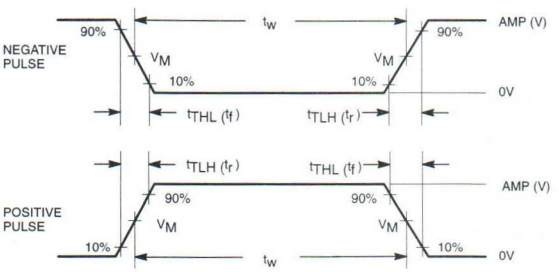


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

Octal buffers (3-State) — 74F244/74F244B

FEATURES

- Octal bus interface
- 3-State output buffer sink 64mA
- 15mA source current
- Guaranteed output skew less than 2.0ns (74F244B)
- Reduced ground bounce (74F244B)
- Reduced I_{CC} (74F244B)
- Reduced loading (74F244B I_{IL} = 40μA)
- Split lead frame offers increased noise immunity (74F244B)
- Industrial temperature range available (-40°C to +85°C) for 74F244
- 74F244 available in SSOP Type II package

DESCRIPTION

The 74F244 is an octal buffer that is ideal for driving bus lines of buffer memory address registers. The outputs are all capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two output enables, $\overline{OE}a$ and $\overline{OE}b$, each controlling four of the 3-State outputs.

The 74F244B is functionally equivalent to the 74F244. It has been designed to reduce effects of ground noise. Other advantages are noted in the features.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F244	4.0ns	53mA
74F244B	4.0ns	33mA

ORDERING INFORMATION

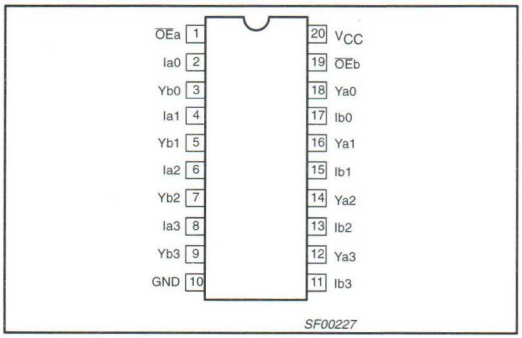
DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = -40°C to +85°C	
20-pin plastic DIP	N74F244N, N74F244BN	I74F244N	SOT146-1
20-pin plastic SOL	N74F244D, N74F244BD	I74F244D	SOT163-1
20-pin plastic SSOP II	N74F244DB		SOT339-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

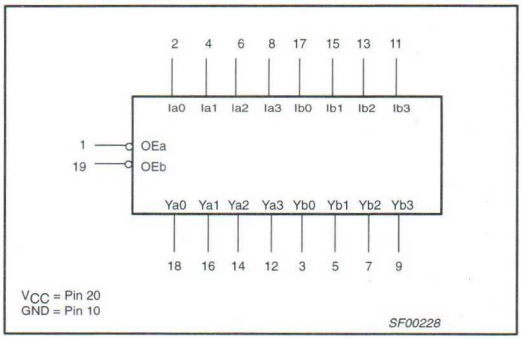
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ian, Ibn	Data inputs (74F244)	1.0/2.67	20μA/1.6mA
	Data inputs (74F244B)	1.0/0.067	20μA/40μA
$\overline{OE}a$, $\overline{OE}b$	Output enable inputs (active low) (74F244)	1.0/1.67	20μA/1.0mA
	Output enable inputs (active low) (74F244B)	1.0/0.067	20μA/40μA
Yan, Ybn	Data outputs	750/106.7	15mA/64mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.

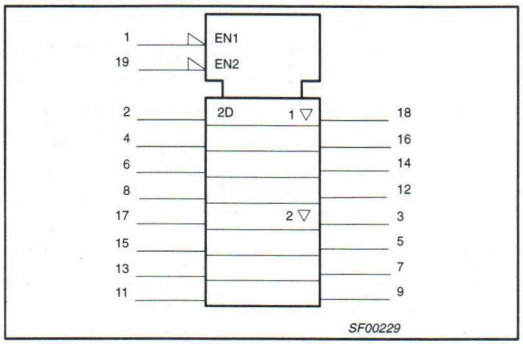
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL

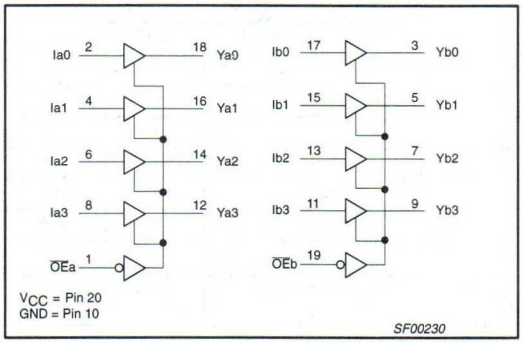


FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE}a$	Ia	$\overline{OE}b$	Ib	Ya	Yb
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	Z	Z

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		-0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		128	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range (74F244 only)	-40 to +85	°C
T_{stg}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IN}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current				–15	mA
i_{ol}	Low-level output current				64	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range (74F244 only)	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -3mA	±10%V_{CC}	2.5			V
						±5%V_{CC}	2.7	3.4		V
					I_{OH} = -15mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = MAX	±10%V_{CC}			0.55	V
				V_{IH} = MIN,		±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	74F244 $\overline{OE}$a, $\overline{OE}$b		V_{CC} = MAX, V_I = 0.5V					-1.0	mA
		74F244 Ian, Ibn							-1.6	mA
		74F244B all inputs							-40	µA
I_{OZH}	Off-state output current, high-level voltage applied			V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, low-level voltage applied			V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	74F244	I_{CCH}	V_{CC} = MAX				40	60	mA
			I_{CCL}					60	90	mA
			I_{CCZ}					60	90	mA
		74F244B	I_{CCH}	V_{CC} = MAX				20	30	mA
			I_{CCL}					50	70	mA
			I_{CCZ}					29	40	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS FOR 74F244

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = -40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Ian, Ibn to Yn	Waveform 1	2.5 2.5	4.0 4.0	5.2 5.2	2.0 2.0	6.2 6.5	1.5 2.0	7.0 7.0	ns
t_{PZH} t_{PZL}	Output enable time to high or low	Waveform 2 Waveform 4	2.0 2.0	4.3 5.0	5.7 7.0	2.0 2.0	6.7 8.0	2.0 2.0	8.0 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low	Waveform 2 Waveform 4	1.5 1.5	2.5 2.5	5.5 5.5	1.0 1.0	6.0 5.5	1.0 1.0	6.0 5.5	ns

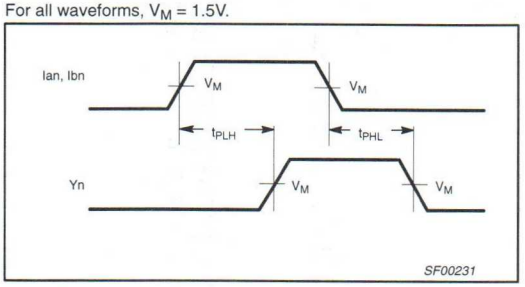
AC ELECTRICAL CHARACTERISTICS FOR 74F244B

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Ian, Ibn to Yn	Waveform 1	2.5 2.5	4.5 4.5	5.7 6.0	2.0 2.5	6.2 6.5	ns
t_{PZH} t_{PZL}	Output enable time to high or low level	Waveform 2 Waveform 4	2.0 3.0	4.0 5.5	6.0 7.5	2.0 3.0	6.5 8.0	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level	Waveform 2 Waveform 4	1.5 1.5	2.5 2.5	5.5 5.5	1.0 1.0	6.0 5.5	ns
$t_{sk(0)}$	Output skew[1, 2]	Waveform 3			1.5		2.0	ns

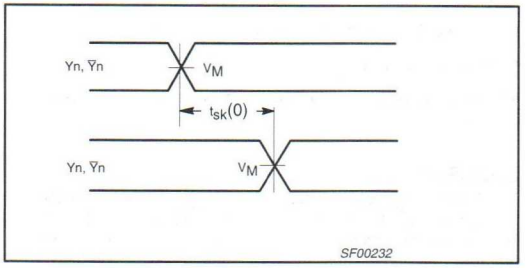
NOTES:
1. t_{PN} actual - t_{PM} actuall for any output compared to any other output where N and M are either LH or HL.
2. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

AC WAVEFORMS

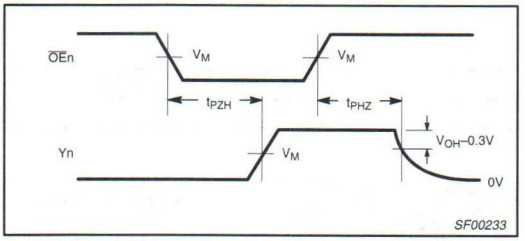
For all waveforms, V_M = 1.5V.



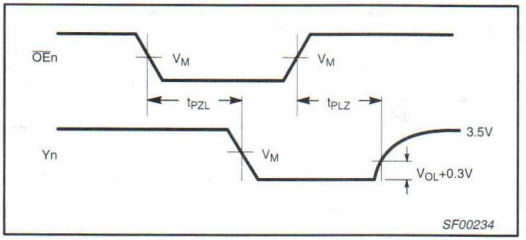
Waveform 1. Propagation Delay for data to outputs



Waveform 3. Output skew



Waveform 2. 3-State output enable time to high level and output disable time from high level

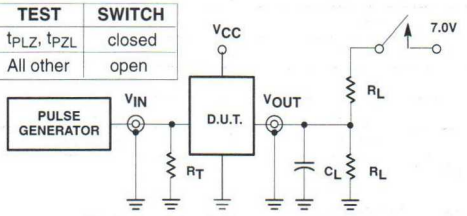


Waveform 4. 3-State output enable time to low level and output disable time from low level

TEST CIRCUIT AND WAVEFORMS

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



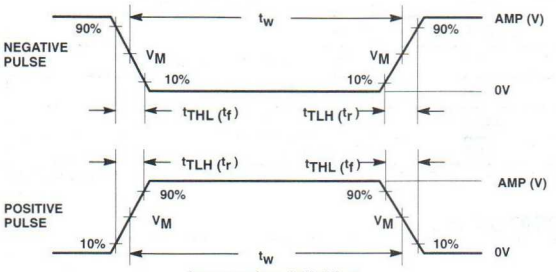
Test circuit for 3-State outputs

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF000235

Octal transceiver (3-State) 74F245

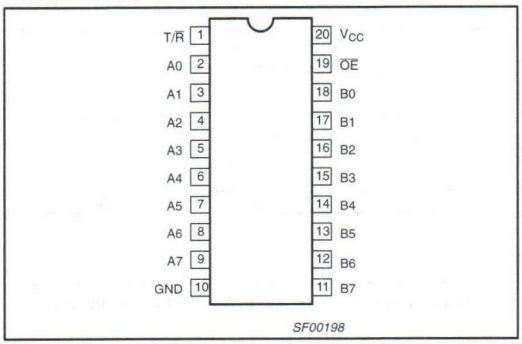
FEATURES

- Octal bidirectional bus interface
- 3-State buffer outputs sink 64mA
- 15mA source current
- Outputs are placed in high impedance state during power-off conditions

DESCRIPTION

The 74F245 is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both transmit and receive directions. The B port outputs are capable of sinking 64mA and sourcing 15mA, producing very good capacitive drive characteristics. The device features an Output Enable ($\overline{OE}$) input for easy cascading and Transmit/Receive ($T/\overline{R}$) input for direction control. The 3-State outputs, B0–B7, have been designed to prevent output bus loading if the power is removed from the device.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F245	4.0ns	70mA

ORDERING INFORMATION

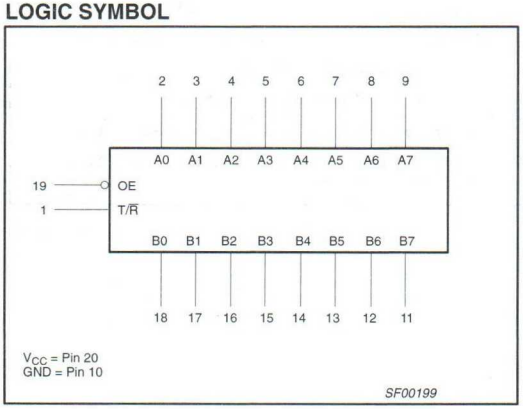
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
20-Pin Plastic DIP	N74F245N	SOT146-1
20-Pin Plastic SO	N74F245D	SOT163-1
20-Pin Plastic SSOP Type II	N74F245DB	SOT339-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

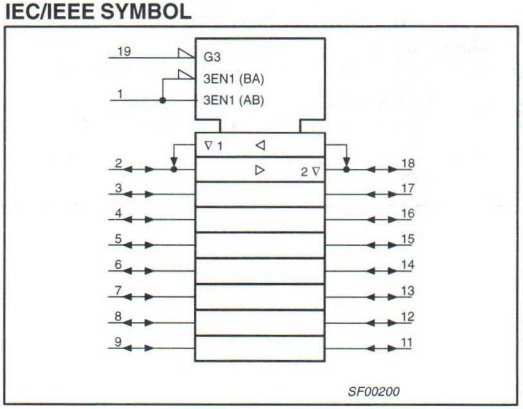
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0–A7, B0–B7	Data inputs	3.5/1.0	70μA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/2.0	20μA/1.2mA
$T/\overline{R}$	Transmit/Receive input	1.0/2.0	20μA/1.2mA
A0–A7	A port outputs	150/40	3.0mA/24mA
B0–B7	B port outputs	750/106.7	15mA/64mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

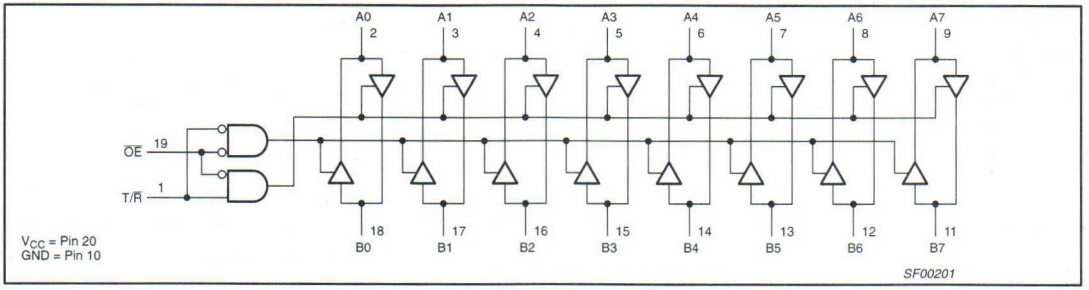
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B data to Bus A
L	H	Bus A data to Bus B
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A0–A7	48	mA
		B0–B7	128	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	A0–A7			−3	mA
		B0–B7			−15	mA
I_{OL}	Low-level output current	A0–A7			24	mA
		B0–B7			64	mA
T_{amb}	Operating free-air temperature range		0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	A0–A7, B0–B7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10% V_{CC}	2.4			V
					±5% V_{CC}	2.7	3.4		V
		B0–B7		I_{OH} = –15mA	±10% V_{CC}	2.0			V
					±5% V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A0–A7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 20mA	±10% V_{CC}		0.30	0.50	V
				I_{OL} = 24mA	±5% V_{CC}		0.35	0.50	V
		B0–B7		I_{OL} = MAX	±10% V_{CC}			0.55	V
V_{OL}	Low-level output voltage	B0–B7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±5% V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	$\overline{OE}$, T/$\overline{R}$	V_{CC} = 5.5V, V_I = 7.0V					100	µA
		A0–A7, B0–B7	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 0.5V					–1.2	mA
I_{IH}+I_{OZH}	Off-state output current High level voltage applied		V_{CC} = MAX, V_O = 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current Low level voltage applied		V_{CC} = MAX, V_O = 0.5V					–600	µA
I_{OS}	Short-circuit output current[3]	A0–A7	V_{CC} = MAX			–60		–150	mA
		B0–B7				–100		–225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				60	87	mA
		I_{CCL}					70	100	mA
		I_{CCZ}					75	110	mA

NOTES:

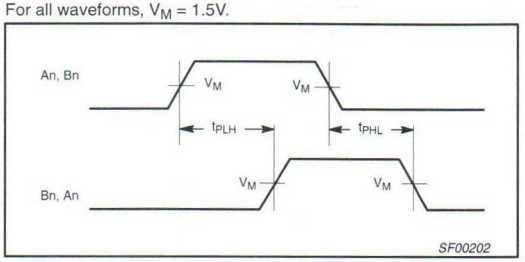
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

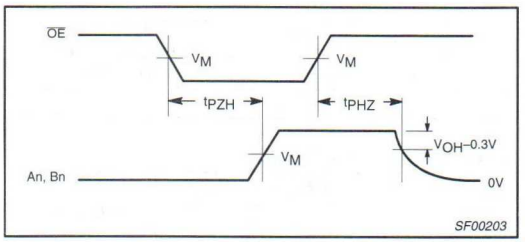
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn, Bn to An	Waveform 1	2.5 2.5	3.5 4.0	6.0 6.0	2.5 2.5	7.0 7.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	2.0 3.5	4.5 5.5	7.0 8.0	2.0 3.5	8.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 2 Waveform 3	2.5 1.0	5.0 3.5	6.5 6.0	2.0 1.0	7.5 7.0	ns

AC WAVEFORMS

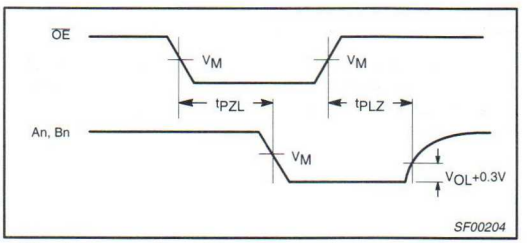
For all waveforms, V_M = 1.5V.



Waveform 1. Propagation Delay for Non-Inverting Output

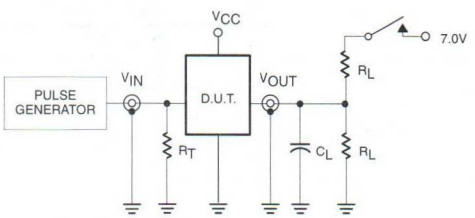


Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level

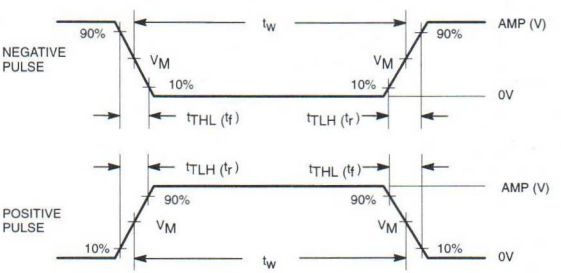


Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

Dual 4-input multiplexer (3-State) 74F253

FEATURES

- 3-State outputs for bus interface and multiplex expansion
- Common select inputs
- Separate Output Enable Inputs

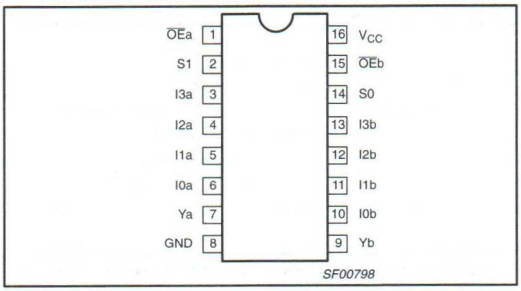
DESCRIPTION

The 74F253 has two identical 4-input multiplexers with 3-State outputs which select two bits from four sources selected by common Select inputs (S0, S1). When the individual Output Enable ($\overline{OE}$a, $\overline{OE}$b) inputs of the 4-input multiplexers are High, the outputs are forced to a high impedance (Hi-Z) state.

The 74F253 is the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two common Select inputs.

To avoid exceeding the maximum current ratings when the outputs of the 3-State devices are tied together, all but one device must be in the high-impedance state. Therefore, only one Output Enable must be active at a time.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F253	7.0ns	12mA

ORDERING INFORMATION

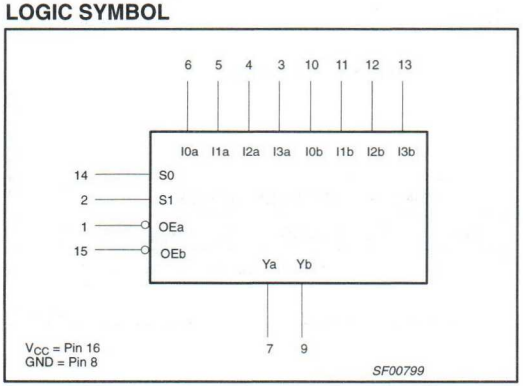
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
16-pin plastic DIP	N74F253N	SOT38-4
16-pin plastic SO	N74F253D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

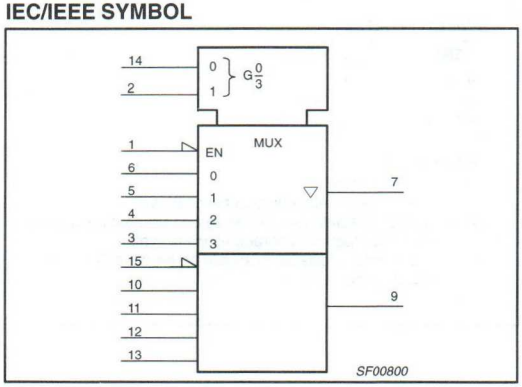
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I0a–I3a	Port A data inputs	1.0/1.0	20µA/0.6mA
I0b–I3b	Port B data inputs	1.0/1.0	20µA/0.6mA
S0, S1	Common Select inputs	1.0/1.0	20µA/0.6mA
$\overline{OE}$a	Port A Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}$b	Port B Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
Ya, Yb	3-State outputs	150/40	3mA/24mA

NOTE:
One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

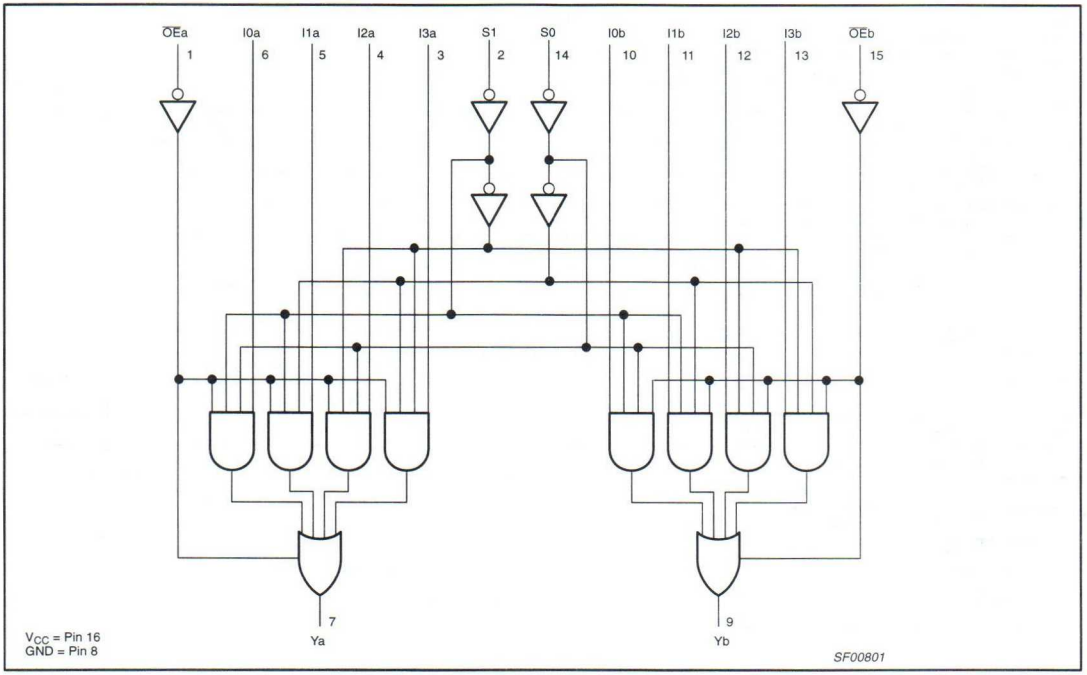
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUT
S0	S1	I0	I1	I2	I3	$\overline{OE}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−3	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OZH}	Off-state output current High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V				–50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	$\overline{OE}$n=GND, Sn=In=4.5V		10	16	mA
		I_{CCL}		$\overline{OE}$n=Sn=In=GND		12	23	mA
		I_{CCZ}		$\overline{OE}$n=4.5V, Sn=In=GND		14	23	mA

NOTES:

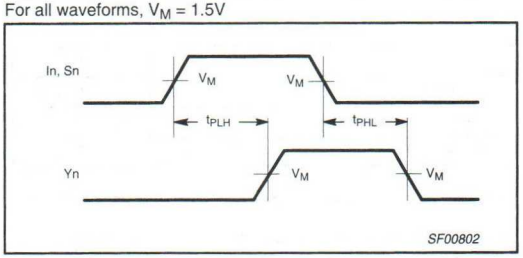
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

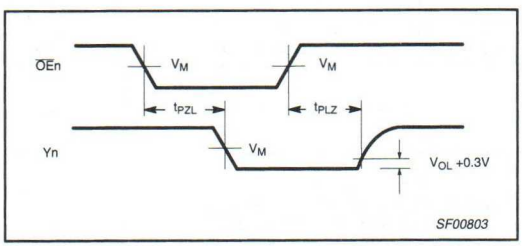
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5V T_{amb} = +25°C C_L = 50pF R_L = 500Ω			V_{CC} = +5V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay In to Yn	Waveform 1	3.0 3.0	4.5 5.0	7.0 7.0	3.0 3.0	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay Sn to Yn	Waveform 1	4.5 5.0	7.5 8.5	10.5 11.0	4.5 4.5	11.0 12.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	3.0 3.0	6.5 6.5	8.0 8.0	3.0 3.0	9.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 2 Waveform 3	2.5 2.0	3.5 3.0	5.0 5.0	2.0 1.5	6.0 6.0	ns

AC WAVEFORMS

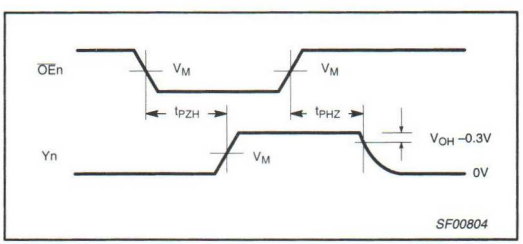
For all waveforms, V_M = 1.5V



Waveform 1. Propagation Deley, Data and Select to Output

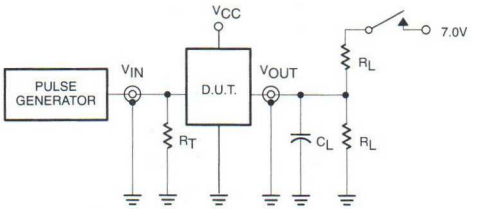


Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

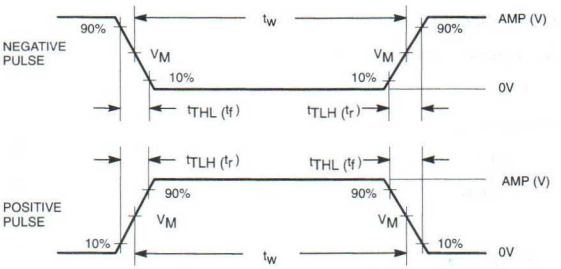


Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

Dual addressable latch | 74F256

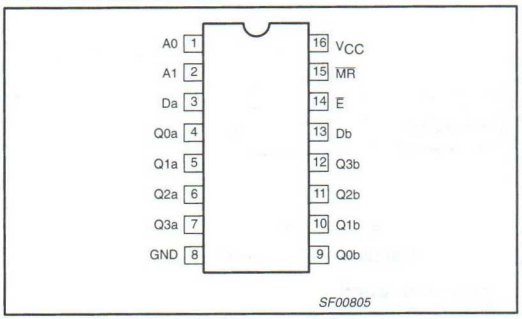
FEATURES

- Combines dual demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common reset input
- Useful as dual 1-of-4 active High decoder

DESCRIPTION

The 74F256 dual addressable latch has four distinct modes of operation which are selectable by controlling the Master Reset ($\overline{MR}$) and Enable ($\overline{E}$) inputs (see Function Table). In the addressable latch mode, data at the Data inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the Data or Address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held High (inactive) while the address lines are changing. In the dual 1-of-4 decoding or demultiplexing mode ($\overline{MR}$=$\overline{E}$=Low), addressed outputs will follow the level of the Data inputs, with all other outputs Low. In the Master Reset mode, all outputs are Low and unaffected by the Address and Data inputs.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F256	7.0ns	28mA

ORDERING INFORMATION

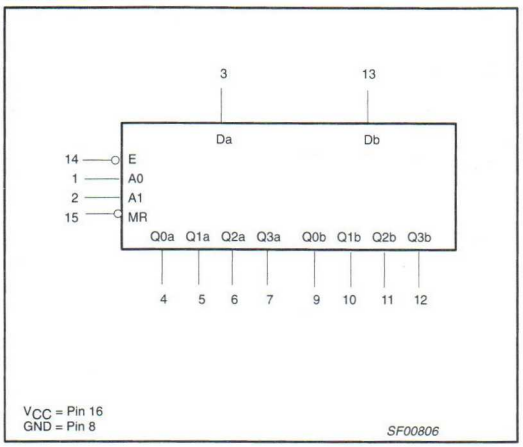
DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
16-pin plastic DIP	N74F256N	SOT38-4
16-pin plastic SO	N74F256D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

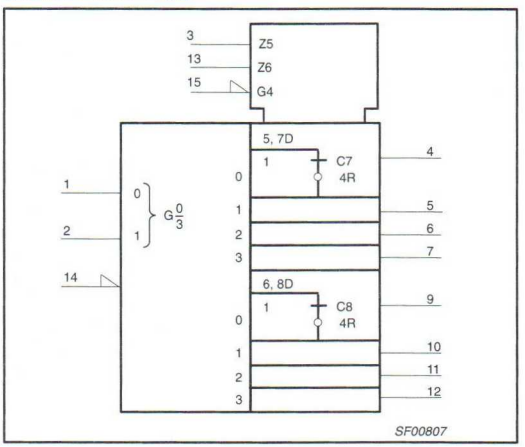
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Da, Db	Port A, port B inputs	1.0/1.0	20µA/0.6mA
A0, A1	Address inputs	1.0/1.0	20µA/0.6mA
$\overline{E}$	Enable (active Low)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset inputs (active Low)	1.0/1.0	20µA/0.6mA
Q0a – Q3a	Port A outputs	50/33	1.0mA/20mA
Q0b – Q3b	Port B outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

LOGIC SYMBOL



IEC/IEEE SYMBOL

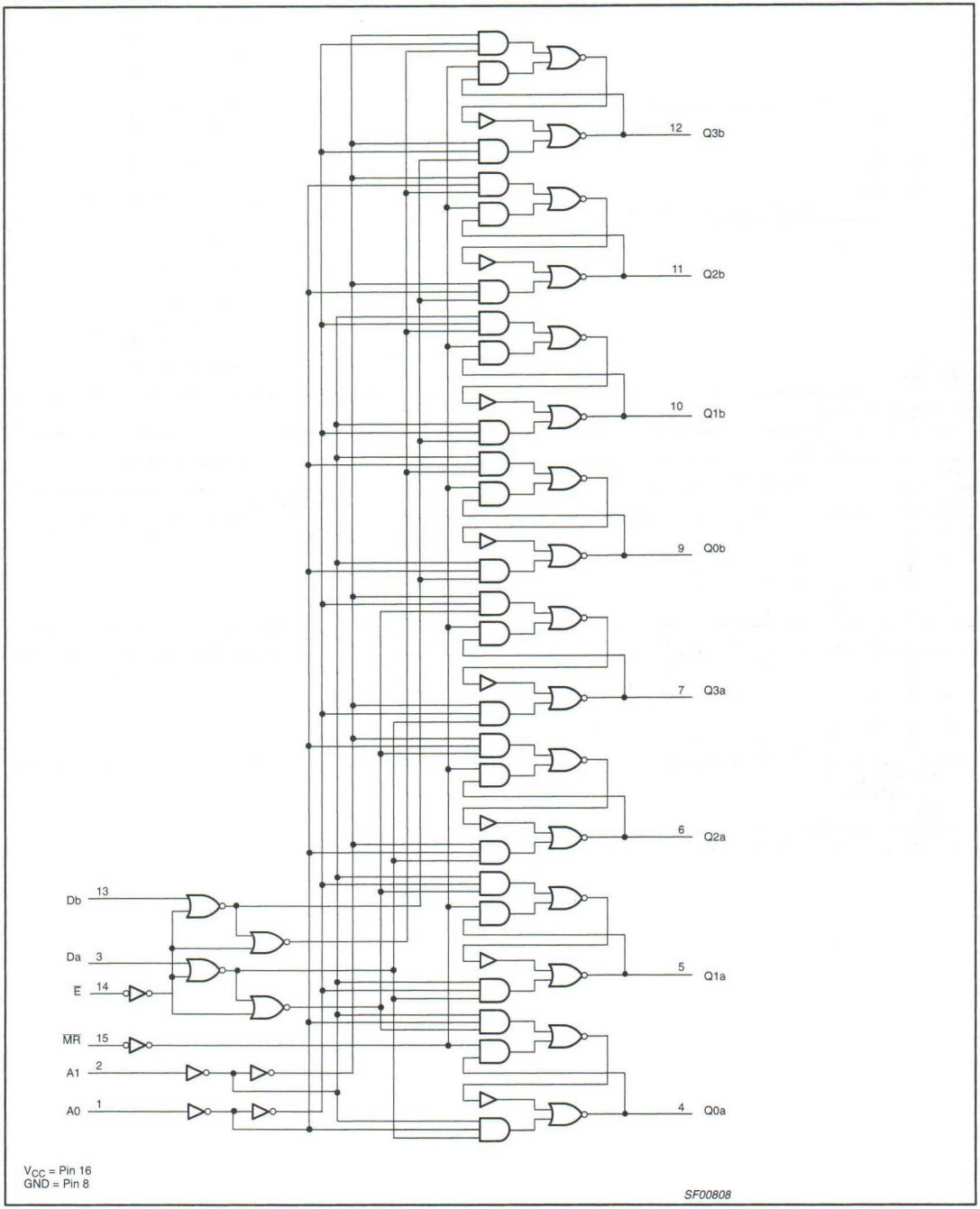


FUNCTION TABLE

INPUTS					OUTPUTS				OPERATING MODE
$\overline{MR}$	$\overline{E}$	D	A0	A1	Q0	Q1	Q2	Q3	
L	H	X	X	X	L	L	L	L	Master Reset
L	L	d	L	L	Q=d	L	L	L	Demultiplex (active-High decoder when D=H)
L	L	d	H	L	L	Q=d	L	L	
L	L	d	L	H	L	L	Q=d	L	
L	L	d	H	H	L	L	L	Q=d	
H	H	X	X	X	q0	q1	q2	q3	Store (do nothing)
H	L	d	L	L	Q=d	q1	q2	q3	Addressable Latch
H	L	d	H	L	q0	Q=d	q2	q3	
H	L	d	L	H	q0	q1	Q=d	q3	
H	L	d	H	H	q0	q1	q2	Q=d	

H = High voltage level
L = Low voltage level
X = Don't care
d = High or Low data one setup time prior to the Low-to-High Enable transition
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			21	42	mA
		I_{CCL}				33	60	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. To reduce the effect of external noise during test.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	Waveform 2	4.0 3.0	7.0 5.0	9.5 7.0	4.0 2.5	10.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Qn	Waveform 1	4.5 3.0	8.0 5.0	10.5 7.0	4.5 3.0	12.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay An to Qn	Waveform 3	5.0 4.5	10.0 8.5	14.0 9.5	5.0 4.0	14.5 10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn	Waveform 4	5.0	7.0	9.0	4.5	10.0	ns

AC SETUP REQUIREMENTS

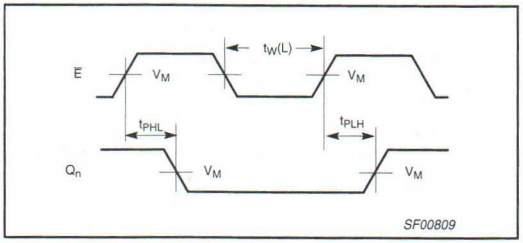
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L= 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low Dn to $\overline{E}$	Waveform 5	3.0 6.5			3.0 7.0		ns
t_h(H) t_h(L)	Hold time, High or Low Dn to $\overline{E}$	Waveform 5	0 0			0 0		ns
t_s(H) t_s(L)	Setup time, High or Low An to $\overline{E}$[1]	Waveform 6	2.0 2.0			2.0 2.0		ns
t_h(H) t_h(L)	Hold time, High or Low An to $\overline{E}$[2]	Waveform 6	0 0			0 0		ns
t_w(L)	$\overline{E}$ Pulse width, Low	Waveform 1	7.5			8.0		ns
t_w(L)	$\overline{MR}$ Pulse width, Low	Waveform 4	3.0			3.0		ns

NOTES:

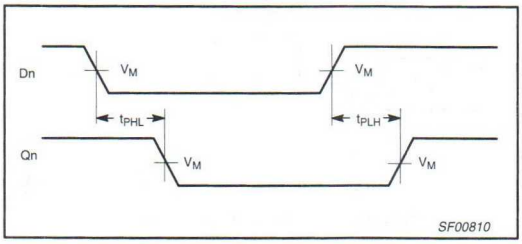
1. The Address to Enable setup time is the time before the High-to-Low Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The Address to Enable hold time is the time before the Low-to-High Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

AC WAVEFORMS

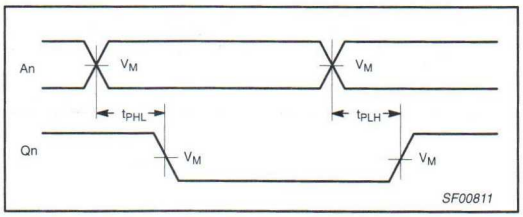
For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.



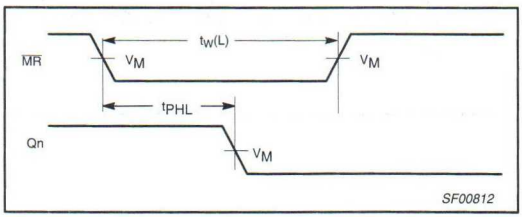
Waveform 1. Propagation Delay, Enable Input to Output, Enable Pulse Width



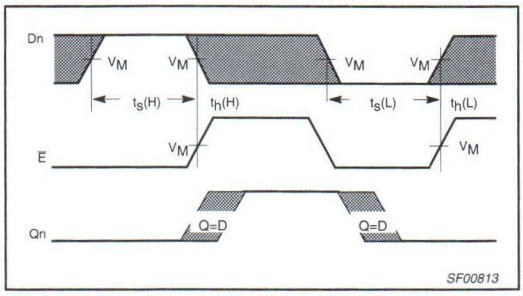
Waveform 2. Propagation Delay, Data to Output



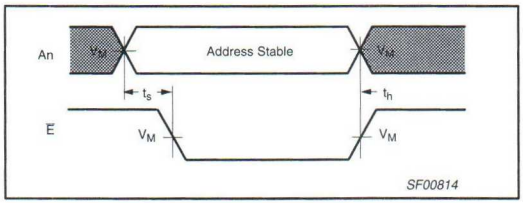
Waveform 3. Propagation Delay Address to Output



Waveform 4. Master Reset Pulse Width and Master Reset to Output Delay

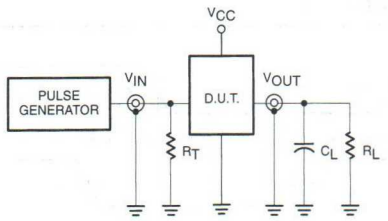


Waveform 5. Data Setup and Hold Times

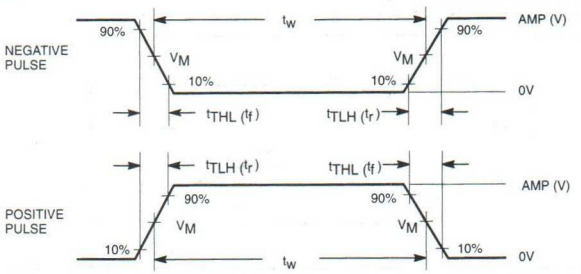


Waveform 6. Address Setup and Hold Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Quad 2-line to 1-line selector/multiplexer, non-inverting (3-State)

74F257A

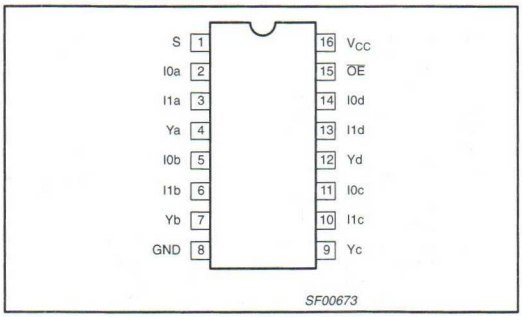
FEATURES

- Industrial range available (–40°C to +85°C)
- Multifunction capability
- Non-inverting data path
- 3-State outputs
- See 74F258A for inverting version

DESCRIPTION

The 74F257A has four identical 2-input multiplexers with 3-State outputs which select 4 bits of data from two sources uncer control of a common Select (S) input. The I0a inputs are selected when the common Select input is Low and the I1n inputs are selected when the common Select input is High. Data appears at the outputs in true non-inverted form from the selected inputs. The 74F257A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the common Slect input. Outputs are forced to a high impedance "off" state when the Output Enable ($\overline{OE}$) is High. All but one device must be in high impedance state to avoid currents that would exceed the maximum rating if the outputs were tied together. Design of the Output Enable signals must ensure that there is no overlap when outputs of 3-state devices were tied together.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F257A	4.3ns	12mA

ORDERING INFORMATION

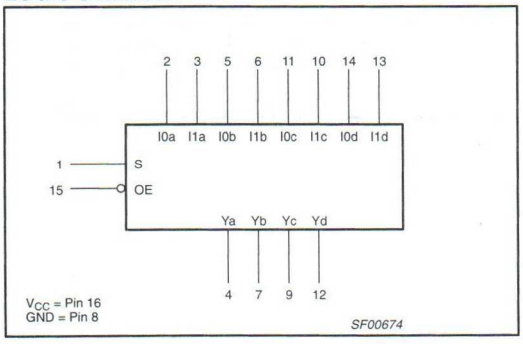
DESCRIPTION	ORDER CODE		DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
16-pin plastic DIP	N74F257AN	I74F257AN	SOT38-4
16-pin plastic SO	N74F257AD	I74F257AD	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

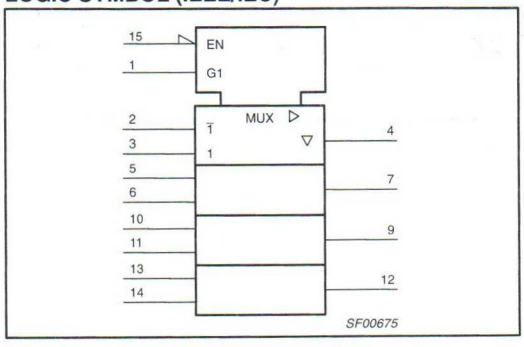
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I0n, I1n	Data inputs	1.0/1.0	20µA/0.6mA
S	Common Select input	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
Ya – Yd	Data outputs	150/33	3.0mA/20mA

NOTE:
One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

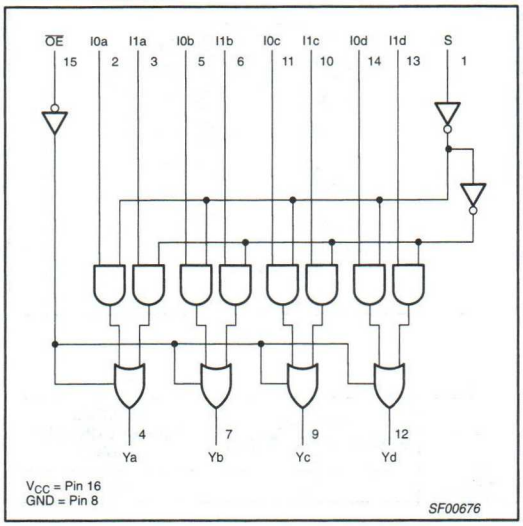
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM

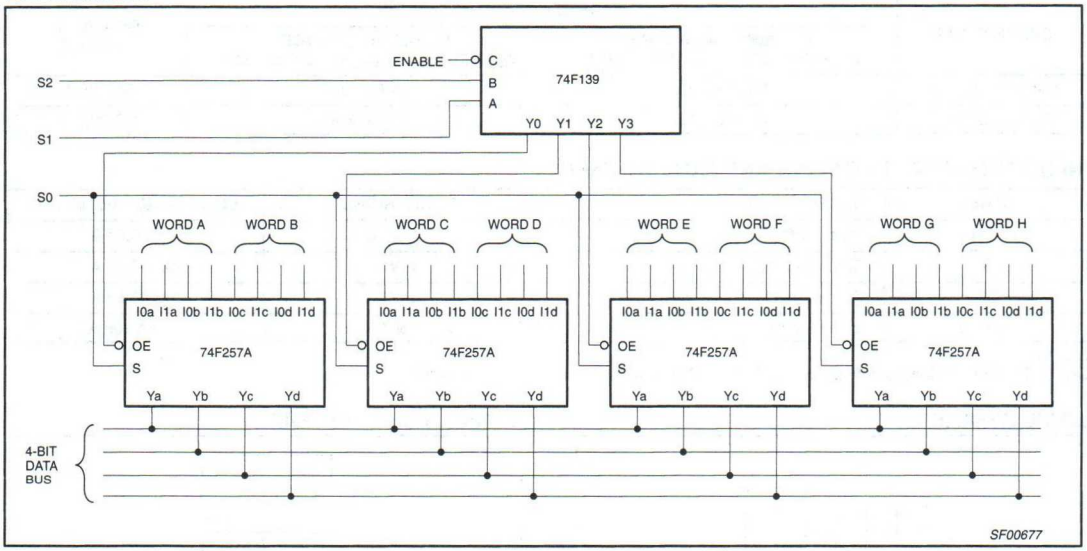


FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	I0	I1	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

APPLICATION



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state		48	mA
T_{amb}	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current				–3	mA
I_{OL}	Low-level output current				24	mA
T_{amb}	Operating free-air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
			±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OZH}	Off state output current, High-level voltage applied	V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off state output current, Low-level voltage applied	V_{CC} = MAX, V_O = 0.5V				–50	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		-60		–150	mA
I_{CC}	Supply current[4] (total)		I_{CCH}		9.0	15.0	mA
		V_{CC} = MAX	I_{CCL}		14.5	22.0	mA
			I_{CCZ}		15.0	23.0	mA

NOTES:

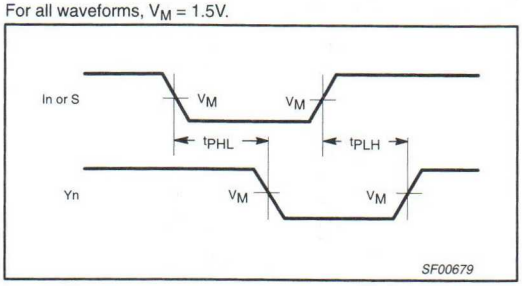
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with all outputs open and inputs grounded.

AC ELECTRICAL CHARACTERISTICS

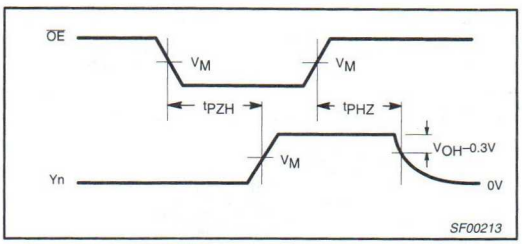
SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay In to Yn	Waveform 1	3.0 2.0	4.5 3.5	6.0 5.0	3.0 2.0	7.0 6.0	3.0 2.0	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay S to Yn	Waveform 1	5.0 4.0	7.5 5.5	9.5 7.0	5.0 4.0	10.5 8.0	5.0 4.0	10.5 8.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	4.5 4.5	6.5 6.0	7.5 7.5	4.5 4.5	8.5 8.5	4.5 4.5	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 2 Waveform 3	2.0 2.0	4.0 3.5	5.5 5.5	2.0 2.0	6.0 6.0	2.0 2.0	6.0 6.0	ns

AC WAVEFORMS

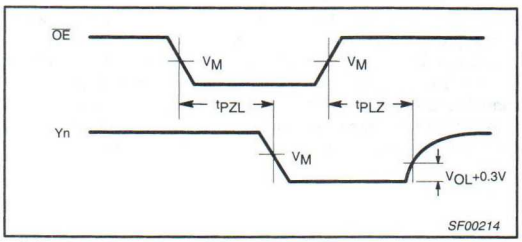
For all waveforms, V_M = 1.5V.



Waveform 1. Propagation Delay, Data and Select to Output

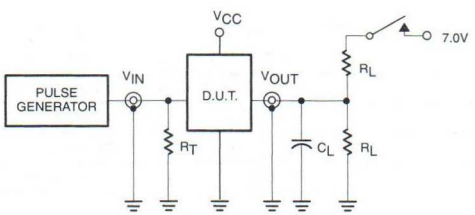


Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level

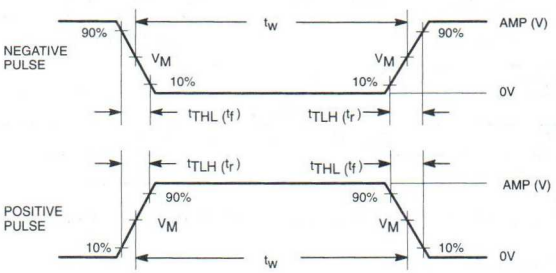


Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

Quad 2-line to 1-line selector/multiplexer, inverting (3-State)

74F258A

FEATURES

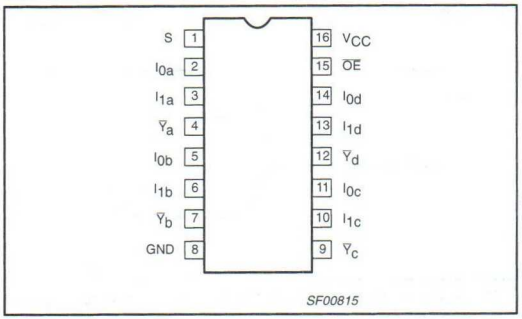
- Multifunction capability
- Non-inverting data path
- 3-State outputs
- See 74F257A for non-inverting version

DESCRIPTION

The 74F258A has four identical 2-input multiplexers with 3-State outputs which select 4 bits of data from two sources under control of a common Select (S) input. The I_{0n} inputs are selected when the Select input is Low and the I_{1n} inputs are selected when the Select input is High. Data appears at the outputs in inverted form.

The 74F258A is the logical implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic level supplied to the Select input. Outputs are forced to a High impedance "off" state when the Output Enable input ($\overline{OE}$) is High. All but one device must be in the High impedance state to avoid currents that would exceed the maximum ratings if outputs are tied together. Design of the output signals must ensure that there is no overlap when outputs of 3-State devices are tied together.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F258A	3.5ns	14mA

ORDERING INFORMATION

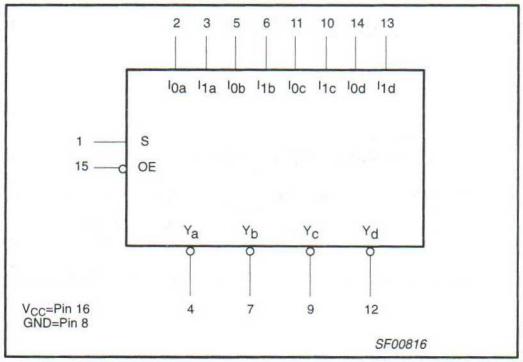
DESCRIPTION	ORDER CODE	PKG. DWG. #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
16-pin plastic DIP	N74F258AN	SOT38-4
16-pin plastic SO	N74F258AD	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

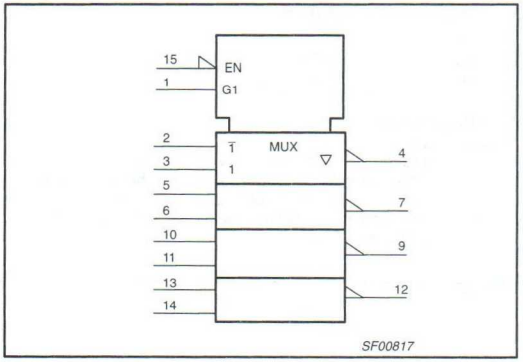
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0n}, I_{1n}	Data inputs	1.0/1.0	20µA/0.6mA
S	Common select input	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{Y}_a$ - $\overline{Y}_d$	Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

LOGIC SYMBOL



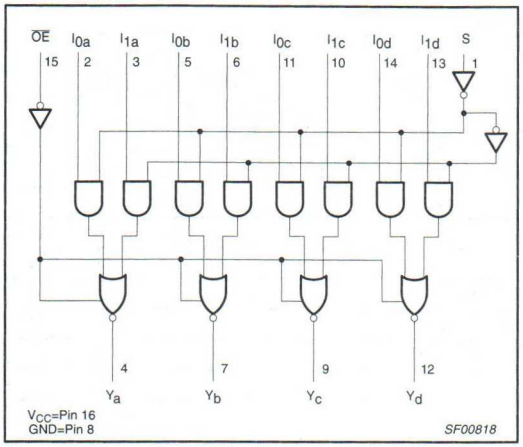
LOGIC SYMBOL (IEEE/IEC)



Quad 2-line to 1-line selector/multiplexer, inverting (3-State)

74F258A

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–3	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}	2.4			V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, High-level voltage applied	V_{CC} = MAX, V_O = 0.5V				–50	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX, I_{1n}=4.5V, $\overline{OE}$=I_{0n}=S=GND		8.5	11.5	mA
		I_{CCL}	V_{CC} = MAX, I_{1n}=S=4.5V, $\overline{OE}$=I_{0n}=GND		17	23	mA
		I_{CCZ}	V_{CC} = MAX, I_{1n}=$\overline{OE}$=4.5V, I_{0n}=S=GND		16	22	mA

NOTES:

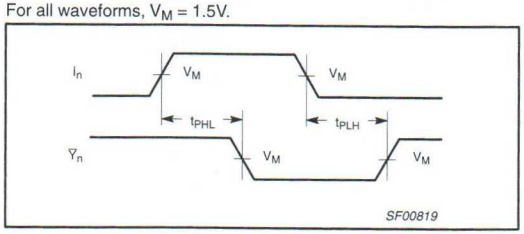
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

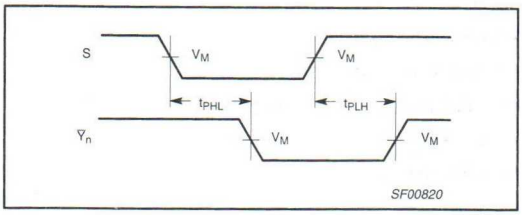
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb}= +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = –55°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$	Waveform 1	3.0 1.0	4.5 2.5	6.0 4.0	2.5 1.0	7.0 4.5	ns ns
t_{PLH} t_{PHL}	Propagation delay S to $\overline{Y}_n$	Waveform 2	3.5 2.5	6.5 6.0	8.0 8.0	3.5 2.5	9.0 9.0	ns ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	Waveform 3 Waveform 4	4.0 4.0	6.0 5.5	7.5 7.5	3.5 3.5	8.5 8.5	ns ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	Waveform 3 Waveform 4	2.0 2.0	3.5 3.5	5.5 5.5	2.0 2.0	6.5 6.0	ns ns

AC WAVEFORMS

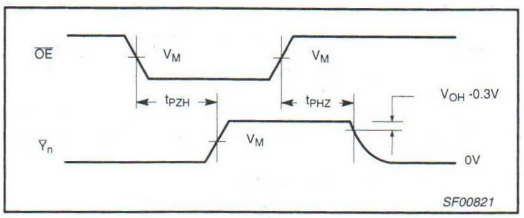
For all waveforms, V_M = 1.5V.



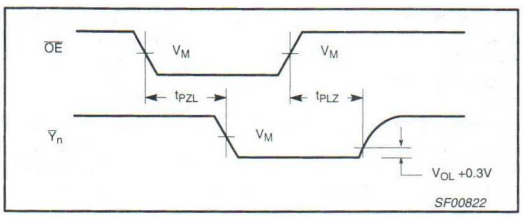
Waveform 1. Propagation Delay Data and Select to Output



Waveform 2. Propagation Delay Select to Output

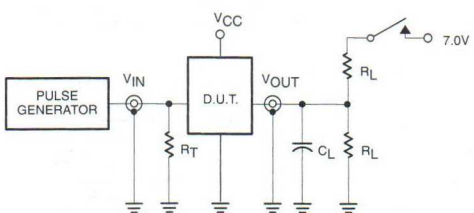


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

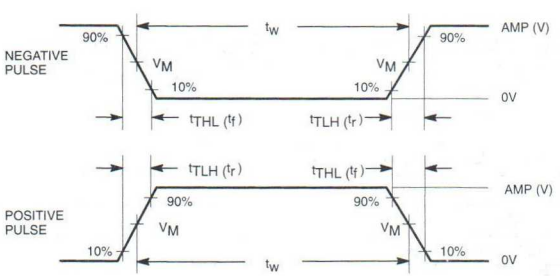


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

Latch | 74F259

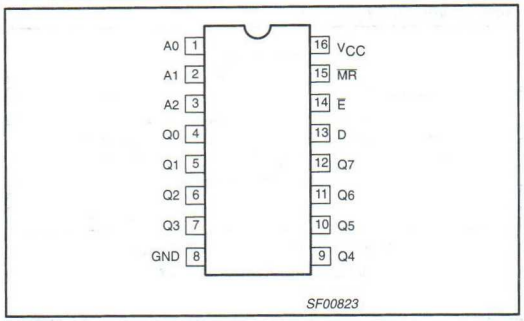
FEATURES

- Combines demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common reset input
- Useful as 1-of-8 active-High decoder

DESCRIPTION

The 74F259 addressable latch has four distinct modes of operation which are selectable by controlling the Master Reset ($\overline{MR}$) and Enable ($\overline{E}$) inputs (see Function Table). In the addressable latch mode, data at the Data inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states. In the store mode, all latches remain in their previous states and are unaffected by the Data or Address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held High (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode ($\overline{MR}$=$\overline{E}$=Low), addressed outputs will follow the level of the Data input, with all other outputs Low. In the Master Reset mode, all outputs are Low and unaffected by the Address and Data inputs.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F259	7.5ns	31mA

ORDERING INFORMATION

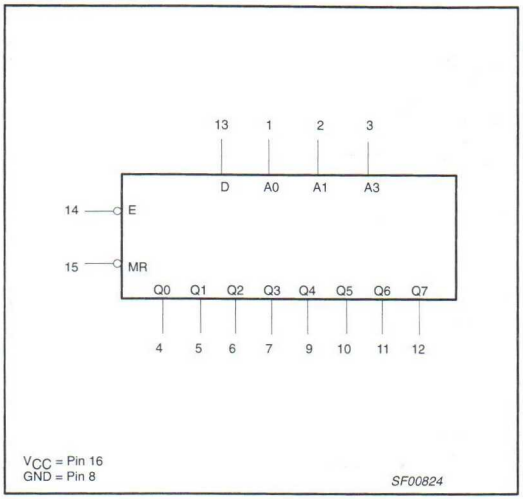
DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
16-pin plastic DIP	N74F259N	SOT38-4
16-pin plastic SO	N74F259D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

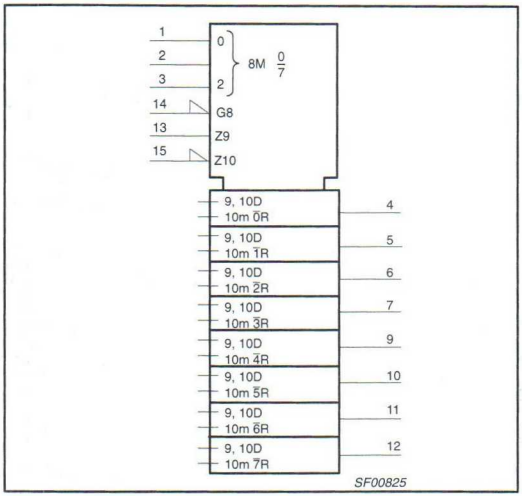
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D	Data input	1.0/1.0	20µA/0.6mA
A0, A1, A2	Address inputs	1.0/1.0	20µA/0.6mA
$\overline{E}$	Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset inputs (active Low)	1.0/1.0	20µA/0.6mA
Q0 – Q7	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

LOGIC SYMBOL



IEC/IEEE SYMBOL

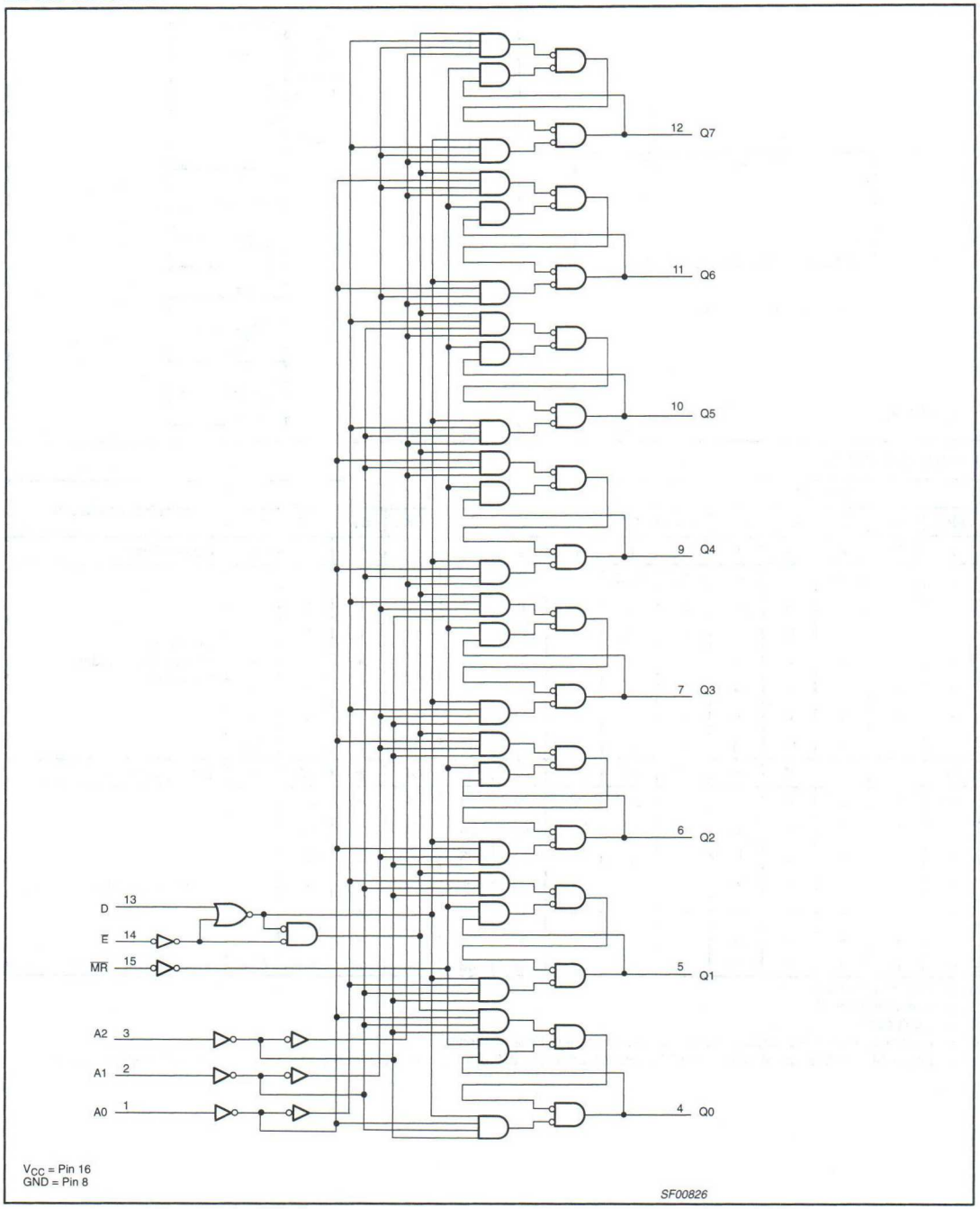


FUNCTION TABLE

INPUTS						OUTPUTS								OPERATING MODE
$\overline{MR}$	$\overline{E}$	D	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	
L	H	X	X	X	L	L	L	L	L	L	L	L	L	Master Reset
L	L	d	L	L	L	Q=d	L	L	L	L	L	L	L	Demultiplex (active-High decoder when D=H)
L	L	d	H	L	L	L	Q=d	L	L	L	L	L	L	
L	L	d	L	H	L	L	L	Q=d	L	L	L	L	L	
•	•	•	•	•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	•	•	•	•	
L	L	d	H	H	H	L	L	L	L	L	L	L	Q=d	
H	H	X	X	X	X	q0	q1	q2	q3	q4	q5	q6	q7	Store (do nothing)
H	L	d	L	L	L	Q=d	q1	q2	q3	q4	q5	q6	q7	Addressable Latch
H	L	d	H	L	L	q0	Q=d	q2	q3	q4	q5	q6	q7	
H	L	d	L	H	L	q0	q1	Q=d	q3	q4	q5	q6	q7	
•	•	•	•	•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	•	•	•	•	
H	L	d	H	H	H	q0	q1	q2	q3	q4	q5	q6	Q=d	

H = High voltage level
L = Low voltage level
X = Don't care
d = High or Low data one setup time prior to the Low-to-High Enable transition
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			24	46	mA
		I_{CCL}				37	75	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. To reduce the effect of external noise during test.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay D to Qn	Waveform 1	4.0 3.0	7.0 5.0	9.0 7.0	4.0 2.5	10.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Qn	Waveform 1	4.5 3.0	8.0 5.0	10.5 7.0	4.5 3.0	12.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay An to Qn	Waveform 3	5.0 4.0	10.0 8.5	14.0 9.5	5.0 4.0	14.5 10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn	Waveform 4	5.0	7.0	9.0	4.5	10.0	ns

AC SETUP REQUIREMENTS

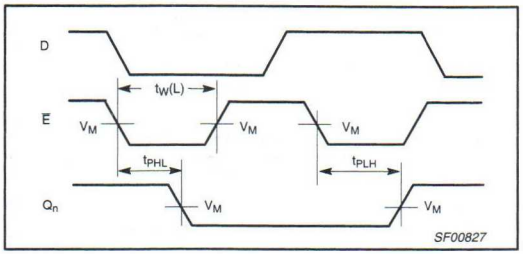
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L= 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low D to $\overline{E}$	Waveform 5	3.0 6.5			3.0 7.0		ns
t_h(H) t_h(L)	Hold time, High or Low D to $\overline{E}$	Waveform 5	0 0			0 0		ns
t_s(H) t_s(L)	Setup time, High or Low An to $\overline{E}$[1]	Waveform 6	2.0 2.0			2.0 2.0		ns
t_h(H) t_h(L)	Hold time, High or Low An to $\overline{E}$[2]	Waveform 6	0 0			0 0		ns
t_w(L)	$\overline{E}$ Pulse width, Low	Waveform 1	7.5			8.0		ns
t_w(L)	$\overline{MR}$ Pulse width, Low	Waveform 4	3.0			3.0		ns

NOTES:

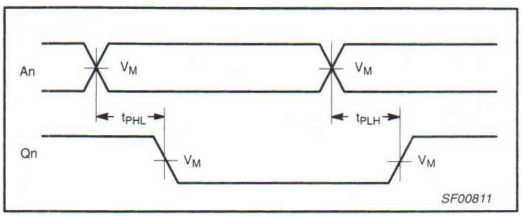
1. The Address to Enable setup time is the time before the High-to-Low Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The Address to Enable hold time is the time before the Low-to-High Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

AC WAVEFORMS

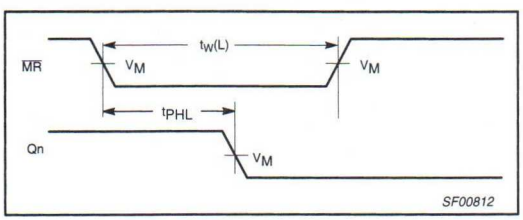
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



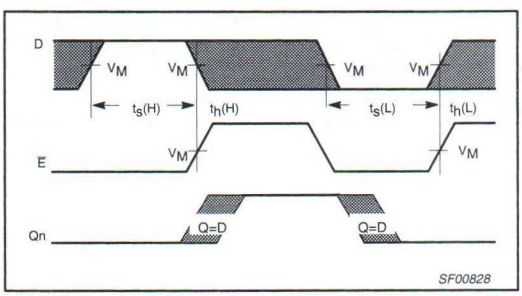
Waveform 1. Propagation Delay, Enable Input to Output, Enable Pulse Width



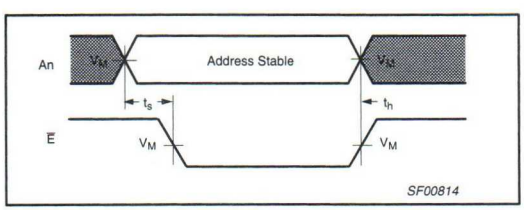
Waveform 2. Propagation Delay Address to Output



Waveform 3. Master Reset Pulse Width and Master Reset to Output Delay

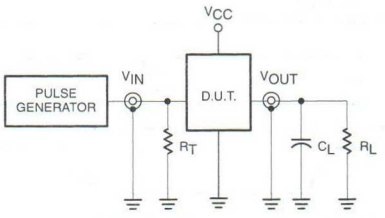


Waveform 4. Data Setup and Hold Times

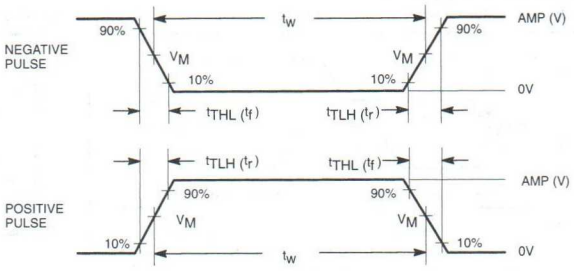


Waveform 5. Address Setup and Hold Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

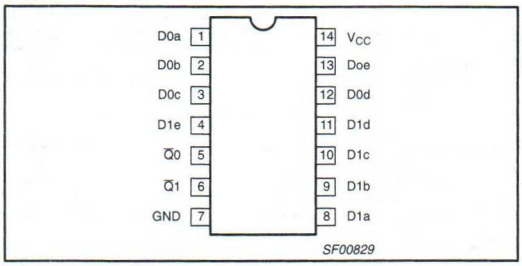
Dual 5-input NOR gate — 74F260

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F260	3.5ns	6mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
14-pin plastic DIP	N74F260N	SOT27-1
14-pin plastic SO	N74F260D	SOT108-1

PIN CONFIGURATION

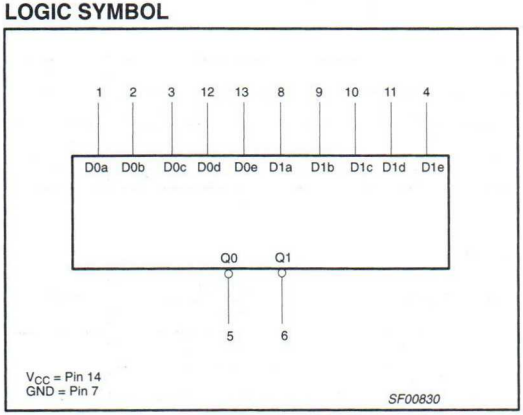


INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

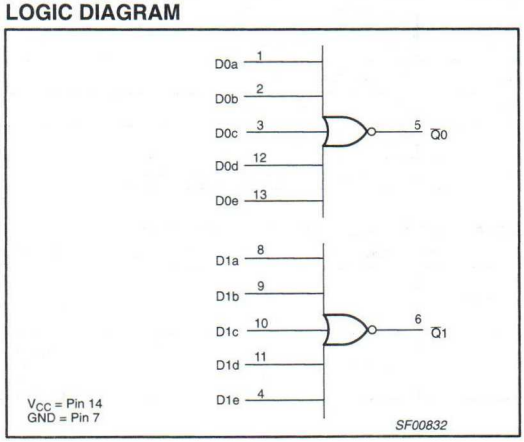
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb, Dnc, Dnd, Dne	Data inputs	1.0/1.0	20µA/0.6mA
Q̄0, Q̄1	Data outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

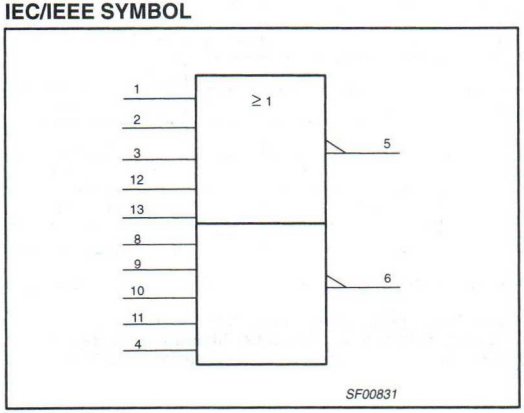
LOGIC SYMBOL



LOGIC DIAGRAM



IEC/IEEE SYMBOL



FUNCTION TABLE

INPUTS					OUTPUT
Dna	Dnb	Dnc	Dnd	Dne	Q̄n
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L
L	L	L	L	L	H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN}=GND		4.6	6.5	mA
		I_{CCL}		V_{IN}=4.5V		7.3	9.5	mA

NOTES:

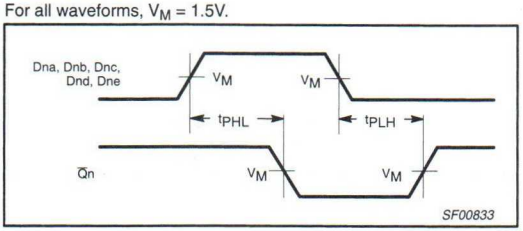
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb, Dnc, Dnd, Dne to $\overline{Q}$n	Waveform 1	2.5 1.5	4.0 2.5	5.5 4.0	2.0 1.0	6.5 4.5	ns

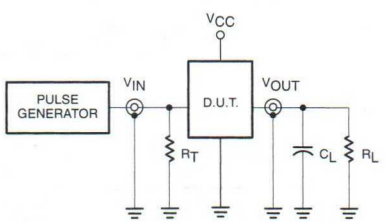
AC WAVEFORM

For all waveforms, V_M = 1.5V.

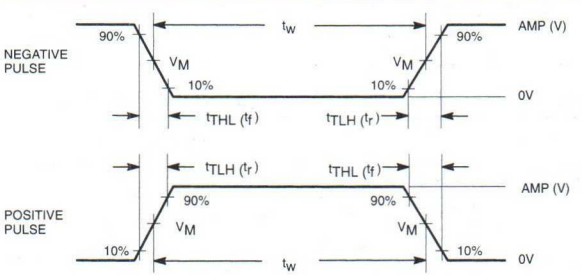


Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

8–bit bidirectional binary counter 74F269

FEATURES

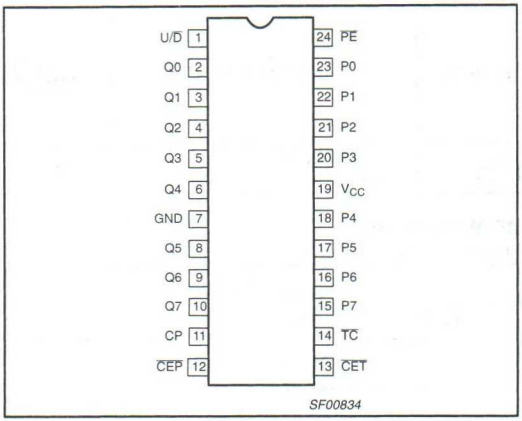
- Synchronous counting and loading
- Built-in look-ahead carry capability
- Count frequency 115MHz typ
- Supply current 95mA typ

DESCRIPTION

The 74F269 is a fully synchronous 8-stage Up/Down Counter featuring a preset capability for programmable operation, carry look-ahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F269	115MHz	95mA

PIN CONFIGURATION



ORDERING INFORMATION

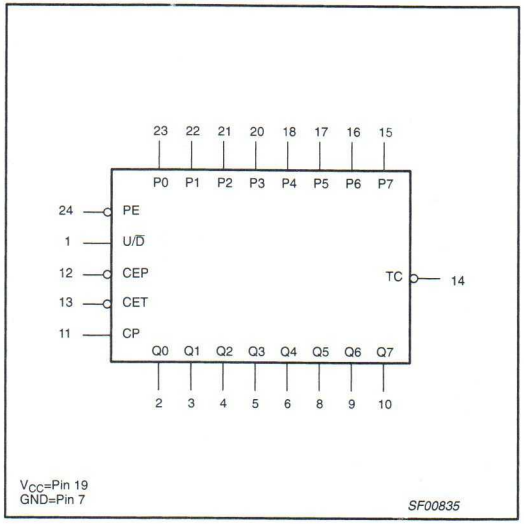
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
24-Pin Plastic Slim DIP (300mil)	N74F269N	SOT222-1
24-Pin Plastic SOL	N74F269D	SOT137-1
24-Pin Plastic SSOP type II	N74F269DB	SOT340-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

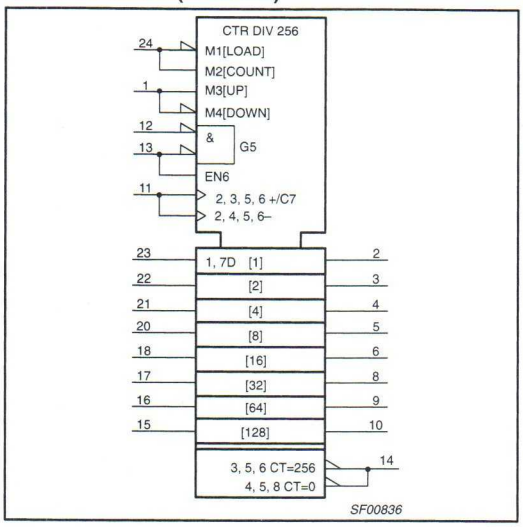
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
P0 - P7	Parallel Data inputs	1.0/1.0	20µA/0.6mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/1.0	20µA/0.6mA
U/$\overline{D}$	Up/Down count control input	1.0/1.0	20µA/0.6mA
$\overline{CEP}$	Count Enable Parallel input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock input	1.0/1.0	20µA/0.6mA
$\overline{TC}$	Terminal Count output (active Low)	50/33	1.0mA/20mA
Q0 - Q7	Flip-flop outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



APPLICATION

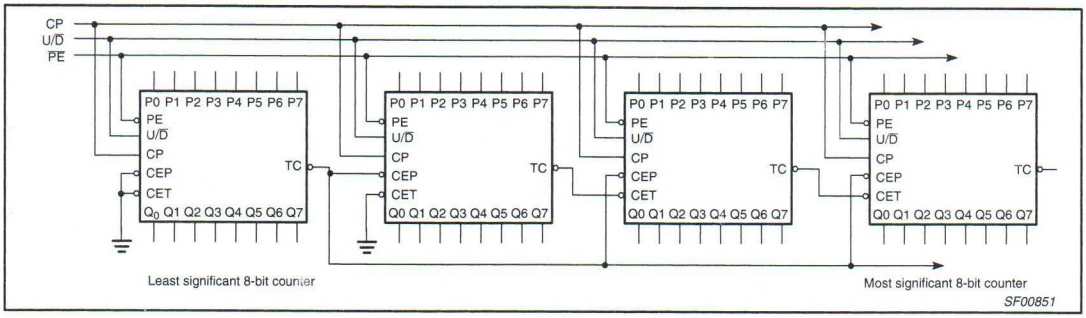


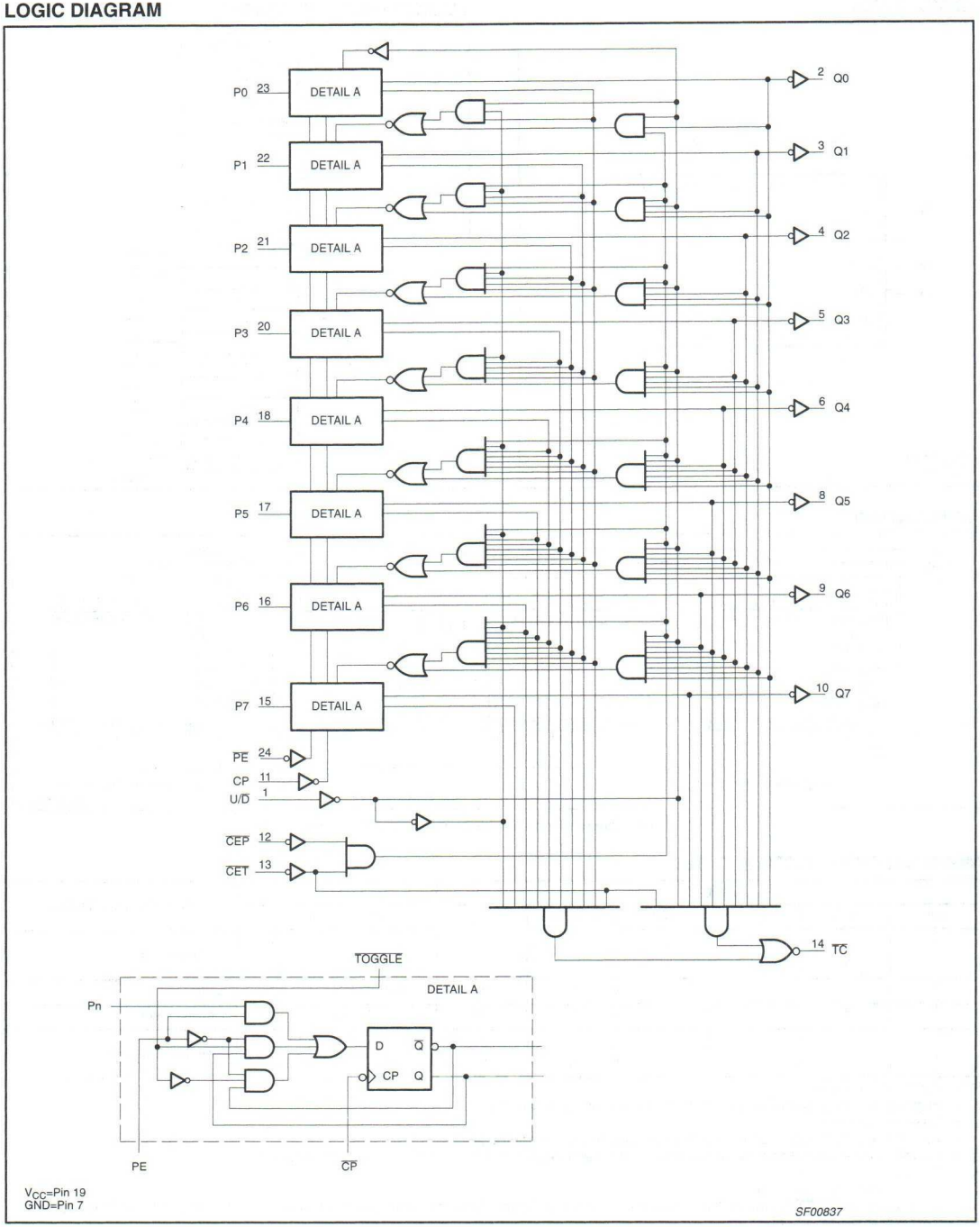
Figure 1. Synchronous Multistage Counting Scheme

MODE SELECT FUNCTION TABLE

INPUTS						OUTPUTS		OPERATING MODE
CP	U/D	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	P_n	Q_n	$\overline{TC}$	
↑	X	X	X	l	l	L	(a)	Parallel load
↑	X	X	X	l	h	H	(a)	
↑	h	l	l	h	X	Count Up	(a)	Count Up
↑	l	l	l	h	X	Count Down	(a)	Count Down
↑	X	h	l	h	X	q_n	(a)	Hold (do nothing)
↑	X	X	h	h	X	q_n	H	

H = High voltage level
h = High voltage level one setup prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to the Low-to-High clock transition
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
(a) = $\overline{TC}$ is Low when $\overline{CET}$ is Low and the counter is at Terminal Count. Terminal Count Up is with all Q_n outputs High and Terminal Count Down is with all Qn outputs Low.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	$\overline{PE}$=$\overline{CET}$=$\overline{CEP}$=U/$\overline{D}$=GND, Pn=4.5V, CP=↑		93	120	mA
		I_{CCL}		$\overline{PE}$=$\overline{CET}$=$\overline{CEP}$=U/$\overline{D}$=GND, Pn=GND, CP=↑		98	125	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

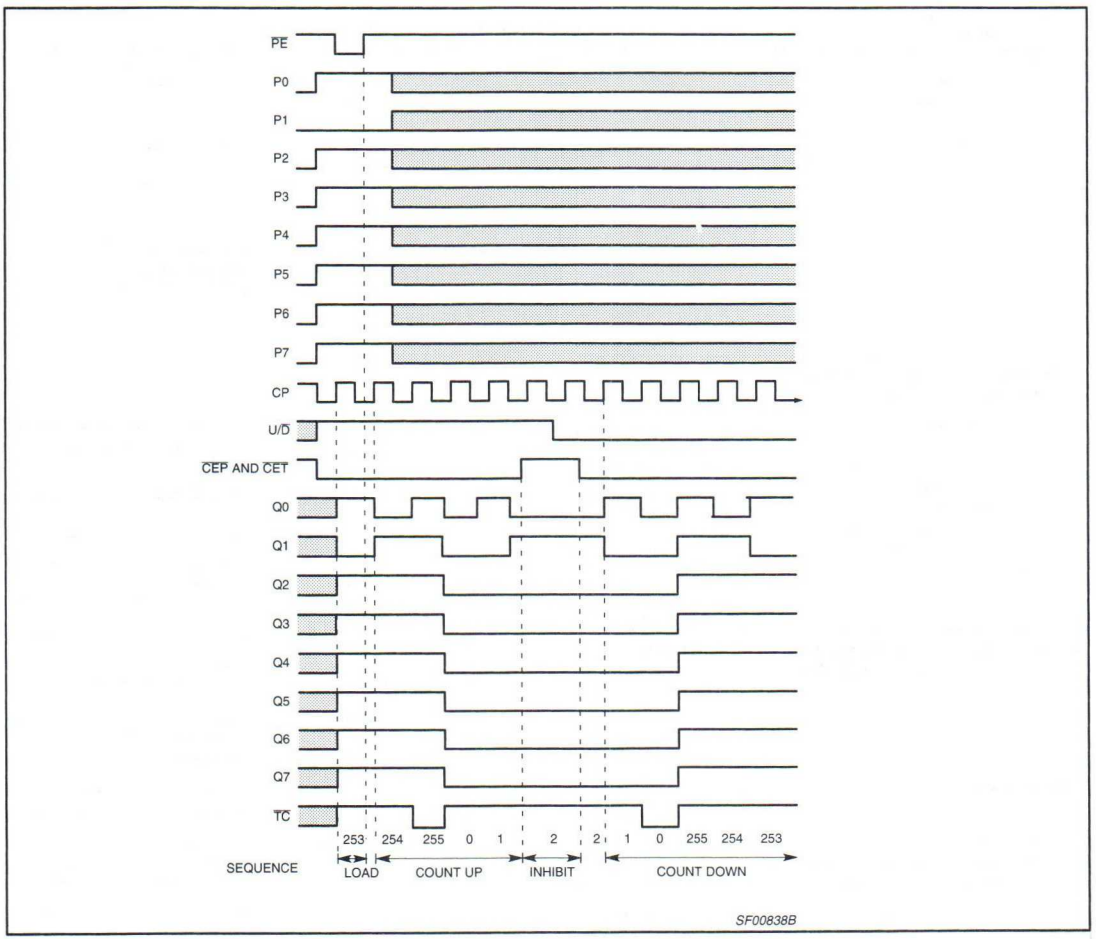
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		85		MHz
t_{PLH} t_{pPHL}	Propagation delay CP to Q_n (Load, $\overline{PE}$ = Low)	Waveform 1	3.0 4.0	6.0 6.5	8.5 8.5	3.0 4.0	9.0 9.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n (Count, $\overline{PE}$ = High)	Waveform 1	3.0 4.5	6.0 7.0	9.0 10.0	3.0 4.0	10.0 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	4.5 5.0	6.5 6.5	9.5 9.5	4.0 5.0	10.5 10.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 2	3.5 3.0	6.0 6.5	9.0 9.0	3.0 3.0	10.0 10.0	ns ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	Waveform 3	4.5 4.5	7.0 7.0	9.0 9.5	4.0 4.0	10.0 10.0	ns ns

AC SETUP REQUIREMENTS

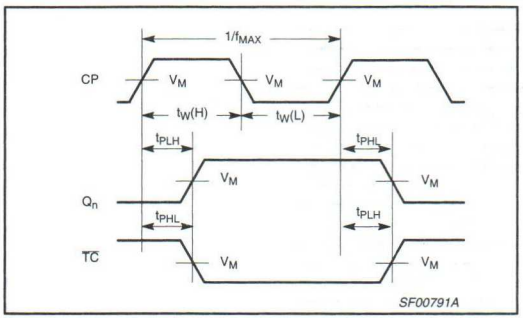
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS				UNIT
			T_{amb} = +25°C, V_{CC} = +5V, C_L = 50pF, R_L = 500Ω		T_{amb} = 0°C to +70°C, V_{CC} = +5V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low P_n to CP	Waveform 4	3.5 3.5		2.5 2.5		ns ns
t_h(H) t_h(L)	Hold time, High or Low P_n to CP	Waveform 4	1.0 1.0		0 1.0		ns ns
t_s(H) t_s(L)	Setup time, High or Low $\overline{PE}$ to CP	Waveform 4	5.5 6.5		5.5 6.5		ns ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{PE}$ to CP	Waveform 4	0 0		0 0		ns ns
t_s(H) t_s(L)	Setup time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	6.0 8.0		5.0 6.5		ns ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	0 0		0 0		ns ns
t_s(H) t_s(L)	Setup time, High or Low U/$\overline{D}$ to CP	Waveform 6	8.0 6.5		6.5 6.5		ns ns
t_h(H) t_h(L)	Hold time, High or Low U/$\overline{D}$ to CP	Waveform 6	0 0		0 0		ns ns
t_w(H) t_w(L)	$\overline{CP}$ Pulse width High or Low	Waveform 1	4.0 4.5		4.0 5.0		ns ns

TIMING DIAGRAM

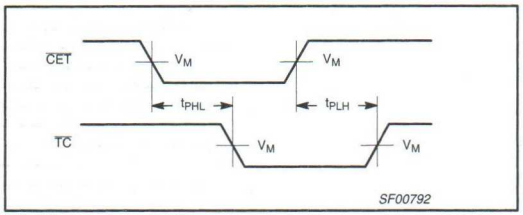


AC WAVEFORMS

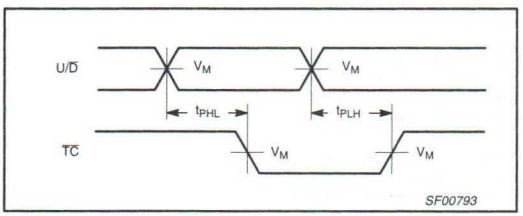
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



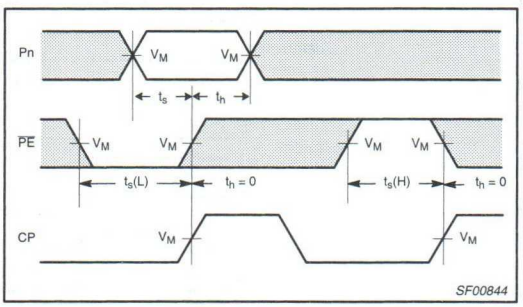
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



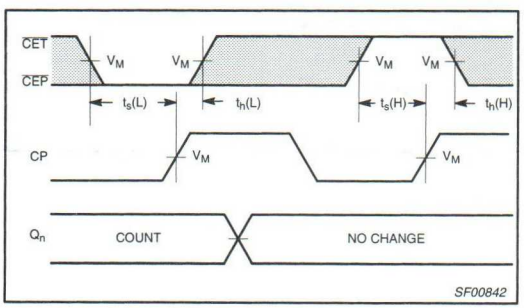
Waveform 2. Propagation Delay, $\overline{CET}$ Input to Terminal Count Output



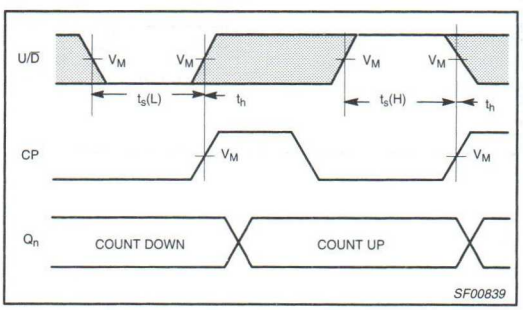
Waveform 3. Propagation Delay, Up/Down Count Control Input to Terminal Count Output



Waveform 4. Parallel Data and Parallel Enable Setup and Hold Times

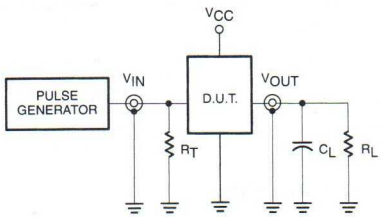


Waveform 5. Count Enables Setup and Hold Times

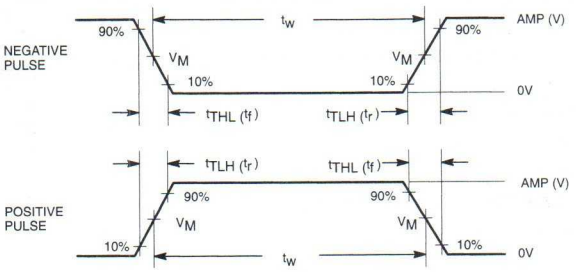


Waveform 6. Up/Down Count Control Setup and Hold Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Octal D flip–flop | 74F273A

FEATURES

- High impedance inputs for reduced loading (20μA in Low and High states)
- Ideal buffer for MOS microprocessor or memory
- Eight edge–triggered D–type flip–flops
- Buffered common clock
- Buffered asynchronous Master Reset
- See 74F377A for clock enable version
- See 74F373 for transparent latch version
- See 74F374 for 3–State version

DESCRIPTION

The 74F273 has eight edge–triggered D–type flip–flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip–flops simultaneously.

The register is fully edge–triggered. The state of each D input, one setup time before the Low–to–High clock transition, is transferred to the corresponding flip–flop's Q output.

All outputs will be forced Low independently of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the CP and $\overline{MR}$ are common to all elements.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F273A	170MHz	25mA

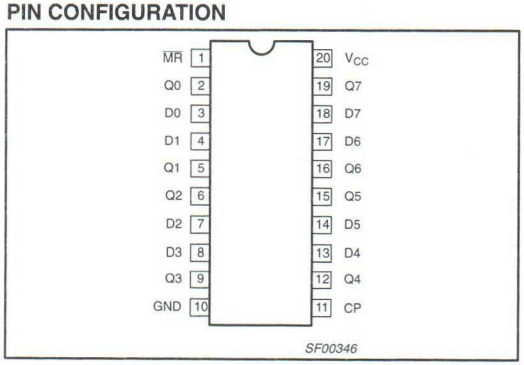
ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_{amb} = 0°C to +70°C	PKG. DWG. #
20–pin plastic DIP	74F273AN	SOT146-1
20–pin plastic SOL	74F273AD	SOT163-1

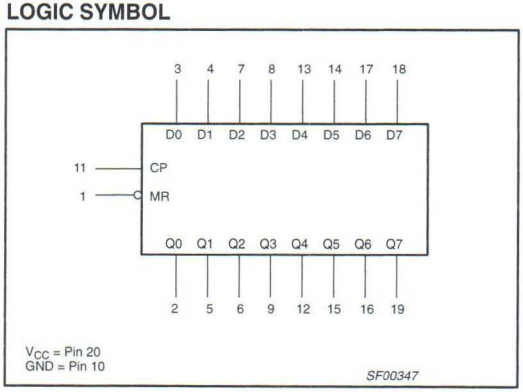
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D7	Data inputs	1.0/0.033	20μA/20μA
$\overline{MR}$	Master Reset input (active–Low)	1.0/0.033	20μA/20μA
CP	Clock pulse input (active rising edge)	1.0/0.033	20μA/20μA
Q0 – Q7	Data outputs	50/33	1.0mA/20mA

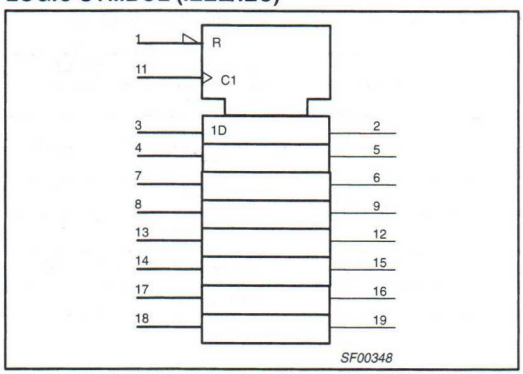
PIN CONFIGURATION



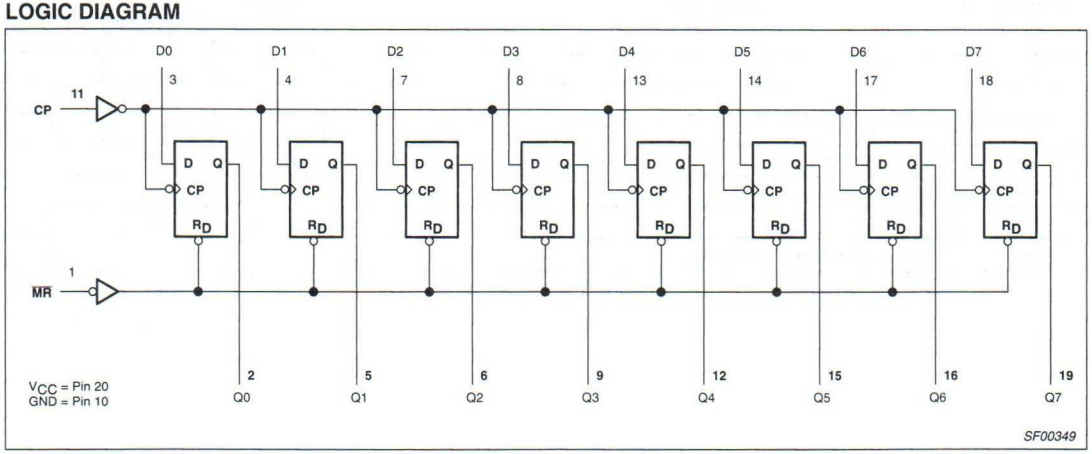
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{MR}$	CP	Dn	Q0 – Q7	
L	X	X	L	Reset (clear)
H	↑	h	H	Load "1"
H	↑	l	L	Load "0"

H = High voltage level
h = High voltage level one set–up time prior to the Low–to–High clock transition
L = Low voltage level
l = Low voltage level one set–up time prior to the Low–to–High clock transition
X = Don't care
↑ = Low–to–High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–1	mA
I_{OL}	Low–level output current			20	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage	MR & CP inputs	V_{CC} = MIN, V_{IL} = 0.0V[3], V_{IH} = 4.5V[3], I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
		other inputs	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}		0.30	0.50	V
				±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				–20	µA
I_{OS}	Short–circuit output current[4]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			24	38	mA
		I_{CCL}				27	43	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. To reduce the effect of external noise during test.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

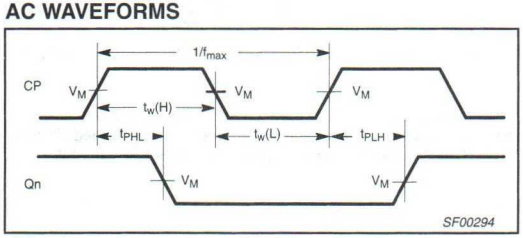
AC CHARACTERISTICS FOR 'F273A

SYMBOL	PARAMETER	WAVEFORM	LIMITS T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
f_{MAX}	Maximum clock frequency	1	150	170		125		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	1	3.5 5.0	5.0 7.0	8.0 9.5	3.0 4.5	9.0 10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn	2	5.0	7.0	9.0	5.0	9.5	ns

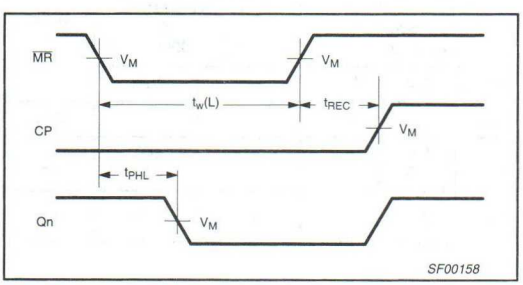
AC SETUP REQUIREMENTS FOR 'F273A

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to CP	3	3.0 2.0			2.5 2.5		
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP	3	0.5 0.0			2.5 1.0		ns
$t_w(H)$ $t_w(L)$	Clock pulse width High or Low	1	4.5 3.5			5.0 4.0		ns
$t_w(L)$	Master Reset pulse width, Low	2	3.0			3.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	4.0			5.0		ns

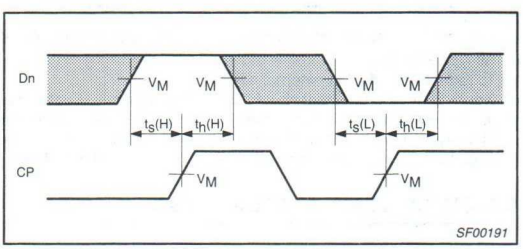
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



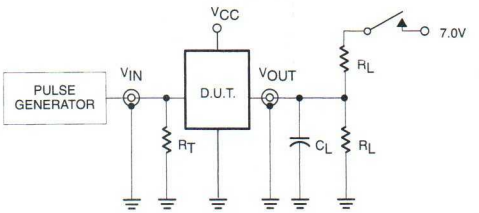
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



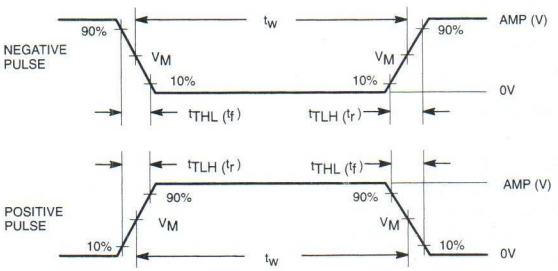
Waveform 3. Data Setup and Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

9-bit odd/even parity generator/checker | 74F280B

FEATURES

- High-impedance NPN base inputs for reduced loading (20μA in Low and High states)
- Buffered inputs — one normalized load
- Word length easily expanded by cascading
- Industrial temperature range available (–40°C to +85°C)

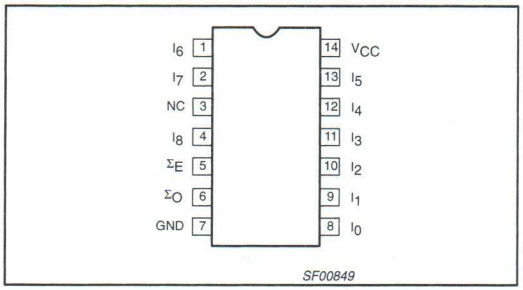
DESCRIPTION

The 74F280B is a 9-bit Parity Generator or Checker commonly used to detect errors in high speed data transmission or data retrieval systems. Both Even (Σ_E) and Odd (Σ_O) parity outputs are available for generating or checking even or odd parity on up to 9 bits.

The Even (Σ_E) parity output is High when an even number of Data inputs (I_0 - I_8) are High. The Odd (Σ_O) parity output is High when an odd number of Data inputs are High.

Expansion to larger word sizes is accomplished by tying the Even (Σ_E) outputs of up to nine parallel devices to the data inputs of the final stage. This expansion scheme allows an 81-bit data word to be checked in less than 20ns.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F280B	5.5ns	26mA

ORDERING INFORMATION

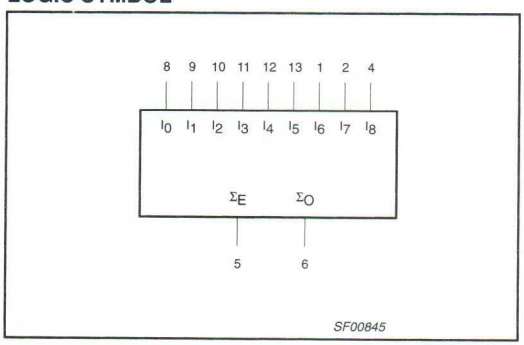
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	PKG. DWG. #
14-pin plastic DIP	N74F280BN	I74F280BN	SOT27-1
14-pin plastic SO	N74F280BD	I74F280BD	SOT108-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

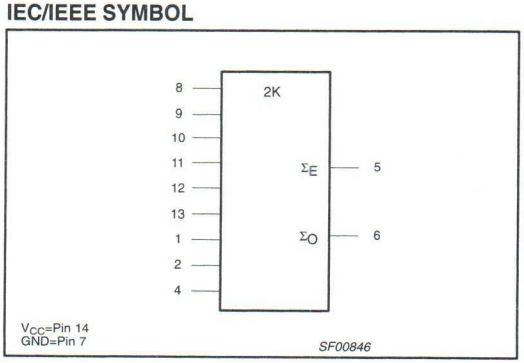
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_0 - I_8	Data inputs	1.0/0.033	20μA/20μA
Σ_E, Σ_O	Parity outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

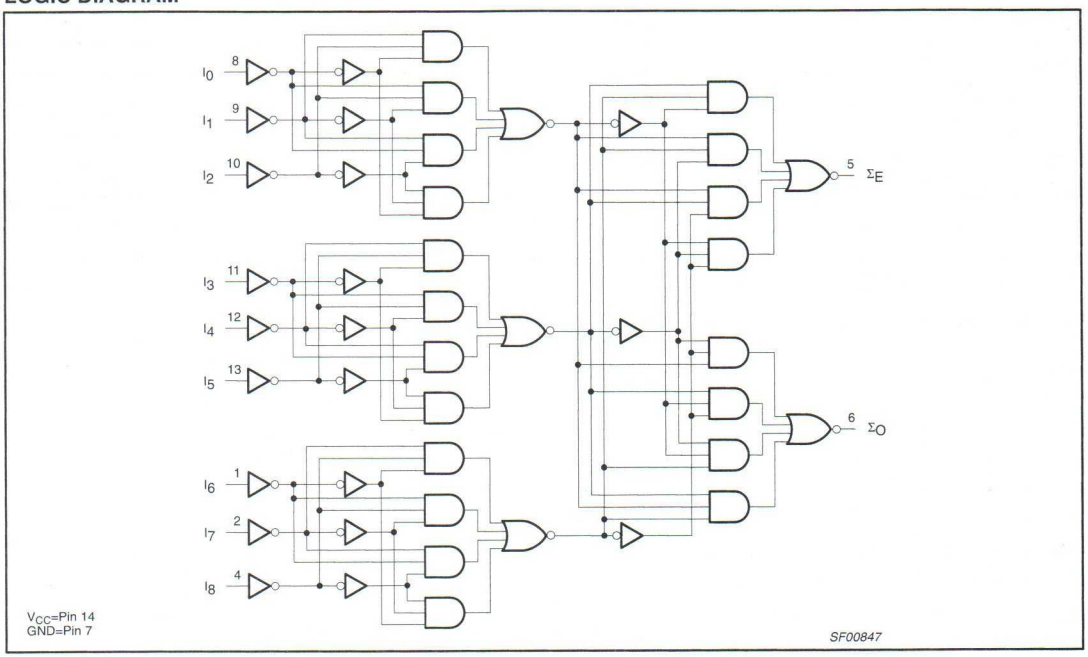
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS	OUTPUTS	
Number of High Data Inputs (I_0 - I_8)	Σ_E	Σ_O
Even — 0, 2, 4, 6, 8	H	L
Odd — 1, 3, 5, 7, 9	L	H

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state		40	mA
T_{amb}	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current				–1	mA
I_{OL}	Low-level output current				20	mA
T_{amb}	Operating free-air temperature range	Commercial range	0		70	°C
		Industrial range	–40		85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH}	High-level input current	Commercial range	V_{CC} = MAX, V_I = 2.7V				20	µA
		Industrial range					40	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–20	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			26	35	mA

NOTES:

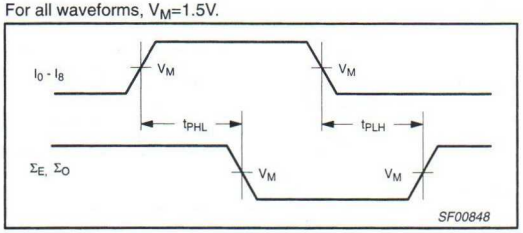
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

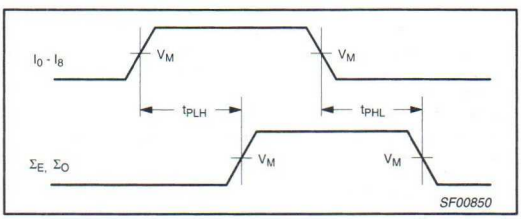
SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS							UNIT
				T_{amb}= +25°C V_{CC} = +5.V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = -40°C to +85°C V_{CC} = +5.V ± 10% C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_0 - I_8 to Σ_E	74F280B	Waveform 1, 2	4.0 4.0	6.5 7.0	9.0 10.0	3.5 3.5	10.0 11.1	3.0 3.5	11.0 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay I_0 - I_8 to Σ_O		Waveform 1, 2	4.0 4.0	6.5 7.0	9.0 10.0	3.5 3.5	10.0 11.0	3.0 3.5	11.0 12.0	ns ns

AC WAVEFORMS

For all waveforms, V_M=1.5V.

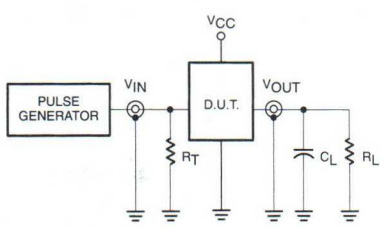


Waveform 1. Propagation Delay for Inverting Outputs

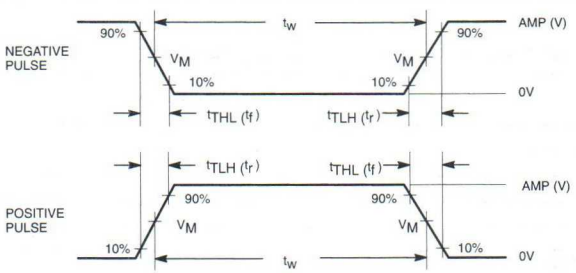


Waveform 2. Propagation Delay for Non-Inverting Outputs

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

4-bit binary full adder with fast carry | 74F283

FEATURES

- High speed 4-bit addition
- Cascadable in 4-bit increments
- Fast Internal carry look-ahead

DESCRIPTION

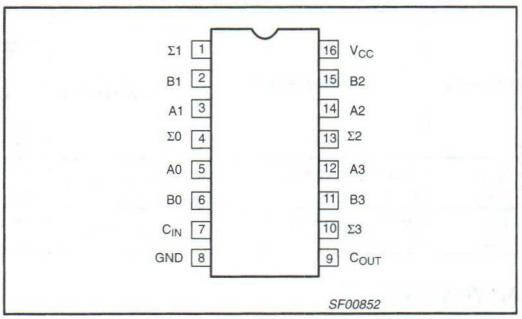
The 74F283 adds two 4-bit binary words (An plus Bn) plus the incoming carry. The binary sum appears on the sum outputs ($\Sigma 0$–$\Sigma 3$) and the outgoing carry (C_{OUT}) according to the equation:

$C_{IN}+2^0(A0+B0)+2^1(A1+B1)+2^2(A2+B2)+2^3(A3+B3)$
$=\Sigma 0+2\Sigma 1+4\Sigma 2+8\Sigma 3+16C_{OUT}$
where (+)=plus

Due to the symmetry of the binary add function, the 74F283 can be used with either all active-High operands (positive logic) or with all active-Low operands (negative logic). See Function Table. In case of all active-Low operands (negative logic) the results $\Sigma 1$–$\Sigma 4$ and C_{OUT} should be interpreted also as active-Low. With active-High inputs, C_{IN} cannot be left open; it must be held Low when no "carry in" is intended. Interchanging inputs of equal weight does not affect the operation, thus A0, B0, C_{IN} can arbitrarily be assigned to pins 5, 6, 7, etc.

Due to pin limitations, the intermediate carries of the 74F283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F283	6.5ns	40mA

ORDERING INFORMATION

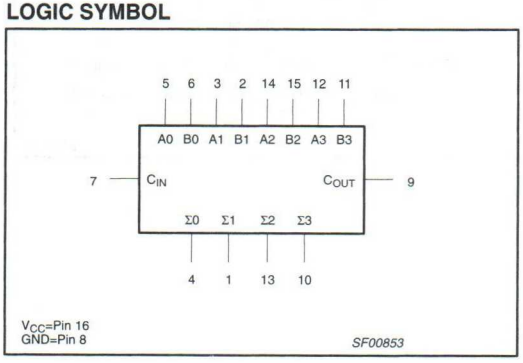
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
16-pin plastic DIP	N74F283N	SOT38-4
16-pin plastic SO	N74F283D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

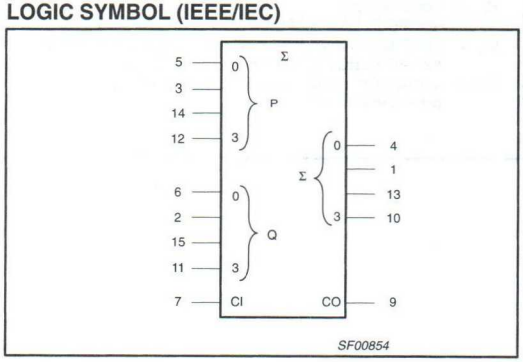
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 - A3	A operand inputs	1.0/2.0	20µA/1.2mA
B0 - B3	B operand inputs	1.0/2.0	20µA/1.2mA
C_{IN}	Carry input	1.0/1.0	20µA/0.6mA
C_{OUT}	Carry output	50/33	1.0mA/20mA
$\Sigma 0$–$\Sigma 3$	Sum outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

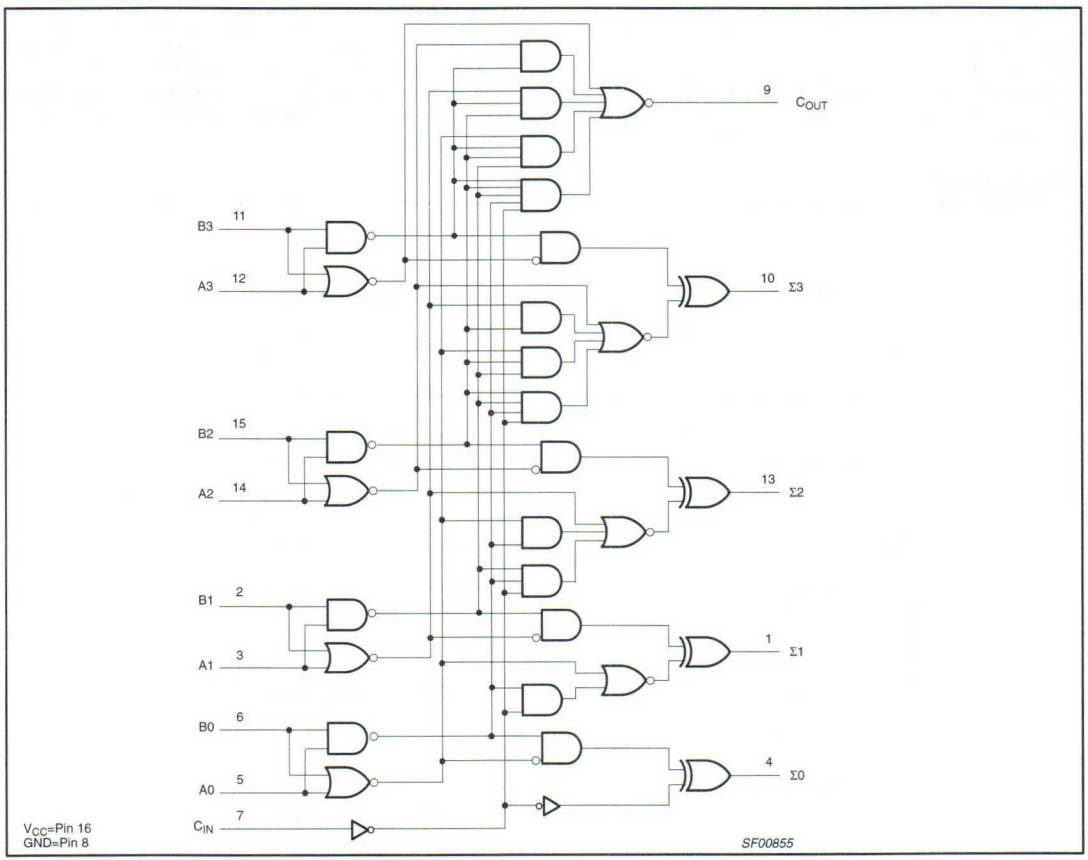
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

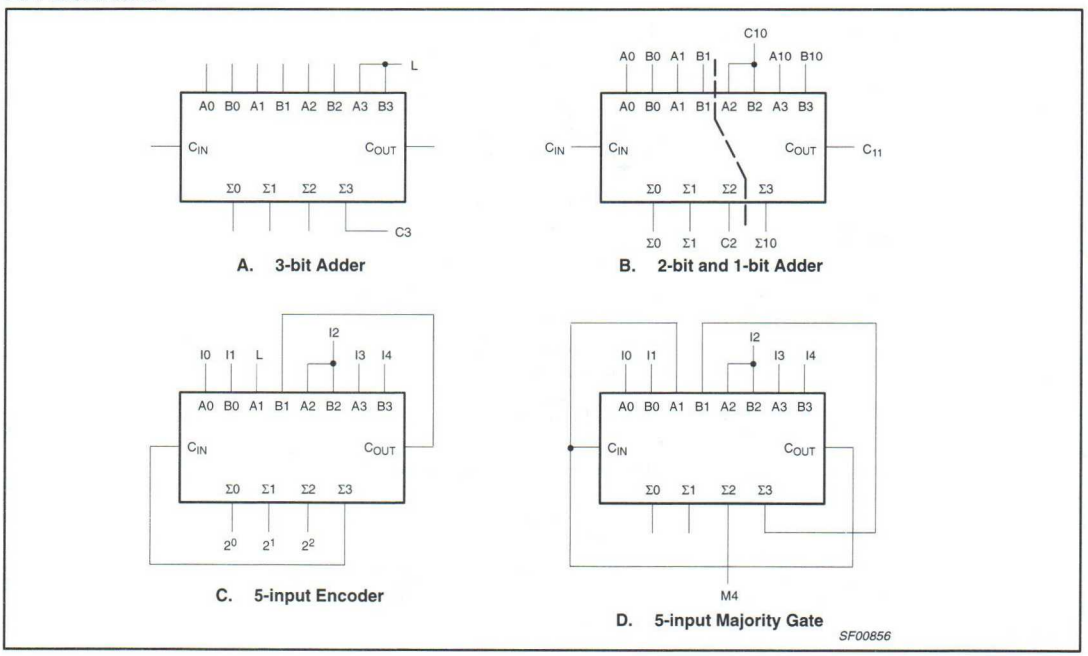
PINS	C_{IN}	A0	A1	A2	A3	B0	B1	B2	B3	Σ0	Σ1	Σ2	Σ3	C_{OUT}
Logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active High	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active Low	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Example:
1001
1010
10011
(10+9=19)
(carry+5+6=12)

H = High voltage level
L = Low voltage level

Figure A shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder (A3, B3) Low makes Σ3 dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle, Figure B shows a way of dividing the 74F283 into a 2-bit and a 1-bit adder. The third stage adder (A2, B2, Σ2) is used as means of getting a carry (C10) signal into the fourth stage adder (via A2 and B2) and bringing out the carry from the second stage on Σ2. Note that as long as A2 and B2 are the same, whether High or Low, they do not influence Σ2. Similarly, when A2 and B2 are the same, the carry into the third stage does not influence the carry out of the third stage. Figure C shows a method of implementing a 5-input encoder where the inputs are equally weighted. The outputs Σ0, Σ1 and Σ2 present a binary number of inputs I0–I4 that are true. Figure D shows one method of implementing a 5-input majority gate. When three or more of the inputs I0–I4 are true, the output M4 is true.

APPLICATIONS



A. 3-bit Adder

B. 2-bit and 1-bit Adder

C. 5-input Encoder

D. 5-input Majority Gate

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	C_{IN} only	V_{CC} = MAX, V_I = 0.5V				−0.6	mA
		An, Bn					−1.2	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)[4]		V_{CC} = MAX			40	55	mA

NOTES:

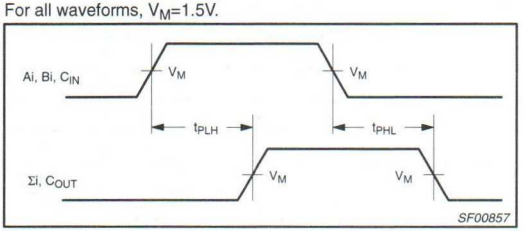
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} should be measured with all outputs open and the following conditions:
   Condition1: all inputs grounded
   Condition 2: all B inputs Low, other inputs at 4.5V
   Condition 3: all inputs at 4.5V

AC ELECTRICAL CHARACTERISTICS

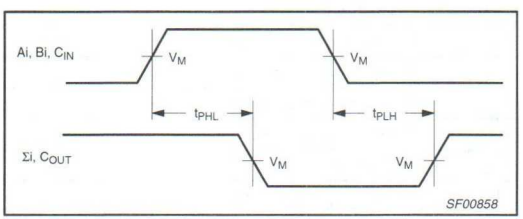
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb}= +25°C V_{CC} = +5.V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay C_{IN} to Σi	Waveform 1, 2	3.5 4.0	7.0 7.0	9.5 9.5	3.0 3.5	10.5 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Ai or Bi to Σi	Waveform 1, 2	3.5 3.5	7.0 7.0	9.5 9.5	2.5 3.5	10.5 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to C_{OUT}	Waveform 2	3.5 3.0	5.7 5.4	7.5 7.0	3.5 2.5	8.5 8.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Ai or Bi to C_{OUT}	Waveform 1, 2	3.5 2.5	5.7 5.3	7.5 7.0	3.0 2.5	8.5 8.0	ns ns

AC WAVEFORMS

For all waveforms, V_M=1.5V.

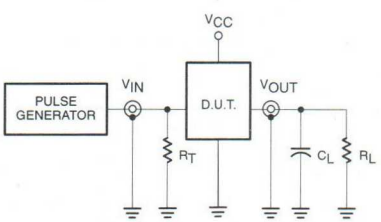


Waveform 1. Propagation Delay Operands and Carry Inputs to Outputs

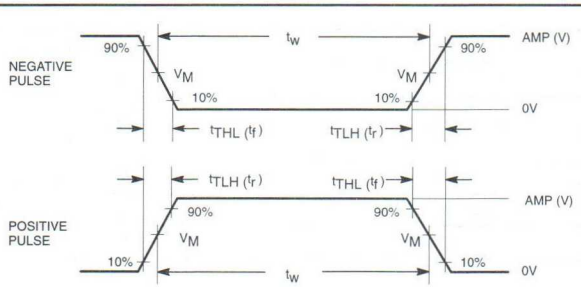


Waveform 2. Propagation Delay Operands and Carry Inputs to Outputs

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Quad 2-input multiplexer with storage | 74F298

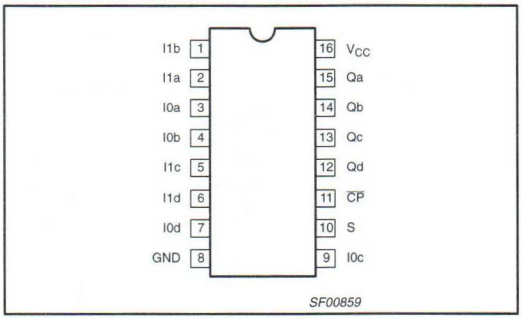
FEATURES

- Fully synchronous operation
- Select from two data sources
- Buffered, negative edge triggered clock
- Provides the equivalent of function capabilities of two separate MSI functions (74F157 and 74F175)

DESCRIPTION

The 74F298 is a high speed Quad 2-Input Multiplexer with storage. It selects 4 bits of data from two sources (ports) under the control of a common Select input (S). The selected data is transferred to the 4-bit output register synchronous with the High-to-Low transition of the clock ($\overline{CP}$). The 4-bit register is fully edge triggered. The data inputs (I0 and I1) and Select input (S) must be stable only one setup time prior to the High-to-Low transition of the clock for predictable operation.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F298	115MHz	30mA

ORDERING INFORMATION

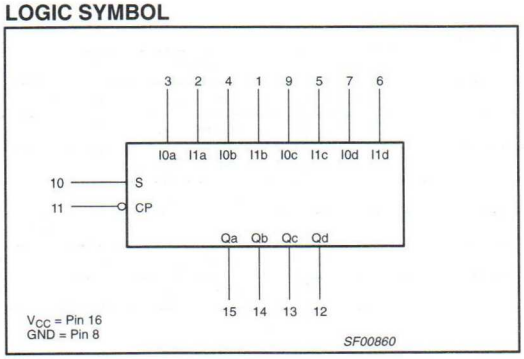
DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
16-pin plastic DIP	N74F298N	SOT38-4
16-pin plastic SO	N74F298D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

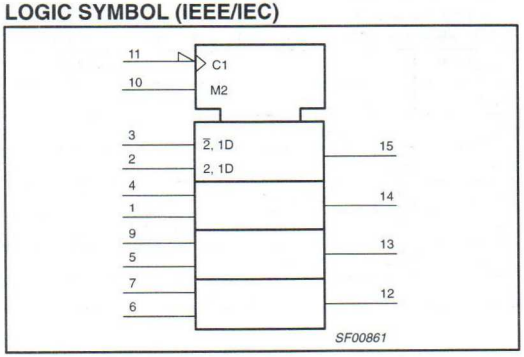
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I0a, I0b, I0c, I0d	Data inputs	1.0/1.0	20µA/0.6mA
I1a, I1b, I1c, I1d	Data inputs	1.0/1.0	20µA/0.6mA
S	Select input	1.0/1.0	20µA/0.6mA
$\overline{CP}$	Clock input (active falling edge)	1.0/1.0	20µA/0.6mA
Qa, Qb, Qc, Qd	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

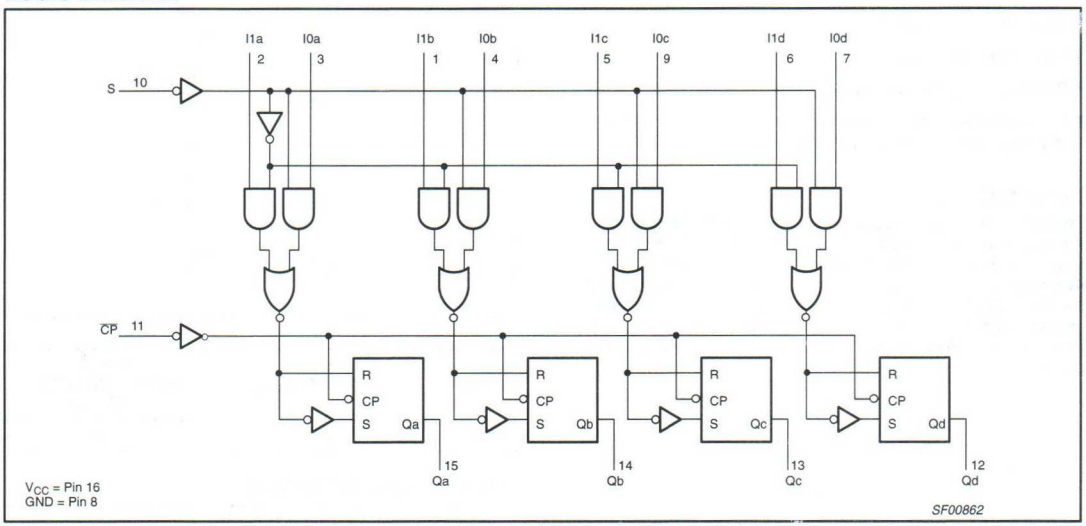
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUT	OPERATING MODE
$\overline{CP}$	S	I0n	I1n	Qn	
↓	l	l	X	L	Load source "0"
↓	l	h	X	H	
↓	h	X	l	L	Load source "1"
↓	h	X	h	H	

H = High voltage level
h = High voltage level one setup time prior to the High-to-Low clock transition
L = Low voltage level
l = Low voltage level one setup time prior to the High-to-Low clock transition
X = Don't care
↓ = High-to-Low clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = –MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
				±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			30	40	mA
		I_{CCL}				32	40	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

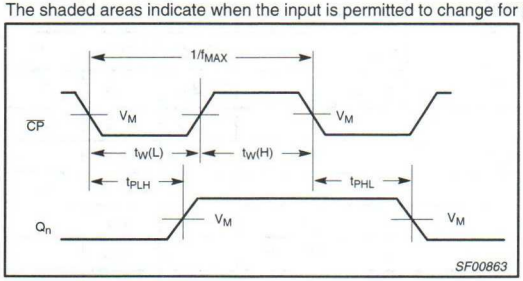
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	110	115		105		ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ tp Qn	Waveform 1	4.0 4.5	5.5 6.5	7.5 8.5	4.0 4.5	9.0 9.5	ns

AC SETUP REQUIREMENTS

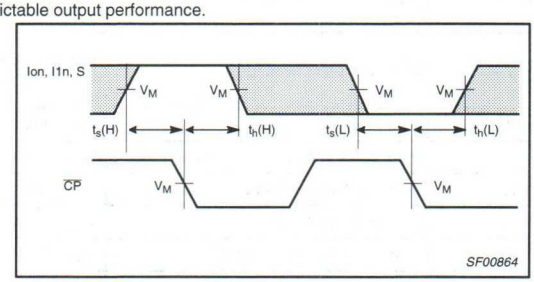
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I0n, I1n to $\overline{CP}$	Waveform 2	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I0n, I1n to $\overline{CP}$	Waveform 2	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S to $\overline{CP}$	Waveform 2	6.0 5.0			7.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S to $\overline{CP}$	Waveform 2	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	$\overline{CP}$ Pulse width, High or Low	Waveform 1	5.0 5.0			5.0 7.0		ns

AC WAVEFORMS

For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

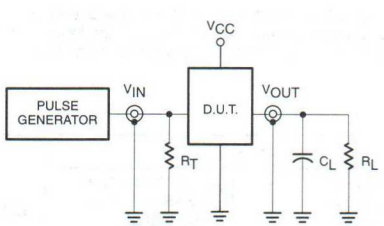


Waveform 1. Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

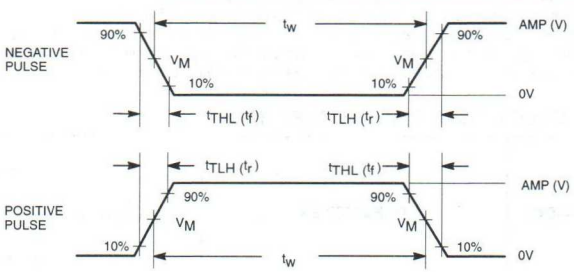


Waveform 2. Data Setup and Hold Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SF00006

8-bit universal shift/storage register (3-State) 74F299

FEATURES

- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: Shift left, shift right, load and store
- 3-State outputs for bus-oriented applications

DESCRIPTION

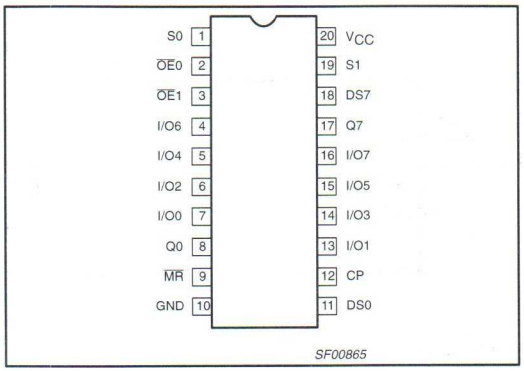
The 74F299 is an 8-bit universal shift/storage register with 3-State outputs. Four modes of operation are possible: Hold (store), shift left, shift right and parallel load. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q0 and Q7 to allow easy serial cascading. A separate active-Low Master Reset is used to reset the register.

The 74F299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S0 and S1, as shown in the Function Table. All flip-flop outputs are brought out through 3-State buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q0 and Q7 are also brought out on other pins for expansion in serial shifting of longer words.

A Low signal on $\overline{MR}$ overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of clock are observed.

A High signal on either $\overline{OE}0$ or $\overline{OE}1$ disables the 3-State buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-State buffers are also disabled by High signals on both S0 and S1 in preparation for a parallel load operation.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F299	115MHz	58mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
20-pin plastic DIP	N74F299N	SOT146-1
20-pin plastic SOL	N74F299D	SOT163-1
20-pin plastic SSOP II	N74F299DB	SOT339-1

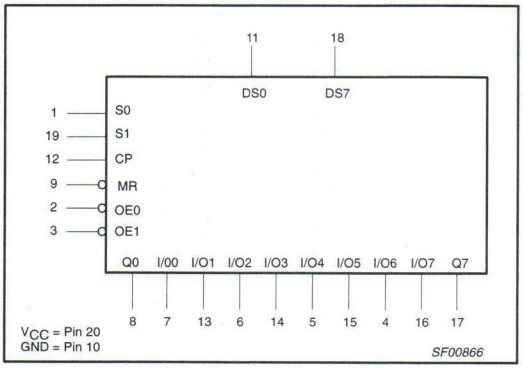
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
DS0	Serial data input for right shift	1.0/1.0	20µA/0.6mA
DS7	Serial data input for left shift	1.0/1.0	20µA/0.6mA
S0, S1	Mode select inputs	1.0/2.0	20µA/1.2mA
CP	Clock pulse input (Active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Asynchronous Master Reset input (Active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}0$, $\overline{OE}1$	Output Enable input (Active Low)	1.0/1.0	20µA/0.6mA
Q0, Q7	Serial outputs	50/33	1.0mA/20mA
I/On	Multiplexed parallel data inputs or	3.5/1.0	70µA/0.6mA
	3-State parallel outputs	150/40	3.0mA/24mA

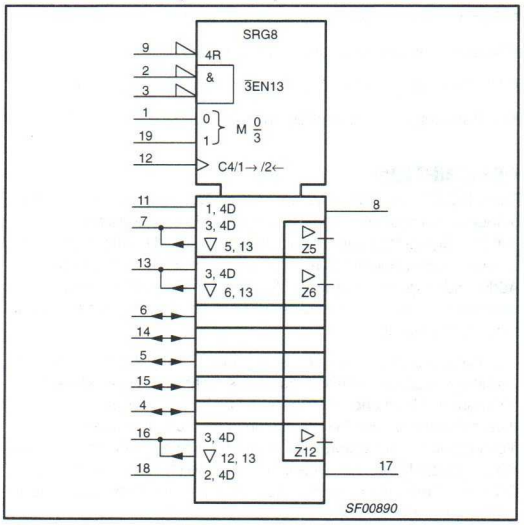
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High State and 0.6mA in the Low state.

8-bit universal shift/storage register (3-State) 74F299

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

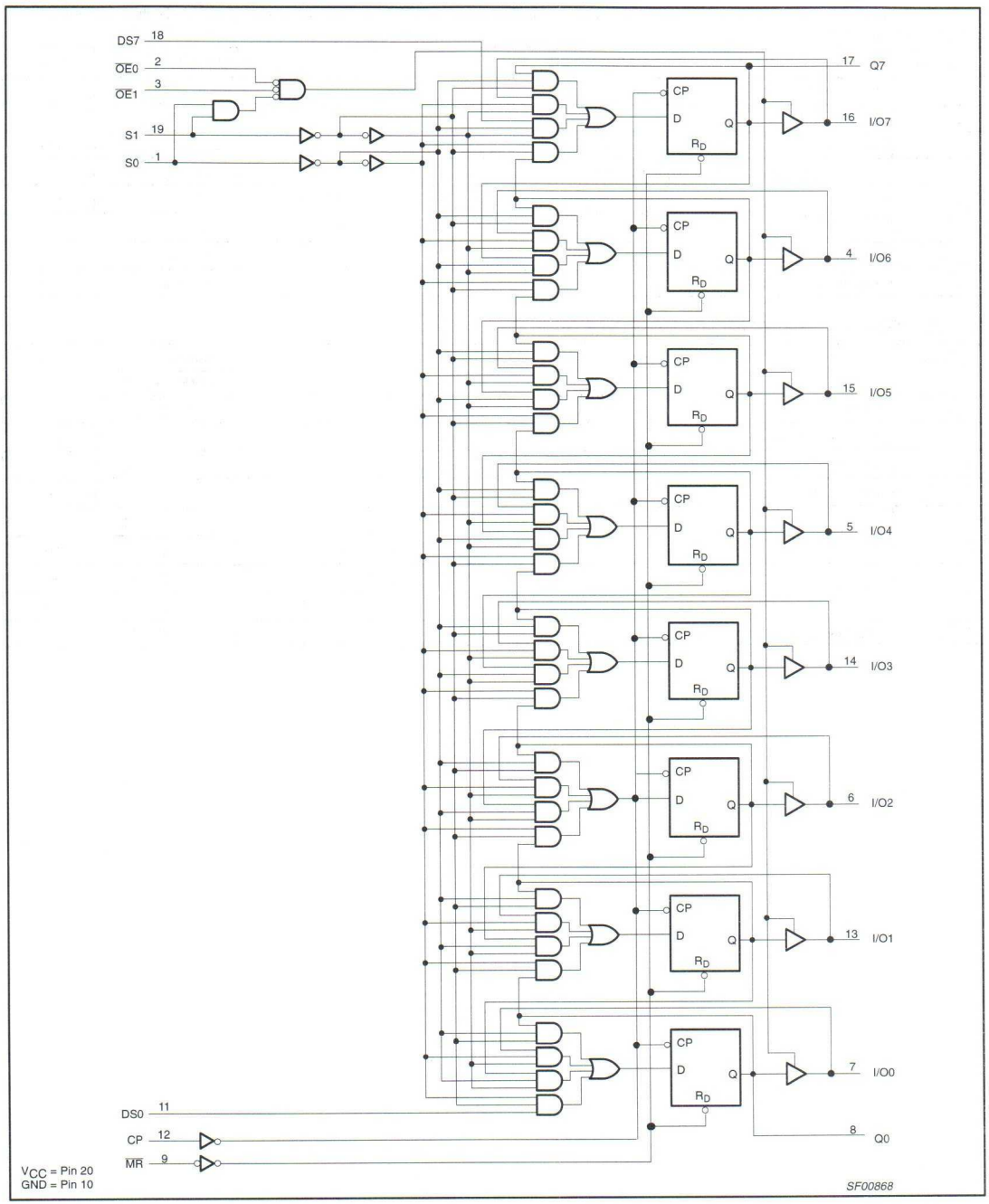


FUNCTION TABLE

INPUTS	INPUTS				OPERATING MODE
$\overline{OE}$n	$\overline{MR}$	S1	S0	CP	
L	L	X	X	X	Asynchronous Reset; Q0 - Q7 = Low
L	H	H	H	↑	Parallel load; I/On → Qn (I/On outputs disabled)
L	H	L	H	↑	Shift right; DS0 → Q0, Q0 → Q1, etc.
L	H	H	L	↑	Shift left; DS7 → Q7, Q7 → Q6, etc.
L	H	L	L	X	Hold
H	X	X	X	X	Outputs in High Z

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	Q0, Q7	40	mA
		I/On	48	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	Q0, Q7			−1	mA
		I/On			−3	mA
I_{OL}	Low-level output current	Q0, Q7			20	mA
		I/On			24	mA
T_{amb}	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	Q0, Q7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/On		I_{OH} = –3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = MAX, V_I = 7.0V					100	µA
		I/On	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	except I/On	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	S0, S1	V_{CC} = MAX, V_I = 0.5V					–1.2	mA
		others						–0.6	mA
I_{IH} + I_{OZH}	Off-state output current, High-level voltage applied	I/On only	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{IL} + I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					–0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				55	60	mA
		I_{CCL}					70	90	mA
		I_{CCZ}					65	95	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	I/O	Waveform 1	70	100		70		MHz
		Qn		85	115		85		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q0 or Q7		Waveform 1	4.0 4.5	5.0 6.0	7.5 8.0	3.5 4.5	8.5 8.5	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to I/On		Waveform 1	4.0 4.0	6.0 6.5	9.0 9.0	4.0 4.0	10.0 10.0	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q0 or Q7		Waveform 2	5.5	7.5	9.5	5.5	10.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to I/On		Waveform 2	5.5	7.5	10.0	5.5	10.5	ns
t_{PZH} t_{PZL}	Output Enable time Sn, $\overline{OE}$ to I/On		Waveform 4 Waveform 5	3.5 4.0	6.0 7.5	8.0 10.0	3.5 4.0	9.0 11.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time Sn, $\overline{OE}$ to I/On		Waveform 4 Waveform 5	2.5 1.5	4.5 2.5	7.0 5.5	2.5 1.5	8.0 6.5	ns ns

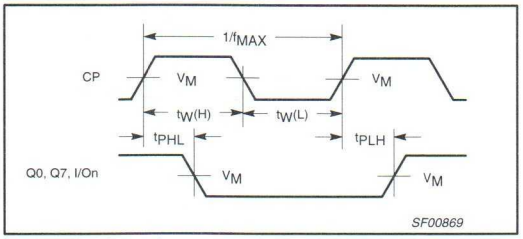
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low S0 or S1 to CP	Waveform 3	6.5 6.5			7.5 7.5		ns ns
t_h(H) t_h(L)	Hold time, High or Low S0 or S1 to CP	Waveform 3	0 0			0 0		ns ns
t_s(H) t_s(L)	Set-up time, High or Low I/On, DS_L or DS_R to CP	Waveform 3	3.5 3.5			4.0 4.0		ns ns
t_h(H) t_h(L)	Hold time, High or Low I/On, DS_L or DS_R to CP	Waveform 3	0 0			0 0		ns ns
t_w(H) t_w(L)	CP Pulse width, High or Low	Waveform 1	5.0 4.5			5.0 4.5		ns
t_w(L)	$\overline{MR}$ Pulse width, Low	Waveform 2	4.5			4.5		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 2	4.0			4.0		ns

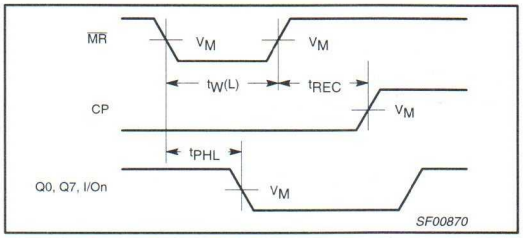
AC WAVEFORMS

For all waveforms, $V_M = 1.5V$

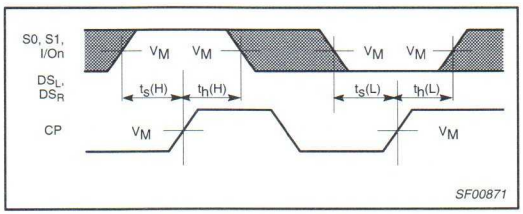
The shaded areas indicate when the input is permitted to change for predictable output performance.



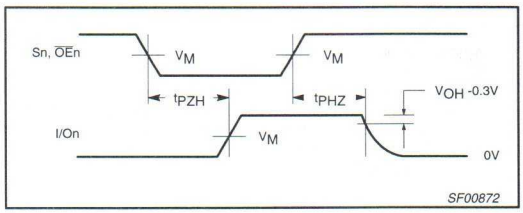
Waveform 1. Propagation Delay, Clock Input to Output, Clock Width, and Maximum Clock Frequency



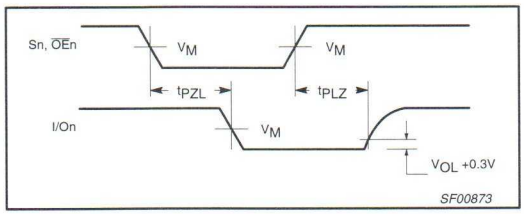
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay, and Master Reset to Clock Recovery Time



Waveform 3. Setup and Hold Times

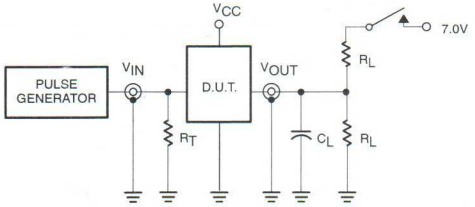


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

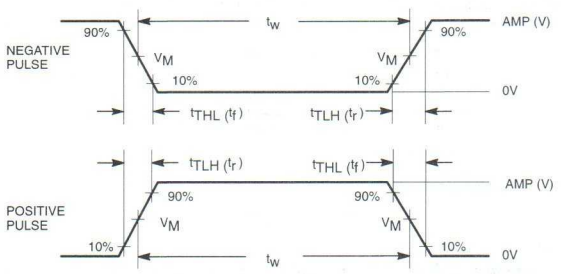


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

Buffers/drivers

74F365, ~~74F366~~*
74F367, ~~74F368~~*

74F365, 74F367 Hex Buffer/Driver (3-State)
74F366, 74F368 Hex Inverter Buffer/Driver (3-State)

FEATURES

- High-impedance NPN base inputs for reduced loading (20µA in High and Low states)
- High-speed
- Bus oriented
- 3-State buffer outputs sink 64mA

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F365, 74F367	5.0ns	36mA
74F366, 74F368	5.0ns	33mA

ORDERING INFORMATION

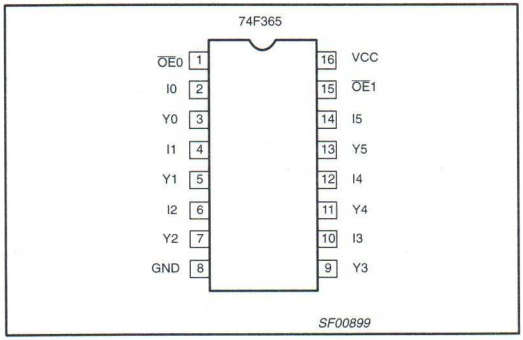
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
16-pin plastic DIP	N74F365N, N74F367N	SOT38-4
16-pin plastic SO	N74F365D, N74F367D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

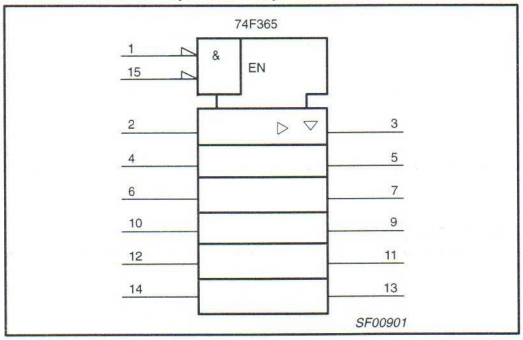
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I0 - I5	Inputs	1.0/0.033	20µA/20µA
$\overline{OE}$0, $\overline{OE}$1	Output enable inputs (active Low)	1.0/0.033	20µA/20µA
Y0 - Y5, $\overline{Y}$0 - $\overline{Y}$5	Data Outputs	750/106.7	15mA/64mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

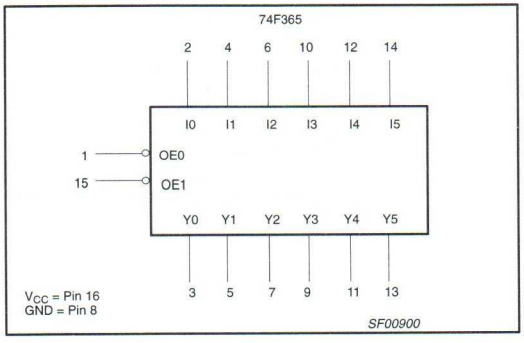
PIN CONFIGURATION



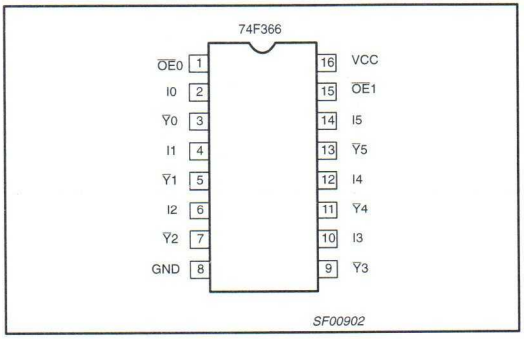
LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL

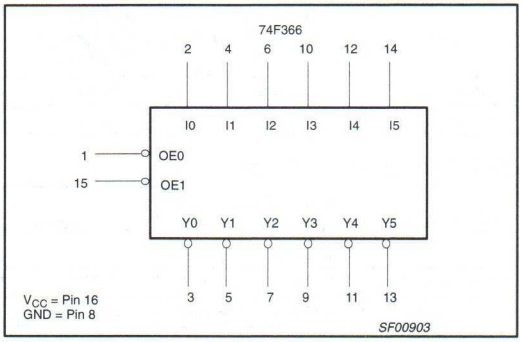


PIN CONFIGURATION

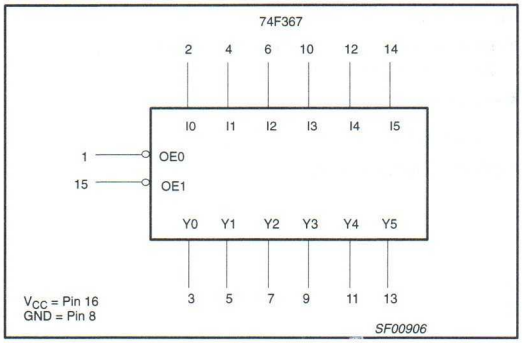


* *Discontinued part. Please see the Discontinued Products List.*

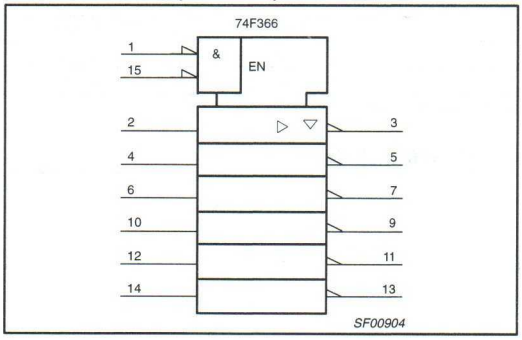
LOGIC SYMBOL



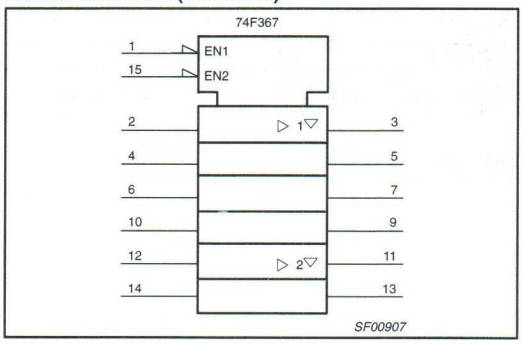
LOGIC SYMBOL



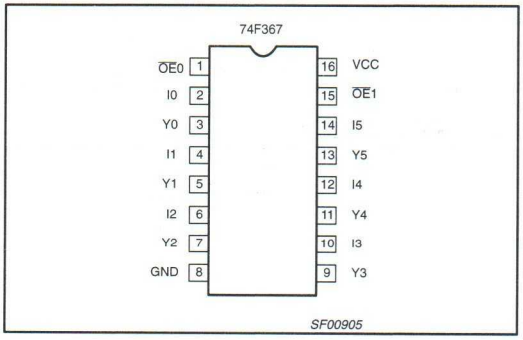
LOGIC SYMBOL (IEEE/IEC)



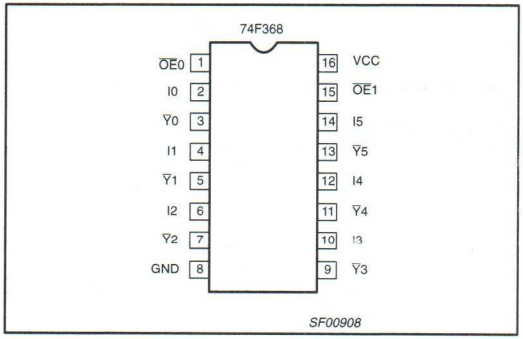
LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION

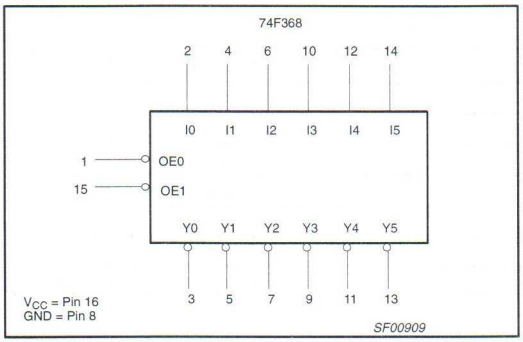


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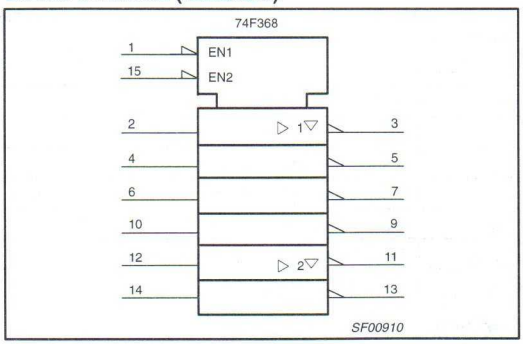


* *Discontinued part. Please see the Discontinued Products List.*

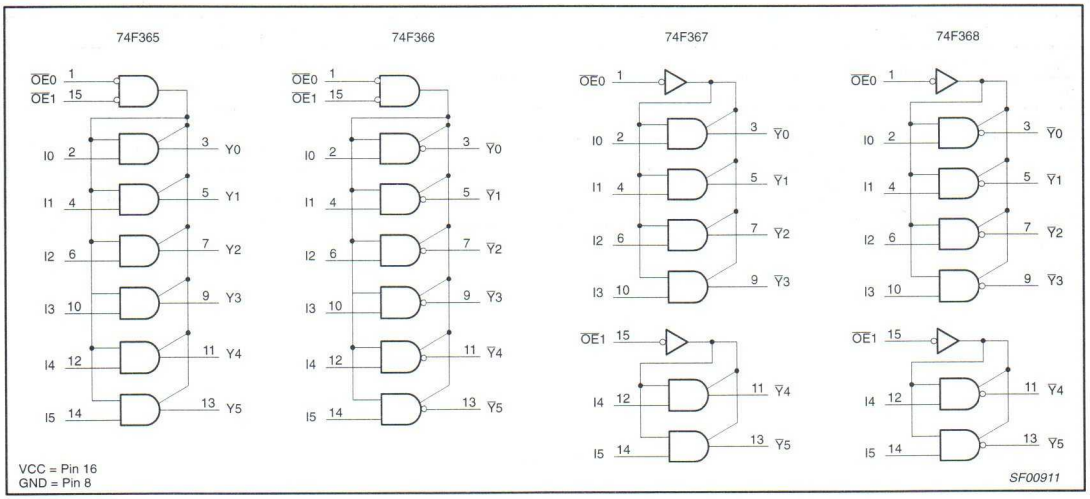
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAMS



FUNCTION TABLE for 74F365 and 74F366

INPUTS			OUTPUTS	
$\overline{OE0}$	$\overline{OE1}$	In	Yn	$\overline{Yn}$
L	L	L	L	H
L	L	H	H	L
X	H	X	Z	Z
H	X	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

FUNCTION TABLE for 74F367 and 74F368

INPUTS		OUTPUTS	
$\overline{OEn}$	In	Yn	$\overline{Yn}$
L	L	L	H
L	H	H	L
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

* *Discontinued part. Please see the Discontinued Products List.*

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	–0.5 to +7.0	V
V_{IN}	Input voltage range	–0.5 to +7.0	V
I_{IN}	Input current range	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state range	–0.5 to 5.5	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–15	mA
I_{OL}	Low-level output current			64	mA
T_{amb}	Operating free-air temperature range	0		70	°C

* *Discontinued part. Please see the Discontinued Products List.*

DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = –3mA	±10%Vcc	2.4			V
					±5%Vcc	2.7	3.3		V
				V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = –15mA	±10%Vcc	2.0			V
					±5%Vcc	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%Vcc			0.55	V
					±5%Vcc		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V				–20	µA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V				–50	µA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX		–100		–225	mA
I_{CC}	Supply current (total)	74F365 74F367	I_{CCH}	V_{CC} = MAX			25	35	mA
			I_{CCL}				47	62	mA
			I_{CCZ}				35	48	mA
		74F366 74F368	I_{CCH}	V_{CC} = MAX			18	25	mA
			I_{CCL}				47	62	mA
			I_{CCZ}				35	48	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

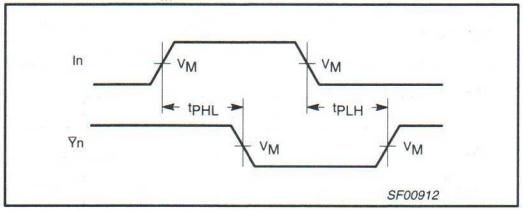
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω MIN	LIMITS TYP	LIMITS MAX	LIMITS T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω MIN	LIMITS MAX	UNIT
t_{PLH}	Propagation delay	74F366,	Waveform 1	3.0	5.0	6.5	3.0	7.5	ns
t_{PHL}	I_n to $\overline{Y}_n$	74F368		2.0	3.0	5.0	1.5	5.5	ns
t_{PLH}	Propagation delay	74F365,	Waveform 2	2.5	4.5	6.5	2.0	7.0	ns
t_{PHL}	I_n to Y_n	74F367		2.5	5.5	7.0	2.0	7.5	ns
t_{PZH}	Output Enable time	74F365,	Waveform 3	2.5	4.0	6.5	2.5	7.5	ns
t_{PZL}	to High or Low level	74F366	Waveform 4	2.5	5.0	8.0	2.5	8.5	ns
t_{PZH}	Output Enable time	74F367,	Waveform 3	3.0	5.5	7.5	3.0	8.5	ns
t_{PZL}	to High or Low level	74F368	Waveform 4	3.0	6.5	8.5	3.0	9.0	ns
t_{PHZ}	Output Disable time		Waveform 3	2.0	4.5	6.5	2.0	7.0	ns
t_{PLZ}	from High to Low level		Waveform 4	2.0	4.0	6.5	2.0	7.0	ns

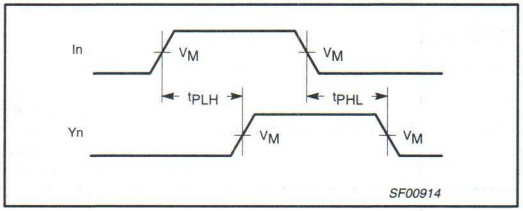
* *Discontinued part. Please see the Discontinued Products List.*

AC WAVEFORMS

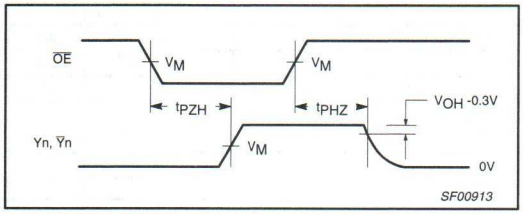
For all waveforms, $V_m = 1.5V$



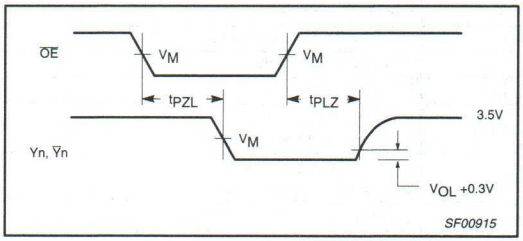
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs

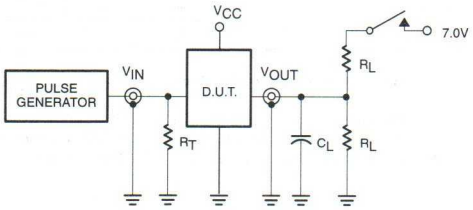


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

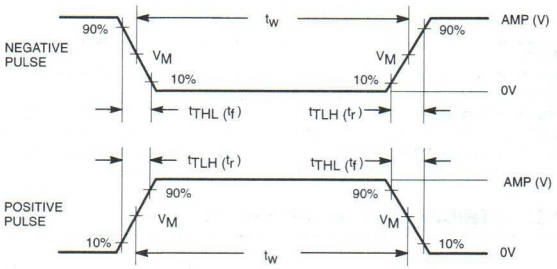


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

* *Discontinued part. Please see the Discontinued Products List.*

Latch/flip-flop 74F373/74F374

74F373 Octal transparent latch (3-State)
74F374 Octal D-type flip-flop (3-State)

FEATURES

- 8-bit transparent latch — 74F373
- 8-bit positive edge triggered register — 74F374
- 3-State outputs glitch free during power-up and power-down
- Common 3-State output register
- Independent register and 3-State buffer operation
- SSOP Type II Package

DESCRIPTION

The 74F373 is an octal transparent latch coupled to eight 3-State output devices. The two sections of the device are controlled independently by enable (E) and output enable ($\overline{OE}$) control gates.

The data on the D inputs is transferred to the latch outputs when the enable (E) input is high. The latch remains transparent to the data input while E is high, and stores the data that is present one setup time before the high-to-low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active low output enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is low, latched or transparent data appears at the output.

When $\overline{OE}$ is high, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

The 74F374 is an 8-bit edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by clock (CP) and output enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of the D input, one setup time before the low-to-high clock transition is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active low output enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is low, the data in the register appears at the outputs. When $\overline{OE}$ is high, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F373	4.5ns	35mA

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F374	165MHz	55mA

ORDERING INFORMATION

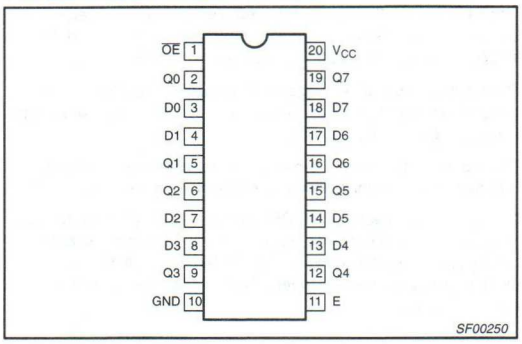
DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
20-pin plastic DIP	N74F373N, N74F374N	SOT146-1
20-pin plastic SOL	N74F373D, N74F374D	SOT163-1
20-pin plastic SSOP type II	N74F373DB, N74374DB	SOT399-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

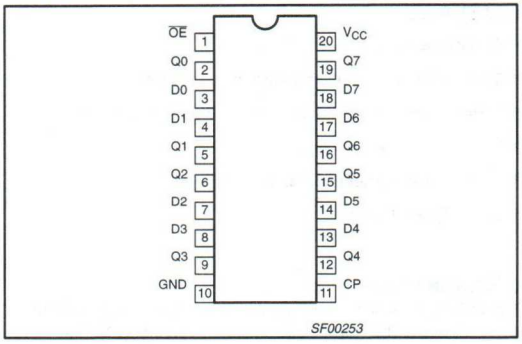
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 - D7	Data inputs	1.0/1.0	20µA/0.6mA
E (74F373)	Enable input (active high)	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output enable inputs (active low)	1.0/1.0	20µA/0.6mA
CP (74F374)	Clock pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
Q0 - Q7	3-State outputs	150/40	3.0mA/24mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

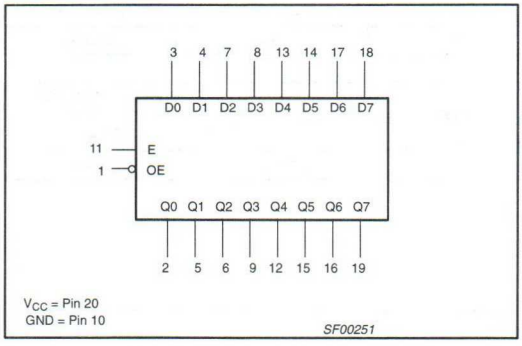
PIN CONFIGURATION – 74F373



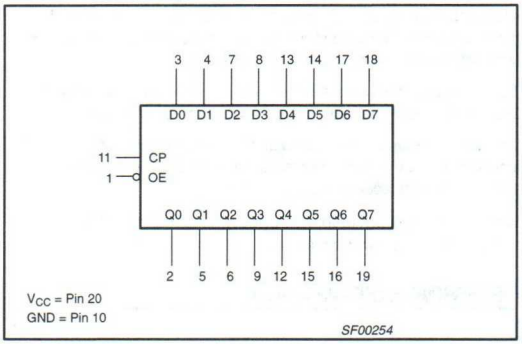
PIN CONFIGURATION – 74F374



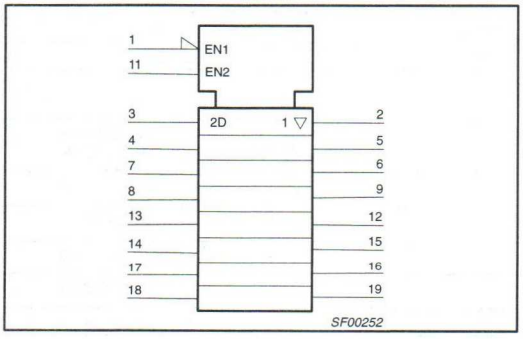
LOGIC SYMBOL – 74F373



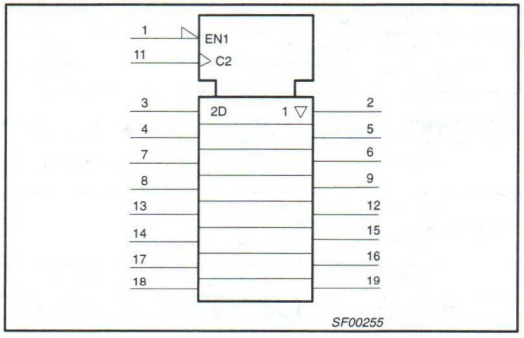
IEC/IEE SYMBOL – 74F374



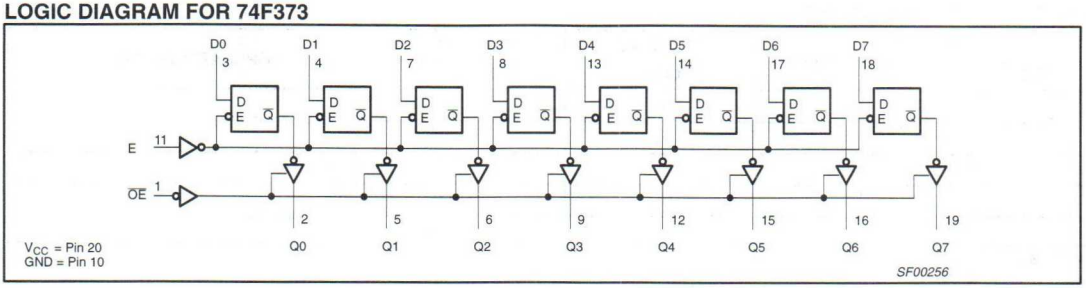
IEC/IEEE SYMBOL – 74F373



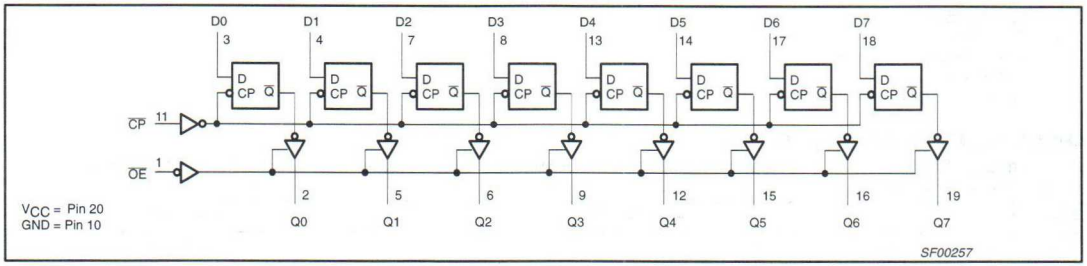
IEC/IEEE SYMBOL – 74F374



LOGIC DIAGRAM FOR 74F373



LOGIC DIAGRAM FOR 74F374



FUNCTION TABLE FOR 74F373

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	Dn		Q0 - Q7	
L	H	L	L	L	Enable and read register
L	H	H	H	H	
L	↓	l	L	L	Latch and read register
L	↓	h	H	H	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	Dn	Dn	Z	

NOTES:

H = High-voltage level
h = High state must be present one setup time before the high-to-low enable transition
L = Low-voltage level
l = Low state must be present one setup time before the high-to-low enable transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-low enable transition

FUNCTION TABLE FOR 74F374

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	Dn	REGISTER	Q0 - Q7	
L	↑	l	L	L	Load and read register
L	↑	h	H	H	
L	↕	X	NC	NC	Hold
H	↕	X	NC	Z	Disable outputs
H	↑	Dn	Dn	Z	

NOTES:
H = High-voltage level
h = High state must be present one setup time before the low-to-high clock transition
L = Low-voltage level
l = Low state must be present one setup time before the low-to-high clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-high clock transition
↕ = Not low-to-high clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	-0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	48	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{Ik}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	74F373	V_{CC} = MAX			35	60	mA
		74F374				57	86	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

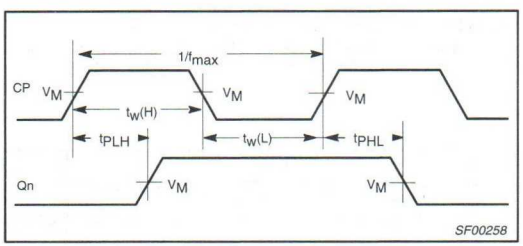
SYMBOL	PARAMETER		TEST CONDITION	LIMITS T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω MIN	TYP	MAX	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω MIN	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	74F373	Waveform 3	3.0 2.0	5.3 3.7	7.0 5.0	3.0 2.0	8.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay E to Qn	74F373	Waveform 2	5.0 3.0	9.0 4.0	11.5 7.0	5.0 3.0	12.0 8.0	ns
t_{PZH} t_{PZL}	Output enable time to high or low level	74F373	Waveform 6 Waveform 7	2.0 2.0	5.0 5.6	11.0 7.5	2.0 2.0	11.5 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level	74F373	Waveform 6 Waveform 7	2.0 2.0	4.5 3.8	6.5 5.0	2.0 2.0	7.0 6.0	ns
f_{max}	Maximum clock frequency	74F374	Waveform 1	150	165		140		ns
t_{PLH} t_{PHL}	Propagation delay CP to Qn	74F374	Waveform 1	3.5 3.5	5.0 5.0	7.5 7.5	3.0 3.0	8.5 8.5	ns
t_{PZH} t_{PZL}	Output enable time to high or low level	74F374	Waveform 6 Waveform 7	2.0 2.0	9.0 5.3	11.0 7.5	2.0 2.0	12.0 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level	74F374	Waveform 6 Waveform 7	2.0 2.0	5.3 4.3	6.0 5.5	2.0 2.0	7.0 6.5	ns

AC SETUP REQUIREMENTS

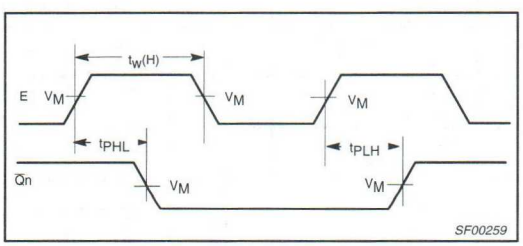
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L= 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low level Dn to E	74F373	Waveform 4	0 1.0			0 1.0		ns
t_h (H) t_h (L)	Hold time, high or low level Dn to E		Waveform 4	3.0 3.0			3.0 3.0		ns
t_w (H)	E Pulse width, high		Waveform 1	3.5			4.0		ns
t_{su} (H) t_{su} (L)	Setup time, high or low level Dn to CP	74F374	Waveform 5	2.0 2.0			2.0 2.0		ns
t_h (H) t_h (L)	Hold time, high or low level Dn to CP		Waveform 5	0 0			0 0		ns
t_w (H) t_w (L)	CP Pulse width, high or low		Waveform 5	3.5 4.0			3.5 4.0		ns

AC WAVEFORMS

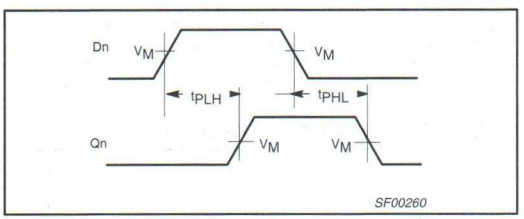
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



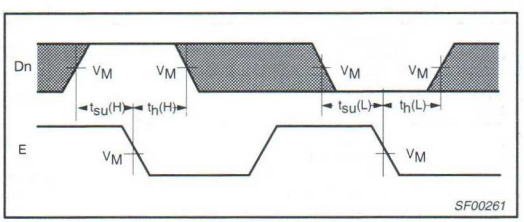
Waveform 1. Propagation delay for clock input to output, clock pulse widths, and maximum clock frequency



Waveform 2. Propagation delay for enable to output and enable pulse width



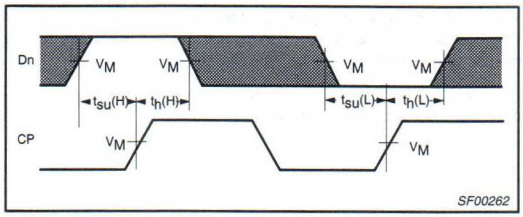
Waveform 3. Propagation delay for data to output



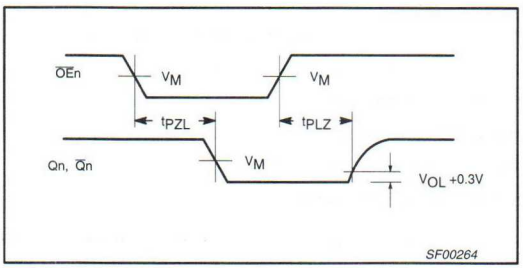
Waveform 4. Data setup time and hold times

AC WAVEFORMS (Continued)

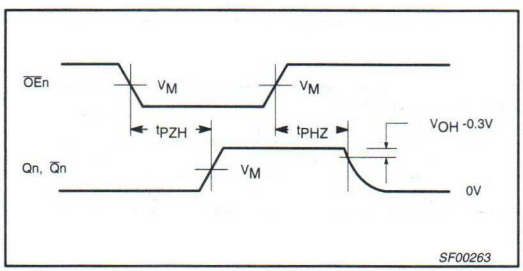
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 5. Data setup time and hold times



Waveform 7. 3-State output enable time to low level and output disable time from low level

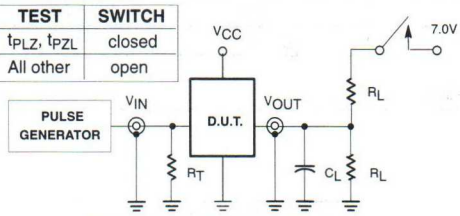


Waveform 6. 3-State output enable time to high level and output disable time from high level

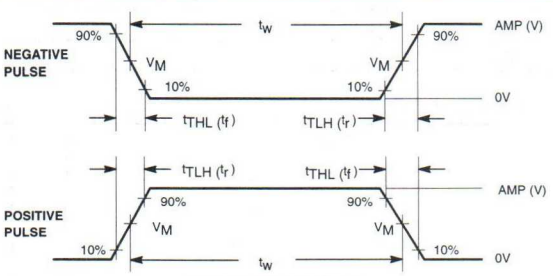
TEST CIRCUIT AND WAVEFORMS

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test circuit for 3-state outputs



Input pulse definition

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00265

Octal D-type flip-flop with enable | 74F377A

FEATURES

- High impedance inputs for reduced loading (20μA in Low and High states)
- Ideal for addressable register applications
- Enable for address and data synchronization applications
- Eight edge–triggered D–type flip–flops
- Buffered common clock
- See 'F273A for Master Reset version
- See 'F373 for transparent latch version
- See 'F374 for 3–State version

DESCRIPTION

The 74F377A has 8 edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered clock (CP) input loads all flip-flops simultaneously when the Enable ($\overline{E}$) input is Low.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The $\overline{E}$ input must be stable one setup time prior to the Low-to-High clock transition for predictable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F377A	165MHz	29mA

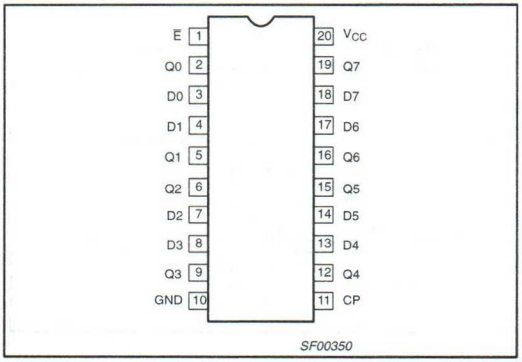
ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_{amb} = 0°C to +70°C	PKG. DWG. #
20–pin plastic DIP	N74F377AN	SOT146-1
20–pin plastic SOL	N74F377AD	SOT163-1

INPUT AND OUTPUT LOADING AND FAN–OUT TABLE

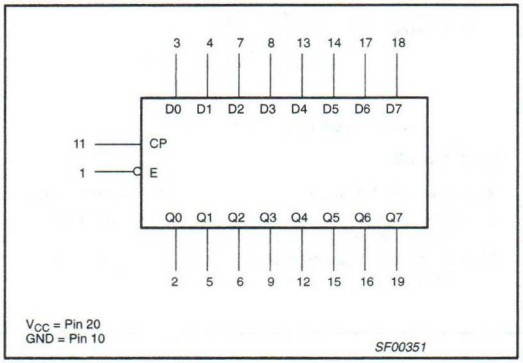
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D7	Data inputs	1.0/0.033	20μA/20μA
CP	Clock pulse input (active rising edge)	1.0/0.033	20μA/20μA
$\overline{E}$	Enable input (active–Low)	1.0/0.033	20μA/20μA
Q0 – Q7	Data outputs	50/33	1.0mA/20mA

PIN CONFIGURATION



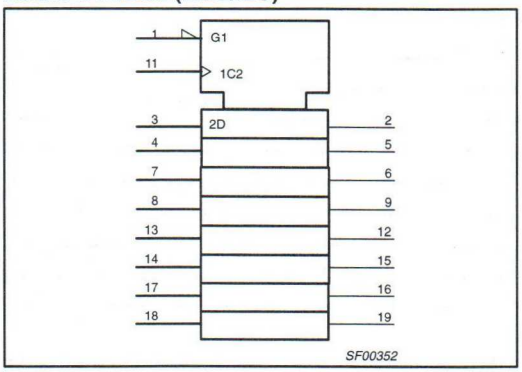
SF00350

LOGIC SYMBOL



SF00351

LOGIC SYMBOL (IEEE/IEC)

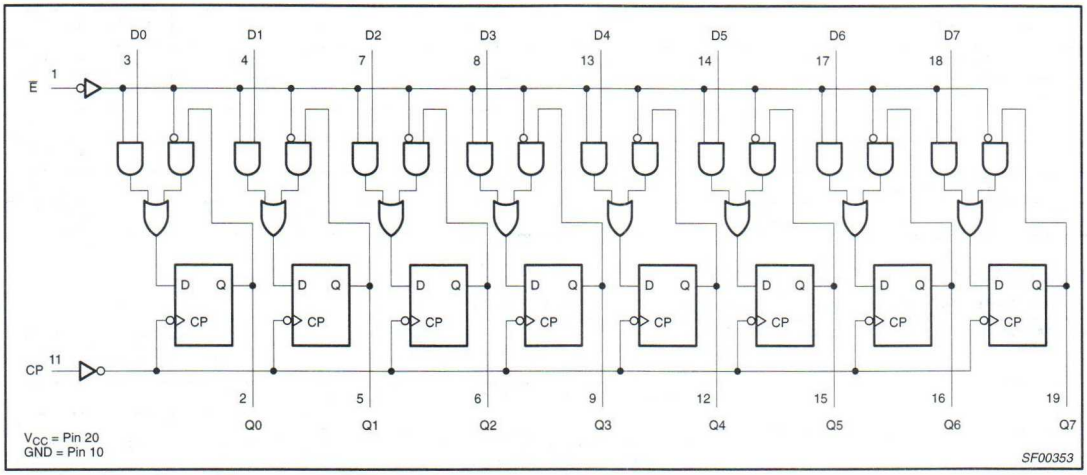


FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{E}$	CP	Dn	Qn	
l	↑	h	H	Load "1"
l	↑	l	L	Load "0"
h H	↑ X	X X	no change no change	Hold (do nothing)

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–1	mA
I_{OL}	Low–level output current			20	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	Ē & CP inputs	V_{CC} = MIN, V_{IL} = 0.0V[3],	±10%V_{CC}	2.5			V
			V_{IH} = 4.5V[3], I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
		Other inputs	V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				–20	µA
I_{OS}	Short circuit output current[4]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			27	40	mA
		I_{CCL}	V_{CC} = MAX			29	43	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. To reduce the effect of external noise during test. Special test conditions are not necessary for the '377A.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

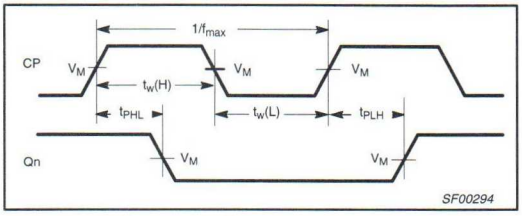
AC CHARACTERISTICS

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_{amb} =0°C to +70°C V_{CC} = +5.0V ±10% C_L = 50pF R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	150	165		120		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	1	3.0 4.5	5.0 6.5	8.0 9.0	2.5 4.0	9.0 10.5	ns

AC SETUP REQUIREMENTS

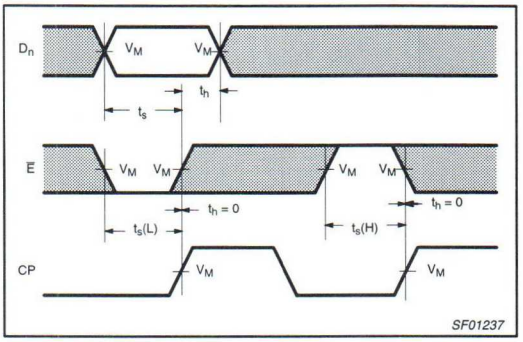
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ±10% C_L = 50pF R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low Dn to CP	2	2.5 2.5			2.5 2.5		ns
t_h(H) t_h(L)	Hold time, High or Low Dn to CP	2	1.0 0.0			1.0 0.0		ns
t_s(H) t_s(L)	Setup time, High or Low $\overline{E}$ to CP	2	3.0 4.0			3.0 4.5		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{E}$ to CP	2	0.0 0.0			0.0 0.0		ns
t_w(H) t_w(L)	Clock Pulse width High or Low	1	4.0 4.0			5.0 4.0		ns

AC WAVEFORMS



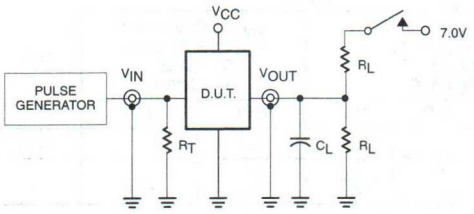
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width and Maximum Clock Frequency

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 2. Data and Enable Setup and Hold Times

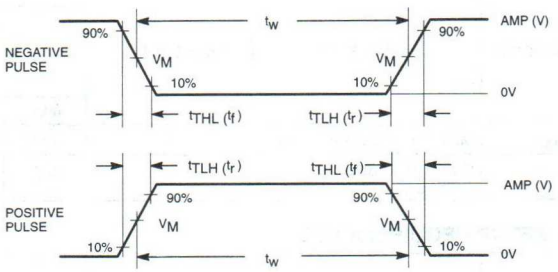
TEST CIRCUIT AND WAVEFORM



Test Circuit for Open Collector Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open



Input Pulse Definition

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

Hex D flip-flop with enable | 74F378

FEATURES

- 6-bit high-speed parallel register
- Positive edge-triggered D-type inputs
- Fully buffered common Clock and Enable inputs
- Input clamp diodes limit high speed termination effects
- Fully TTL and CMOS compatible

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F378	100MHz	35mA

ORDERING INFORMATION

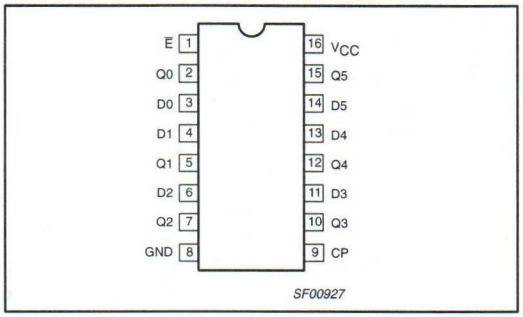
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
16–pin plastic DIP	N74F378N	SOT38-4
16–pin plastic SO	N74F378D	SOT109-1

DESCRIPTION

The 74F378 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Enable ($\overline{E}$) input is Low.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transformed to the corresponding flop-flop's Q output. The $\overline{E}$ input must be stable one setup time prior to the Low-to-High clock transition for predictable operation.

PIN CONFIGURATION

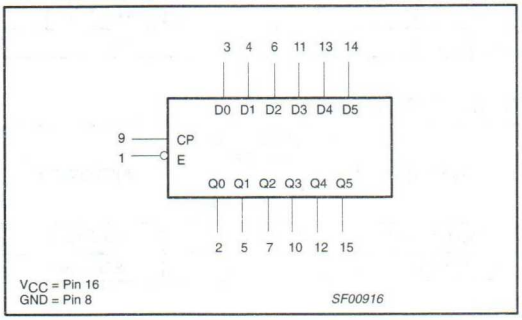


INPUT AND OUTPUT LOADING AND FAN OUT TABLE

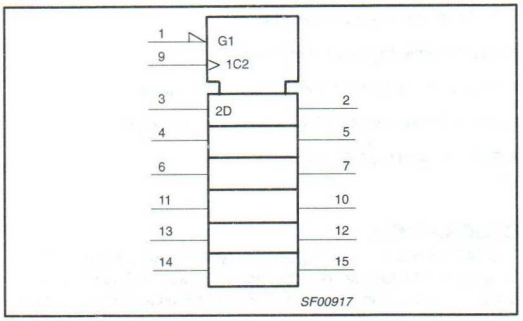
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D5	Data inputs	1.0/1.0	20µA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{E}$	Enable input (active low)	1.0/1.0	20µA/0.6mA
Q0 – Q5	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

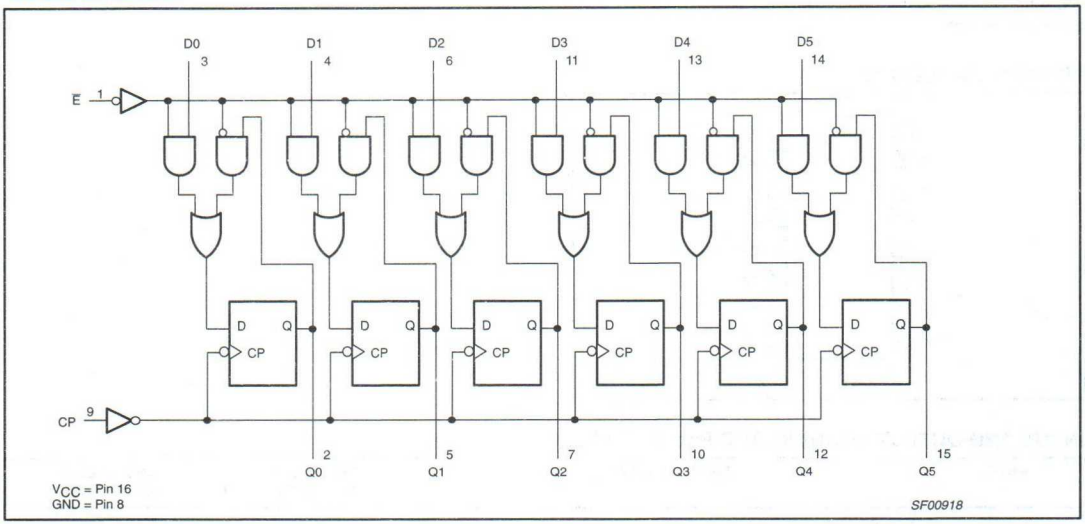
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{E}$	CP	Dn	Qn	
l	↑	h	H	Load "1"
l	↑	l	L	Load "0"
h H	↑ X	X X	no change no change	Hold (do nothing)

H = High-voltage level
h = High-voltage level one setup time prior to the Low-to-High clock transition
L = Low-voltage level
l = Low-voltage level one setup time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARMETER SYMBOL	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			32	45	mA
		I_{CCL}				35	45	mA

Notes:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	80	100		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	Waveform 1	3.0 3.5	5.5 6.0	7.5 8.5	3.0 3.5	8.5 9.5	ns

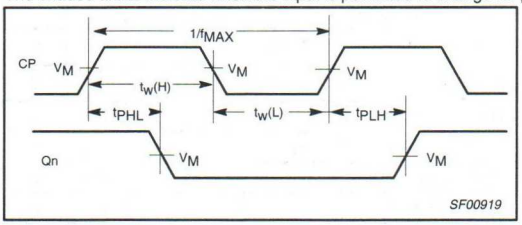
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L= 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s (H) t_s (L)	Setup time, High or Low Dn to CP	Waveform 2	4.0 4.0			4.0 4.0		ns
t_h (H) t_h (L)	Hold time, High or Low Dn to CP	Waveform 2	0 0			0 0		ns
t_s (H) t_s (L)	Setup time, High or Low $\overline{E}$ to CP	Waveform 2	4.0 10.0			4.0 10.0		ns
t_h (H) t_h (L)	Hold time, High or Low $\overline{E}$ to CP	Waveform 2	0 0			0 0		ns
t_w (H) t_w (L)	CP Pulse width, High or Low	Waveform 1	4.0 6.0			4.0 6.0		ns

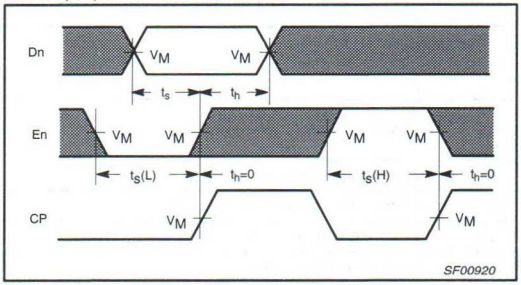
AC WAVEFORMS

For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

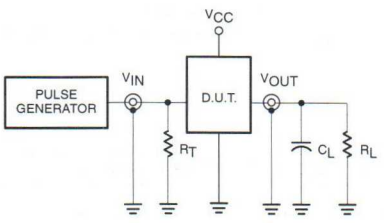


Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

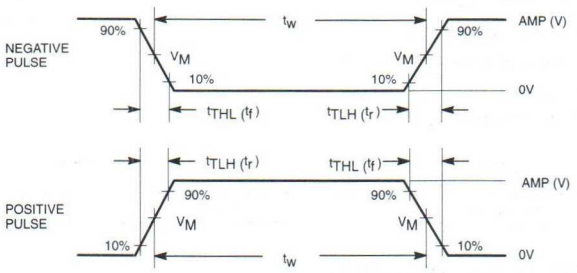


Waveform 2. Data and Enable Setup Time and Hold Times

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Quad register | 74F379A

FEATURES

- Edge–triggered D–type inputs
- Buffered positive edge–triggered clock
- Buffered common enable input
- True and complementary outputs
- Offers light loading PNP inputs (I_{IL} = –20μA)

DESCRIPTION

The 74F379A is a 4–bit register with buffered common enable ($\overline{E}$). This device is similar to the 74F175A but features the common enable rather than common master reset.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F379A	200MHz	29mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG, DWG. #
16–pin plastic DIP	N74F379AN	SOT38–4
16–pin plastic SO	N74F379AD	SOT109–1

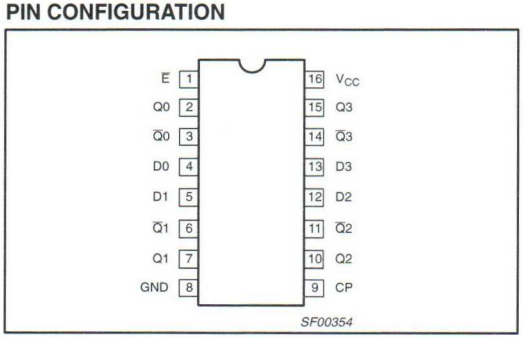
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

TYPE	PINS	DESCRIPTION	74F (U.L.) HIGH/ LOW	LOAD VALUE HIGH/LOW
74F379A	D0 – D3	Data inputs	1.0/0.033	20μA/20μA
	CP	Clock pulse input (active rising edge)	1.0/0.033	20μA/20μA
	$\overline{E}$	Enable input (active low)	1.0/0.033	20μA/20μA
	Q0 – Q3	True outputs	50/33	1.0mA/20mA
	$\overline{Q0}$ – $\overline{Q3}$	Complementary outputs	50/33	15mA/20mA

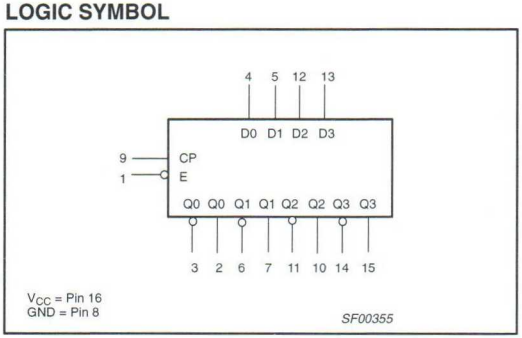
Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.

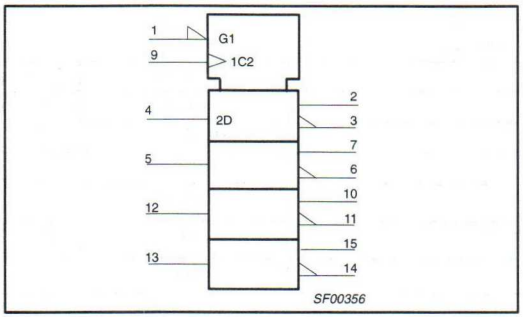
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL



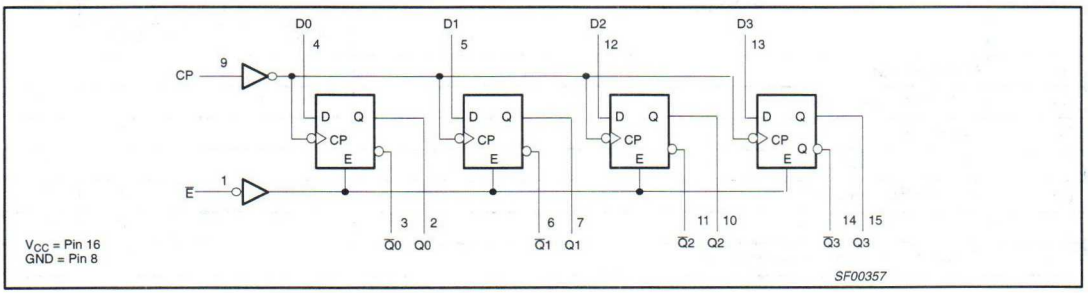
FUNCTION TABLE

INPUTS			OUTPUTS	OUTPUT
$\overline{E}$	CP	Dn	Qn	$\overline{Q}n$
H	↑	X	NC	NC
L	↑	h	H	L
L	↑	l	L	H

Notes to function table

H = High–voltage level
h = High state must be present one setup time before the low–to–high clock transition
L = Low–voltage level
l = Low state must be present one setup time before the low–to–high clock transition
NC= No change
X = Don't care
↑ = Low–to–high clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	40	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–1	mA
I_{OL}	Low–level output current			20	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}		0.35	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			–0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH}	High–level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current					–20	µA
I_{OS}	Short–circuit output current3	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)				29	42	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

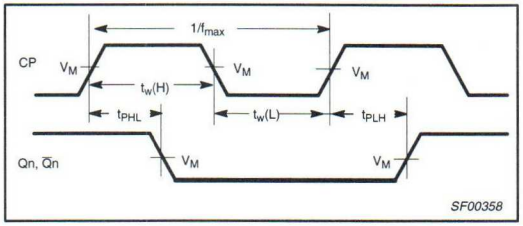
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	175	200		155		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn or $\overline{Q}$n	Waveform 1	2.0 4.0	3.5 5.5	6.5 8.0	2.0 3.5	7.0 8.5	ns

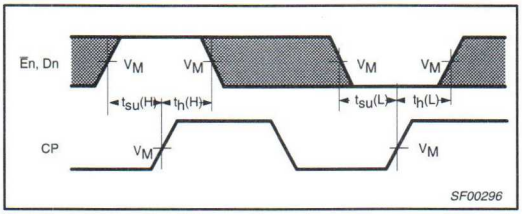
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L= 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low level Dn to CP	Waveform 2	3.0 3.0			3.5 3.5		ns
t_h (H) t_h (L)	Hold time, high or low level Dn to CP	Waveform 2	0 0			0 0		ns
t_{su} (H) t_{su} (L)	Setup time, high or low level $\overline{E}$ to CP	Waveform 2	4.0 3.5			4.5 4.0		ns
t_h (H) t_h (L)	Hold time, high or low level $\overline{E}$ to CP	Waveform 2	0 0			0 0		ns
t_w (H) t_w (L)	CP Pulse width, high or low	Waveform 1	3.5 4.5			3.5 4.5		ns

AC WAVEFORMS



Waveform 1. Propagation delay for clock input to output, clock pulse widths, and maximum clock frequency

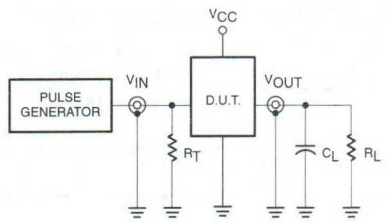


Waveform 2. Data and enable setup time and hold times

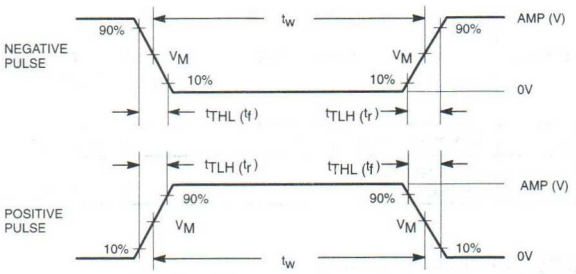
Notes to AC waveforms

1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Arithmetic logic unit 74F382

FEATURES

- Performs six arithmetic and logic functions
- Selectable Low (clear) and High (preset) functions
- Low-input loading minimizes drive requirements
- Carry output for ripple expansion
- Overflow output for Two's Complement arithmetic

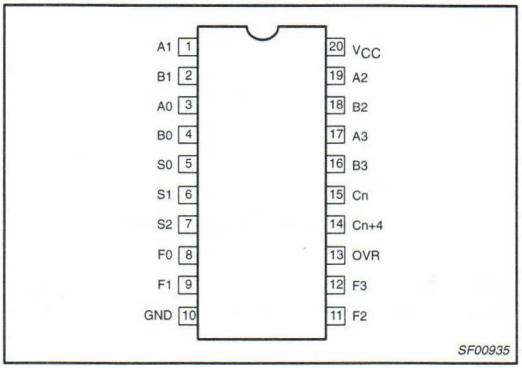
DESCRIPTION

The 74F382 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional Select (S0–S2) input codes force the Function outputs Low or High. An overflow output is provided for convenience in Two's Complement arithmetic.

A carry output is provided for ripple expansion. For high-speed expansion using a carry look-ahead generator, refer to the 74F381 data sheet.

Signals applied to the Select inputs, S0–S2, determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output levels is shown in the Function Table. The circuit performs the arithmetic functions for either active-HIgh or active-Low operands, with output levels in the same convention. In the subtract operating modes, it is necessary to force a carry (High for active-HIgh operands, Low for active-Low operands) into the Cn input of the least significant package. Ripple expansion is illustrated in Figure 1. The overflow output OVR is the Exclusive-OR of Cn+3 and Cn+4; a High signal on OVR indicates overflow in Two's complement operation (See Table 2 for Two's complement arithmetic). Typical delays for Figure 1 are given in Table 1. When the 74F382 is cascaded to handle word lengths longer than 4 bits, only the most significant overflow (OVR) output is used.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F382	7.0ns	54mA

ORDERING INFORMATION

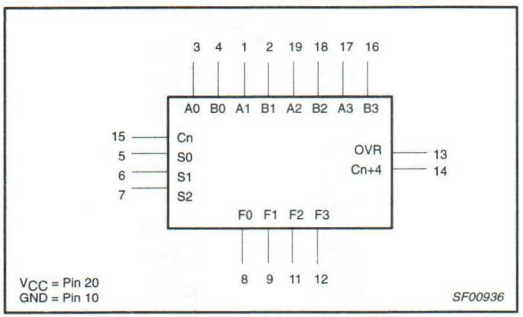
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
20-pin plastic DIP	N74F382N	SOT146-1
20-pin plastic SO	N74F382D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

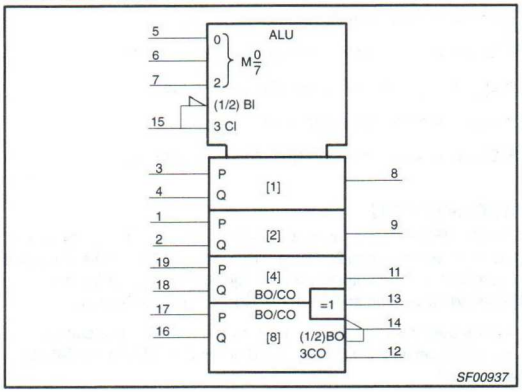
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A3	A operand inputs	1.0/4.0	20µA/2.4mA
B0 – B3	B operand inputs	1.0/4.0	20µA/2.4mA
S0 – S2	Function select inputs	1.0/1.0	20µA/0.6mA
Cn	Carry input	1.0/5.0	20µA/3.0mA
Cn+4	Carry output	50/33	1.0mA/20mA
OVR	Overflow output	50/33	1.0mA/20mA
F0–F3	Outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST unit load is defined as 20µA in the High state and 0.6mA in the Low state.

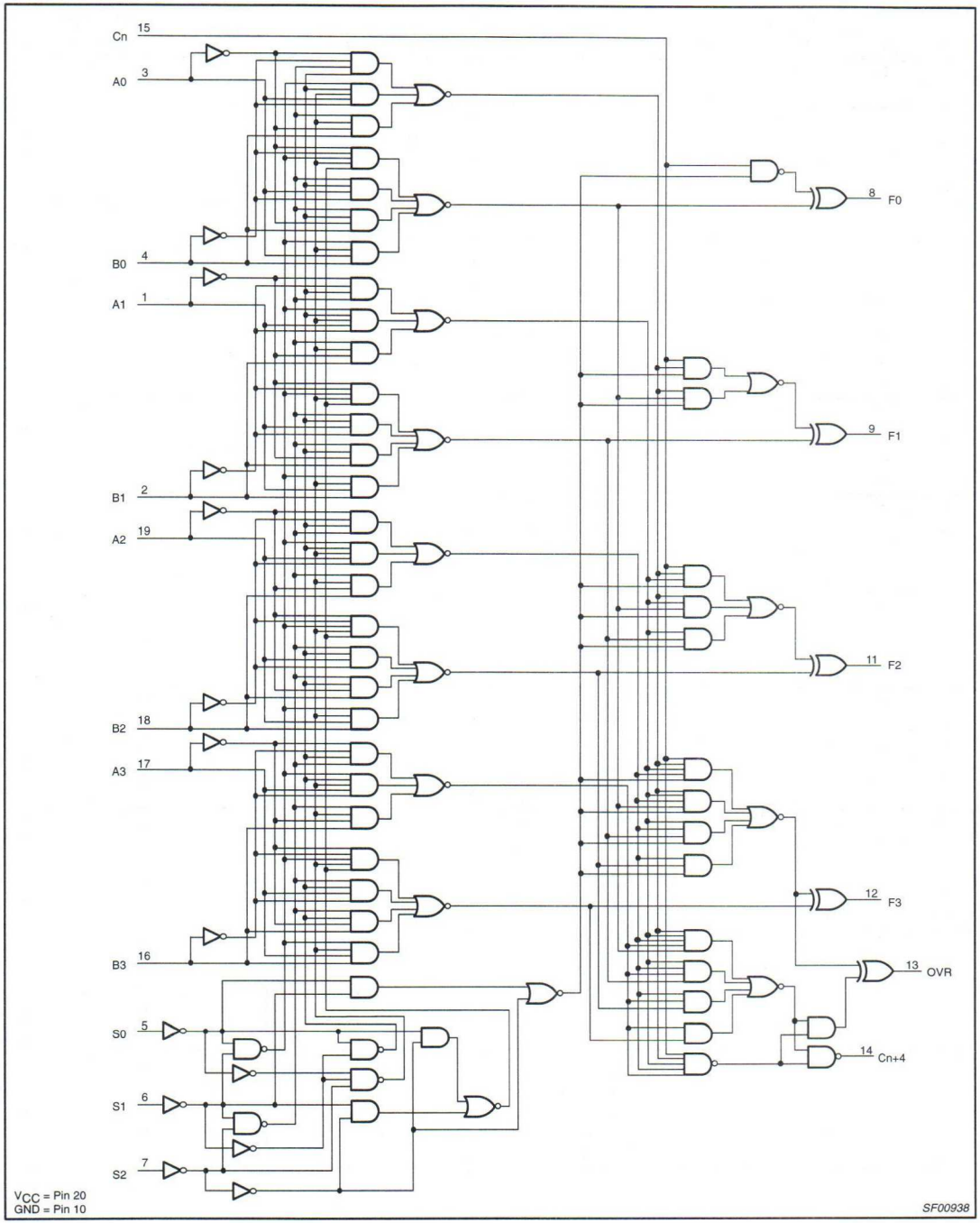
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS						OPERANDS	OPERATING MODE
S0	S1	S2	Cn	An	Bn	F0	F1	F2	F3	OVR	Cn+4		
L	L	L	L	X	X	L	L	L	L	H	H		Clear
L	L	L	H	X	X	L	L	L	L	H	H		
H	L	L	L	L	L	H	H	H	H	L	L	Active-Low	B minus A
H	L	L	L	L	H	L	H	H	H	L	H		
H	L	L	L	H	L	L	L	L	L	L	L		
H	L	L	L	H	H	H	H	H	H	L	L		
H	L	L	H	L	L	L	L	L	L	L	H	Active-High	
H	L	L	H	L	H	H	H	H	H	L	H		
H	L	L	H	H	L	H	L	L	L	L	L		
H	L	L	H	H	H	L	L	L	L	L	H		
L	H	L	L	L	L	H	H	H	H	L	L	Active-Low	A minus B
L	H	L	L	L	H	L	L	L	L	L	L		
L	H	L	L	H	L	L	H	H	H	L	H		
L	H	L	L	H	H	H	H	H	H	L	L		
L	H	L	H	L	L	L	L	L	L	L	H	Active-High	
L	H	L	H	L	H	H	L	L	L	L	L		
L	H	L	H	H	L	H	H	H	H	L	H		
L	H	L	H	H	H	L	L	L	L	L	H		
H	H	L	L	L	L	L	L	L	L	L	L		A Plus B
H	H	L	L	L	H	H	H	H	H	L	L		
H	H	L	L	H	L	H	H	H	H	L	L		
H	H	L	L	H	H	L	H	H	H	L	H		
H	H	L	H	L	L	H	L	L	L	L	L		
H	H	L	H	L	H	L	L	L	L	L	H		
H	H	L	H	H	L	L	L	L	L	L	H		
H	H	L	H	H	H	H	H	H	H	L	H		
L	L	H	X	L	L	L	L	L	L	L	L		A ⊕ B
L	L	H	X	L	H	H	H	H	H	L	L		
L	L	H	L	H	L	H	H	H	H	L	L		
L	L	H	X	H	H	L	L	L	L	H	H		
L	L	H	H	H	L	H	H	H	H	H	H		
H	L	H	X	L	L	L	L	L	L	L	L		A + B
H	L	H	X	L	H	H	H	H	H	L	L		
H	L	H	X	H	L	H	H	H	H	L	L		
H	L	H	L	H	H	H	H	H	H	L	L		
H	L	H	H	H	H	H	H	H	H	H	H		
L	H	H	X	L	L	L	L	L	L	H	H		AB
L	H	H	X	L	H	L	L	L	L	L	L		
L	H	H	X	H	L	L	L	L	L	H	H		
L	H	H	L	H	H	H	H	H	H	L	L		
L	H	H	H	H	H	H	H	H	H	H	H		
H	H	H	X	L	L	H	H	H	H	L	L		Preset
H	H	H	X	L	H	H	H	H	H	L	L		
H	H	H	X	H	L	H	H	H	H	L	L		
H	H	H	L	H	H	H	H	H	H	L	L		
H	H	H	H	H	H	H	H	H	H	H	H		

H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION SELECT TABLE

SELECT			OPERATING MODE
S0	S1	S2	
L	L	L	Clear
H	L	L	B minus A
L	H	L	A minus B
H	H	L	A Plus B
L	L	H	A ⊕ B
H	L	H	A + B
L	H	H	AB
H	H	H	Preset

H = High voltage level
L = Low voltage level

Table 1. 16-Bit Delay Tabulation

PATH SEGMENT	TOWARD F	OUTPUT Cn+4, OVR
Ai or Bi to Cn+4	6.5ns	6.5ns
Cn to Cn+4	6.3ns	6.3ns
Cn to Cn+4	6.3ns	6.3ns
Cn to F	8.1ns	–
Cn to Cn+4, OVR	–	8.0ns
Total Delay	27.2ns	27.1ns

Table 2. Two's Complement Arithmetic

MSB			LSB	Numerical Values
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	–8
H	L	L	H	–7
H	L	H	L	–6
H	L	H	H	–5
H	H	L	L	–4
H	H	L	H	–3
H	H	H	L	–2
H	H	H	H	–1

H = High voltage level
L = Low voltage level

APPLICATION

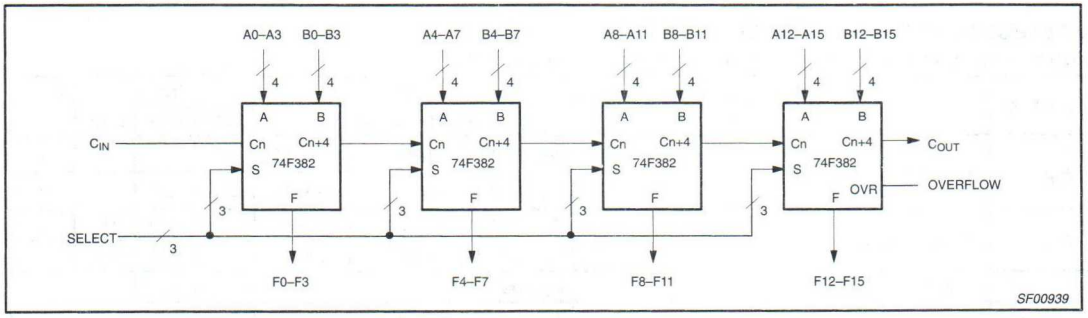


Figure 1. 16-bit Look-ahead Carry ALU Expansion

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARMETER SYMBOL	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	Cn	V_{CC} = MAX, V_I = 0.5V				−3.0	mA
		A0–A3, B0–B3					−2.4	mA
		S0, S1, S2					−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			54	81	mA

NOTES:

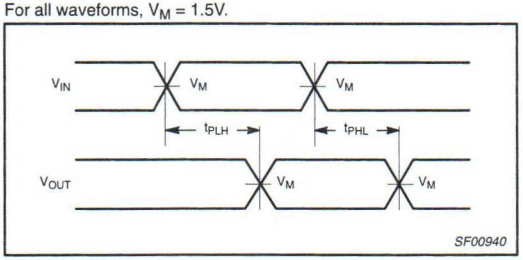
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Cn to Fn	Waveform 1	3.0 2.5	7.0 4.5	12.0 6.5	2.5 2.5	13.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay An or Bn to Fn	Waveform 1	3.5 3.0	8.0 6.0	13.5 10.0	3.5 2.5	17.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay Si to Fi	Waveform 1	5.5 5.5	9.0 7.5	15.0 10.5	5.5 5.5	16.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay Ai to Bi to Cn+4	Waveform 1	3.5 3.5	7.0 6.5	10.5 9.5	3.5 3.5	11.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay Si to OVR or Cn+4	Waveform 1	7.0 5.0	10.5 8.0	14.5 11.0	6.5 5.0	17.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay Cn to Cn+4	Waveform 1	3.0 3.5	4.5 5.0	6.0 6.5	2.5 3.5	6.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay Cn to OVR	Waveform 1	4.5 3.0	9.0 5.0	13.5 6.5	4.0 3.0	15.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay Ai or Bi to OVR	Waveform 1	6.0 3.5	9.0 6.5	12.5 9.0	5.5 3.5	16.5 10.0	ns

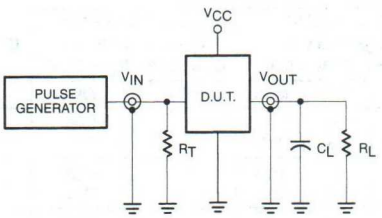
AC WAVEFORMS

For all waveforms, V_M = 1.5V.

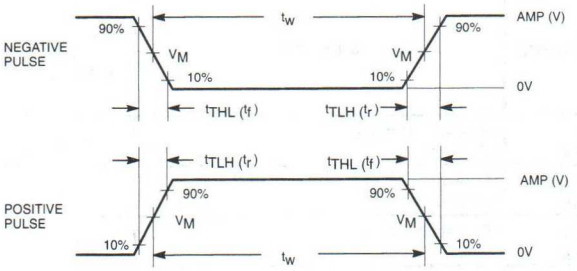


Waveform 1. Propagation Delay for Non-Inverting or Inverting paths

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor;
see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Dual 4-bit binary ripple counter | 74F393

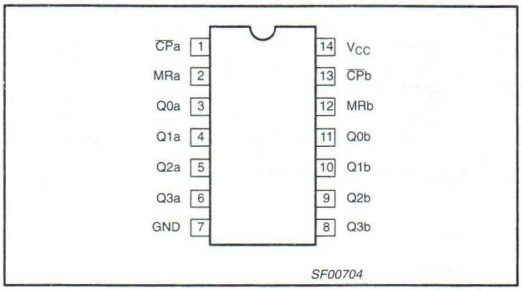
FEATURES

- Two 4-bit binary counters
- Two Master Resets to clear each 4-bit counter individually

DESCRIPTION

The 74F393 is a Dual Ripple Counter with separate Clock ($\overline{CP}_n$) and Master Reset (MR) inputs to each counter. The two counters are identified by the "a" and "b" suffixes in the pin configuration. The operation of each half of the 74F393 is the same. The counters are triggered by a High-to-Low transition of the Clock ($\overline{CP}_a$ and $\overline{CP}_b$) inputs. The counter outputs are internally connected to provide Clock inputs to succeeding stages. The outputs of the ripple counter do not change synchronously and should not be used for high speed address decoding. The Master Resets (MR_a and MR_b) are active High asynchronous inputs; one for each 4-bit counter. A High level in the MR input overrides the Clock and sets the outputs Low.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F393	125MHz	40mA

ORDERING INFORMATION

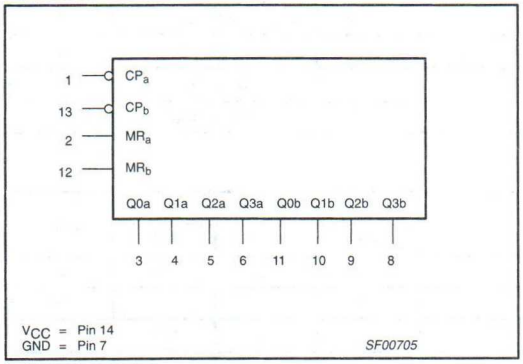
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
14-pin plastic DIP	N74F393N	SOT27-1
14-pin plastic SO	N74F393D	SOT108-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

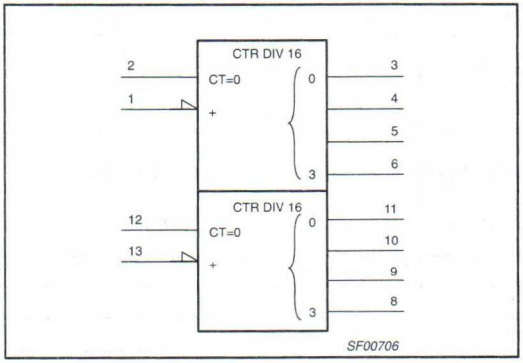
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{CP}_a$, $\overline{CP}_b$	Clock inputs	1.0/1.0	20μA/0.6mA
MR_a, MR_b	Master Reset inputs	1.0/1.0	20μA/0.6mA
Q_{na} – Q_{nb}	Data outputs	50/33.3	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

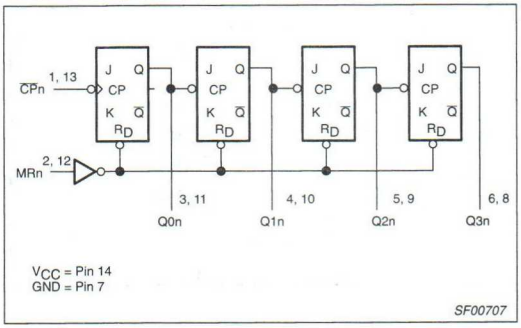
LOGIC SYMBOL



IEC/IEEE SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

COUNT	OUTPUTS			
	Q_{0n}	Q_{1n}	Q_{2n}	Q_{3n}
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

H = High voltage level transition
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			25	36	mA
		I_{CCL}				42	58	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

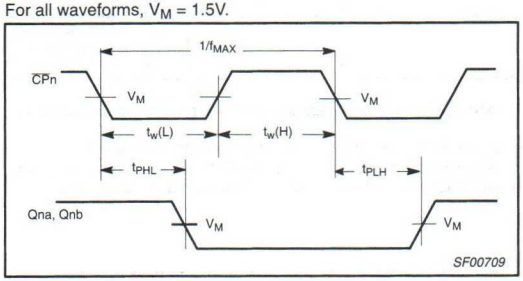
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	100	130		100		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$n to Q0a or Q0b	Waveform 1	3.5 5.0	5.5 7.0	8.0 10.0	3.5 5.0	9.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$n to Q1a, Q1b	Waveform 1	5.0 7.5	7.0 9.5	10.0 12.0	4.5 7.0	13.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$n to Q2a, Q2b	Waveform 1	8.0 9.5	10.0 11.5	13.0 14.5	7.0 9.0	15.0 15.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$n to Q3a, Q3b	Waveform 1	10.5 12.0	12.5 14.0	15.5 16.5	10.0 11.5	17.0 17.5	ns
t_{PHL}	Propagation delay MR to Qna, Qnb	Waveform 2	4.0	6.0	9.0	4.0	9.0	ns

AC SETUP REQUIREMENTS

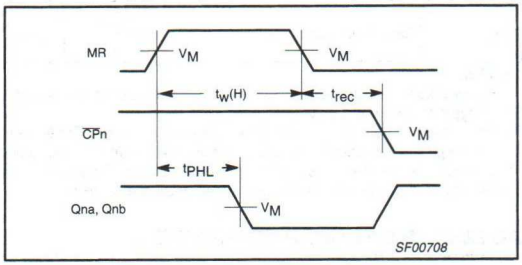
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_W(H)$ $t_W(L)$	$\overline{CP}n$ Pulse width High or Low	Waveform 1	4.5 3.5			5.0 4.0		ns
$t_W(H)$	MR Pulse width High	Waveform 2	3.5			4.5		ns
t_{REC}	Recovery time MR to $\overline{CP}n$	Waveform 2	2.5			3.0		ns

AC WAVEFORMS

For all waveforms, V_M = 1.5V.

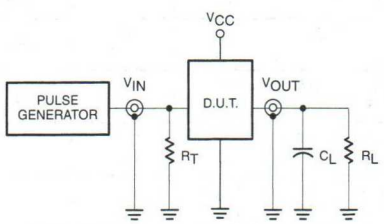


Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

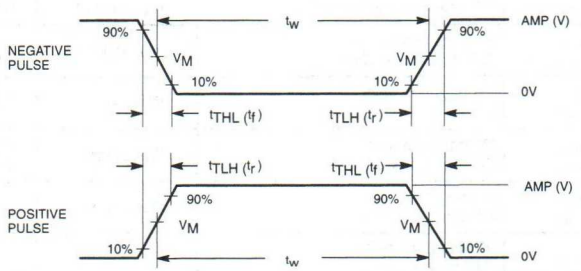


Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay, and Master Reset to Clock Recovery Time

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

74F398 Quad 2-Port Register with True and Complementary Outputs
74F399 Quad 2-Port Register

FEATURES

- Select inputs from two data sources
- Fully positive edge-triggered
- Both True and Complementary outputs–74F398

DESCRIPTION

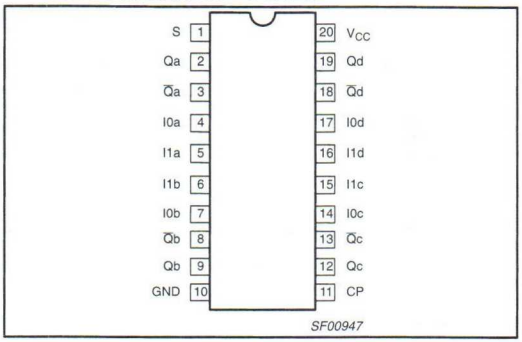
The 74F398 and 74F399 are the logical equivalent of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of two 4-bit words is accepted. The selected data enters the flip-flops on the rising edge of the clock.

The 74F399 is the 16-pin version of the 74F398, with only the true (Qn) outputs of the flip-flops available.

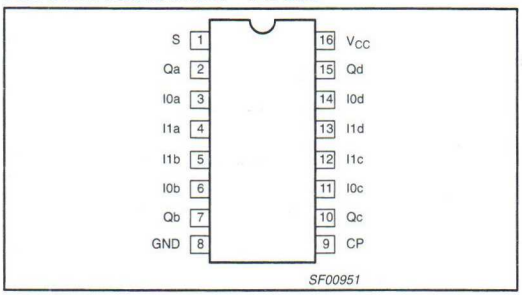
The 74F398 and 74F399 are high speed quad 2-port registers. They select 4 bits of data from either of two sources (Ports) under control of a common select input (S). The selected data is transferred to a 4-bit output register synchronous with the Low-to-High transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I0n, I1n) and Select input (S) must be stable only a setup time prior to and hold time after the Low-to-High transition of the Clock input for predictable operation. The 74F398 has both Q and $\overline{Q}$ outputs.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F398	120MHz	25mA
74F399	120MHz	22mA

PIN CONFIGURATION – 74F398



PIN CONFIGURATION – 74F399



ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
16-pin plastic DIP	N74F399N	SOT38-4
16-pin plastic SO	N74F399D	SOT109-1

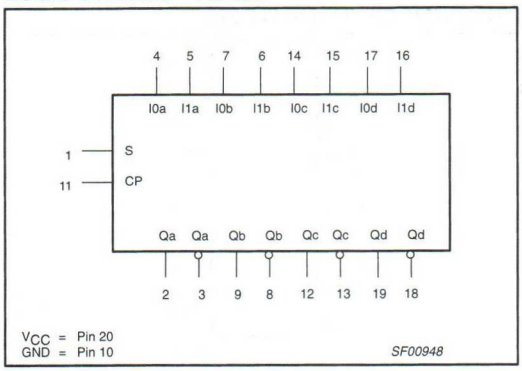
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I0a, I0b, I0c, I0d	Data inputs from source 0	1.0/1.0	20µA/0.6mA
I1a, I1b, I1c, I1d	Data inputs from source 1	1.0/1.0	20µA/0.6mA
S	Common Select input	1.0/1.0	20µA/0.6mA
CP	Clock input (active rising edge)	1.0/1.0	20µA/0.6mA
Qa, Qb, Qc, Qd	Register true outputs	50/33	1.0mA/20mA
$\overline{Q}$a, $\overline{Q}$b, $\overline{Q}$c, $\overline{Q}$d	Register complementary outputs (74F398)	50/33	1.0mA/20mA

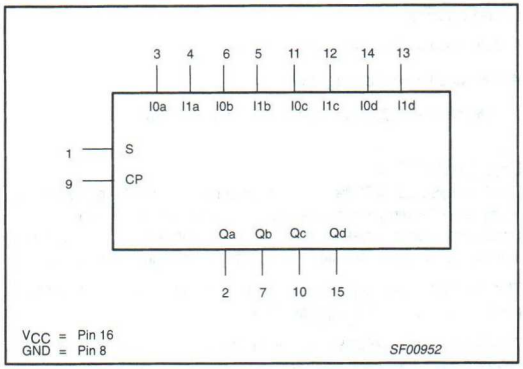
NOTE:
One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

* *Discontinued part. Please see the Discontinued Products List..*

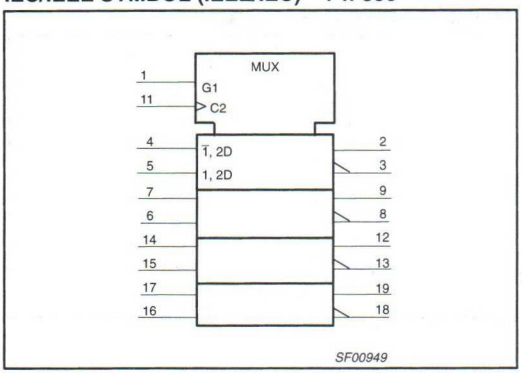
LOGIC SYMBOL – 74F398



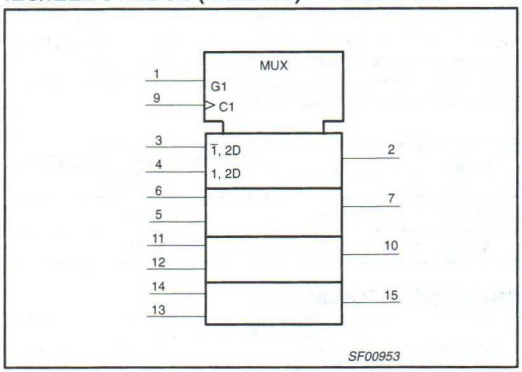
LOGIC SYMBOL – 74F399



IEC/IEEE SYMBOL (IEEE/IEC) – 74F398



IEC/IEEE SYMBOL (IEEE/IEC) – 74F399



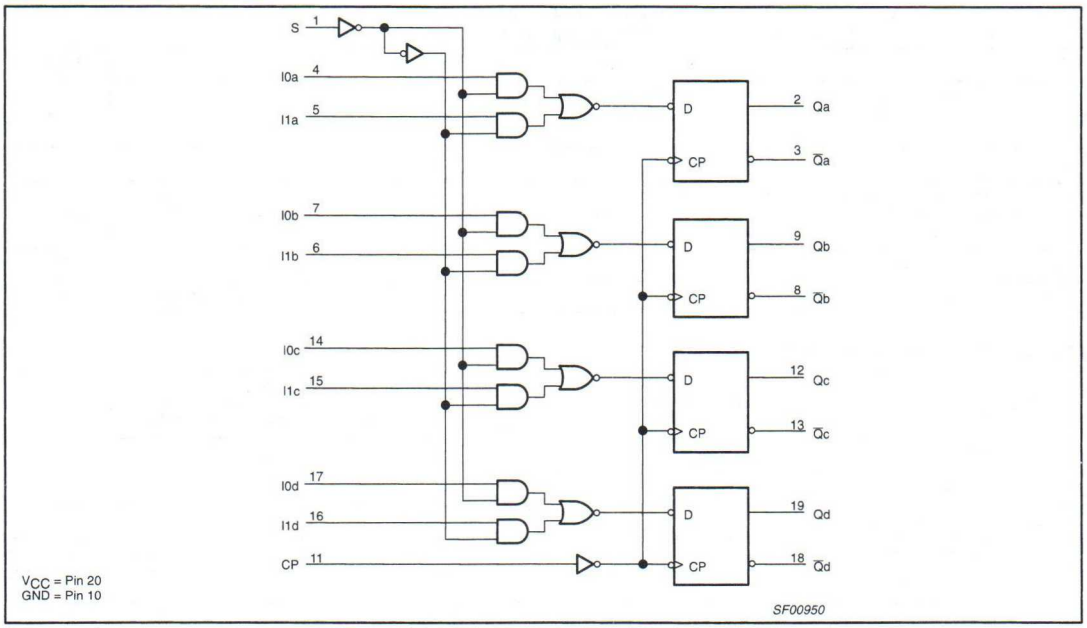
FUNCTION TABLE

INPUTS				OUTPUTS	
CP	S	I0n	I1n	Qn	$\overline{Q}$n (74F398 only)
↑	l	l	X	L	H
↑	l	h	X	H	L
↑	h	X	l	L	H
↑	h	X	h	H	L

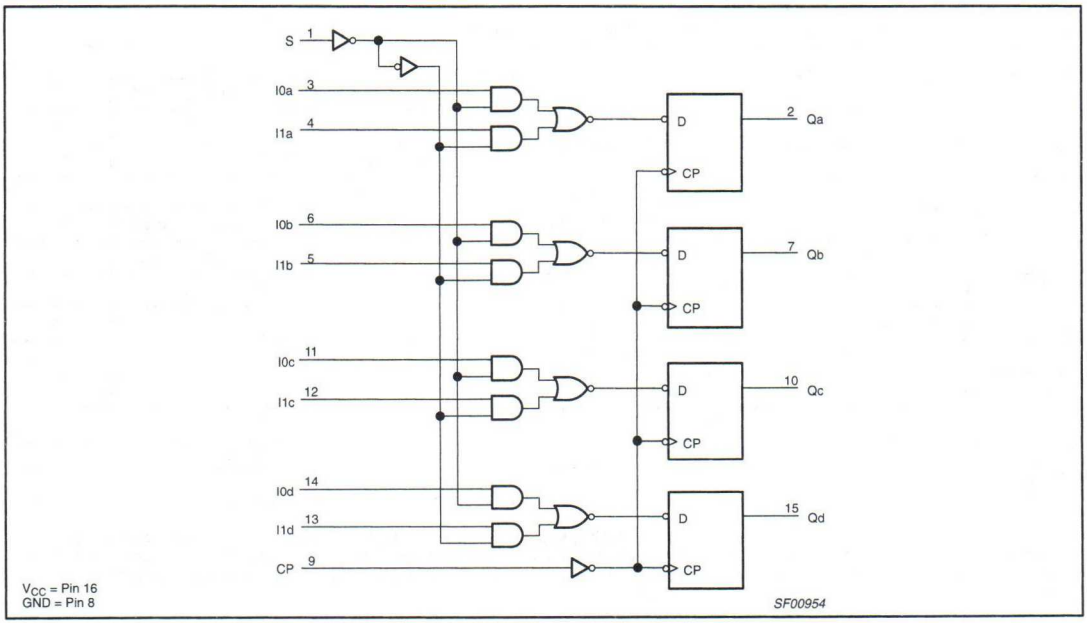
H = High voltage level
h = High voltage level one setup time prior to the High-to-Low clock transition
L = Low voltage level
l = Low voltage level one setup time prior to the High-to-Low clock transition
X = Don't care
↑ = Low-to-High clock transition

** Discontinued part. Please see the Discontinued Products List..*

LOGIC DIAGRAM – 74F398



LOGIC DIAGRAM – 74F399



* *Discontinued part. Please see the Discontinued Products List..*

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
				±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	74F398	V_{CC} = MAX			25	38	mA
		74F399				22	34	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

** Discontinued part. Please see the Discontinued Products List..*

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	100	120		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn or $\overline{Q}$n	Waveform 1	3.0 3.0	5.7 6.5	7.5 8.5	3.0 3.0	8.5 9.0	ns

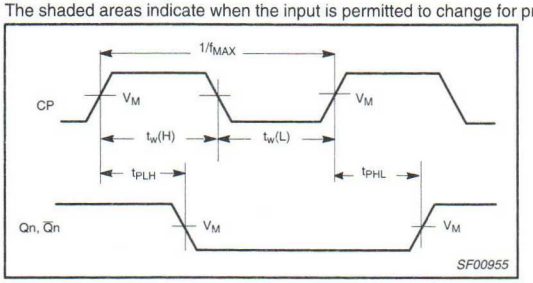
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low I0n, I1n to CP	Waveform 2	3.0 3.0			3.0 3.0		ns
t_h(H) t_h(L)	Hold time, High or Low I0n, I1n to CP	Waveform 2	1.0 1.0			1.0 1.0		ns
t_s(H) t_s(L)	Setup time, High or Low S to CP	Waveform 2	7.5 7.5			8.5 8.5		ns
t_h(H) t_h(L)	Hold time, High or Low S to CP	Waveform 2	0 0			0 0		ns
t_W(H) t_W(L)	CP Pulse width High or Low	Waveform 1	4.0 6.0			4.0 6.0		ns

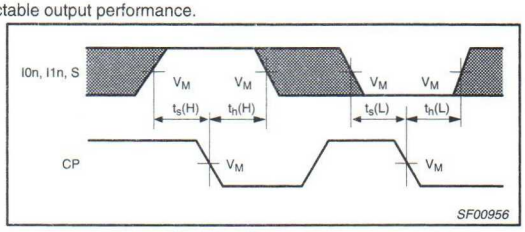
AC WAVEFORMS

For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.



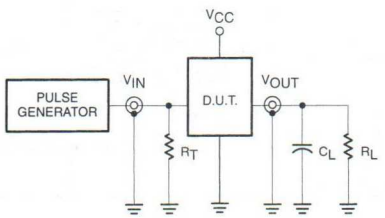
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



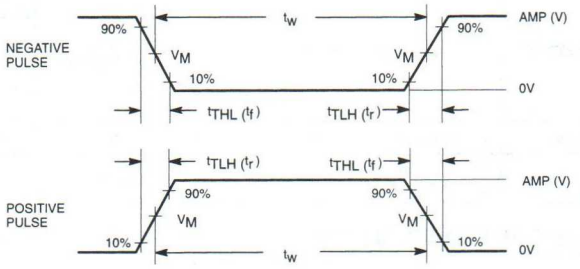
Waveform 2. Data and Select Setup and Hold Times

* *Discontinued part. Please see the Discontinued Products List..*

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

* *Discontinued part. Please see the Discontinued Products List..*

Buffers/Drivers

~~74F455,~~* 74F456

74F455 Octal Buffer/Driver with Parity, Inverting (3-State)
74F456 Octal Buffer/Driver with Parity, Non-Inverting (3-State)

FEATURES

- High impedance NPN base inputs for reduced loading (40µA in High and Low states)
- 74F456 combines 74F244 and 74F280A functions in one package
- 74F456 is a center pin version of the 74F656A
- 74F456 Non-Inverting
- 3-State outputs sink 64mA and source 15mA
- 24-pin plastic Slim DIP (300 mil) package
- Broadside pinout simplifies PC board layout

DESCRIPTION

The 74F455 and 74F456 are octal buffers and line drivers with parity generation/checking designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers. These parts include parity generator/checker to improve PC board density.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F455	6.5ns	64mA
74F456	7.5ns	64mA

ORDERING INFORMATION

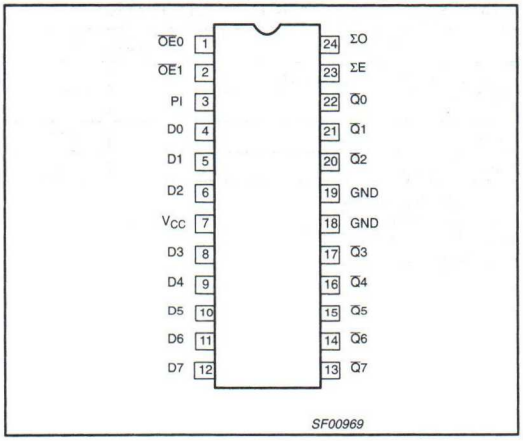
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
24-pin plastic Slim DIP (300mil)	N74456N	SOT222-1
24-pin plastic SOL	N74456D	SOT137-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0–D7	Data inputs	2.0/0.066	40µA/40µA
PI	Parity input	1.0/0.033	20µA/20µA
$\overline{OE}$0, $\overline{OE}$1	Output Enable inputs (active Low)	1.0/0.033	20µA/20µA
ΣE, ΣO	Parity outputs	750/106.7	15mA/64mA
$\overline{Q}$0–$\overline{Q}$7	Data outputs (75F455)	750/106.7	15mA/64mA
Q0–Q7	Data outputs (75F456)	750/106.7	15mA/64mA

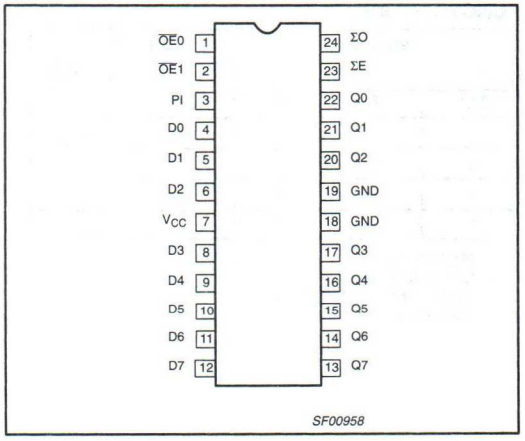
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION – 74F455



SF00969

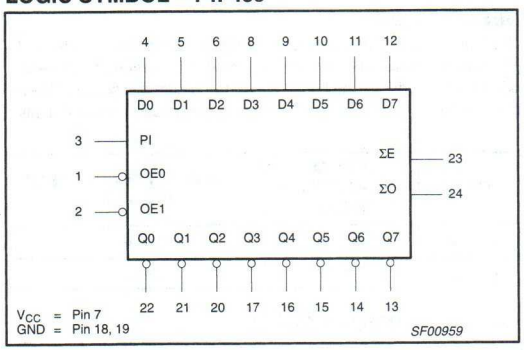
PIN CONFIGURATION – 74F456



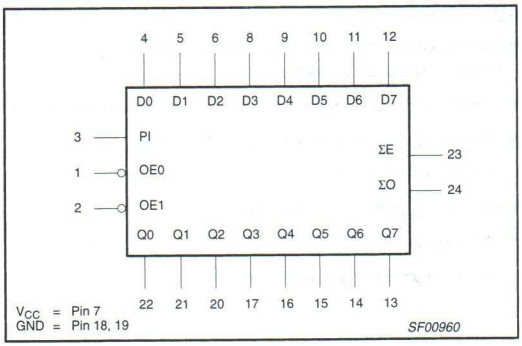
SF00958

* *Discontinued part. Please see the Discontinued Products List.*

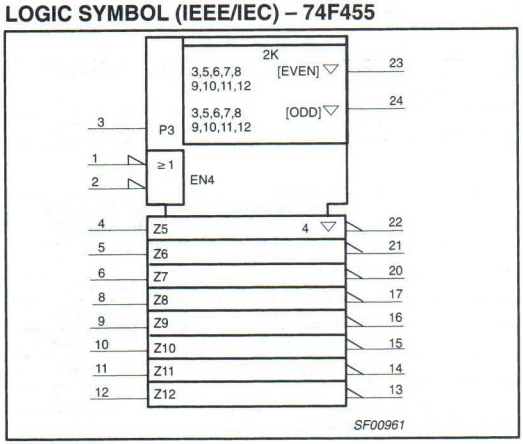
LOGIC SYMBOL – 74F455



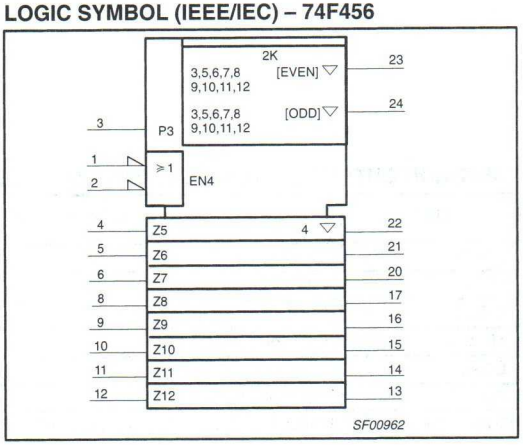
LOGIC SYMBOL – 74F456



LOGIC SYMBOL (IEEE/IEC) – 74F455



LOGIC SYMBOL (IEEE/IEC) – 74F456



FUNCTION TABLE

INPUTS			OUTPUTS	
			74F455	74F456
$\overline{OE0}$	$\overline{OE1}$	Dn	$\overline{Qn}$	Qn
L	L	L	H	L
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z

H = High voltage level
L = Low voltage level
Z = High impedance "off" state
X = Don't care

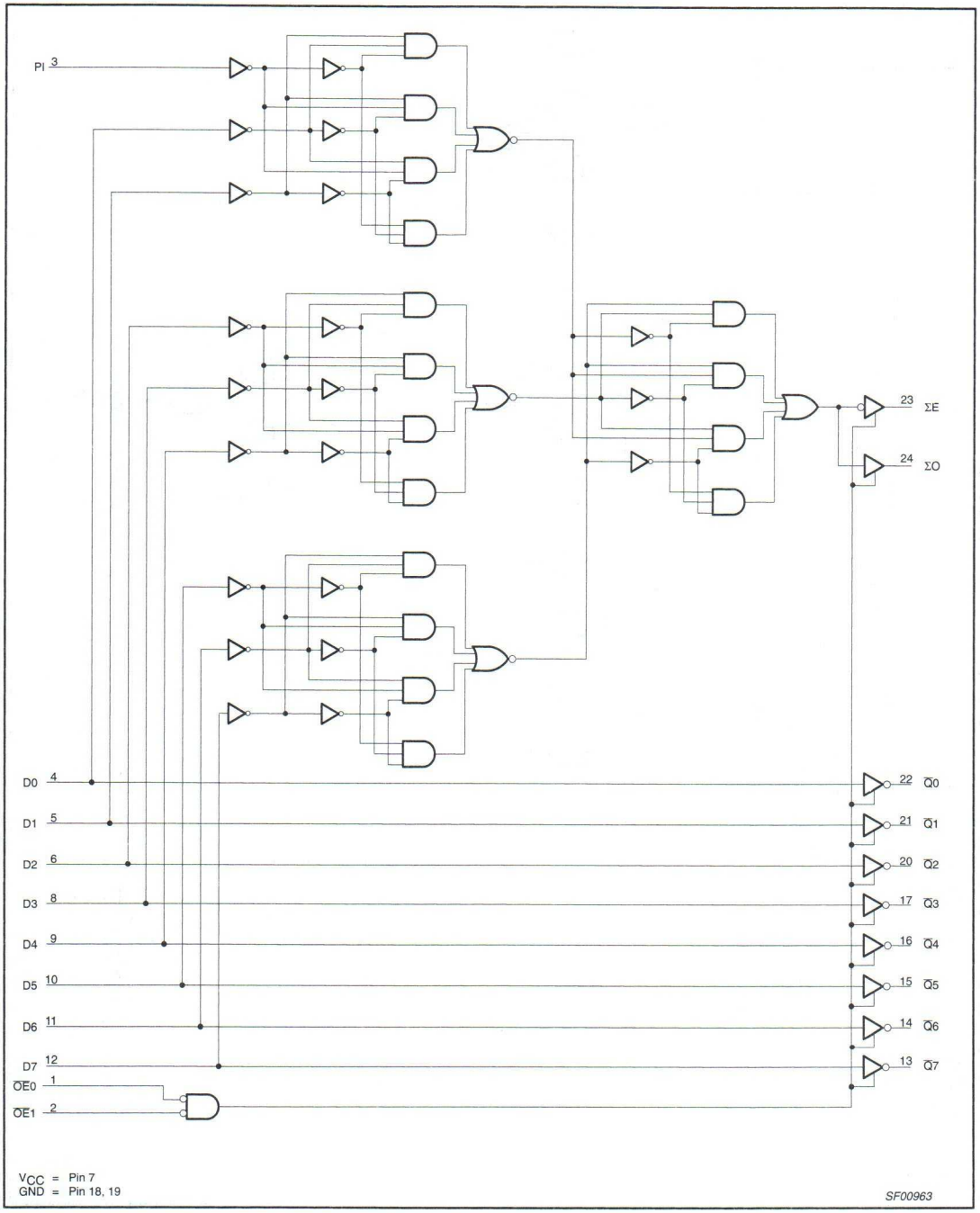
FUNCTION TABLE for PARITY OUTPUTS

INPUTS	OUTPUTS	
Number of inputs, High (PI, D0 - D7)	ΣE	ΣO
Even - 0, 2, 4, 6, 8	H	L
Odd - 1, 3, 5, 7, 9	L	H
Any $\overline{OE}$n = High	Z	Z

H = High voltage level
L = Low voltage level
Z = High impedance "off" state
X = Don't care

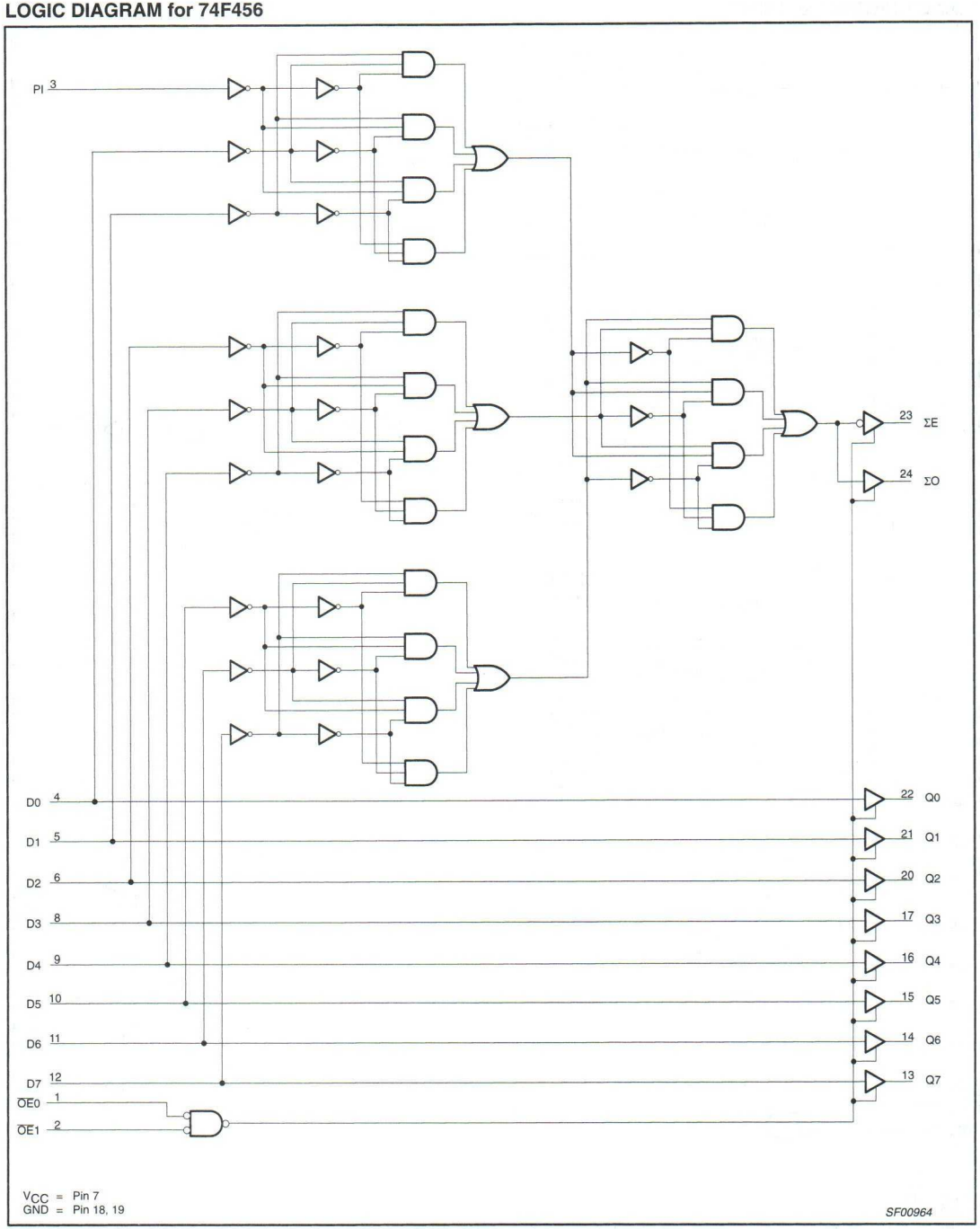
** Discontinued part. Please see the Discontinued Products List.*

LOGIC DIAGRAM for 74F455



* *Discontinued part. Please see the Discontinued Products List.*

LOGIC DIAGRAM for 74F456



* *Discontinued part. Please see the Discontinued Products List.*

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–15	mA
I_{OL}	Low-level output current			64	mA
T_{amb}	Operating free-air temperature range	0		70	°C

* *Discontinued part. Please see the Discontinued Products List.*

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=–3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
				I_{OH} =–15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	Dn	V_{CC} = MAX, V_I = 2.7V					40	µA
		PI, $\overline{OE}$n						20	µA
I_{IL}	Low-level input current	Dn	V_{CC} = MAX, V_I = 0.5V					–40	µA
		PI, $\overline{OE}$n						–20	µA
I_{OZH}	Off-state output current High-level voltage applied		V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			–100		–225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				50	80	mA
		I_{CCL}					78	110	mA
		I_{CCZ}					63	90	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

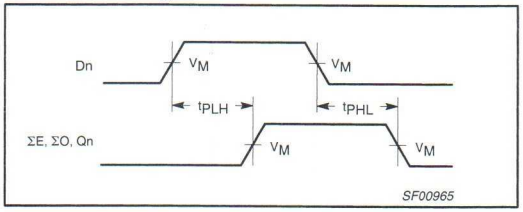
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				V_{CC} = +5V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to $\overline{Q}$n	74F455	Waveform 2	2.0 1.0	4.5 2.0	6.5 4.0	2.0 1.0	7.5 4.5	ns
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	74F456	Waveform 1	2.0 2.5	4.5 5.0	6.5 7.0	2.0 2.5	7.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay Dn to ΣE, ΣO		Waveform 1, 2	5.5 5.5	10.0 11.0	13.0 14.5	5.5 5.5	14.0 16.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	2.5 4.0	4.0 8.0	8.0 10.5	2.5 4.0	9.0 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 3 Waveform 4	1.5 2.0	4.0 5.0	6.5 7.5	1.5 2.0	7.5 8.0	ns

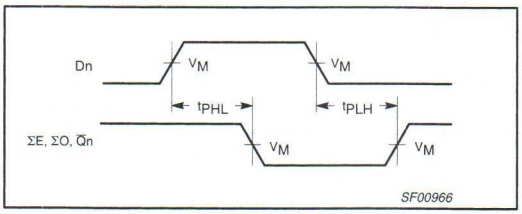
* *Discontinued part. Please see the Discontinued Products List.*

AC WAVEFORMS

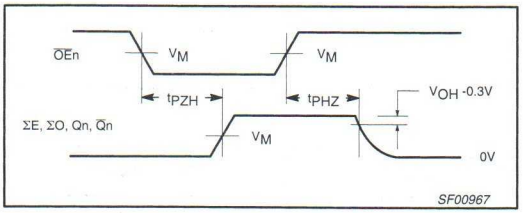
For all waveforms, V_M = 1.5V.



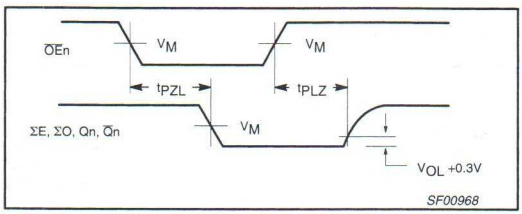
Waveform 1. Propagation Delay, Non-Inverting Outputs



Waveform 2. Propagation Delay, Inverting Outputs

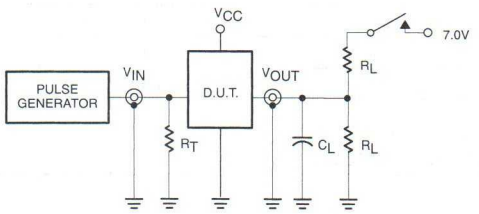


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

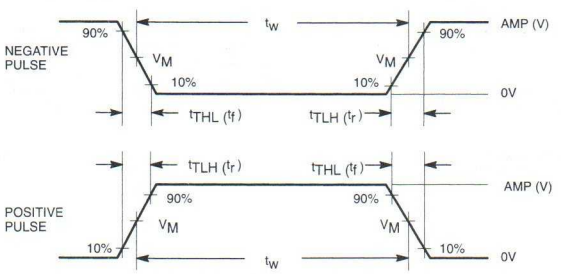


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

* *Discontinued part. Please see the Discontinued Products List.*

8-bit identity comparator | 74F521

FEATURES

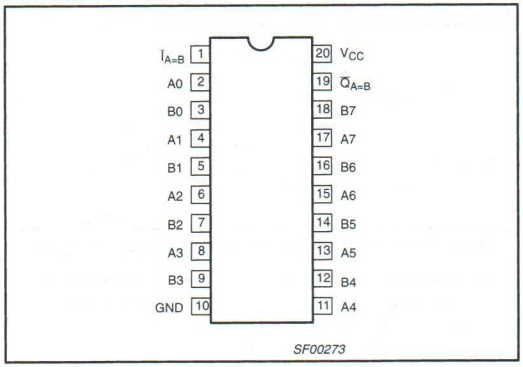
- Compares two 8-bit words in 6.5ns typical
- Expandable to any word length

DESCRIPTION

The 74F521 is an expandable 8-bit comparator. It compares two words of up to 8 bits each and provides a Low output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active-Low enable input.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F521	7.0ns	24mA

PIN CONFIGURATION



ORDERING INFORMATION

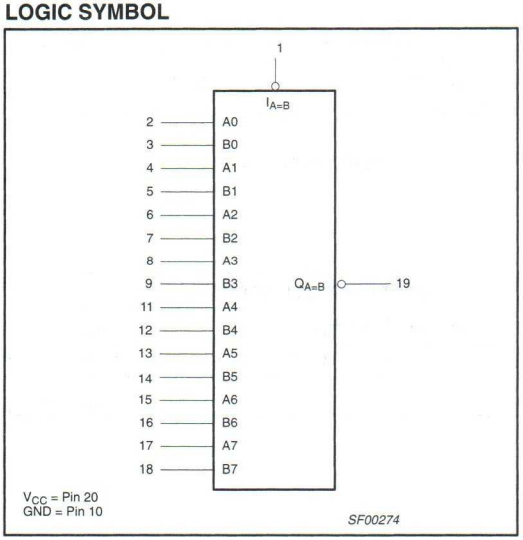
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
20-pin plastic DIP	N74F521N	SOT146-1
20-pin plastic SOL	N74F521D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

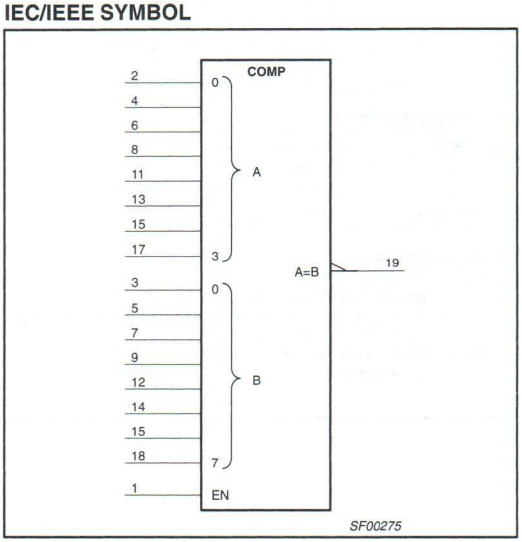
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A7	Word A inputs	1.0/1.0	20µA/0.6mA
B0 – B7	Word B inputs	1.0/1.0	20µA/0.6mA
$\overline{I}_{A=B}$	Expansion or Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{Q}_{A=B}$	Identity output (active Low)	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

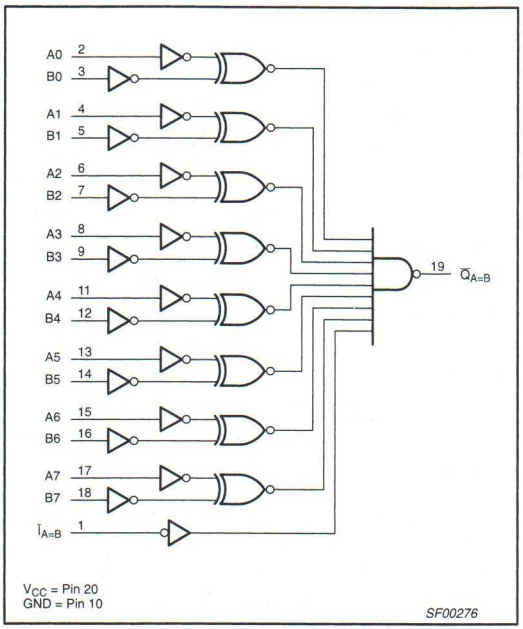
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM

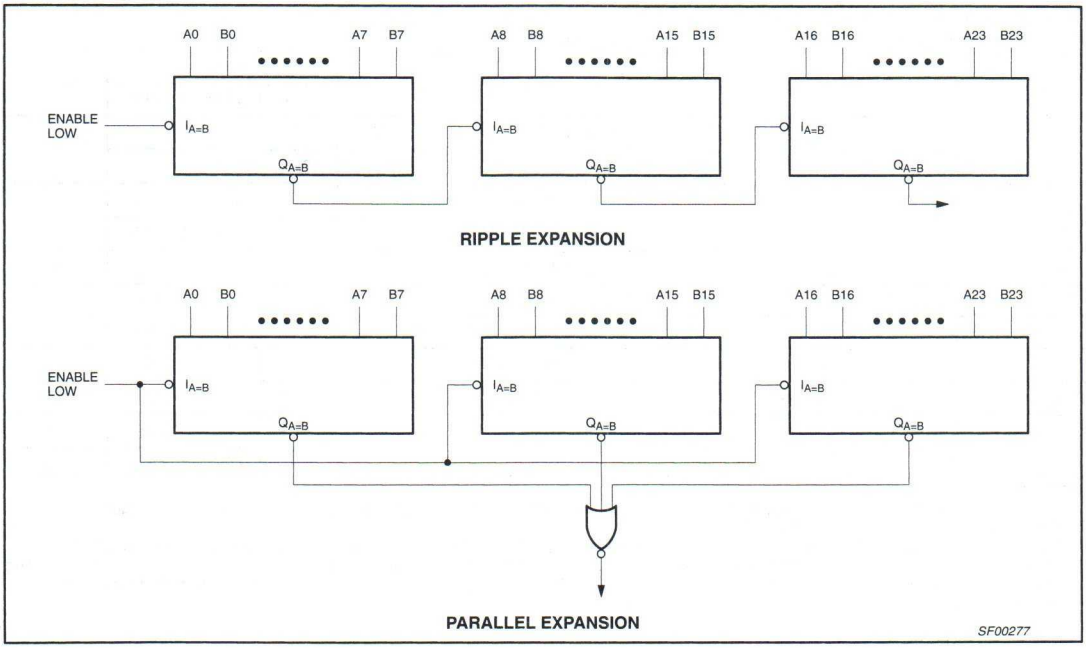


FUNCTION TABLE

INPUTS		OUTPUT
$\overline{I}_{A=B}$	A, B	$\overline{Q}_{A=B}$
L	A=B*	L
L	A≠B	H
H	A=B*	H
H	A≠B	H

H = High voltage level
L = Low voltage level
X = Don't care
* A0=B0, A1=B1, A2=B2, etc.

APPLICATIONS



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			24	36	mA
		I_{CCL}				24	36	mA

NOTES:

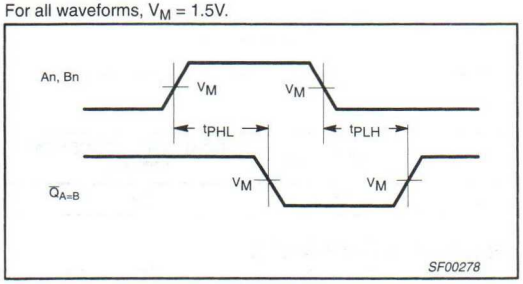
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

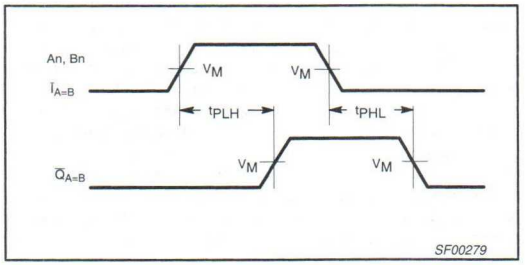
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An or Bn to $\overline{Q}_{A=B}$	Waveform 1, 2	3.5 3.0	8.0 8.0	9.5 9.0	3.5 2.5	11.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{I}_{A=B}$ to $\overline{Q}_{A=B}$	Waveform 2	3.0 3.5	5.0 6.5	6.5 7.0	3.0 3.5	7.5 8.0	ns

AC WAVEFORMS

For all waveforms, V_M = 1.5V.

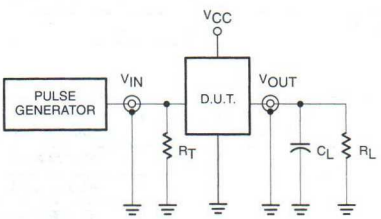


Waveform 1. For Inverting Outputs

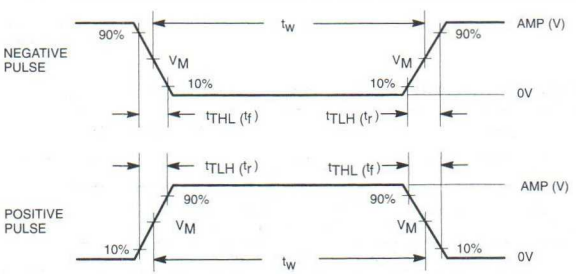


Waveform 2. For Non-Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor;
see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

8-bit register comparator (open collector + 3-State) 74F524

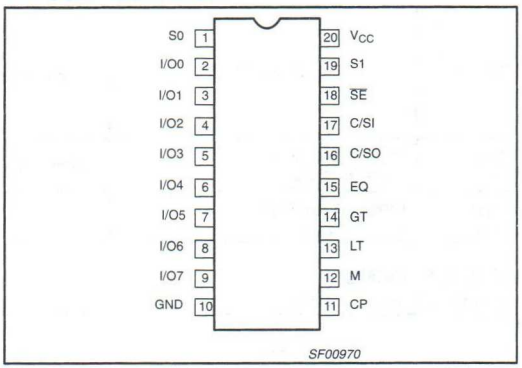
FEATURES

- 8-Bit bidirectional register with bus-oriented input-output
- Independent serial input-output to register
- Register bus comparator with 'equal to', 'greater than' and 'less than' outputs
- Cascadable in groups of 8-bits
- Open collector comparator outputs for AND-wired expansion
- Two's complement or magnitude compare

DESCRIPTION

The 74F524 is an 8-bit bidirectional register with parallel input and output, plus serial input and output progressing from MSB to LSB. All data inputs, serial and parallel, are loaded by the rising edge of the clock. The device functions are controlled by two control lines (S0, S1) to execute shift, load, hold and read out. An 8-bit comparator examines the data stored in the registers and on the data bus. Three true-High, open collector outputs representing 'register equal to bus', 'register greater than bus' and 'register less than bus' are provided. These outputs can be disabled to the OFF state by the use of Status Enable ($\overline{SE}$). A mode control has also been provided to allow Two's Complement as well as magnitude compare. Linking inputs are provided for expansion to longer words.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F524	65MHz	110mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
20-pin plastic DIP	N74F524N	SOT146-1
20-pin plastic SOL	N74F524D	SOT163-1

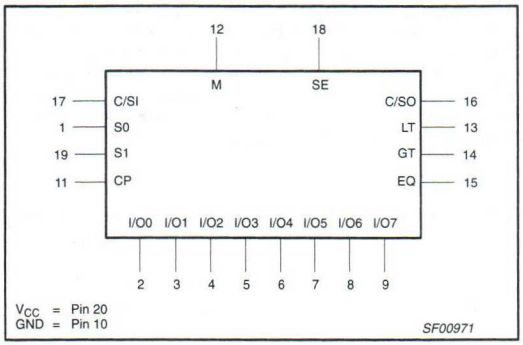
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I/On	Parallel data inputs	3.5/1.0	70µA/0.6mA
S0, S1	Mode select inputs	1.0/1.0	20µA/0.6mA
C/SI	Status priority or serial data input	1.0/1.0	20µA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{SE}$	Status enable input (active Low)	1.0/1.0	20µA/0.6mA
M	Compare mode select input	1.0/1.0	20µA/0.6mA
I/On	3-state parallel data outputs	150/40	3.0mA/24mA
C/SO	Status priority or serial data output	50/33	1.0mA/20mA
LT	Register less than bus output	OC/33	OC/20mA
EQ	Register equal to bus output	OC/33	OC/20mA
GT	Register greater than bus output	OC/33	OC/20mA

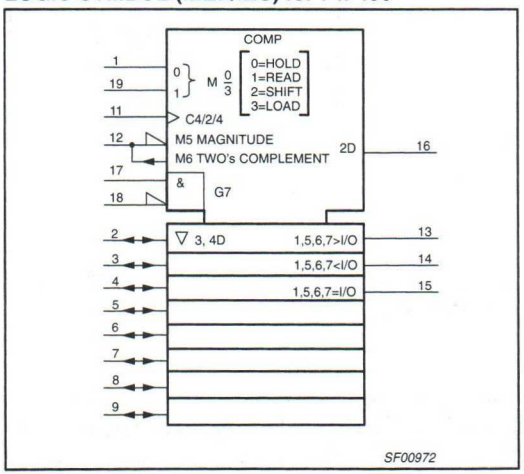
NOTE:
One (1.0) FAST Unit Load (U.L.) is defined as 20µA in the High state and 0.6mA in the Low state.
OC=Open Collector

8-bit register comparator (open collector + 3-State) 74F524

LOGIC SYMBOL for 74F456



LOGIC SYMBOL (IEEE/IEC) for 74F456



FUNCTIONAL DESCRIPTION

The 74F524 contains eight D-type flip-flops connected as a shift register with provision for either parallel or serial loading. Parallel data may be read from or loaded into the registers via the data bus I/O0–I/O7. Serial data is loaded into the register from the C/SI input and may be shifted through the register and out through the C/SO output. Both parallel and serial data entry occurs on the rising edge of the clock (CP). The operation of the shift register is controlled by two signals, S0 and S1, according to the Select Function Table. The 3-State parallel output buffers are enabled only in the READ mode.

SELECT FUNCTION TABLE

S0	S1	OPERATION
L	L	HOLD–Retains data in shift register
L	H	READ–Read contents in register onto data bus
H	L	SHIFT–Allows serial shifting on next rising clock edge
H	H	LOAD–Load data on bus into register

H = High voltage level
L = Low voltage level

One port of an 8-bit comparator is attached to the data bus while the other port is tied to the outputs of the internal register. Three active-OFF Open Collector outputs indicate whether the contents held in the shift register are 'greater than' (GT), 'less than' (LT), or 'equal to' (EQ) the data on the input bus. A High signal on the Status Enable ($\overline{SE}$) input disables these outputs to the OFF state. A mode control (M) input allows selection between a straightforward magnitude compare or a comparison between Two's complement numbers.

NUMBER REPRESENTATION SELECT TABLE

M	OPERATION
L	Magnitude compare
H	Two's Complement compare

H = High voltage level
L = Low voltage level

For 'greater than' or 'less than' detection, the C/SI input must be held High, as indicated in the Function Table. The internal logic is arranged such that a Low signal on the C/SI input places the 'greater than' and 'less than' outputs in their off state. (Note that this off state serves also as the active state when C/SI is High. It is intended for use in expansion to word lengths greater than 8 bits using multiple 74S524s as explained in the next 3 paragraphs.) The C/SO output will be forced High if the 'equal to' status condition exists; otherwise, C/SO will be held Low.

Word length expansion (in groups of 8 bits) can be achieved by connecting the C/SO output of the more significant byte to the C/SI input of the next less significant byte and also to its own $\overline{SE}$ input (see Application Figure 1). The CS/I input of the most significant device is held High while the $\overline{SE}$ input of the least significant device is held Low. The corresponding status outputs are AND-wired together. In the case of two's complement number compare, only the Mode input to the most significant device should be High. the Mode inputs to all other cascaded devices are held Low.

Suppose that an inequality condition is detected in the most significant device. Assuming that the byte stored in the register is greater than the byte on the data bus, then the EQ and LT outputs will be pulled Low, whereas the GT output will float High. Also, the

CS/O output of the most significant device will be forced Low, disabling the subsequent devices but enabling its own status outputs. The corrected status condition is thus indicated. The same applies if the register byte is less than the data byte, only in this case the EQ and GT outputs go Low, whereas the LT output floats High.

If an equality condition is detected in the most significant device, its C/SO output is forced High. This enables the next less significant device and disables its own status outputs. In this way, the status output proximity is handed down to the next less significant device which now effectively becomes the most significant byte. The worst case propagation delay for a compare operation involving 'n' cascaded 74F524s will be when an equality condition is detected in all but the least significant byte. In this case, the status priority has to ripple all the way down the chain before the correct status output is established. Typically, this will take 35+6(n–2) ns.

APPLICATION

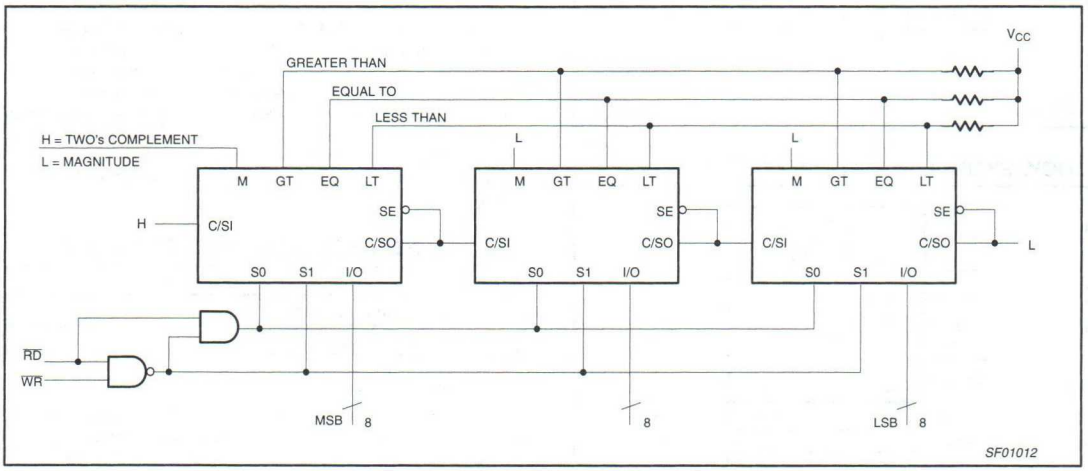


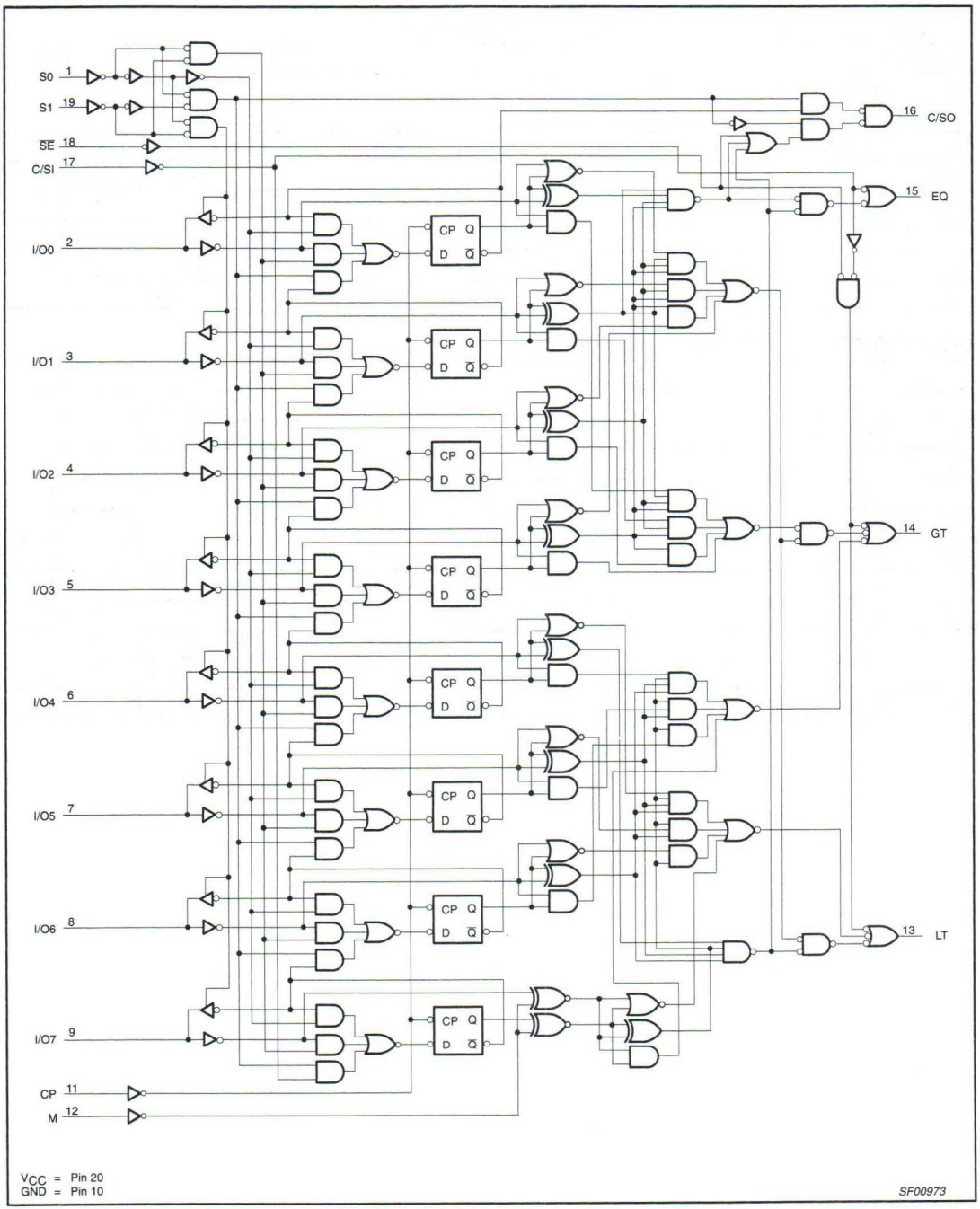
Figure 1. Cascading 74F524s for Comparing Longer Words

FUNCTION TABLE

INPUTS					OUTPUTS				OPERATING MODE
$\overline{SE}$	C/SI	S0	S1	Data comparison	EQ	GT	LT	C/SO	
H	H	L	L	X	H	H	H	(1)	Hold
H	L	L	L	X	H	H	H	L	
H	X	H	L	X	H	H	H	Q0	Shift
H	H	L	H	X	H	H	H	(1)	Read
H	L	L	H	X	H	H	H	L	
H	H	H	H	X	H	H	H	(1)	Load
H	L	H	H	X	H	H	H	L	
L	L	H or L[2]	H or L[2]	OA–OH > I/O0–I/O7	L	H	H	L	Compare (GT=CT=off)
L	L	H or L[2]	H or L[2]	OA–OH = I/O0–I/O7	H	H	H	L	
L	L	H or L[2]	H or L[2]	OA–OH < I/O0–I/O7	L	H	H	L	
L	H	H or L[2]	H or L[2]	OA–OH > I/O0–I/O7	L	H	L	L	Compare (GT=CT=on)
L	H	H or L[2]	H or L[2]	OA–OH = I/O0–I/O7	H	L	L	H	
L	H	H or L[2]	H or L[2]	OA–OH < I/O0–I/O7	L	L	H	L	

(1) = High if I/On=Dn, otherwise Low
2 = Must meet setup and hold time requirements
H = High voltage level
L = Low voltage level
X = Don't care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	All except I/O	40	mA
		I/O only	48	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	High-level output voltage	LT, EQ, GT only			4.5	V
I_{OH}	High-level output current	Not LT, EQ, GT, C/SO			−3	mA
		C/SO only			−1	mA
I_{OL}	Low-level output current	All except I/O			20	mA
		I/O only			24	mA
T_{amb}	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
I_{OH}	High-level output current	LT, EQ, GT only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX					250	µA
V_{OH}	High-level output voltage	C/SO only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=MAX	±10%V_{CC}	2.5			V
		I/On only			±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	I/On	V_{CC} = MAX, V_I = 5.5V					1	mA
		Except I/On	V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current	Except I/On	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					–0.6	mA
I_{OZH}	Off-state output current High-level voltage applied	I/On only	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					–0.6	mA
I_{OS}	Short-circuit output current[3]	Except LT, EQ, GT	V_{CC} = MAX			–60		–150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX				110	150	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 4	50	65		45		MHz
t_{PLH} t_{PHL}	Propagation delay I/On to EQ	Waveform 2	9.0 4.5	11.5 7.5	17.0 11.0	9.0 4.5	18.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay I/On to GT	Waveform 2	8.5 6.5	11.0 9.5	17.0 15.5	8.5 6.5	18.0 16.5	ns
t_{PLH} t_{PHL}	Propagation delay I/On to LT	Waveform 2	8.0 6.0	11.0 10.5	17.0 14.0	8.0 6.0	18.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay I/On to C/SO	Waveform 2	7.0 6.5	13.0 9.0	16.0 14.0	7.0 5.5	17.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to EQ	Waveform 4	11.0 4.0	17.0 8.0	22.0 14.0	10.0 4.0	23.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to GT	Waveform 4	11.0 10.0	16.0 16.5	20.0 21.0	10.0 10.0	21.0 22.0	ns
t_{PHL} t_{PLH}	Propagation delay CP to LT	Waveform 4	11.0 8.0	16.0 14.0	23.0 18.0	10.0 8.0	24.0 19.0	ns
t_{PLH}	Propagation delay CP to C/SO (Load)	Waveform 4	10.0	16.0	20.0	10.0	21.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to C/SO (Serial shift)	Waveform 4	5.0 4.5	10.0 9.0	13.0 11.5	5.0 4.5	14.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay C/SI to GT	Waveform 1	8.0 3.0	10.5 4.5	16.0 8.5	9.0 2.5	17.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay C/SI to LT	Waveform 1	8.0 3.0	10.5 6.0	17.0 8.5	8.0 2.5	18.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay Sn to C/SO	Waveform 2	6.5 5.5	8.0 10.0	14.5 17.0	6.5 5.5	15.5 18.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SE}$ to EQ	Waveform 2	3.5 2.5	7.0 4.5	10.5 8.0	3.5 2.5	11.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SE}$ to GT	Waveform 2	6.0 3.5	8.0 5.0	13.0 8.0	6.0 3.0	14.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SE}$ to LT	Waveform 2	5.0 3.5	8.0 5.5	12.0 8.0	5.0 3.0	13.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay C/SI to C/SO	Waveform 2	4.0 4.0	7.0 7.0	11.0 11.0	4.0 4.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay M to GT	Waveform 2	8.0 8.0	13.0 10.0	18.0 15.5	8.0 8.0	19.0 16.5	ns
t_{PLH} t_{PHL}	Propagation delay M to LT	Waveform 2	10.0 6.0	15.0 8.0	20.0 12.0	10.0 5.0	21.0 13.0	ns
t_{PZH} t_{PZL}	Output Enable time Sn to I/On	Waveform 3 Waveform 4	4.5 5.5	7.0 9.0	13.0 15.0	4.5 5.5	14.0 16.0	ns
t_{PHZ} t_{PLZ}	Output Disable time Sn to I/On	Waveform 3 Waveform 4	3.0 4.5	5.0 8.0	12.0 12.5	2.0 4.5	13.0 13.5	ns

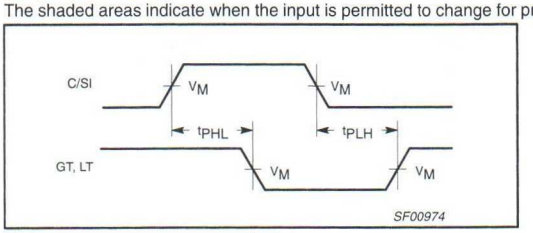
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/On to CP	Waveform 3	6.0 6.0			6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/On to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S0, S1 to CP	Waveform 3	13.5 10.0			15.0 10.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S0, S1 to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low C/SI to CP	Waveform 3	7.0 7.0			7.0 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low C/SI to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low	Waveform 4	5.0 10.0			5.0 10.0		ns

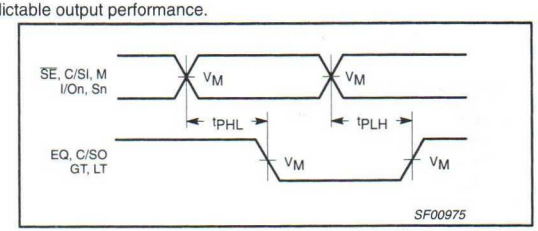
AC WAVEFORMS

For all waveforms, V_M = 1.5V.

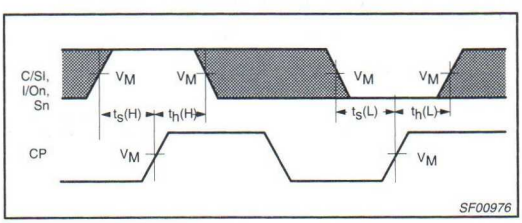
The shaded areas indicate when the input is permitted to change for predictable output performance.



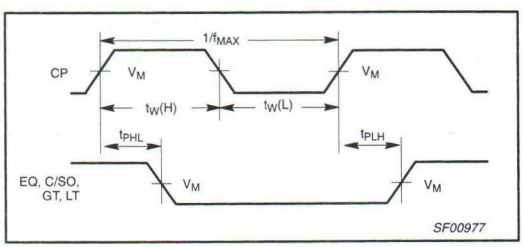
Waveform 1. Propagation Delay for Inverting Outputs



Waveform 2. Propagation Delay for Non-Inverting Outputs



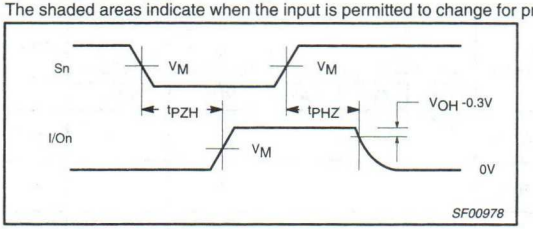
Waveform 3. Setup and Hold Times



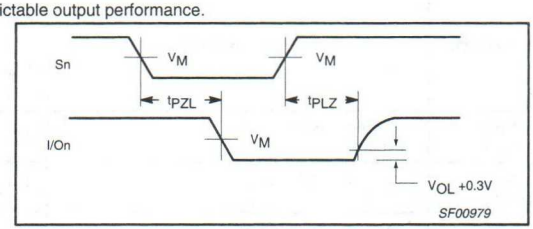
Waveform 4. Propagation Delay, Clock to Output, Clock Pulse Width, and Maximum Clock Frequency

AC WAVEFORMS (Continued)

For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

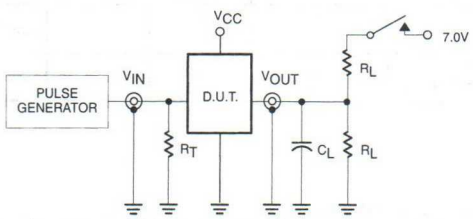


Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

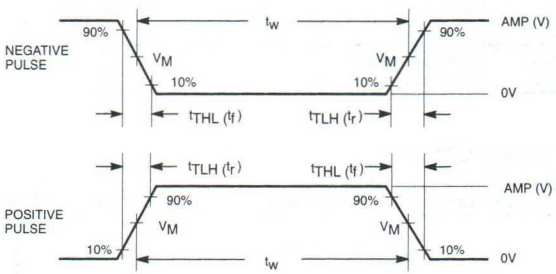


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs and Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
Open Collector	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00980

Latch/flip-flop

~~74F533,~~* 74F534

74F533 Octal Transparent Latch, Inverting (3-State)
74F534 Octal D Flip-Flop, Inverting (3-State)

FEATURES

- 8-bit positive edge-triggered register – 74F534
- 3-State inverting output buffers
- Common 3-State Output register
- Independent register and 3-State buffer operation

DESCRIPTION

The 74F533 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs is transferred to the latch outputs when the Enable (E) input is High. The latch remains transparent to the data input while E is High and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

The 74F534 is an 8-bit edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's $\overline{Q}$ output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F533	5.5ns	41mA

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F534	165MHz	51mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
20-Pin Plastic DIP	N74F534N	SOT146-1
20-Pin Plastic SOL	N74F534D	SOT163-1

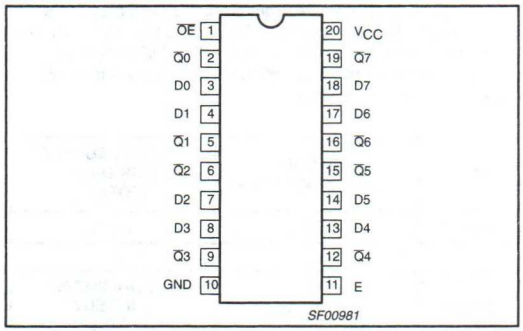
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 - D7	Data inputs	1.0/1.0	20µA/0.6mA
E (74F533)	Enable input (active High)	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
CP (74F534)	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{Q0}$ - $\overline{Q7}$	Data outputs	150/40	3.0mA/24mA

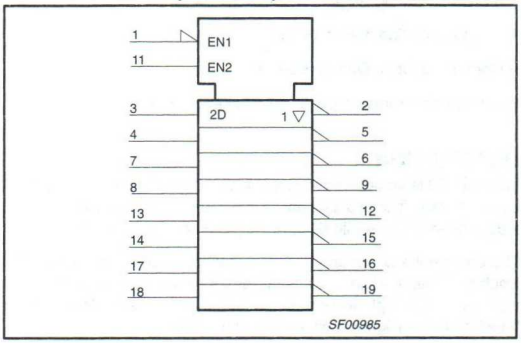
* *Discontinued part. Please see the Discontinued Products List.*

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

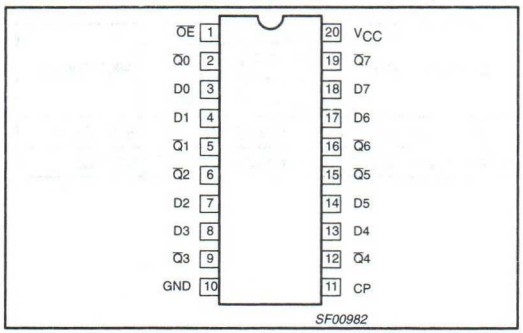
PIN CONFIGURATION – 74F533



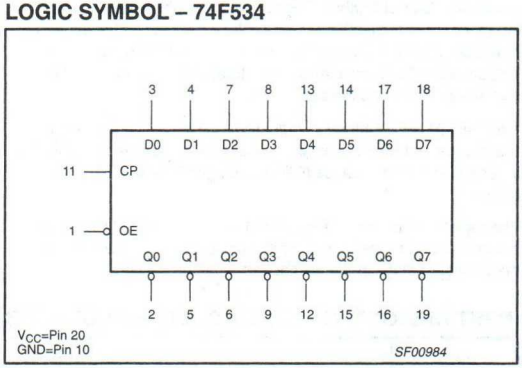
LOGIC SYMBOL (IEEE/IEC) – 74F533



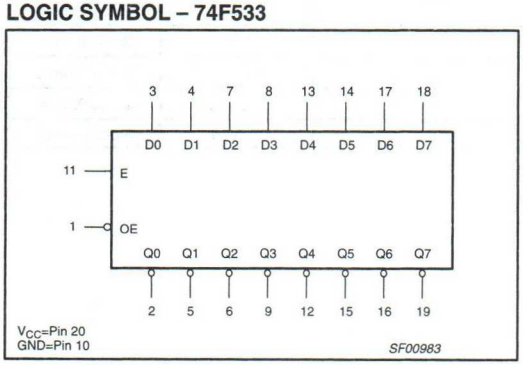
PIN CONFIGURATION – 74F534



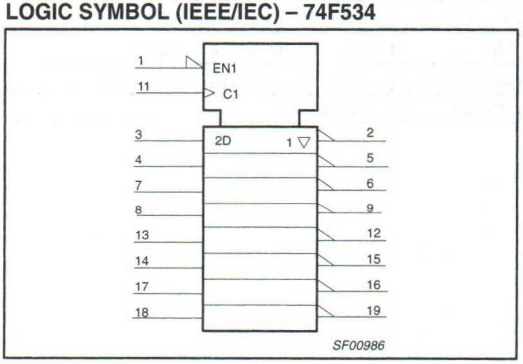
LOGIC SYMBOL – 74F534



LOGIC SYMBOL – 74F533

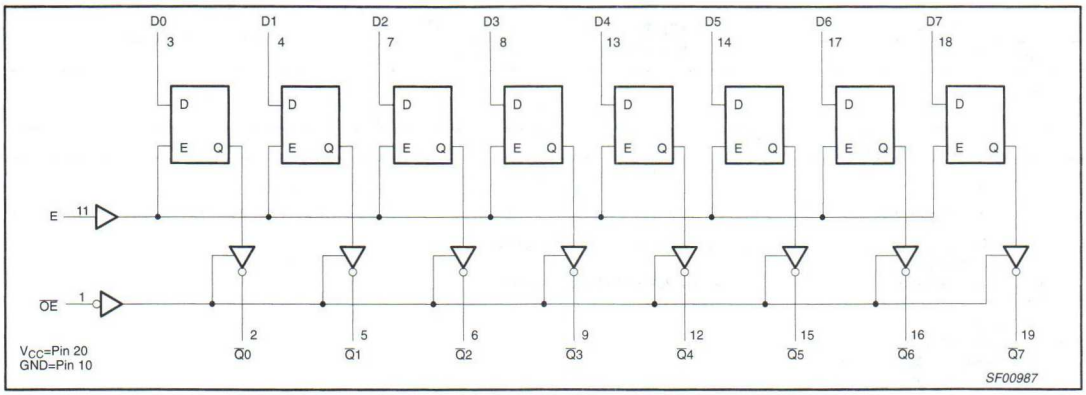


LOGIC SYMBOL (IEEE/IEC) – 74F534

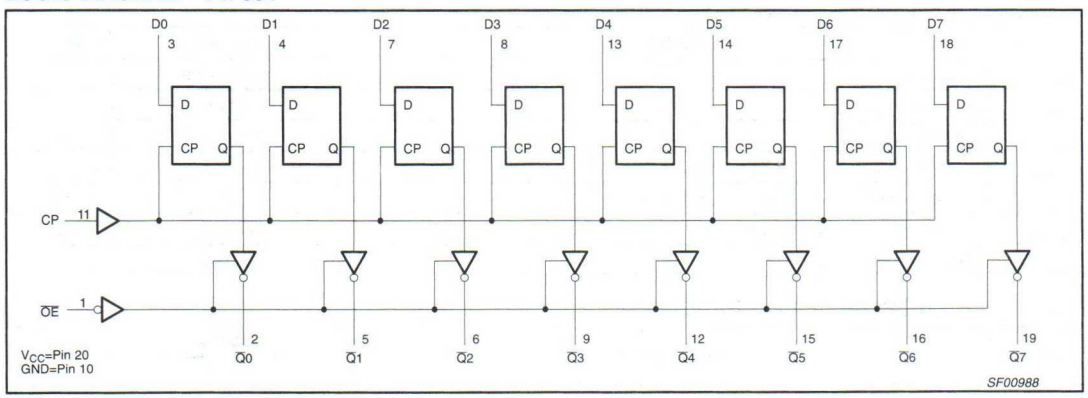


* *Discontinued part. Please see the Discontinued Products List.*

LOGIC DIAGRAM – 74F533



LOGIC DIAGRAM – 74F534



FUNCTION TABLE – 74F533

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODES
$\overline{OE}$	$\overline{E}$	Dn		$\overline{Q0} - \overline{Q7}$	
L	H	L	L	H	Load and read register
L	H	H	H	L	
L	↓	l	L	H	Enable and read register
L	↓	h	H	L	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	Dn	Dn	Z	

H = High voltage level
h = High voltage level one setup time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one setup time prior to the High-to-Low E transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

* *Discontinued part. Please see the Discontinued Products List.*

FUNCTION TABLE – 74F534

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODES
$\overline{OE}$	CP	Dn		$\overline{Q0} - \overline{Q7}$	
L	↑	l	L	H	Load and read register
L	↑	h	H	L	
L	↑	X	NC	NC	Hold
H	↑	X	NC	Z	Disable outputs
H	↑	Dn	Dn	Z	

H = High voltage level
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↑ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	–65 to +125	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–3	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		70	°C

* *Discontinued part. Please see the Discontinued Products List.*

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				–50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	74F533	V_{CC} = MAX	$\overline{OE}$=4.5V, Dn=E=GND		41	61	mA
		74F534		$\overline{OE}$=4.5V, Dn=GND		51	86	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb}= +25°C, V_{CC} = +5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5V ± 10%, C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to $\overline{Qn}$	74F533	Waveform 2	4.0 3.0	6.0 4.5	8.5 7.0	4.0 3.0	9.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay E to $\overline{Qn}$		Waveform 3	5.0 3.0	6.5 4.5	9.5 7.0	5.0 3.0	10.0 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	4.5 5.0	7.0 7.0	2.0 2.0	8.0 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 6 Waveform 7	2.0 2.0	3.5 3.0	6.0 5.5	2.0 2.0	7.0 6.5	ns
f_{MAX}	Maximum Clock frequency	74F534	Waveform 1	150	165		135		MHz
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Qn}$		Waveform 1	3.0 3.0	4.5 4.5	7.0 7.0	2.5 2.5	7.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	4.5 5.0	7.5 7.5	2.0 2.0	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 6 Waveform 7	2.0 2.0	3.5 3.5	6.5 5.5	2.0 2.0	7.5 6.5	ns

* *Discontinued part. Please see the Discontinued Products List.*

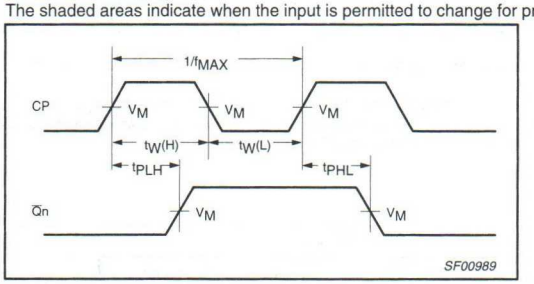
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb}= +25°C, V_{CC} = +5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, Dn to E	74F533	Waveform 4	1.5 0			1.5 0		ns
$t_h(H)$ $t_h(L)$	Hold time, Dn to E		Waveform 4	2.5 2.5			2.5 2.5		ns
$t_w(H)$	E Pulse width, High		Waveform 3	3.0			3.0		ns
$t_s(H)$ $t_s(L)$	Setup time, Dn to CP	74F534	Waveform 5	2.0 2.0			2.5 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, Dn to CP		Waveform 5	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low		Waveform 1	3.0 3.5			3.5 4.0		ns

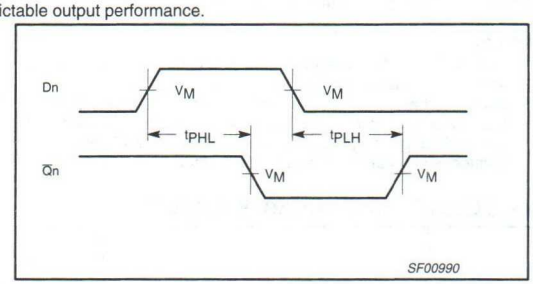
AC WAVEFORMS

For all waveforms, V_M = 1.5V

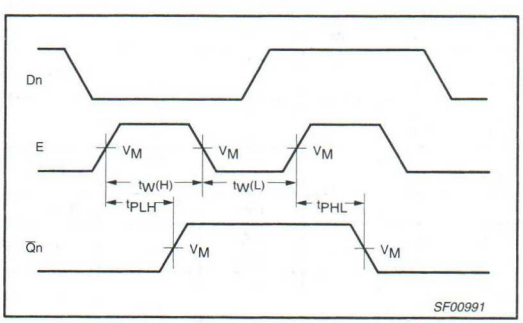
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay, Clock and Enable Inputs to Output, Enable, Clock Pulse Widths, and Maximum Clock Frequency



Waveform 2. Propagation Delay for Data to Output



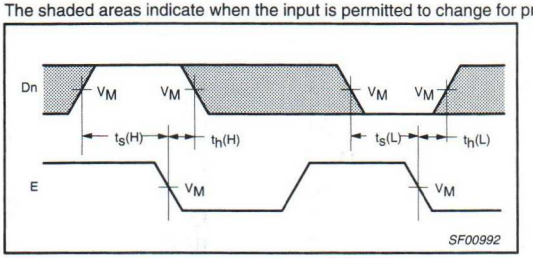
Waveform 3. Propagation Delay, Enable Input to Output, and Enable Pulse Width

* *Discontinued part. Please see the Discontinued Products List.*

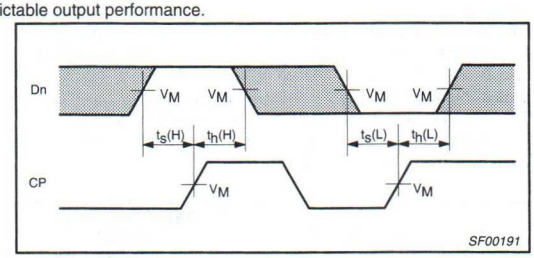
AC WAVEFORMS (Continued)

For all waveforms, V_M = 1.5V

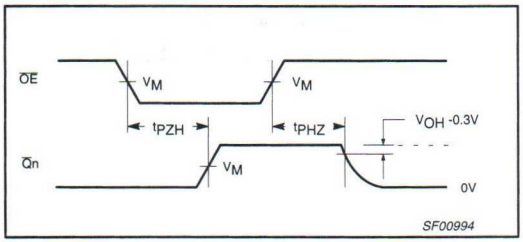
The shaded areas indicate when the input is permitted to change for predictable output performance.



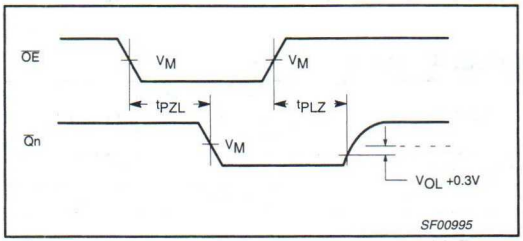
Waveform 4. Data Setup and Hold Times



Waveform 5. Data Setup and Hold Times

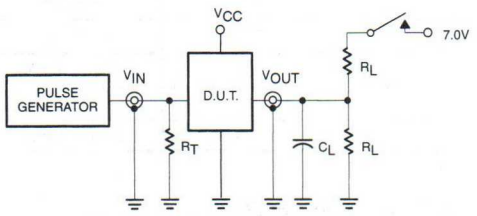


Waveform 6. 3-State Output Enable Time to High Level and Output Disable Time from High Level

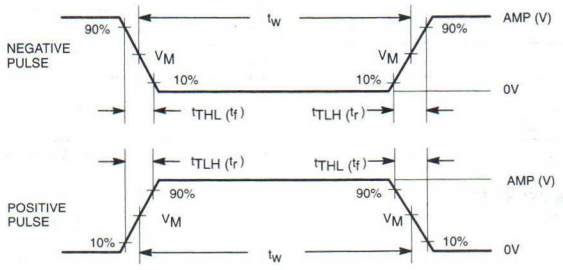


Waveform 7. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

* *Discontinued part. Please see the Discontinued Products List.*

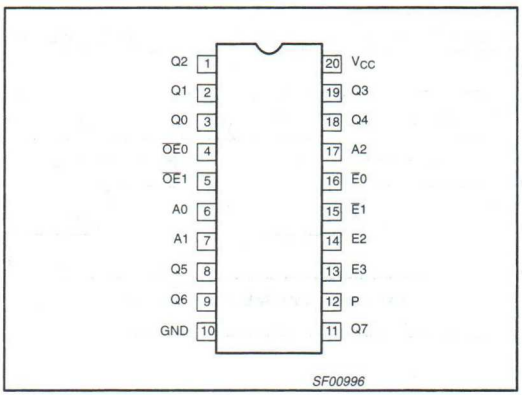
1-of-8 decoder (3-State) 74F538

DESCRIPTION

The 74F538 decoder/demultiplexer accepts three address (A0 - A2) input signals and decodes them to select one of eight mutually exclusive outputs. A Polarity control (P) input determines whether the outputs are active Low or active High. The 74F538 has 3-State outputs, and a High signal on the Output Enables ($\overline{OE}n$) inputs will force all outputs to the high impedance state. Two active High (E2, E3) and two active Low ($\overline{E}0$, $\overline{E}1$) inputs are available for easy expansion to 1-of-32 decoding with four packages, or for data demultiplexing to 1-of-8 or 1-of-16 destinations.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F538	8.5ns	35mA

PIN CONFIGURATION



ORDERING INFORMATION

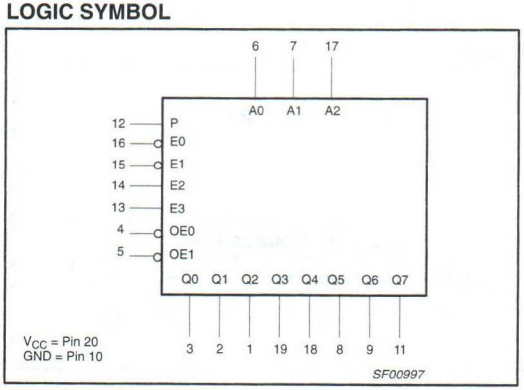
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
20-Pin Plastic DIP	N74F538N	SOT146-1
20-Pin Plastic SOL	N74F538D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

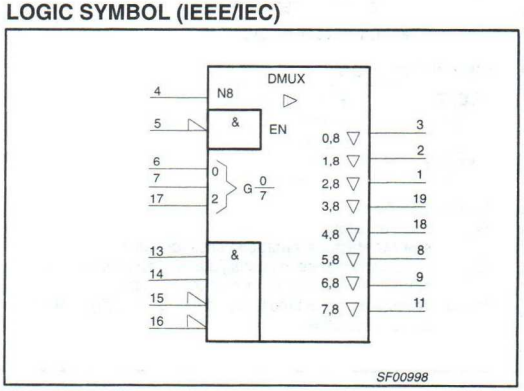
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 - A2	Address inputs	1.0/1.0	20µA/0.6mA
$\overline{E}0$, $\overline{E}1$	Enable inputs (active Low)	1.0/1.0	20µA/0.6mA
E2, E3	Enable inputs (active High)	1.0/1.0	20µA/0.6mA
P	Polarity control input	1.0/1.0	20µA/0.6mA
$\overline{OE}0$, $\overline{OE}1$	Output Enable inputs	1.0/1.0	20µA/0.6mA
Q0 - Q7	Data outputs	150/40	3.0mA/24mA

NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

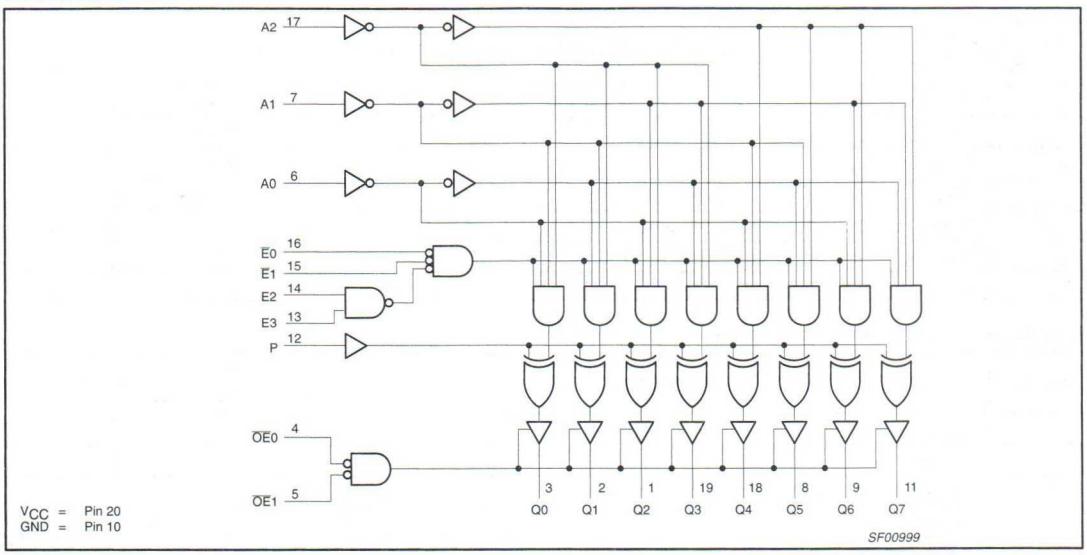
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS									OUTPUTS								OPERATING MODE
$\overline{OE}_0$	$\overline{OE}_1$	$\overline{E}_0$	$\overline{E}_1$	E_2	E_3	A_2	A_1	A_0	Q_0	Q_1	Q2	Q3	Q4	Q5	Q6	Q7	
H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	High Impedance
X	H	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	
L	L	H	X	X	X	X	X	X	Outputs equal P input								Disable
L	L	X	H	X	X	X	X	X									
L	L	X	X	L	X	X	X	X									
L	L	X	X	X	L	X	X	X									
L	L	L	L	H	H	L	L	L	H	L	L	L	L	L	L	L	Active High output (P = L)
L	L	L	L	H	H	L	L	H	L	H	L	L	L	L	L	L	
L	L	L	L	H	H	L	H	L	L	L	H	L	L	L	L	L	
L	L	L	L	H	H	L	H	H	L	L	L	H	L	L	L	L	
L	L	L	L	H	H	H	L	L	L	L	L	L	H	L	L	L	
L	L	L	L	H	H	H	L	H	L	L	L	L	L	L	H	L	
L	L	L	L	H	H	H	H	L	L	L	L	L	L	L	L	H	
L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L	H	
L	L	L	L	H	H	L	L	L	L	H	H	H	H	H	H	H	Active Low output (P = H)
L	L	L	L	H	H	L	L	H	H	L	H	H	H	H	H	H	
L	L	L	L	H	H	L	H	L	H	H	L	H	H	H	H	H	
L	L	L	L	H	H	L	H	H	H	H	H	L	H	H	H	H	
L	L	L	L	H	H	H	L	L	H	H	H	H	L	H	H	H	
L	L	L	L	H	H	H	L	H	H	H	H	H	L	H	H	H	
L	L	L	L	H	H	H	H	L	H	H	H	H	H	L	H	H	
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–3.0	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OZH}	Off-state output current High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				–50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current	I_{CCH}	V_{CC} = MAX			30	40	mA
		I_{CCL}				35	50	mA
		I_{CCZ}				35	50	mA

NOTES:

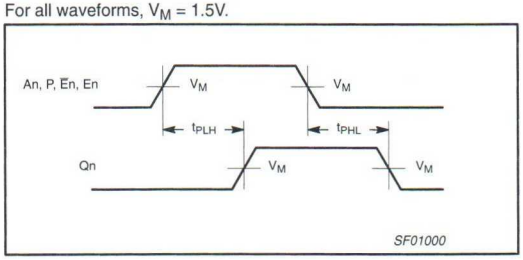
1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.

AC ELECTRICAL CHARACTERISTICS

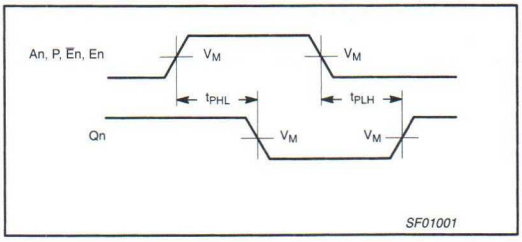
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Qn	Waveform 1, 2	5.5 3.0	8.5 7.5	13.0 12.5	5.0 3.0	14.0 13.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}0$ or $\overline{E}1$ to Qn	Waveform 1, 2	5.5 3.0	8.5 7.5	12.0 12.0	5.0 3.0	13.0 12.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}2$ or $\overline{E}3$ to Qn	Waveform 1, 2	6.5 4.0	9.0 7.0	12.5 12.5	5.5 3.5	13.5 13.0	ns ns
t_{PLH} t_{PHL}	Propagation delay P to Qn	Waveform 1, 2	4.5 3.5	9.5 6.5	15.0 10.0	4.0 3.5	16.5 10.5	ns ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}0$ or $\overline{OE}1$ to Qn	Waveform 3 Waveform 4	2.5 6.5	5.5 9.5	9.5 13.5	2.0 6.0	11.0 15.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}0$ or $\overline{OE}1$ to Qn	Waveform 3 Waveform 4	1.0 1.0	3.0 3.5	6.0 8.5	1.0 1.0	7.0 9.5	ns ns

AC WAVEFORMS

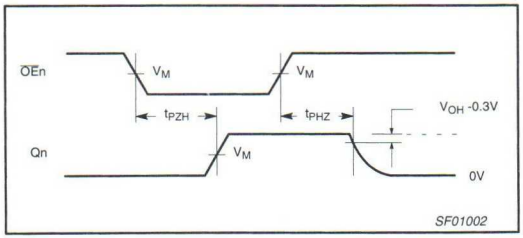
For all waveforms, V_M = 1.5V.



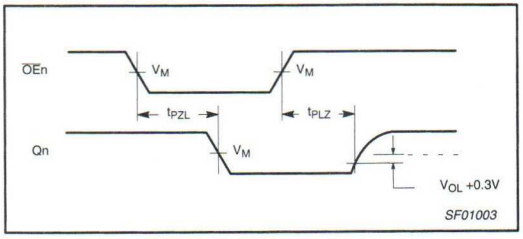
Waveform 1. Propagation Delay for Non-Inverting Outputs



Waveform 2. Propagation Delay for Inverting Outputs

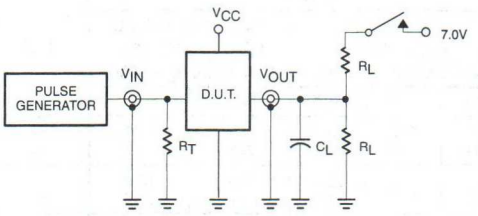


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

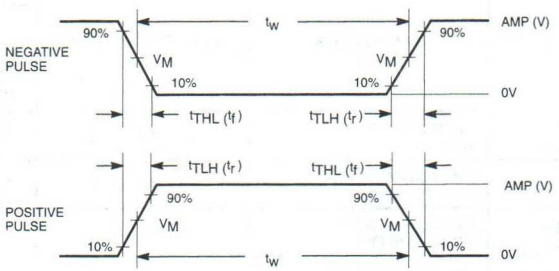


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

74F540 Octal Inverter Buffer (3-State)
74F541 Octal Buffer (3-State)

FEATURES

- High impedance NPN base inputs for reduced loading (20μA in High and Low states)
- Low power, light bus loading
- Functionally similar to the 74F240 and 74F241
- Provides ideal interface and increases fan-out of MOS microprocessors
- Efficient pinout to facilitate PC board layout
- Octal bus interface
- 3-State buffer outputs sink 64mA
- 15mA source current

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F540	3.5ns	58mA
74F541	5.5ns	55mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
20-Pin Plastic DIP	N74F540, N74F541N	SOT146-1
20-Pin Plastic SOL	N74F540D, N74F541D	SOT163-1

DESCRIPTION

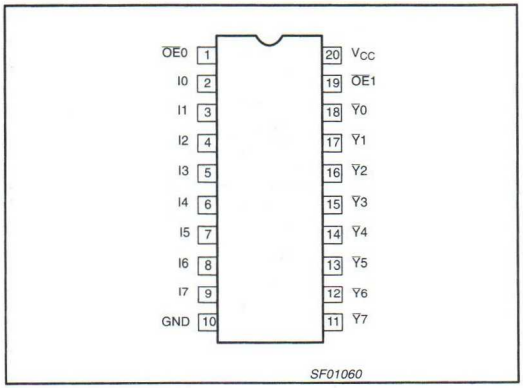
The 74F540 and 74F541 are octal buffers that are ideal for driving bus lines or buffer memory address registers. The outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The devices feature input and outputs on opposite sides of the package to facilitate printed circuit board layout.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I0–I7	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE}$0, $\overline{OE}$1	3-State output enable inputs (active Low)	1.0/0.033	20μA/20μA
Y0 - Y7	Data outputs (74F541)	750/106.7	15mA/64mA
$\overline{Y}$0 - $\overline{Y}$7	Data outputs (74F540)	750/106.7	15mA/64mA

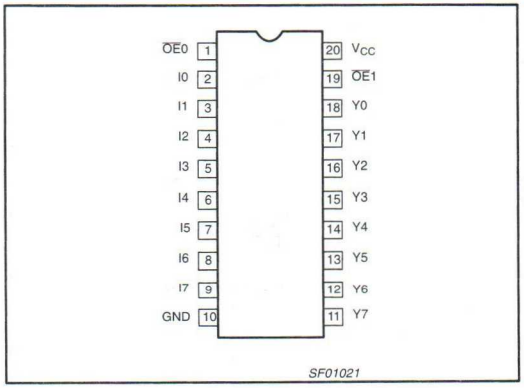
NOTE: One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION – 74F540



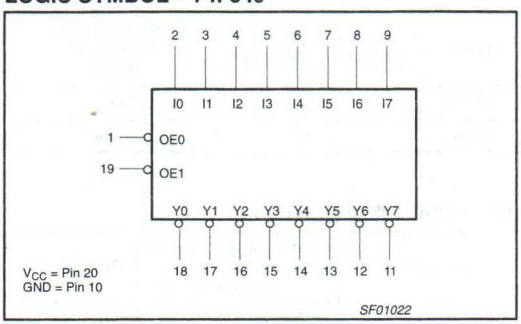
SF01060

PIN CONFIGURATION – 74F541

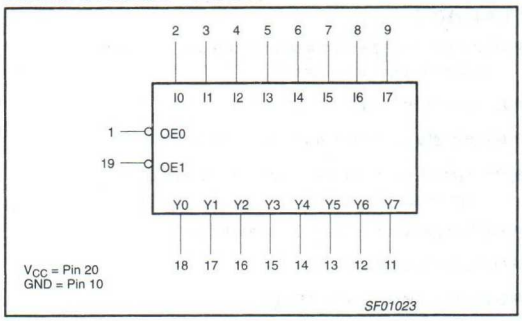


SF01021

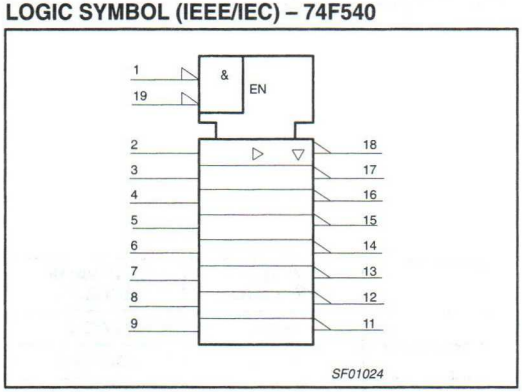
LOGIC SYMBOL – 74F540



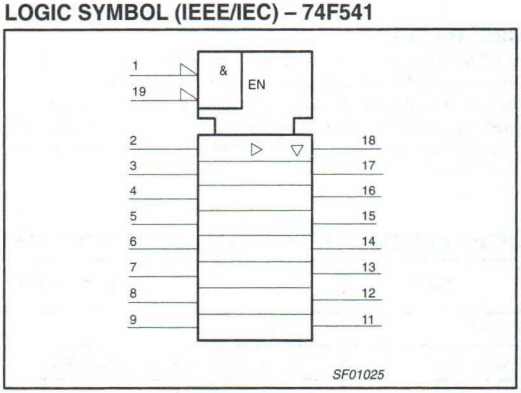
LOGIC SYMBOL – 74F541



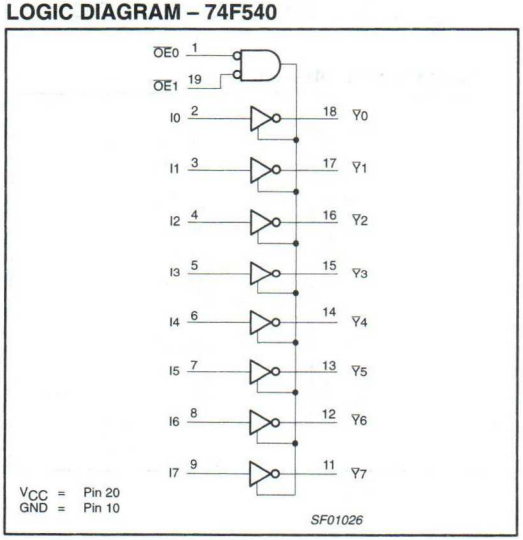
LOGIC SYMBOL (IEEE/IEC) – 74F540



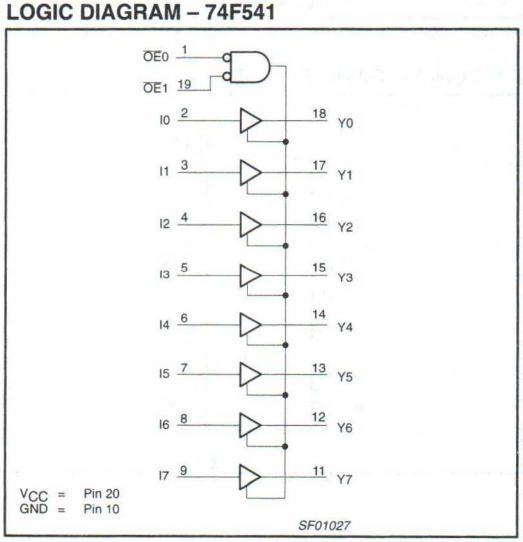
LOGIC SYMBOL (IEEE/IEC) – 74F541



LOGIC DIAGRAM – 74F540



LOGIC DIAGRAM – 74F541



FUNCTION TABLE

INPUTS			OUTPUTS	
			74F541	74F540
$\overline{OE0}$	$\overline{OE1}$	In	Yn	$\overline{Yn}$
L	L	L	L	H
L	L	H	H	L
X	H	X	Z	Z
H	X	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–15	mA
I_{OL}	Low-level output current			64	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
			I_{OH} = –15mA	±10%V_{CC}	2.0			V
				±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}			0.55	V
				±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{OZH}	Off-state output current High-level voltage applied	V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current Low-level voltage applied	V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			–100		–225	mA
I_{CC}	Supply current (total)	74F540	I_{CCH}	V_{CC} = MAX	In=$\overline{OE}$n=GND		22	30	mA
			I_{CCL}		In=4.5V, $\overline{OE}$n=GND		58	75	mA
			I_{CCZ}		In=GND, $\overline{OE}$n=4.5V		40	55	mA
		74F541	I_{CCH}		In=4.5V, $\overline{OE}$n=GND		30	40	mA
			I_{CCL}		In=$\overline{OE}$n=GND		55	72	mA
			I_{CCZ}		In=GND, $\overline{OE}$n=4.5V		45	58	mA

NOTES:

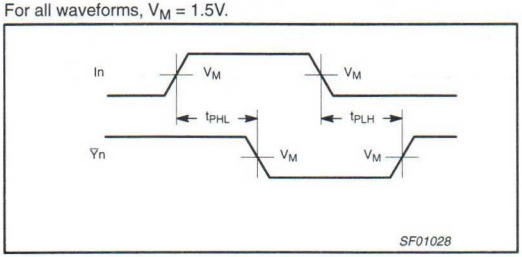
1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.

AC ELECTRICAL CHARACTERISTICS

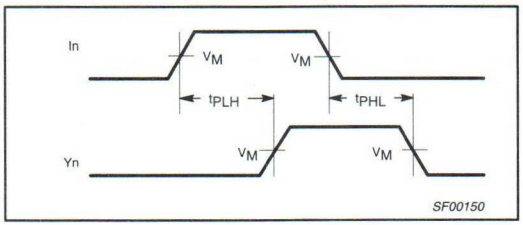
SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay In to $\overline{Y}$n	74F540	Waveform 1	3.0 1.5	4.5 2.5	6.5 4.5	2.5 1.5	7.5 5.0	ns ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	2.0 4.0	3.5 7.5	6.5 9.5	2.0 4.0	7.0 10.0	ns ns
t_{PZH} t_{PZL}	Output Disable time from High or Low level		Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	6.0 5.5	2.0 2.0	6.5 6.0	ns ns
t_{PLH} t_{PHL}	Propagation delay In to Yn	74F541	Waveform 2	2.5 3.5	5.0 6.0	6.5 7.0	2.5 3.0	7.0 7.5	ns ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	3.0 3.0	5.5 6.5	7.0 8.5	3.0 3.0	7.5 9.5	ns ns
t_{PZH} t_{PZL}	Output Disable time from High or Low level		Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	7.0 7.0	2.0 2.0	7.5 7.5	ns ns

AC WAVEFORMS

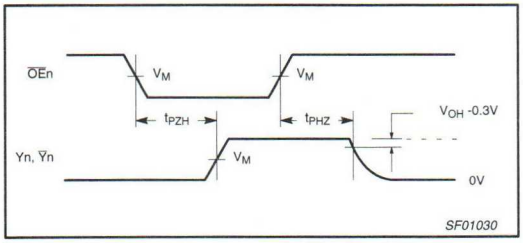
For all waveforms, V_M = 1.5V.



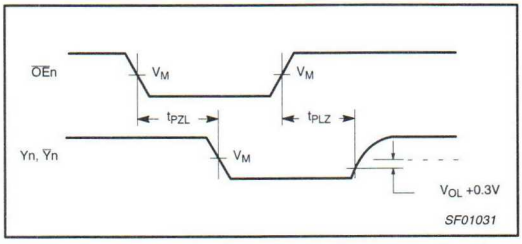
Waveform 1. Propagation Delay Data to Outputs for 74F540



Waveform 2. Propagation Delay Data to Outputs for 74F541

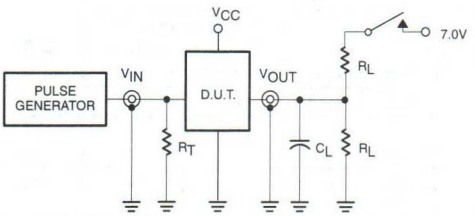


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

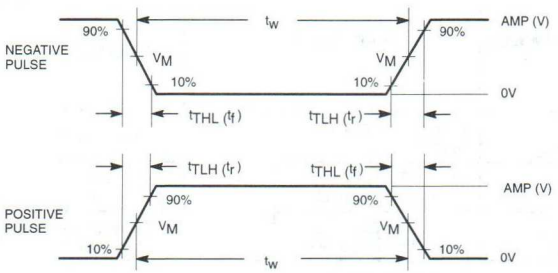


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

Octal registered transceivers 74F543, 74F544

74F543 Octal registered transceiver, non-inverting (3-State)
74F544 Octal registered transceiver, inverting 93-State)

FEATURES

- Combines74F245 and 74F373 type functions in one chip
- 8-bit octal transceiver with D-type latch
- 74F543 Non-inverting
  74F544 Inverting
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- A outputs sink 20mA and source 3mA
- B outputs sink 64mA and source 15mA
- 3-State outputs for bus-oriented applications
- 74F543 available in SSOP Type II package

DESCRIPTION

The 74F543 and 74F544 Octal Registered Transceivers contain two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. While the 74F543 has non-inverting data path, the 74F544 inverts data in both directions. The A outputs are guaranteed to sink 24mA, while the B outputs are rated for 64mA.

FUNCTIONAL DESCRIPTION

The 74F543 and 74F544 contain two sets of eight D-type latches, with separate input and controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{EAB}$) input must be Low in order to enter data from A0 - A7 or take data from B0 - B7, as indicated in the Function Table. With $\overline{EAB}$ Low, a Low signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent Low-to-High transition for the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches. Control of data flow from B to A is similar, but using the $\overline{EBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F543	6.0ns	80mA
74F544	6.5ns	95mA

ORDERING INFORMATION

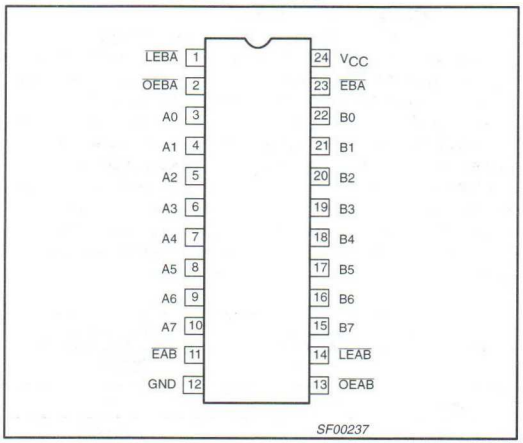
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_A = 0°C to +70°C	DRAWING NUMBER
24-pin plastic skinny DIP (300mil)	N74F543N, N74F544N	SOT222–1
24-pin plastic SOL	N74F543D, N74F544D	SOT137-1
24-pin plastic SSOP Type II	74F543DB	SOT340-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

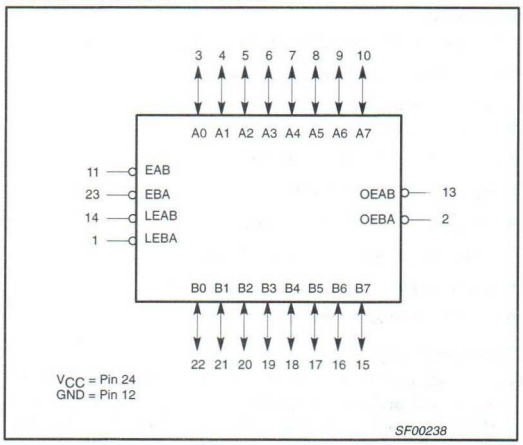
PINS		DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
74F543 74F544	A0 - A7	Port A, 3-State inputs	3.5/1.0	70μA/0.6mA
	B0 - B7	Port B, 3-State inputs	3.5/1.0	70μA/0.6mA
	$\overline{OEAB}$	A-to-B Output Enable input (Active Low)	1.0/1.0	20μA/0.6mA
	$\overline{OEBA}$	B-to-A Output Enable input (Active Low)	1.0/1.0	20μA/0.6mA
	$\overline{EAB}$	A-to-B Enable input (Active Low)	1.0/2.0	20μA/1.2mA
	$\overline{EBA}$	B-to-A Enable input (Active Low)	1.0/2.0	20μA/1.2mA
	$\overline{LEAB}$	A-to-B Latch Enable input (Active Low)	1.0/1.0	20μA/0.6mA
	$\overline{LEBA}$	B-to-A Latch Enable input (Active Low)	1.0/1.0	20μA/0.6mA
74F543	A0 - A7	Port A, 3-State outputs	150/40	3.0mA/24mA
	B0 - B7	Port B, 3-State outputs	750/106.7	15mA/64mA
74F544	$\overline{A}$0 - $\overline{A}$7	Port $\overline{A}$, 3-State outputs	150/40	3.0mA/24mA
	$\overline{B}$0 - $\overline{B}$7	Port $\overline{B}$, 3-State outputs	750/106.7	15mA/64mA

NOTE: One (1.0) FAST Unit Load is defined as: 20μA in the High State and 0.6mA in the Low state.

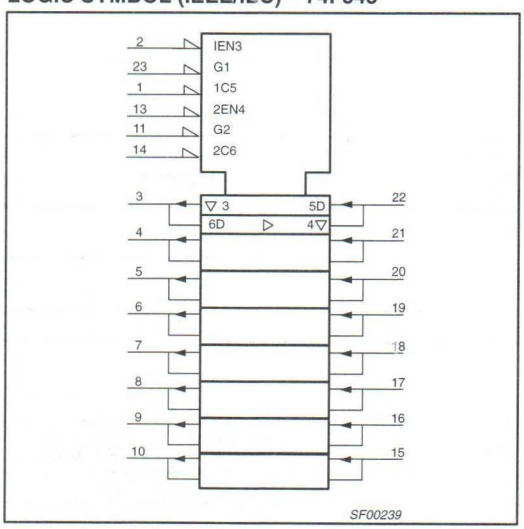
PIN CONFIGURATION – 74F543



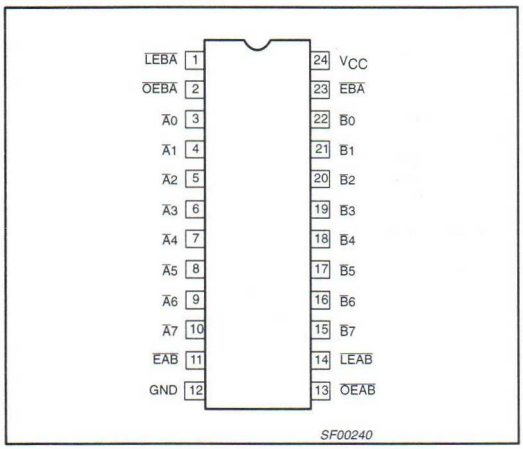
LOGIC SYMBOL – 74F543



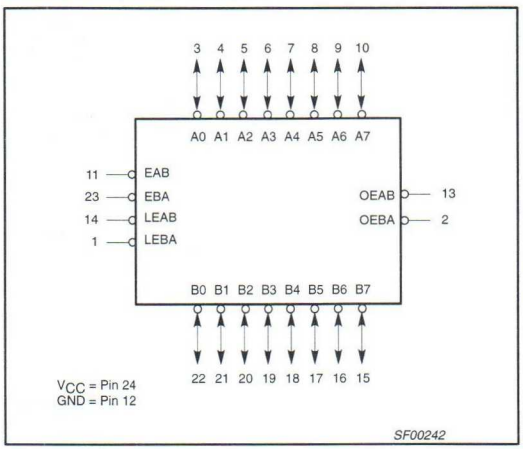
LOGIC SYMBOL (IEEE/IEC) – 74F543



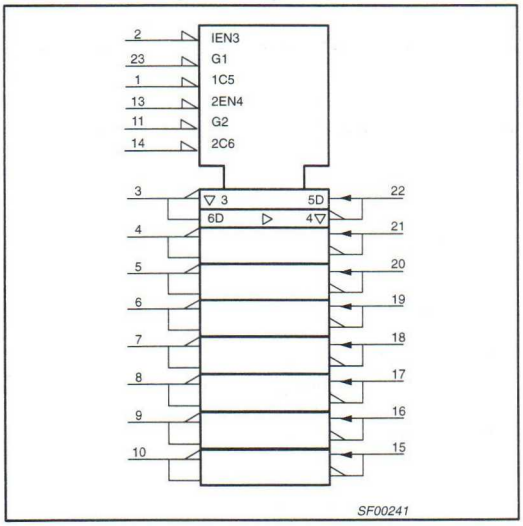
PIN CONFIGURATION – 74F544



LOGIC SYMBOL – 74F544



LOGIC SYMBOL (IEEE/IEC) – 74F544

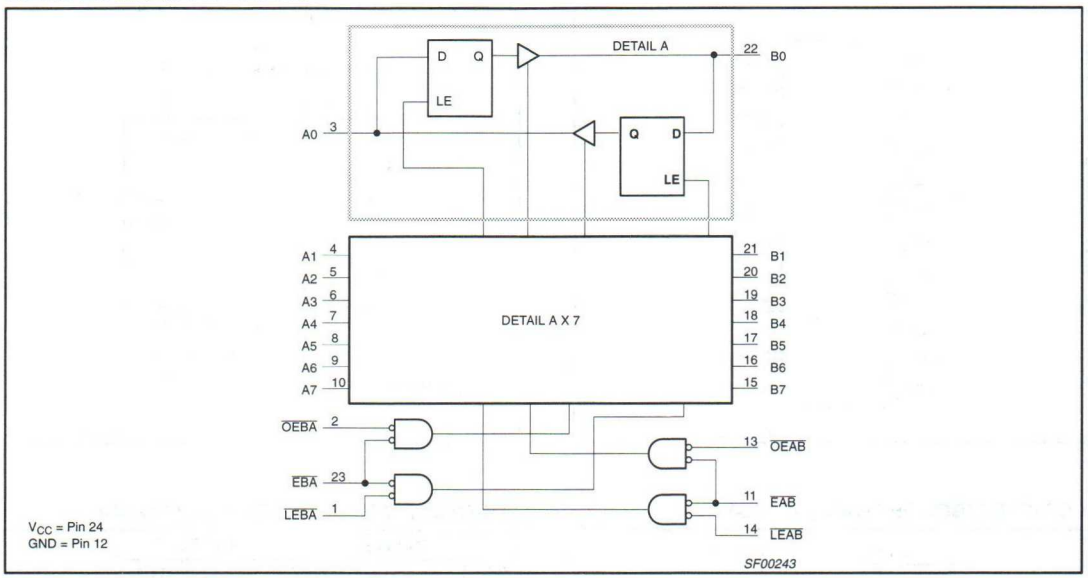


FUNCTION TABLE for 74F543 and 74F544

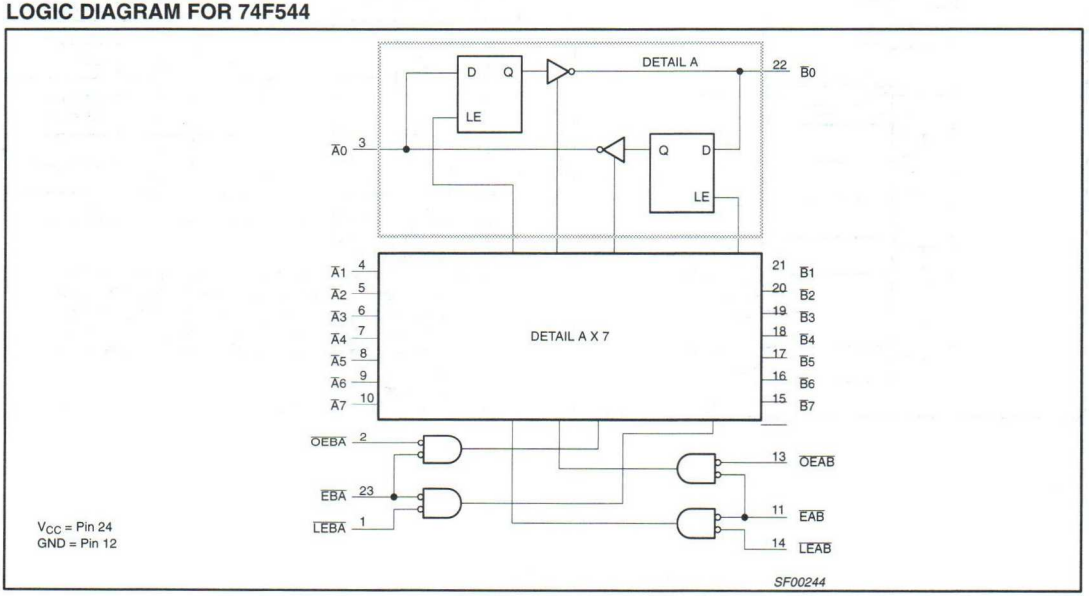
INPUTS				OUTPUTS		STATUS
$\overline{OEXX}$	$\overline{EXX}$	$\overline{LEXX}$	DATA	74F543	74F544	
H	X	X	X	Z	Z	Disabled
X	H	X	X	Z	Z	Disabled
L	↑	L	h	Z	Z	Disable + Latch
L	↑	L	l	Z	Z	
L	L	↑	h	H	L	Latch + Display
L	L	↑	l	L	H	
L	L	L	H	H	L	Transparent
L	L	L	L	L	H	
L	L	H	X	NC	NC	Hold

H = High voltage level
L = Low voltage level
h = High state must be present one setup time before the Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
l = Low state must be present one setup time before the Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
↑ = Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ XX = AB or BA
X = Don't care
NC = No change
Z = High impedance "off" state

LOGIC DIAGRAM FOR 74F543



LOGIC DIAGRAM FOR 74F544



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A0 - A7, $\overline{A0}$ - $\overline{A7}$	48	mA
		B0 - B7, $\overline{B0}$ - $\overline{B7}$	128	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A0 - A7, $\overline{A0}$ - $\overline{A7}$			-3	mA
		B0 - B7, $\overline{B0}$ - $\overline{B7}$			-15	mA
I_{OL}	Low-level output current	A0 - A7, $\overline{A0}$ - $\overline{A7}$			24	mA
		B0 - B7, $\overline{B0}$ - $\overline{B7}$			64	mA
T_{amb}	Operating free-air temperature range		-0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage	A0 - A7, $\overline{A0}$ - $\overline{A7}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		B0 - B7, $\overline{B0}$ - $\overline{B7}$		I_{OH} = -15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A0 - A7, $\overline{A0}$ - $\overline{A7}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B0 - B7, $\overline{B0}$ - $\overline{B7}$		I_{OL} = 64mA	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	$\overline{OEAB}$, $\overline{OEBA}$, $\overline{EAB}$	V_{CC} = MAX, V_I = 7.0 V					100	µA
		Others	V_{CC} = 5.5, V_I = 5.5V					1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	Others	V_{CC} = MAX, V_I = 0.5V					–0.6	mA
		$\overline{EAB}$, $\overline{EBA}$						–1.2	mA
I_{OZH} + I_{IH}	Off-state output current, high-level voltage applied		V_{CC}= MAX, V_O = 2.7V					70	µA
I_{OZH} + I_{IL}	Off-state output current, Low-level voltage applied		V_{CC}= MAX, V_O = 0. 5V					–600	µA
I_{OS}	Short-circuit output current[3]	A0 - A7, $\overline{A0}$ - $\overline{A7}$	V_{CC} = MAX			–60		–150	mA
		B0 - B7, $\overline{B0}$ - $\overline{B7}$				–100		–225	mA
I_{CC}	Supply current (total)	74F543	I_{CCH}	V_{CC} = MAX			70	105	mA
			I_{CCL}				95	135	mA
			I_{CCZ}				95	135	mA
		74F544	I_{CCH}	V_{CC} = MAX			80	110	mA
			I_{CCL}				105	140	mA
			I_{CCZ}				100	135	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under the recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS FOR 74F543

SYMBOL	PARAMETER	TEST CONDITIONS	74F543 LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = 5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 2	3.5 3.0	5.5 5.0	8.5 8.0	3.0 2.5	9.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 2	2.5 2.5	4.0 4.5	7.0 7.5	2.5 2.5	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to A_n	Waveform 1, 2	5.0 4.0	7.0 6.0	10.0 9.0	4.5 4.0	11.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEAB}$ to B_n	Waveform 1, 2	6.0 4.5	8.5 6.5	11.5 9.5	5.5 4.0	12.5 10.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBA}$ to A_n or $\overline{OEAB}$ to B_n	Waveform 4 Waveform 5	2.0 3.5	4.0 5.0	7.5 8.5	1.5 3.0	8.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBA}$ to A_n or $\overline{OEAB}$ to B_n	Waveform 4 Waveform 5	1.0 1.5	3.0 4.0	6.5 7.5	1.0 1.0	7.5 8.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{EBA}$ to A_n or $\overline{EAB}$ to B_n	Waveform 4 Waveform 5	4.5 5.0	7.0 7.0	10.5 10.5	4.0 4.5	11.5 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{EBA}$ to A_n or $\overline{EAB}$ to B_n	Waveform 4 Waveform 5	2.5 4.5	5.0 7.0	8.5 11.0	2.0 3.0	9.5 12.0	ns

AC SETUP REQUIREMENTS FOR 74F543

SYMBOL	PARAMETER	TEST CONDITIONS	74F543 LIMITS				UNIT
			T_{amb} = +25°C, V_{CC} = 5.0V, C_L = 50pF, R_L = 500Ω		T_{amb} = 0°C to +70°C, V_{CC} = 5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low A_n to $\overline{LEAB}$ or B_n to $\overline{LEBA}$	Waveform 3	0.0 2.5		0.0 3.0		ns
t_h(H) t_h(L)	Hold time, High or Low A_n to $\overline{LEAB}$ or B_n to $\overline{LEBA}$	Waveform 3	0.0 1.5		0.0 2.0		ns
t_s(H) t_s(L)	Setup time, High or Low A_n to $\overline{EAB}$ or B_n to $\overline{EBA}$	Waveform 3	1.0 2.5		1.5 3.0		ns
t_h(H) t_h(L)	Hold time, High or Low A_n to $\overline{EAB}$ or B_n to $\overline{EBA}$	Waveform 3	0.0 1.5		0.0 2.0		ns
t_w(L)	Latch enable pulse width, Low	Waveform 3	4.0		4.5		ns

AC ELECTRICAL CHARACTERISTICS FOR 74F544

SYMBOL	PARAMETER	TEST CONDITIONS	74F544 LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = 5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{B}_n$ or $\overline{B}_n$ to $\overline{A}_n$	Waveform 1	3.0 3.0	6.5 5.0	9.5 8.0	3.0 3.0	10.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to $\overline{A}_n$	Waveform 1, 2	4.0 4.0	7.0 7.0	9.5 9.5	4.0 4.0	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEAB}$ to $\overline{B}_n$	Waveform 1, 2	5.0 4.0	8.0 7.5	11.5 9.5	4.0 4.0	12.5 10.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBA}$ to $\overline{A}_n$ or $\overline{OEAB}$ to $\overline{B}_n$	Waveform 4 Waveform 5	2.0 3.5	4.0 5.5	7.0 8.5	1.5 3.0	7.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBA}$ to $\overline{A}_n$ or $\overline{OEAB}$ to $\overline{B}_n$	Waveform 4 Waveform 5	1.0 1.5	4.0 4.0	6.5 6.5	1.0 1.5	7.0 7.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{EBA}$ to $\overline{A}_n$ or $\overline{EAB}$ to $\overline{B}_n$	Waveform 4 Waveform 5	4.0 4.5	7.0 8.0	9.5 11.0	3.5 4.5	10.0 12.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{EBA}$ to $\overline{A}_n$ or $\overline{EAB}$ to $\overline{B}_n$	Waveform 4 Waveform 5	2.5 4.5	5.0 8.5	8.0 11.5	2.5 4.0	9.0 11.5	ns

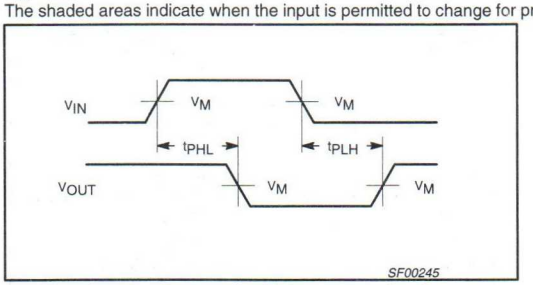
AC SETUP REQUIREMENTS FOR 74F544

SYMBOL	PARAMETER	TEST CONDITIONS	74F544 LIMITS				UNIT
			T_{amb} = +25°C, V_{CC} = 5.0V, C_L = 50pF, R_L = 500Ω		T_{amb} = 0°C to +70°C, V_{CC} = 5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low $\overline{A}_n$ to $\overline{LEAB}$ or $\overline{B}_n$ to $\overline{LEBA}$	Waveform 3	1.5 1.5		2.0 2.5		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{A}_n$ to $\overline{LEAB}$ or B_n to $\overline{LEBA}$	Waveform 3	1.5 2.0		2.5 2.5		ns
t_s(H) t_s(L)	Setup time, High or Low A_n to $\overline{EAB}$ or B_n to $\overline{EBA}$	Waveform 3	1.5 1.5		2.5 2.5		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{A}_n$ to $\overline{EAB}$ or $\overline{B}_n$ to $\overline{EBA}$	Waveform 3	1.5 2.0		2.0 2.0		ns
t_w(L)	Latch enable pulse width, Low	Waveform 3	4.0		4.5		ns

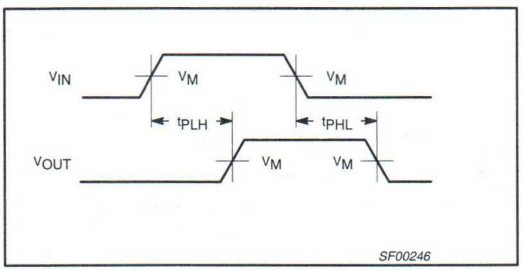
AC WAVEFORMS

V_M = 1.5V

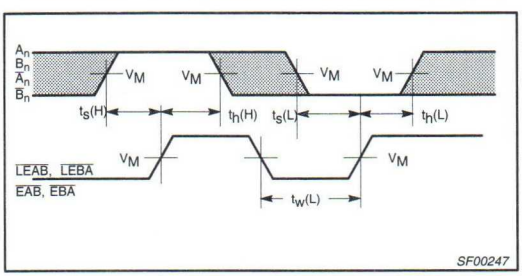
The shaded areas indicate when the input is permitted to change for predictable output performance.



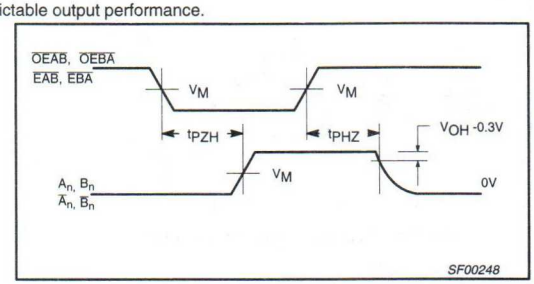
Waveform 1. Propagation Delay for Inverting Outputs



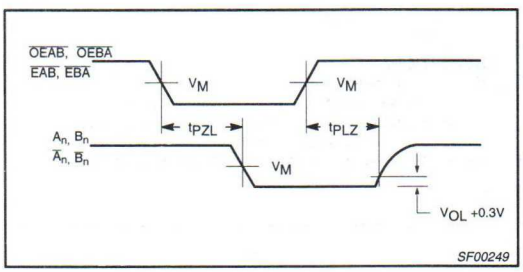
Waveform 2. Propagation Delay for Non-Inverting Outputs



Waveform 3. Data Setup Time and Hold Times, and Latch Enable Pulse Width

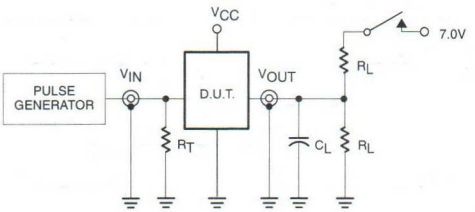


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

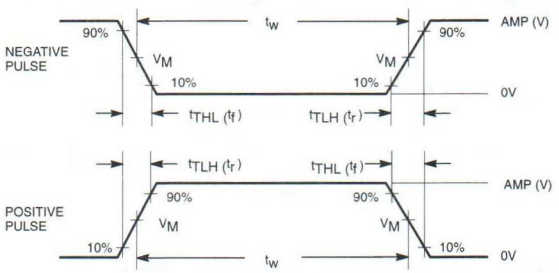


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

Octal bidirectional transceiver (with 3-State inputs/outputs) 74F545

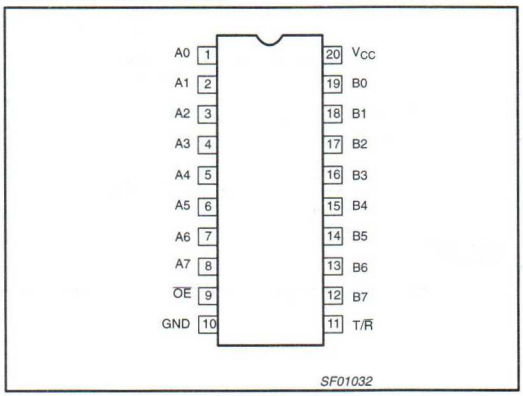
FEATURES

- High impedance NPN base inputs for reduced loading (70µA in High and Low states) output
- 8-bit bidirectional data flow reduces system package count
- 3-State inputs/outputs for interfacing with bus oriented systems
- 24mA and 64mA bus drive capability on A and B ports, respectively
- Transmit/Receive and Output Enable simplify control logic

DESCRIPTION

The 74F545 is an 8-bit, 3-State, high speed transceiver. It provides bidirectional drive for the bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 24mA bus drive capability on the A ports and 64mA bus drive capability on the B ports. One input, Transmit/Receive ($T/\overline{R}$) determines the direction of logic signals through the bidirectional transceiver. Transmit enables data from A ports to B ports; Receive enables data from B ports to A ports. The Output Enable input disables both A and B ports by placing them in a 3-State condition. The 74F545 performs the same function as the 74F245, the only difference being package pin assignment.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F545	4.0ns	87mA

ORDERING INFORMATION

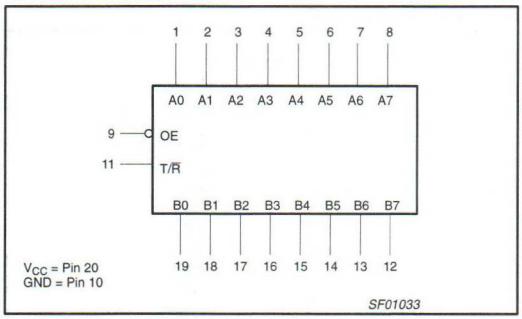
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
20-Pin Plastic DIP	N74F545N	SOT146-1
20-Pin Plastic SOL	N74F545D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

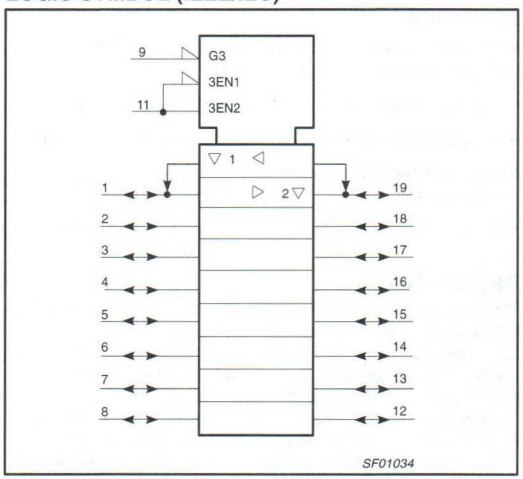
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0–A7, B0–B7	Data inputs	3.5/0.117	70µA/70µA
$\overline{OE}$	Output Enable input (active Low)	2.0/0.067	40µA/40µA
$T/\overline{R}$	Transmit/Receive input	2.0/0.067	40µA/40µA
A0 - A7	Port A 3-State outputs	150/40	3.0mA/24mA
B0 - B7	Port B 3-State outputs	750/107	15mA/64mA

NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

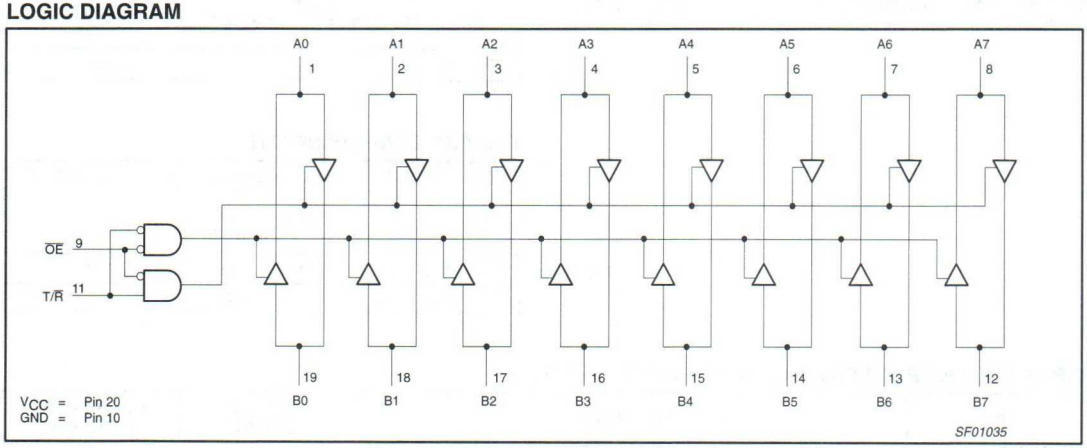
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}$	T/R	
L	L	Bus B data to Bus A
L	H	Bus A data to Bus B
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A0–A7	48	mA
		B0–B7	128	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A0–A7			–3	mA
		B0–B7			–15	mA
I_{OL}	Low-level output current	A0–A7			24	mA
		B0–B7			64	mA
T_{amb}	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage	A0–A7 B0–B7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
		B0–B7		I_{OH} = –15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A0–A7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B0–B7		I_{OL} = MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	$\overline{OE}$, T/$\overline{R}$	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A0–A7, B0–B7	V_{CC} = 5.5V, V_I = 5.5V					1.0	mA
I_{IH}	High-level input current	OE, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 2.7V					40	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					–40	µA
I_{OZH}+I_{IH}	Off-state output current High-level voltage applied		V_{CC} = MAX, V_I = 2.7V					70	µA
I_{OZL}+I_{IL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_I = 0.5V					–70	µA
I_{OS}	Short-circuit output current[3]	A0–A7	V_{CC} = MAX			–60		–150	mA
		B0–B7				–100		–225	µA
I_{CC}	Supply current (total)4	I_{CCH}	V_{CC} = MAX	T/$\overline{R}$=An=4.5V, $\overline{OE}$=GND			84	100	mA
		I_{CCL}		$\overline{OE}$=T/$\overline{R}$ =Bn=GND			96	120	mA
		I_{CCZ}		T/$\overline{R}$=Bn=GND, $\overline{OE}$=4.5V			96	120	mA

NOTES:

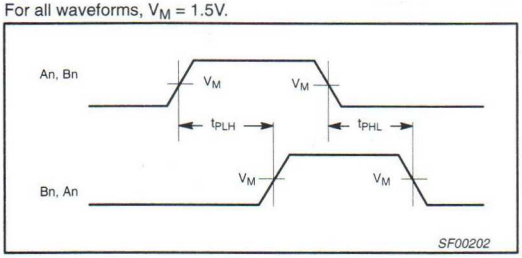
1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.
4. Measure I_{CC} with outputs open.

AC ELECTRICAL CHARACTERISTICS

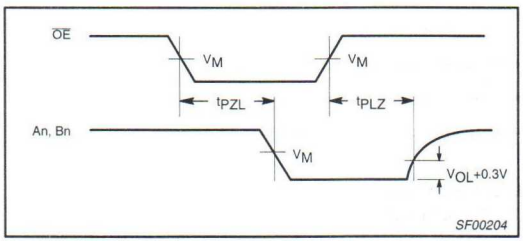
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω MIN	TYP	MAX	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω MIN	MAX	UNIT
t_{PLH}	Propagation delay	Waveform 1	1.5	3.5	5.5	1.5	6.5	ns
t_{PHL}	An to Bn, Bn to An		2.5	4.5	6.5	2.5	7.0	ns
t_{PZH}	Output Enable time	Waveform 2	6.0	8.5	10.5	6.0	11.0	ns
t_{PZL}	to High or Low level	Waveform 3	5.5	8.0	9.5	5.5	10.0	ns
t_{PHZ}	Output Disable time	Waveform 2	2.5	5.0	7.0	2.5	8.0	ns
t_{PLZ}	from High or Low level	Waveform 3	2.0	4.5	6.5	2.0	7.5	ns

AC WAVEFORMS

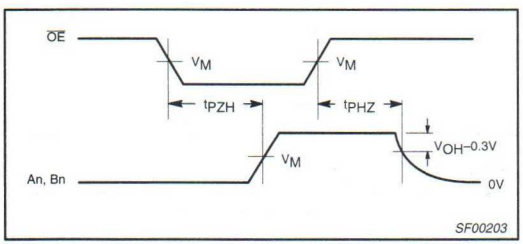
For all waveforms, V_M = 1.5V.



Waveform 1. Propagation Delay Data for Non-Inverting Output

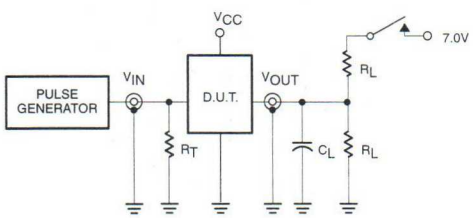


Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

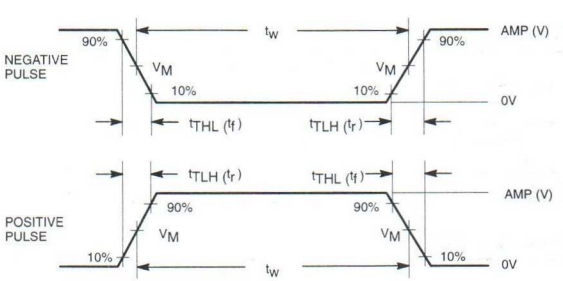


Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

Octal registered transceiver with parity and flags (3-State) 74F552

FEATURES

- 8-bit bidirectional I/O port with handshake
- Register status flag flip-flops
- Separate clock enable and output enable
- Parity generation and parity check
- B outputs and parity output sink 64mA

DESCRIPTION

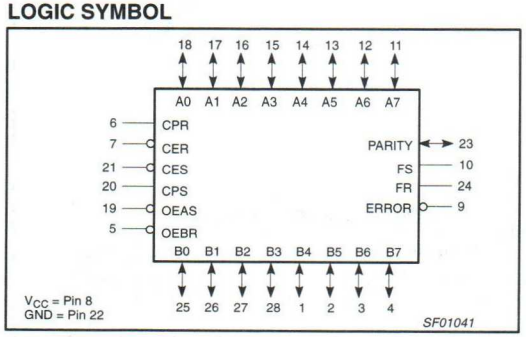
The 74F522 Octal Registered Transceiver contains two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own clock (CPR, CPS) and Clock Enable ($\overline{CER}$, $\overline{CES}$) inputs, as well as a flag flip-flop that is set automatically as the register is loaded. The flag output will be reset when the Output Enable returns to High after reading the output port. Each register has a separate Output Enable ($\overline{OEAS}$, $\overline{OEBR}$) for its 3-State buffer. The separate Clocks, Flags and Enables provide considerable flexibility as I/O ports for demand-response data transfer. When data is transferred from the A port to the B port, a parity bit is generated. On the other hand, when data is transferred from the B port to the A port, the parity of input data on B0–B7 is checked.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F552	85MHz	120mA

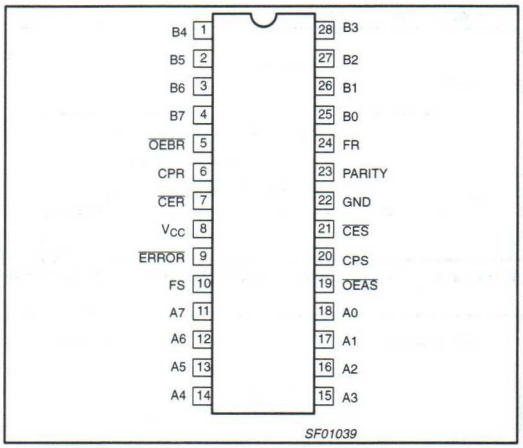
ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
28-Pin Plastic DIP (600mil)	N74F552N	SOT117-2
28-Pin Plastic SOL	N74F552D	SOT136-1

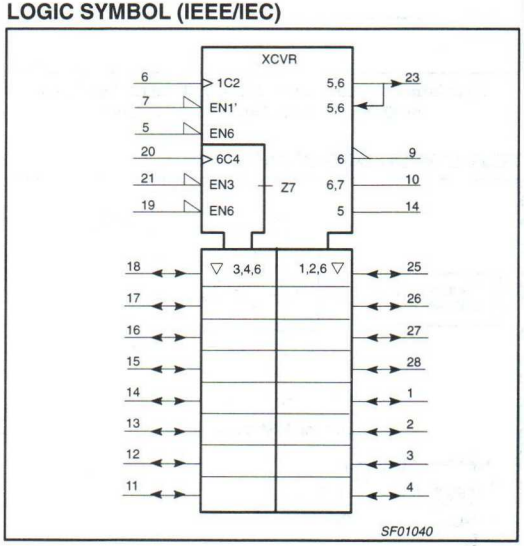
LOGIC SYMBOL



PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0–A7	A Data inputs	3.5/1.0	70μA/0.6mA
B0–B7	B Data inputs	3.5/1.0	70μA/0.6mA
CPR	R registers clock input (active rising edge)	1.0/1.0	20μA/0.6mA
CPS	S registers clock input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{CER}$	R registers clock Enable input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{CES}$	S registers clock Enable input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{OEBR}$	A-to-B Output Enable input (active Low) and clear FS output (active Low)	1.0/2.0	20μA/1.2mA
$\overline{OEAS}$	B-to-A Output Enable input (active Low) and clear FR output (active Low)	1.0/2.0	20μA/1.2mA
PARITY	Parity bit transceiver input	3.5/1.0	70μA/0.6mA
	Parity bit transceiver output	750/106.7	15mA/64mA
$\overline{ERROR}$	Parity check output (active Low)	50/33.3	1.0mA/20mA
A0–A7	A Data outputs	150/40	3.0mA/24mA
B0–B7	B Data outputs	750/106.7	15mA/64mA
FR	A-to-B Status Flag output (active High)	50/33.3	1.0mA/20mA
FS	B-to-A Status Flag output (active High)	50/33.3	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

FUNCTIONAL DESCRIPTION

Data applied to the A inputs are entered and stored on the rising edge of the CPR clock pulse, provided that the $\overline{CER}$ is Low; simultaneously, the status flip-flop is set and the A-to-B flag (FR) output goes High. As the $\overline{CER}$ returns to High, the data will be held in R register. This data entered from the A inputs will appear at the B port I/O pins after the $\overline{OEBR}$ has gone Low. When $\overline{OEBR}$ is Low, a parity bit appears at the PARITY pin, which will be set High when there is an even number of 1s or all 0s at the Q outputs of the R register. After the data is assimilated, the receiving system clears the flag FR, by changing the signal at the $\overline{OEBR}$ pin from Low to High. Data flow from B-to-A proceeds in the same manner described for A-to-B flow. A Low at the $\overline{CES}$ pin and a Low-to-High transition at the CPS pin enters the B input data and the parity input data into the S register and the parity register respectively and set the flag output FS to High. A Low signal at the $\overline{OEAS}$ pin enables the A port I/O pins and a Low-to-High transition of the $\overline{OEAS}$ signal clears the FS flag. When $\overline{OEAS}$ is Low, the parity check output $\overline{ERROR}$ will be High if there is an odd number of 1s at the Q outputs of the S register and the parity register.

R or S REGISTER FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
An or Bn	CPX	$\overline{CEX}$	INTERNAL Q	
X	X	H	NC	Hold data
L H	↑ ↑	L L	L H	Load data
X	↕	L	NC	Keep old data

H = High voltage level
L = Low voltage level
NC= No change
X = Don't care
X = **R** or **S** for **CPX** and $\overline{\textbf{CEX}}$
↑ = Low-to-High transition
↕ = Not Low-to-High transition

OUTPUT CONTROL TABLE

INPUT	OUTPUTS		OPERATING MODE
$\overline{OEXX}$	INTERNAL Q	An or Bn	
H	X	Z	Disable outputs
L L	L H	L H	Enable outpus

H = High voltage level
L = Low voltage level
X = Don't care
XX= **AS** or **BR**
Z = High impedance "off" state

R or S FLAG FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{CEX}$	CPX	$\overline{OEXX}$	FR or FS	
H	X	↑	NC	Hold flag
L	↑	↑	H	Set flag
X	X	↑	L	Clear flag

H = High voltage level
L = Low voltage level
NC= No change
X = Don't care
X = **R** or **S** for **CPX** and $\overline{\textbf{CEX}}$
XX= **AS** or **BR**
↑ = Low-to-High transition
↑ = Not Low-to-High transition

PARITY GENERATION FUNCTION TABLE

INPUTS		OUTPUTS		OPERATING MODE
$\overline{OEBR}$	CPR	Number of Highs in the Q outputs of the R register	PARITY	
H	X	X	Z	Hold flag
L L	↑ ↑	0,2,4,6,8 1,3,5,7	H L	Load data

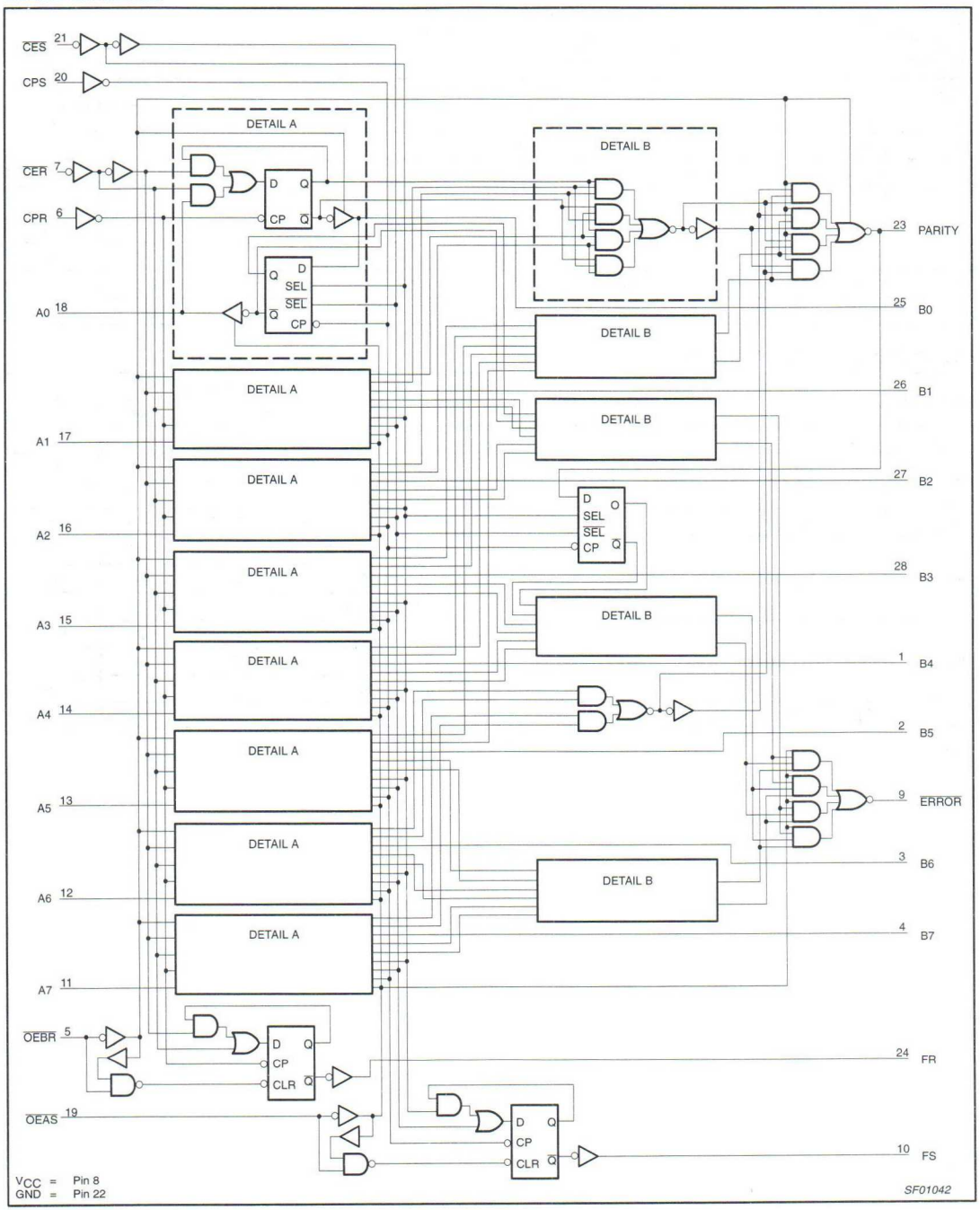
H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High transition

PARITY CHECK FUNCTION TABLE

INPUTS			OUTPUTS		OPERATING MODE
$\overline{OEAS}$	CPS	PARITY	Number of Highs in the Q outputs of the R register	$\overline{ERROR}$	
H	X	X	X	H	Parity check
L	↑	L	0,2,4,6,8	L	
L	↑	L	1,3,5,7	H	
L	↑	H	0,2,4,6,8	H	
L	↑	H	1,3,5,7	L	

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +V_{CC}	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	FR, FS, $\overline{ERROR}$	40	mA
		A0–A7	48	mA
		B0–B7, PARITY	128	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	FR, FS, $\overline{ERROR}$			−1	mA
		A0–A7			−3	mA
		B0–B7, PARITY			−15	mA
I_{OL}	Low-level output current	FR, FS, $\overline{ERROR}$			20	mA
		A0–A7			24	mA
		B0–B7, PARITY			64	mA
T_{amb}	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	FR, FS, $\overline{ERROR}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		A0–A7		I_{OH} = –3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
		B0–B7, PARITY		I_{OH} = –15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	FR. FS. $\overline{ERROR}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 20mA	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
		A0–A7		I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B0–B7, PARITY		I_{OL} = 48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL} = 64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = MAX, V_I = 7.0V					100	µA
		A0–A7, B0–B7, PARITY	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	others except A0–A7, B0–B7, PARITY	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	others	V_{CC} = MAX, V_I = 0.5V					–0.6	mA
		$\overline{OEAS}$, $\overline{OEBA}$						–1.2	mA
I_{OZH}+I_{IH}	Off-state output current High-level voltage applied	A0–A7, B0–B7, PARITY	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{OZL}+I_{IL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					–600	µA
I_{OS}	Short-circuit output current[3]	A0–A7, FS, FR, $\overline{ERROR}$	V_{CC} = MAX			–60		–150	mA
		B0–B7, PARITY				–100		–225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				115	170	mA
		I_{CCL}					125	185	mA
		I_{CCZ}					120	180	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.

AC ELECTRICAL CHARACTERISTICS

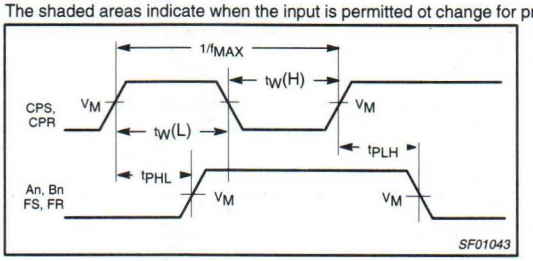
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum Clock Frequency	Waveform 1	70	85		60		MHz
t_{PLH} t_{PHL}	Propagation delay CPS to An or CPR to Bn	Waveform 1	3.5 4.0	5.0 6.0	8.0 9.0	3.0 3.5	8.5 9.0	ns ns
t_{PLH}	Propagation delay CPS to FS or CPR to FR	Waveform 1	3.0	5.0	7.5	2.5	8.5	ns
t_{PHL}	Propagation delay $\overline{OEAS}$ to FS or $\overline{OEBR}$ to FR	Waveform 2	4.0	6.0	8.5	3.5	9.0	ns
t_{PLH} t_{PHL}	Propagation delay CPS to $\overline{ERROR}$	Waveform 4	6.5 7.5	13.0 11.5	16.5 15.0	6.0 7.0	18.0 16.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CPR to PARITY	Waveform 4	6.5 10.5	8.5 13.5	11.0 17.0	5.5 10.0	12.5 18.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OEAS}$ to $\overline{ERROR}$	Waveform 1	3.5 3.0	5.5 5.0	8.0 7.0	3.0 2.5	8.5 8.0	ns ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEAS}$ to An or $\overline{OEBR}$ to Bn	Waveform 6 Waveform 7	2.5 4.0	4.0 6.5	7.0 9.5	2.0 4.0	8.0 10.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEAS}$ to An or $\overline{OEBR}$ to Bn	Waveform 6 Waveform 7	2.0 2.0	4.0 3.5	7.0 7.0	1.5 1.5	8.5 7.5	ns ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBR}$ to PARITY	Waveform 6 Waveform 7	2.0 4.0	4.0 5.5	7.0 8.0	2.0 3.0	7.5 9.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBR}$ to PARITY	Waveform 6 Waveform 7	2.0 2.0	4.0 4.0	7.0 7.5	2.0 2.0	7.5 8.0	ns ns

AC ELECTRICAL CHARACTERISTICS

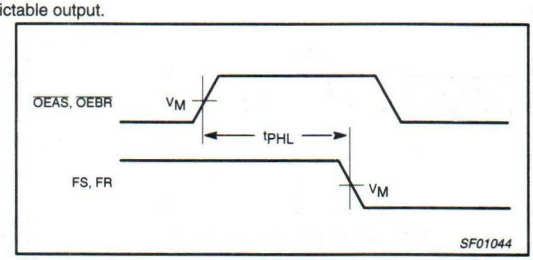
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low An or Bn or PARITY to CPS or CPR	Waveform 5	7.5 4.5			8.5 5.5		ns
t_h(H) t_h(L)	Hold time, High or Low An or Bn or PARITY to CPS or CPR	Waveform 5	0 0			0 0		ns
t_s(H) t_s(L)	Setup time, High or Low $\overline{CES}$ to CPS or $\overline{CER}$ to CPR	Waveform 5	7.0 7.0			7.5 7.5		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{CES}$ to CPS or $\overline{CER}$ to CPR	Waveform 5	0 0			0 0		ns
t_w(H) t_w(L)	CPS or CPR Pulse width, High or Low	Waveform 1	5.0 6.5			6.5 7.5		ns
t_{REC}	Recovery time $\overline{OEBR}$ to CPR or $\overline{OEAS}$ to CPS	Waveform 6	14.5			16.5		ns

AC WAVEFORMS

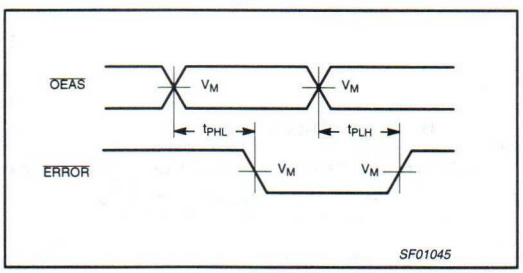
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted ot change for predictable output.



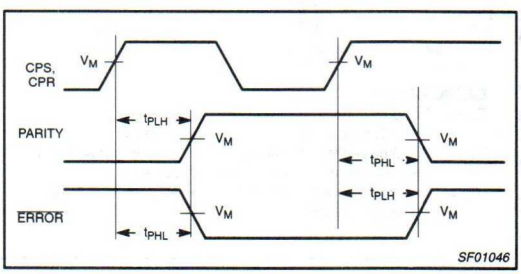
Waveform 1. Propagation Delay, Clock Input to Output and Maximum Clock Frequency



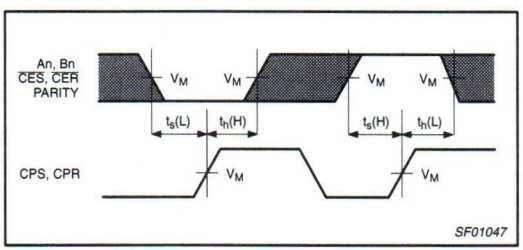
Waveform 2. Propagation Delay, Output Enable to Flag Output



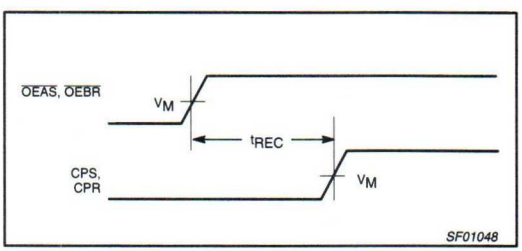
Waveform 3. Propagation Delay, Output Enable to ERROR



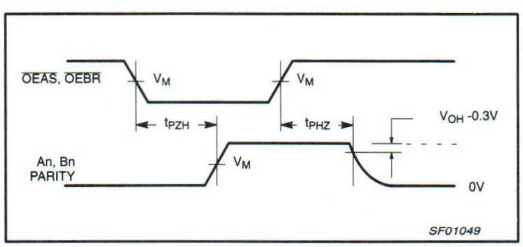
Waveform 4. Propagation Delay, Clock to PARITY and ERROR



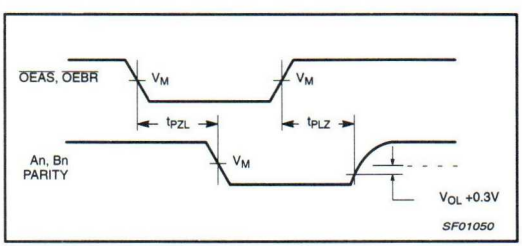
Waveform 5. Data Setup and Hold Times



Waveform 6. Recovery Time from Output Enable to Clock

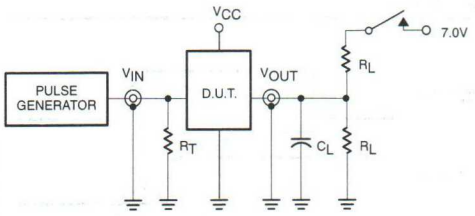


Waveform 7. 3-State Output Enable Time to High Level and Output Disable Time from High Level

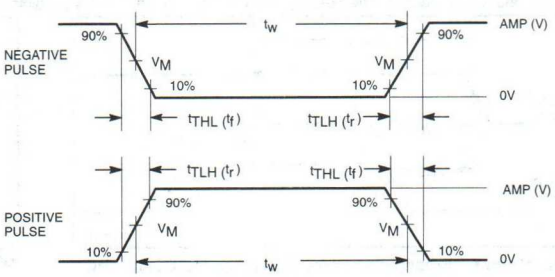


Waveform 8. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

Octal D flip-flop (3-State) 74F564

FEATURES

- 74F564 is broadside pinout version of 74F534
- Inputs and Outputs on opposite side of package allow easy interface to Microprocessors
- Useful as an Input or Ouput port for Microprocessors
- 3-State Ouputs for Bus interfacing
- Common Output Enable
- 74F574 is a non-inverting version of 74F564

DESCRIPTION

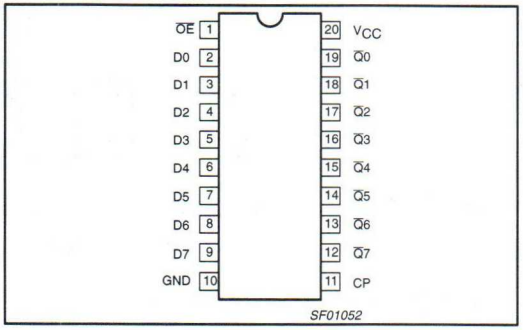
The 74F564 has a broadside pinout configuration to facilitate PC board layout and allows easy interface with microprocessors.

It is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's $\overline{Q}$ output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independently of the register operation. When $\overline{OE}$ is Low, data in the register appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F564	180MHz	50mA

ORDERING INFORMATION

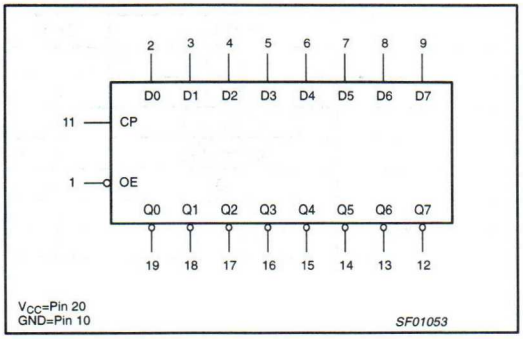
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG. DWG #
20-Pin Plastic DIP	N74F564N	SOT146-1
20-Pin Plastic SOL	N74F564D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

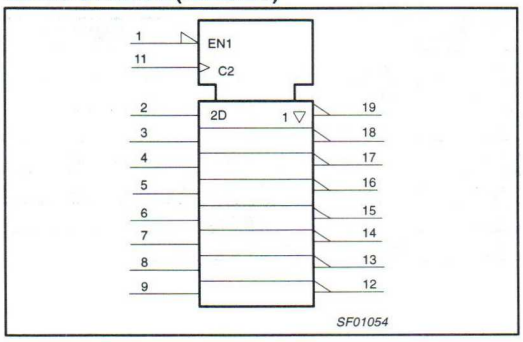
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 - D7	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{Q}0$ - $\overline{Q}7$	3-State outputs	150/40	3.0mA/24mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

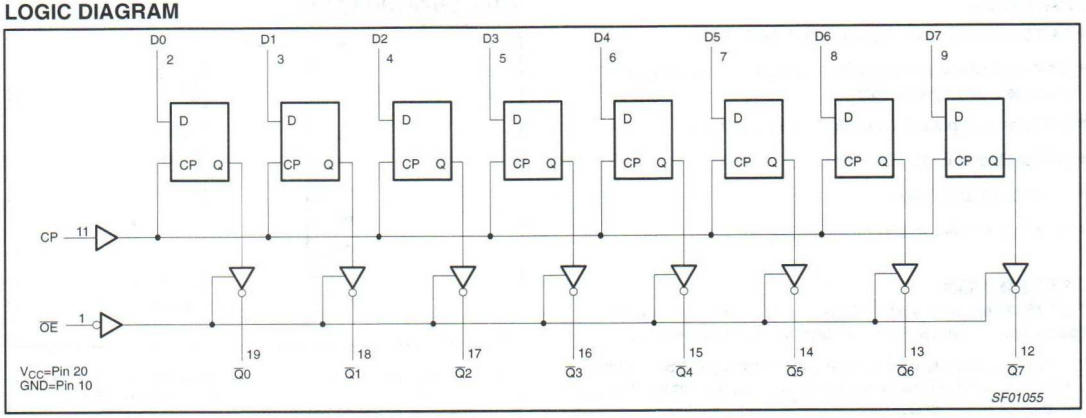
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODES
$\overline{OE}$	CP	Dn		$\overline{Q0} - \overline{Q7}$	
L	↑	l	L	H	Load and read register
L	↑	h	H	L	
L	↕	X	NC	NC	Hold
H	↕	X	NC	Z	Disable outputs
H	↑	Dn	Dn	Z	

H = High voltage level
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↕ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–3	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				–50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			45	65	mA
		I_{CCL}				50	75	mA
		I_{CCZ}				55	80	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb}= +25°C V_{CC} = +5V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum Clock frequency	Waveform 1	160	180		150		MHz
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}$n	Waveform 1	3.5 3.5	5.0 5.0	8.0 8.0	3.0 3.0	8.5 8.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 4 Waveform 5	2.5 4.0	4.5 5.5	7.5 8.0	2.0 3.5	8.0 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 4 Waveform 5	1.0 1.0	3.0 2.5	6.0 5.5	1.0 1.0	7.0 6.0	ns

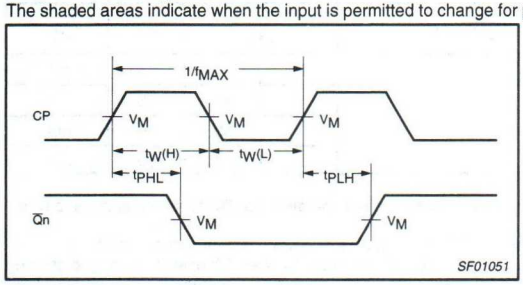
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb}= +25°C V_{CC} = +5V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time, Dn to CP	Waveform 3	2.0 2.0			2.0 2.5		ns
t_h(H) t_h(L)	Hold time, Dn to CP	Waveform 3	1.0 1.0			1.5 1.5		ns
t_w(H) t_w(L)	CP pulse width, High or Low	Waveform 1	3.5 3.5			3.5 3.5		ns

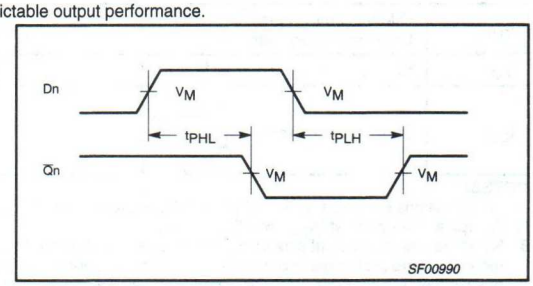
AC WAVEFORMS

For all waveforms, V_M = 1.5V

The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay, Clock and Enable Inputs to Output, Enable, Clock Pulse Widths, and Maximum Clock Frequency

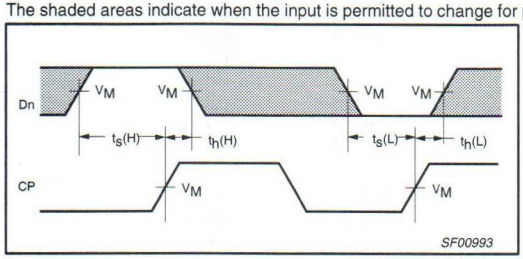


Waveform 2. Propagation Delay for Data to Outputs

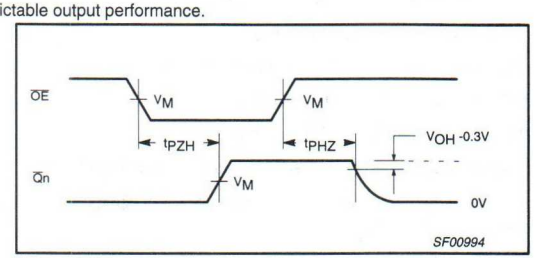
AC WAVEFORMS (Continued)

For all waveforms, $V_M = 1.5V$

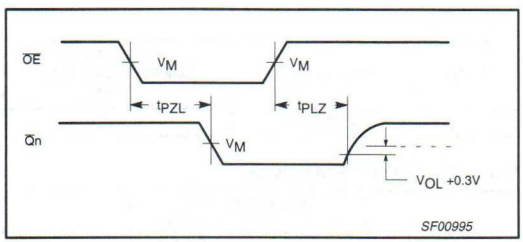
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 3. Data Setup and Hold Times

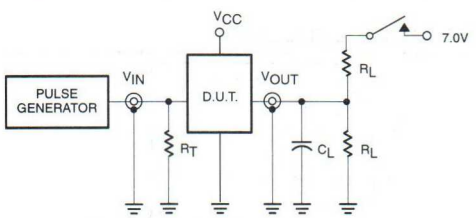


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

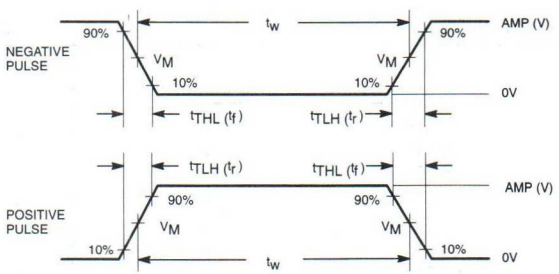


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

4-bit bidirectional binary synchronous counter (3-State) 74F569

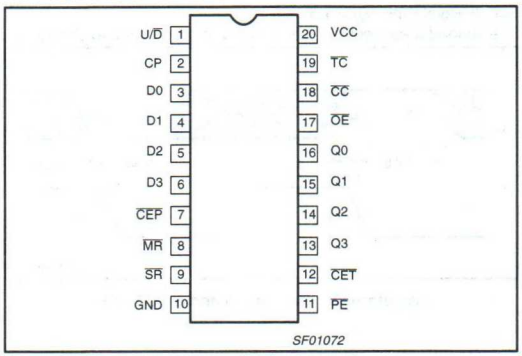
FEATURES

- 4-bit bidirectional counting – binary counter
- Synchronous counting and loading
- Look ahead carry capability for easy cascading
- Preset capability for programmable operation
- Master Reset ($\overline{MR}$) overrides all other inputs
- Synchronous Reset ($\overline{SR}$) overrides counting and parallel loading
- Clock Carry ($\overline{CC}$) output to be used as a clock for flip-flops, register and counters
- 3-State outputs for bus organized systems

DESCRIPTION

The 74F569 is a fully synchronous Up/Down binary counter. It features preset capabilities for programmable operation, carry look ahead for programmable operation, carry look ahead for easy cascading, and U/$\overline{D}$ input to control the direction of counting. For maximum flexibility there are both Synchronous and Master Reset inputs as well as both Clocked Carry ($\overline{CC}$) and Terminal Count ($\overline{TC}$) outputs. All state changes except Master Reset are initiated by rising edge of the clock. A High signal on the Output Enable ($\overline{OE}$) input forces the output buffers into the high impedance state but does not prevent counting, resetting or parallel loading.

PIN CONFIGURATION

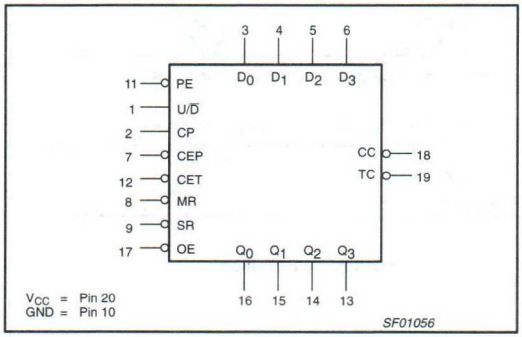


TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F569	115MHz	40mA

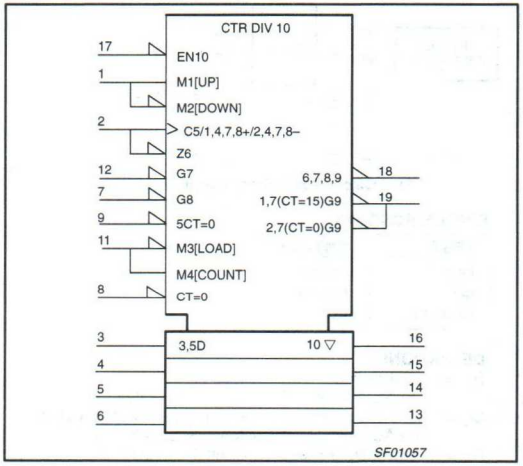
ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PKG. DWG. #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
20-pin plastic DIP	N74F569N	SOT146-1
20-pin plastic SO	N74F569D	SOT163-1

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 - D3	Parallel data inputs	1.0/1.0	20μA/0.6mA
$\overline{CEP}$	Count Enable parallel input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/2.0	20μA/1.2mA
CP	Clock input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/2.0	20μA/1.2mA
U/$\overline{D}$	Up/Down count control input	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output Enable input	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master Reset input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{SR}$	Synchronous Reset (active Low)	1.0/1.0	20μA/0.6mA
$\overline{TC}$	Terminal count output (active Low)	50/33	1.0mA/20mA
$\overline{CC}$	Clocked carry output (active Low)	50/33	1.0mA/20mA
Q0 - Q3	Data outputs	150/40	3.0mA/24mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

FUNCTIONAL DESCRIPTION

The 74F569 counts in the modulo-16 binary sequence. From state 0 (LLLL) it will increment to 15 in the up mode; in the down mode it will decrement from 15 to 0. The clock inputs of all flip-flops are driven parallel through a clock buffer. All state changes (except due to Master Reset) occur synchronously with the Low-to-High transition of the Clock Pulse ($\overline{CP}$) input.

The circuit has five fundamental modes of operation, in order of precedence: asynchronous reset, synchronous reset, parallel load, count and hold. Six control inputs–Master Reset ($\overline{MR}$), Synchronous Reset ($\overline{SR}$), Count Enable Trickle ($\overline{CET}$), Parallel Enable ($\overline{PE}$), Count Enable Parallel ($\overline{CEP}$), and the Up/Down (U/$\overline{D}$) input – determine the mode of operation, as shown in the Function Table.

A Low signal on $\overline{MR}$ overrides all other inputs and asynchronously forces the flip-flop Q outputs Low. A Low signal on $\overline{SR}$ overrides counting and parallel loading and allows the Q output to go Low on the next rising edge of CP. A Low signal on $\overline{PE}$ overrides counting and allows information on the parallel data (Dn) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{MR}$, $\overline{SR}$, and $\overline{PE}$ High, $\overline{CEP}$ and $\overline{CET}$ permit counting when both are Low. Conversely, a High signal on either $\overline{CEP}$ and $\overline{CET}$ inhibits counting.

The 74F569 uses edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, $\overline{CEP}$, $\overline{CET}$ or U/$\overline{D}$ inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed. Two types of outputs are provided as overflow/underflow indicators. The Terminal Count ($\overline{TC}$) output is normally High and goes Low provided $\overline{CET}$ is Low, when the counter reaches zero in the down mode, or reaches maximum 15 in the up mode

$\overline{TC}$ will then remain Low until a state change occurs by counting or presetting, or until U/$\overline{D}$ or $\overline{CET}$ is changed.

To implement synchronous multistage counters, the connections between the $\overline{TC}$ output and the $\overline{CEP}$ and $\overline{CET}$ inputs can provide either slow or fast carry propagation. Figure 1 shows the connections for a simple ripple carry, in which the clock period must be longer than the CP to $\overline{TC}$ delay of the first stage, plus the cumulative $\overline{CET}$ to $\overline{TC}$ delays of the intermediate stages, plus the $\overline{CET}$ to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry look ahead connections in Figure 2 are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from Max to Min in the up mode, or Min to Max in the down mode, to start its final cycle. Since this takes 16 clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to $\overline{TC}$ delay of the first stage plus the $\overline{CEP}$ to CP setup time of the last stage. The $\overline{TC}$ output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, register or counters.

For such applications, the Clocked Carry ($\overline{CC}$) output is provided. The $\overline{CC}$ output is normally High. When $\overline{CEP}$, $\overline{CET}$, and $\overline{TC}$ are Low, the $\overline{CC}$ output will go Low, when the clock next goes Low and will stay Low until the clock goes High again; as shown in the $\overline{CC}$ Function Table. When the Output Enable ($\overline{OE}$) is Low, the parallel data outputs Q0–Q3 are active and follow the flip-flop Q outputs. A High signal on $\overline{OE}$ forces Q0–Q3 to the High impedance state but does not prevent counting, loading or resetting.

LOGIC EQUATIONS:
Count Enable=$\overline{CEP}\times\overline{CET}\times\overline{PE}$
Up: $\overline{TC}=Q0\times Q1\times Q2\times Q3\times(Up)\times\overline{CET}$
Down: $\overline{TC}=\overline{Q0}\times\overline{Q1}\times\overline{Q2}\times\overline{Q3}\times(Down)\times\overline{CET}$

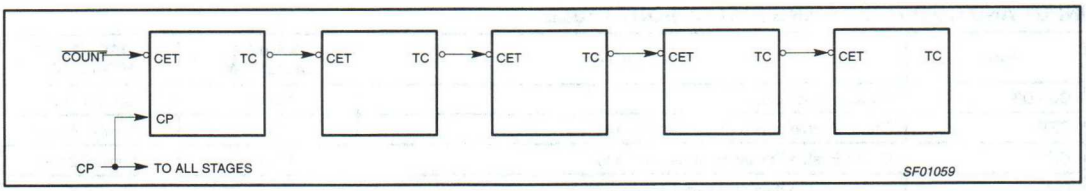


Figure 1. Multistage Counter with Ripple Carry

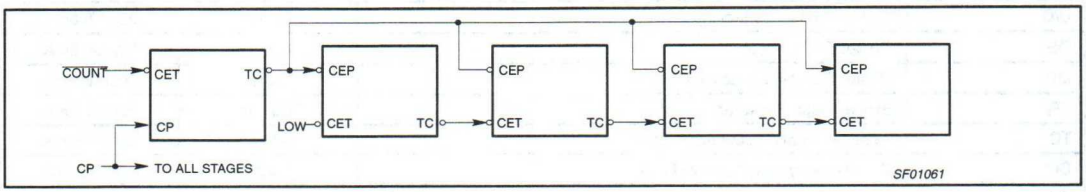
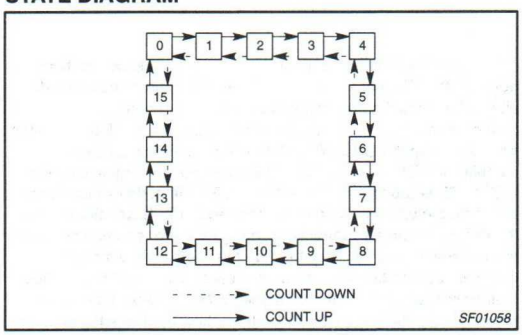


Figure 2. Multistage Counter with Look-Ahead Carry

STATE DIAGRAM



$\overline{CC}$ FUNCTION TABLE

INPUTS						OUTPUT
$\overline{SR}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	$\overline{TC}$*	CP	$\overline{CC}$
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	H	X	X	X	H
X	X	X	H	X	X	H
X	X	X	X	H	X	H
H	H	L	L	L	⊓	⊓

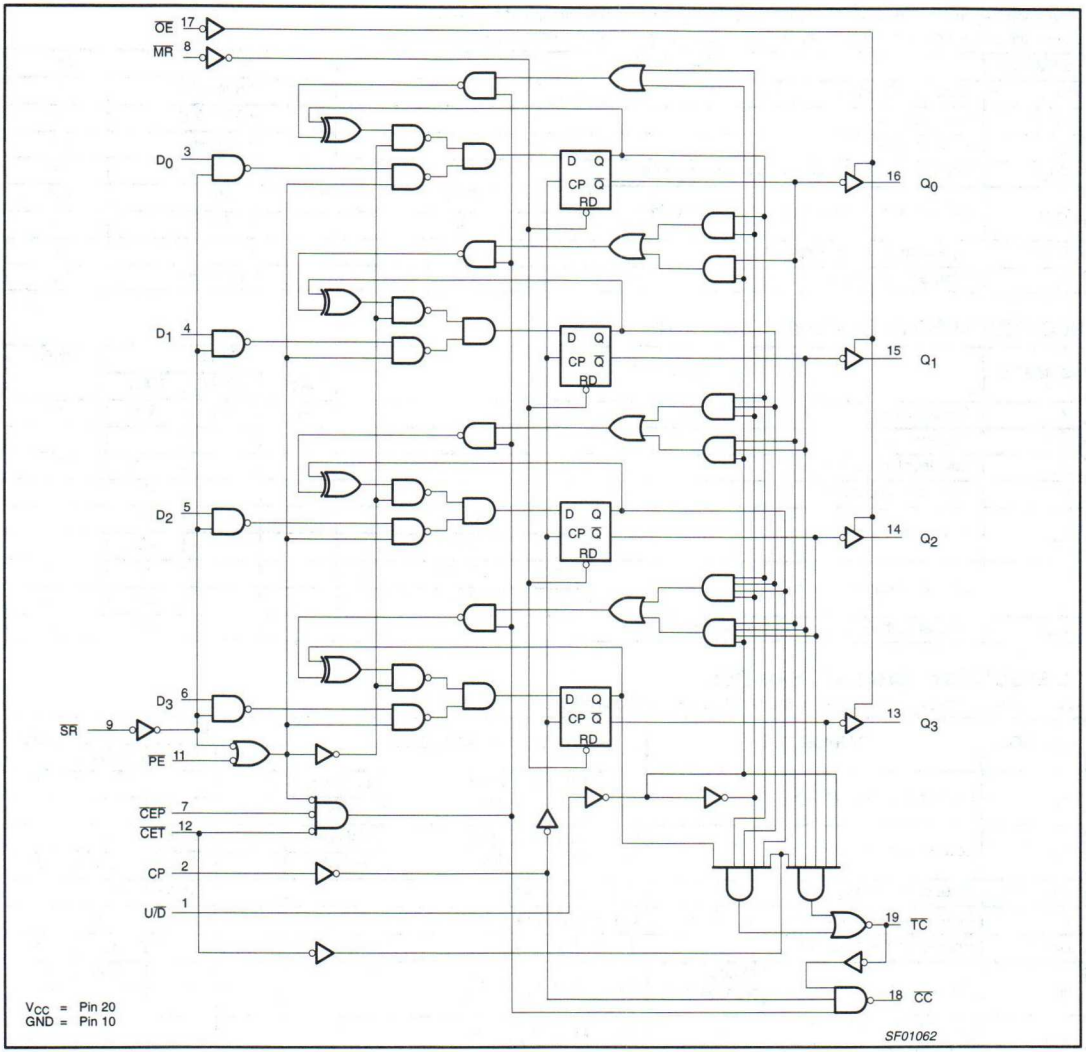
* = $\overline{TC}$ is generated internally
H = High voltage level
L = Low voltage level
X = Don't care
⊓ = Low Pulse

FUNCTION TABLE

INPUTS							OPERATING MODE
$\overline{MR}$	$\overline{SR}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	CP	
L	X	X	X	X	X	X	Asynchronous reset
h	l	X	X	X	X	↑	Synchronous reset
h	h	l	X	X	X	↑	Parallel load
h	h	h	l	l	h	↑	Count Up (increment)
h	h	h	l	l	l	↑	Count Down (decrement)
h	H	H	H	X	X	X	Hold (do nothing)
h	H	H	X	H	X	X	

H = High voltage level
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	$\overline{TC}$, $\overline{CC}$	40	mA
		Qn	48	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	$\overline{TC}$, $\overline{CC}$			−1	mA
		Qn			−3	mA
I_{OL}	Low-level output current	$\overline{TC}$, $\overline{CC}$			20	mA
		Qn			24	mA
T_{amb}	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	Others	V_{CC} = MAX, V_I = 0.5V				−0.6	mA
		$\overline{CET}$, $\overline{PE}$					−1.2	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 0.5V				−50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			38	60	mA
		I_{CCL}				43	62	mA
		I_{CCZ}				40	60	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = +5.V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.V ± 10%, C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Qn	Waveform 1	100	115		90		MHz
		$\overline{CC}$, $\overline{TC}$	Waveform 2	50	65		45		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$, High or Low)		Waveform 1	3.0 4.0	6.0 7.5	9.5 11.0	3.0 4.0	10.0 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$		Waveform 2	5.5 4.0	10.0 7.5	15.0 11.0	5.5 4.0	16.0 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$		Waveform 3	1.5 2.5	3.0 5.0	6.0 8.0	1.0 2.5	7.0 9.0	ns ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$		Waveform 4	4.0 4.0	7.5 6.5	11.0 11.0	4.0 4.0	12.0 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{CC}$		Waveform 2	2.5 2.0	4.5 4.0	7.5 6.6	2.0 2.0	6.0 7.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CEP}$, $\overline{CET}$ to $\overline{CC}$		Waveform 2	2.0 3.5	4.0 5.5	7.0 9.0	1.5 3.0	7.5 10.0	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn		Waveform 5	6.0	8.0	11.0	5.5	12.0	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{CC}$		Waveform 4	4.5 5.0	9.0 11.0	12.0 16.0	4.0 5.0	13.5 17.0	ns ns
t_{PHL}	Propagation delay MR to $\overline{TC}$, $\overline{CC}$		Waveform 5	8.0	11.0	15.0	7.5	16.0	ns ns
t_{PLH} t_{PHL}	Propagation delay SR to $\overline{CC}$		Waveform 3	5.5 7.5	8.0 9.5	11.0 12.0	5.0 7.0	12.0 13.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PE}$ to $\overline{CC}$		Waveform 3	3.0 4.0	5.0 6.0	8.0 8.5	2.5 4.0	8.5 9.5	ns ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level $\overline{OE}$ to Qn		Waveform 10 Waveform 11	2.0 4.5	4.0 6.5	7.0 9.5	2.0 4.0	7.5 10.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level $\overline{OE}$ to Qn		Waveform 10 Waveform 11	1.5 1.5	3.5 3.5	6.5 6.0	1.5 1.5	7.5 6.5	ns ns

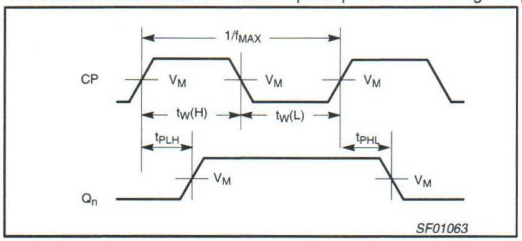
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS				UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω		T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 6	4.0 4.0		4.5 4.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 6	2.0 2.0		2.5 2.5		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 7	5.0 5.0		6.0 6.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 7	0 0		0 0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP	Waveform 6	8.0 8.0		9.0 9.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP	Waveform 6	0 0		0 0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low U/$\overline{D}$ to CP	Waveform 8	10.0 8.0		12.5 8.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low U/$\overline{D}$ to CP	Waveform 8	0 0		0 0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{SR}$ to CP	Waveform 9	8.0 8.0		9.0 9.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{SR}$ to CP	Waveform 9	0 0		0 0		ns ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	7.0 5.0		8.0 6.0		ns ns
$t_w(H)$	$\overline{MR}$ Pulse width, Low	Waveform 5	4.5		5.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP	Waveform 5	6.0		7.0		ns

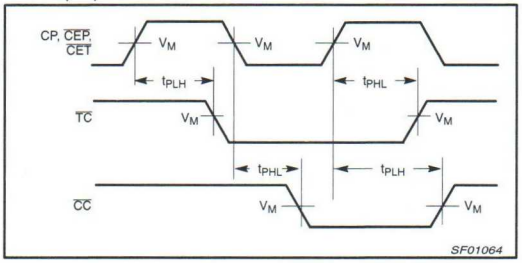
AC WAVEFORMS

For all waveforms, V_M = 1.5V

The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

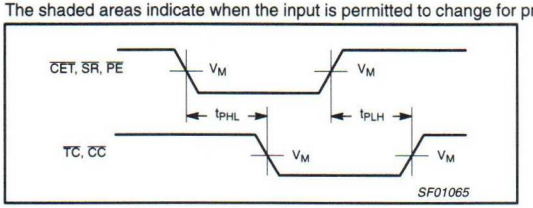


Waveform 2. Propagation Delay, CP, $\overline{CET}$, and $\overline{CEP}$ to $\overline{CC}$ and CP to $\overline{TC}$

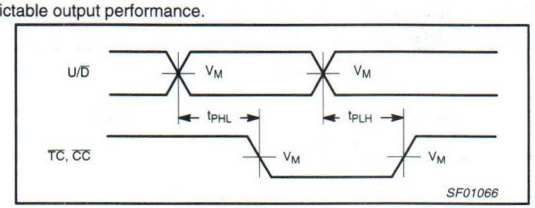
AC WAVEFORMS (Continued)

For all waveforms, $V_M = 1.5V$

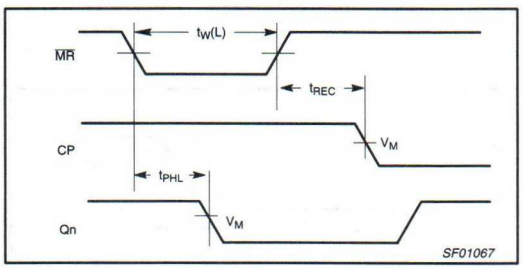
The shaded areas indicate when the input is permitted to change for predictable output performance.



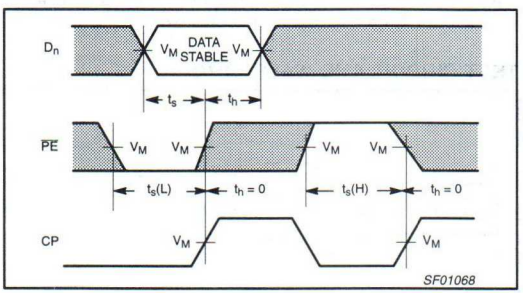
Waveform 3. Propagation Delays $\overline{CET}$ to $\overline{TC}$ and $\overline{SR}$ or $\overline{PE}$ to $\overline{CC}$



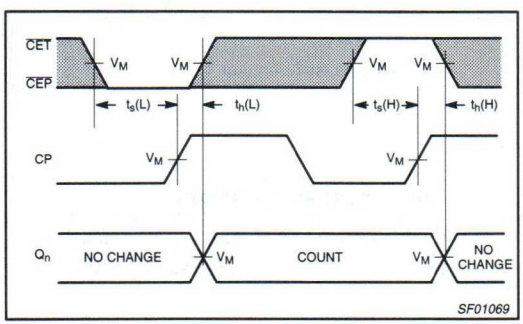
Waveform 4. Propagation Delays U/D to $\overline{TC}$ and $\overline{CC}$



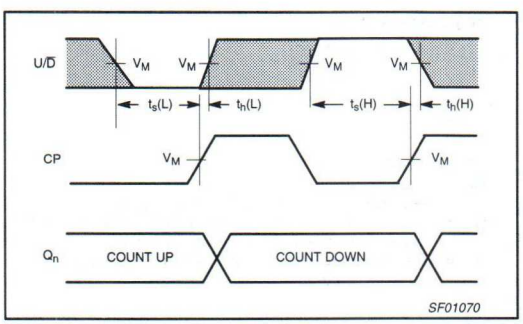
Waveform 5. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



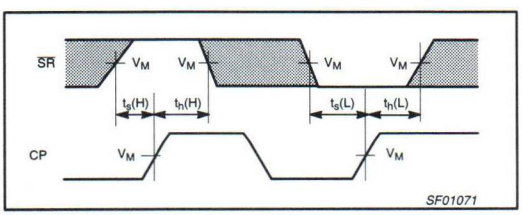
Waveform 6. Parallel Data and Parallel Enable Setup and Hold Times



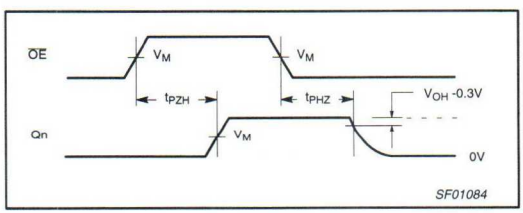
Waveform 7. Count Enable Data Setup and Hold Times



Waveform 8. Up/Down Control Setup and Hold Times



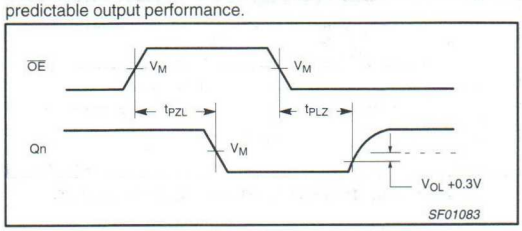
Waveform 9. Synchronous Reset Setup and Hold Times



Waveform 10. 3-State Output Enable Time to High Level and Output Disable Time from High Level

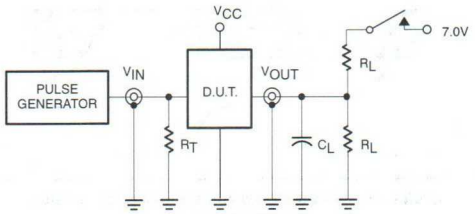
AC WAVEFORMS (Continued)

For all waveforms, V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

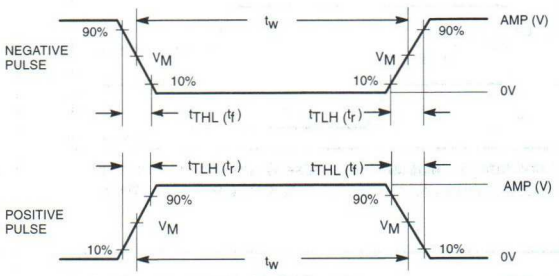


Waveform 11. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

Latch/flip-flop | 74F573/74F574

74F573 Octal Transparent Latch (3-State)
74F574 Octal D Flip-Flop (3-State)

FEATURES

- 74F573 is broadside pinout version of 74F373
- 74F574 is broadside pinout version of 74F374
- Inputs and Outputs on opposite side of package allow easy interface to Microprocessors
- Useful as an Input or Output port for Microprocessors
- 3-State Outputs for Bus interfacing
- Common Output Enable
- 74F563 and 74F564 are inverting version of 74F573 and 74F574 respectively
- 3-State Outputs glitch free during power-up and power-down
- These are High-Speed replacements for N8TS805 and N8TS806

DESCRIPTION

The 74F573 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.

The 74F573 is functionally identical to the 74F373 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

The data on the D inputs is transferred to the latch outputs when the Enable (E) input is High. The latch remains transparent to the data input while E is High and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent to the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

The 74F574 is functionally identical to the 74F374 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocesors.

It is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independently of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F573	5.0ns	35mA

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F574	180MHz	50mA

ORDERING INFORMATION

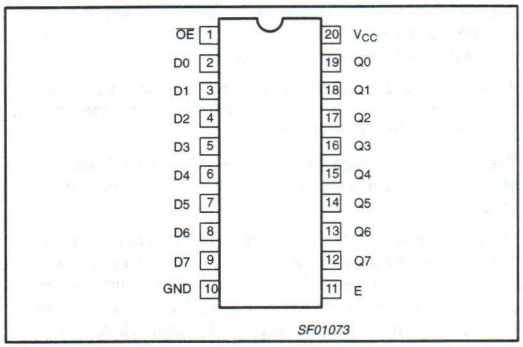
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
20-Pin Plastic DIP	N74F573N, N74F574N	SOT146-1
20-Pin Plastic SOL	N74F573D, N74F574D	SOT163-1
20-Pin Plastic SSOP	N74F573DB	SOT339-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

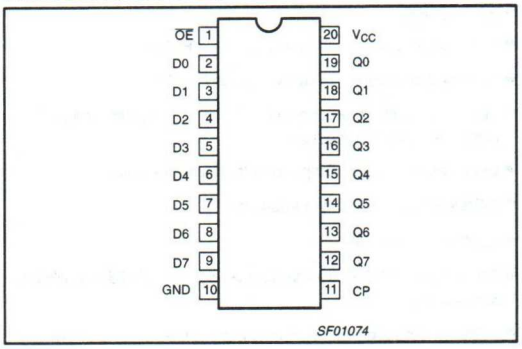
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 - D7	Data inputs	1.0/1.0	20µA/0.6mA
E (74F573)	Latch Enable input (active falling edge)	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
CP (74F574)	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
Q0 - Q7	3-State outputs	150/40	3.0mA/24mA

NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

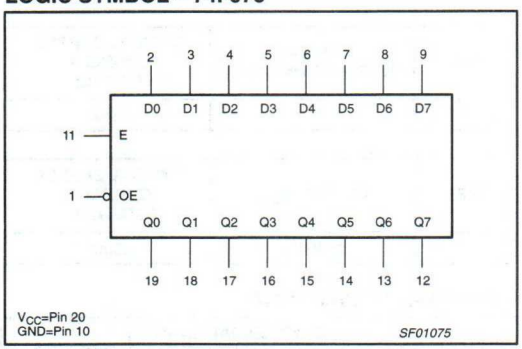
PIN CONFIGURATION – 74F573



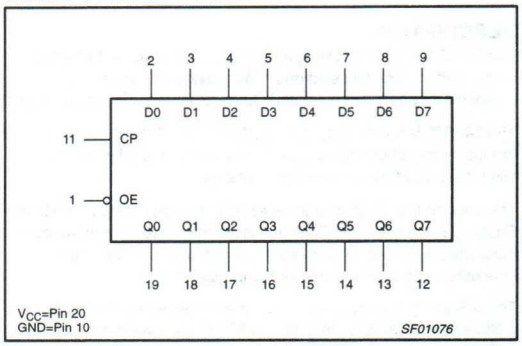
PIN CONFIGURATION – 74F574



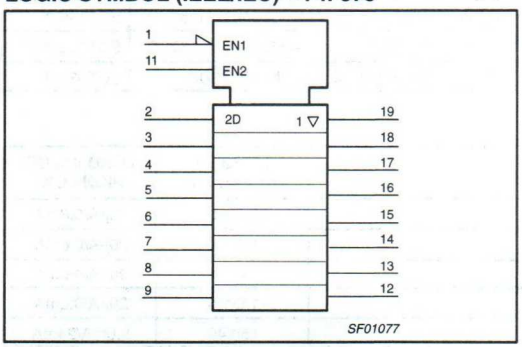
LOGIC SYMBOL – 74F573



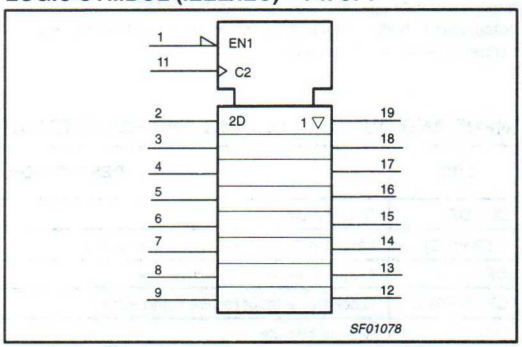
LOGIC SYMBOL – 74F574



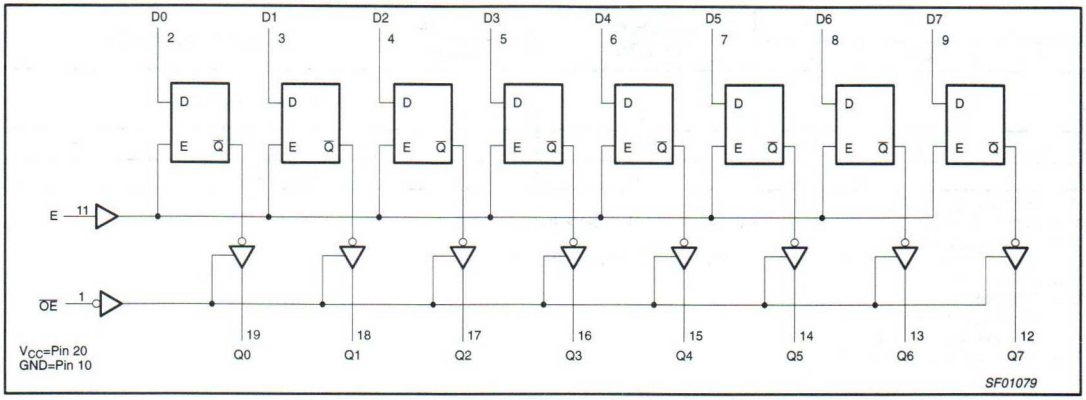
LOGIC SYMBOL (IEEE/IEC) – 74F573



LOGIC SYMBOL (IEEE/IEC) – 74F574



LOGIC DIAGRAM – 74F573

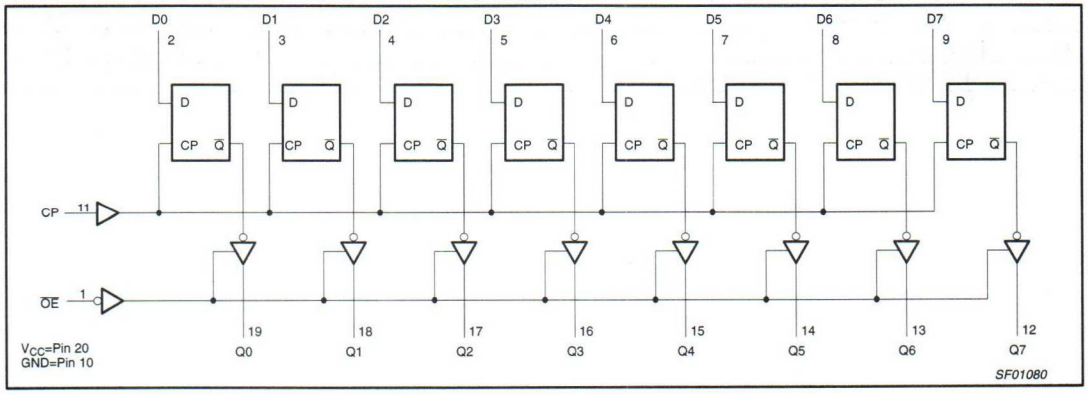


FUNCTION TABLE – 74F573

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODES
$\overline{OE}$	E	Dn		Q0 – Q7	
L	H	L	L	L	Load and read register
L	H	H	H	H	
L	↓	l	L	L	Latch and read register
L	↓	h	H	H	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	Dn	Dn	Z	

H = High voltage level
h = High voltage level one setup time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one setup time prior to the High-to-Low E transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

LOGIC DIAGRAM – 74F574



FUNCTION TABLE – 74F574

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODES
$\overline{OE}$	CP	Dn		Q0 – Q7	
L	↑	l	L	L	Load and read register
L	↑	h	H	H	
L	↧	X	NC	NC	Hold
H	↑	Dn	Dn	Z	Disable outputs

H = High voltage level
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↧ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–3	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V				–50	µA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	74F573	V_{CC} = MAX			30	40	mA
		I_{CCL}					35	50	mA
		I_{CCZ}					40	60	mA
		I_{CCH}	74F574	V_{CC} = MAX			45	65	mA
		I_{CCL}					50	70	mA
		I_{CCZ}					55	85	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb}= +25°C, V_{CC} = +5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5V ± 10%, C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	74F573	Waveform 2	3.0 1.0	5.5 3.5	8.0 6.0	2.5 1.0	9.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay E to Qn		Waveform 1	4.5 3.0	8.5 5.0	11.5 7.0	4.0 2.5	12.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 6 Waveform 7	2.5 2.5	5.5 5.5	9.5 8.0	2.0 2.0	10.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 6 Waveform 7	1.0 1.0	3.0 2.5	6.0 5.5	1.0 1.0	6.5 5.5	ns
f_{MAX}	Maximum Clock frequency	74F574	Waveform 1	160	180		150		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn		Waveform 1	3.5 3.5	5.0 5.0	7.5 7.5	3.0 3.0	8.0 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 6 Waveform 7	2.5 3.0	4.5 5.0	7.5 8.0	2.0 3.0	7.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 6 Waveform 7	1.0 1.0	3.0 2.5	5.5 5.5	1.0 1.0	6.0 6.0	ns

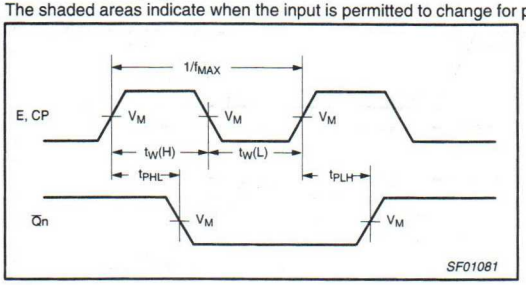
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb}= +25°C, V_{CC} = +5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, Dn to E	74F573	Waveform 4	0.0 1.5			0.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, Dn to E		Waveform 4	2.5 4.0			2.5 4.0		ns
$t_w(H)$	E pulse width, High		Waveform 1	3.0			3.5		ns
$t_s(H)$ $t_s(L)$	Setup time, Dn to CP	74F574	Waveform 5	2.5 2.5			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, Dn to CP		Waveform 5	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low		Waveform 1	3.0 3.5			3.0 4.0		ns

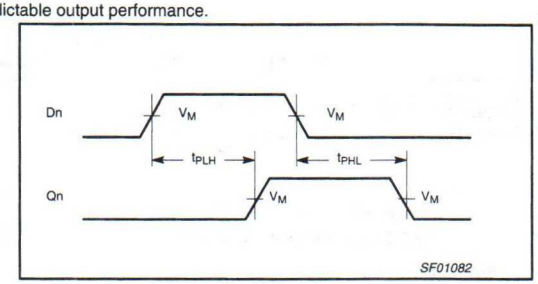
AC WAVEFORMS

For all waveforms, $V_M = 1.5V$

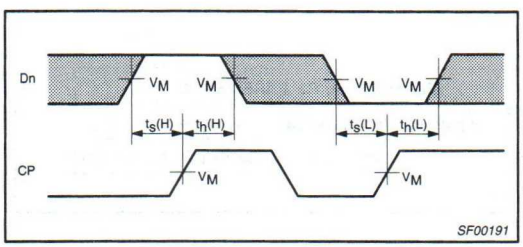
The shaded areas indicate when the input is permitted to change for predictable output performance.



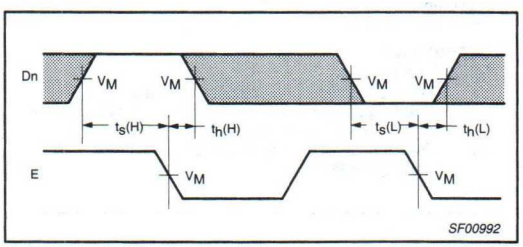
Waveform 1. Propagation Delay, Clock and Enable Inputs to Output, Enable, Clock Pulse Widths, and Maximum Clock Frequency



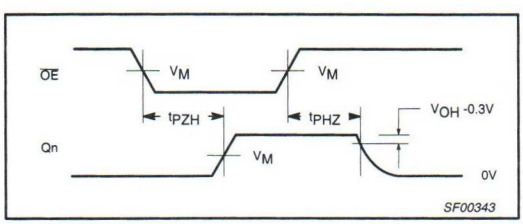
Waveform 2. Propagation Delay for Data to Outputs



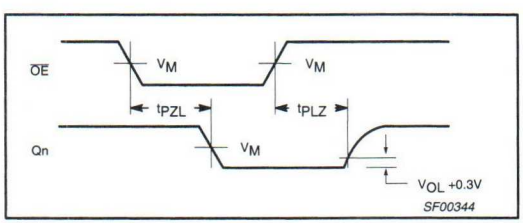
Waveform 3. Data Setup and Hold Times



Waveform 4. Data Setup and Hold Times

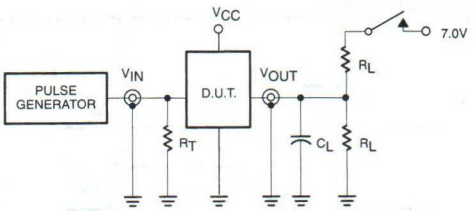


Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

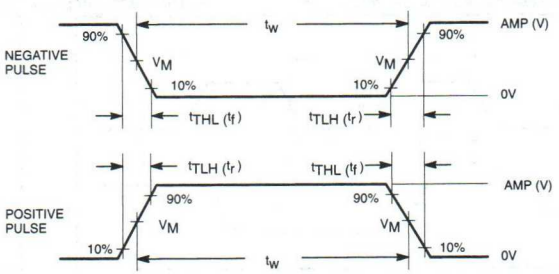


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

8-bit bidirectional binary counter (3-State) 74F579

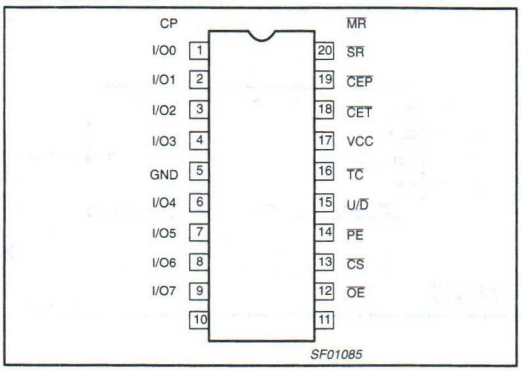
FEATURES

- Fully synchronous operation
- Multiplexed 3-State I/O ports for bus oriented applications
- Built in cascading carry capability
- U/$\overline{D}$ pin to control direction of counting
- Separate pins for Master reset and Synchronous operation
- Center power pins to reduce effects of package inductance
- Count frequency 115MHz Typ
- Supply current 100mA Typ
- See 74F269 for 24-pin separate I/O port version
- See 74F779 for 16-pin version

DESCRIPTION

The 74F579 is a fully synchronous 8-stage Up/Down Counter with multiplexed 3-State I/O ports for bus-oriented applications. It features a preset capability for programmable operation, carry look-ahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, except for the case of asynchronous reset, are initiated by the rising edge of the clock. $\overline{TC}$ output is not recommended for use as a clock or asynchronous reset due to the possibility of decoding spikes.

PIN CONFIGURATION



ORDERING INFORMATION

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F579	115MHz	100mA

ORDERING INFORMATION

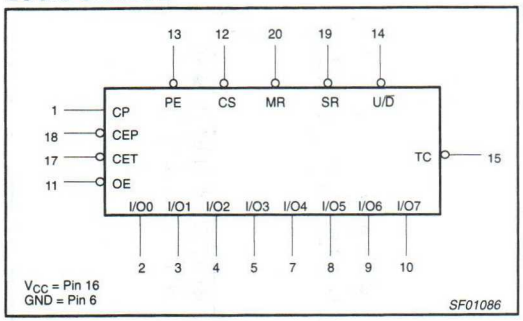
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
20-Pin Plastic DIP	N74F579N	SOT146-1
20-Pin Plastic SOL	N74F579D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

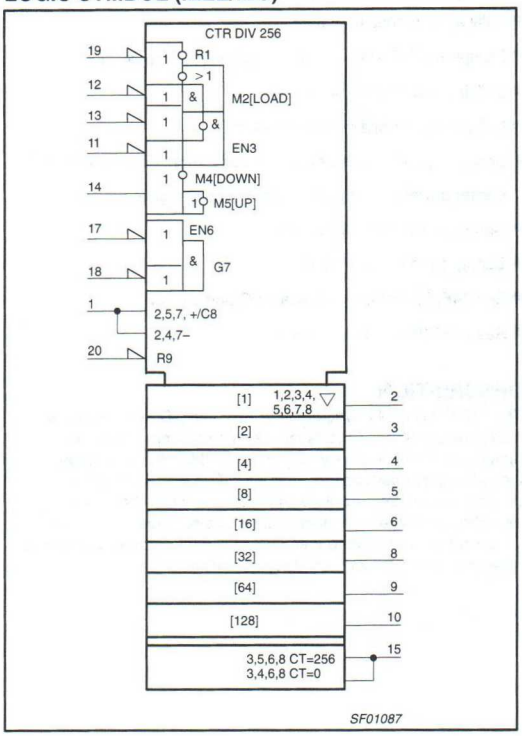
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I/O_n	Data Inputs	3.5/1.0	70µA/0.6mA
	Data Outputs	150/40	3.0mA/24mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/1.0	20µA/0.6mA
U/$\overline{D}$	Up/Down count control input	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{SR}$	Synchronous Reset input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CEP}$	Count Enable Parallel input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CS}$	Chip Select input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock input (active Rising Edge)	1.0/1.0	20µA/0.6mA
$\overline{TC}$	Terminal Count Output (active Low)	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

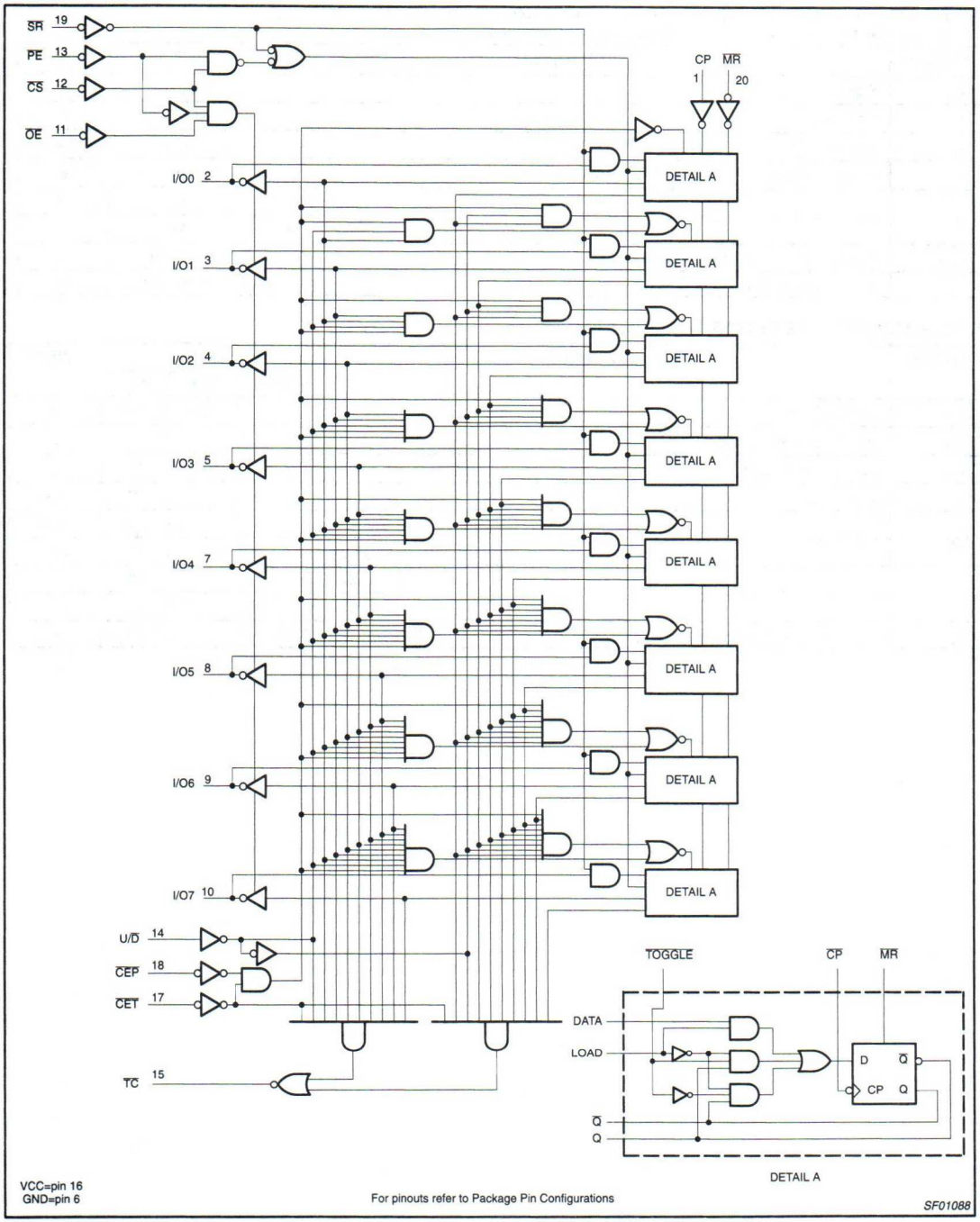


FUNCTION TABLE

INPUTS									OPERATING MODE
$\overline{MR}$	$\overline{SR}$	$\overline{CS}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	$\overline{OE}$	$\overline{CP}$	
X	X	H	X	X	X	X	X	X	I/O0 to I/O7 in high impedance ($\overline{PE}$ disabled)
X	X	L	H	X	X	X	H	X	I/O0 to I/O7 in high impedance
X	X	L	H	X	X	X	L	X	Flip-flop output appears on I/On lines
L	X	X	X	X	X	X	X	X	Asynchronous reset for all flip-flops
H	L	X	X	X	X	X	X	↑	Synchronous reset for all flip-flops
H	H	L	L	X	X	X	X	↑	Parallel load all flip-flops
H	H	(not LL)		H	X	X	X	↑	Hold
H	H	(not LL)		X	H	X	X	↑	Hold ($\overline{TC}$ held High)
H	H	(not LL)		L	L	H	X	↑	Count up
H	H	(not LL)		L	L	L	X	↑	Count down

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
(not LL) = $\overline{CS}$ and $\overline{PE}$ should never be Low voltage level at the same time.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_O	Voltage applied to output in High output state		–0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	$\overline{TC}$	40	mA
		I/O0	48	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	$\overline{TC}$			–1	mA
		I/O_n			–3	mA
I_{OL}	Low-level output current	$\overline{TC}$			20	mA
		I/O_n			24	mA
T_{amb}	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	$\overline{TC}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN (V_{IL} = 0.0V, V_{IH} = 4.5V for $\overline{MR}$, CP inputs)	I_{OH} = −1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/O_n		I_{OH} = −3mA	±10%V_{CC}	2.4	3.3		V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX,	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	I/O_n	V_{CC} = MAX, V_I = 5.5V					1	mA
		others	V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current	except I/O_n	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					−0.6	mA
I_{OZH}+ I_{IH}	Off-state output current High-level voltage applied	I/O_n	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{OZL}+ I_{IL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					−600	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				95	135	mA
		I_{CCL}					105	145	mA
		I_{CCZ}					105	150	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

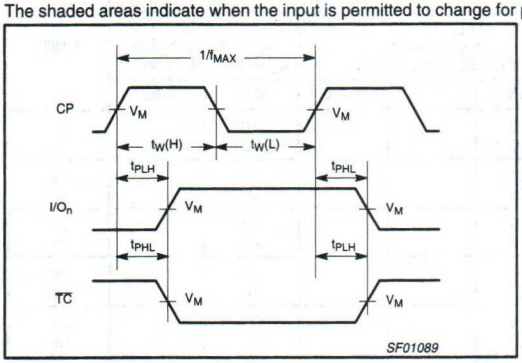
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 1	5.0 5.0	7.5 7.5	10.5 10.5	4.5 5.0	11.5 11.5	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	5.5 5.5	7.5 7.5	10.0 10.0	5.0 5.0	11.0 11.0	ns ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	Waveform 4	3.5 4.5	5.5 6.5	8.0 8.0	3.5 4.5	9.0 9.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 3	3.5 3.5	5.5 6.0	7.0 8.0	3.5 3.5	8.5 8.5	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to I/O_n	Waveform 2	5.0	7.0	9.0	5.0	10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to $\overline{TC}$	Waveform 4	4.0 6.0	6.5 8.0	9.0 10.5	4.0 6.0	10.5 12.5	ns ns
t_{PZH} t_{PZL}	Output Enable time $\overline{CS}$ to I/O_n	Waveform 6 Waveform 7	4.0 5.5	5.0 7.0	8.5 10.5	3.5 5.0	10.0 11.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{CS}$ to I/O_n	Waveform 6 Waveform 7	3.0 5.0	5.0 7.5	7.5 9.5	3.0 4.5	9.0 11.0	ns ns
t_{PZH} t_{PZL}	Output Enable time $\overline{PE}$ to I/O_n	Waveform 6 Waveform 7	3.0 5.0	4.5 6.5	8.0 10.0	3.0 4.5	9.0 11.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{PE}$ to I/O_n	Waveform 6 Waveform 7	3.0 2.5	4.0 4.0	7.5 7.5	3.0 2.0	9.0 8.5	ns ns
t_{PZH} t_{PZL}	Output Disable time $\overline{OE}$ to I/O_n	Waveform 6 Waveform 7	2.5 4.5	4.0 5.5	7.0 9.0	2.5 4.0	8.5 10.5	ns ns
t_{PHZ} t_{PLZ}	Output Enable time $\overline{OE}$ to I/O_n	Waveform 6 Waveform 7	1.0 2.0	2.5 4.0	4.0 7.0	1.0 2.0	5.5 8.0	ns ns

AC SETUP REQUIREMENTS

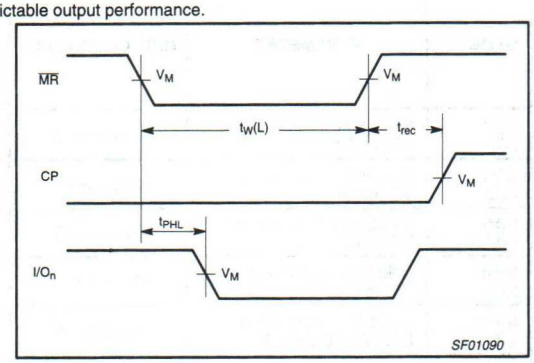
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_n to CP	Waveform 5	3.0 3.0			4.0 4.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n to CP	Waveform 5	0 0			0 0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $U/\overline{D}$ to CP	Waveform 5	8.0 8.0			9.0 9.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $U/\overline{D}$ to CP	Waveform 5	0 0			0 0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$, $\overline{SR}$ or $\overline{CS}$ to CP	Waveform 5	9.5 9.5			10.0 10.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$, $\overline{SR}$ or $\overline{CS}$ to CP	Waveform 5	0 0			0 0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	5.0 9.0			5.5 10.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	0 0			0 0		ns ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.5 4.5			4.5 4.5		ns ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 2	3.0			3.0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 2	4.0			4.5		ns

AC WAVEFORMS

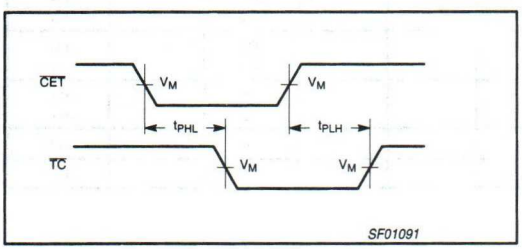
NOTE: For all waveforms V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



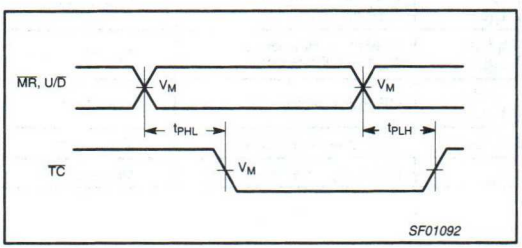
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width and Maximum Clock Frequency



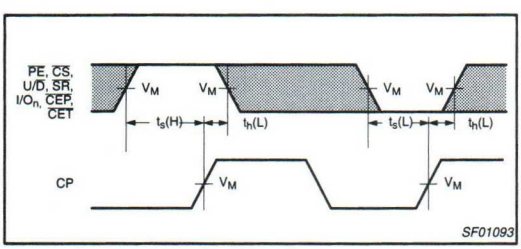
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



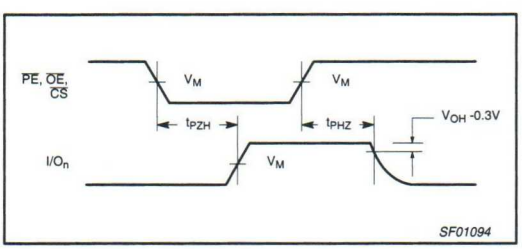
Waveform 3. Propagation Delay, $\overline{CET}$ Input to Terminal Count Output



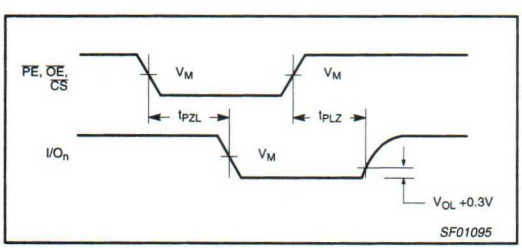
Waveform 4. Propagation Delay, U/$\overline{D}$ and $\overline{MR}$ Inputs to Terminal Count Output



Waveform 5. Setup and Hold Times

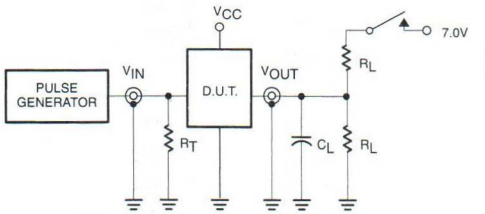


Waveform 6. 3-State Output Enable Time to High Level and Output Disable Time from High Level

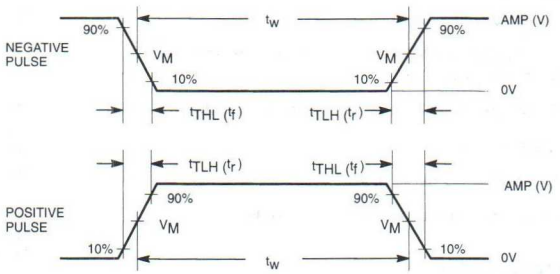


Waveform 7. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

8-bit shift register with output latches (3-State) 74F595

FEATURES

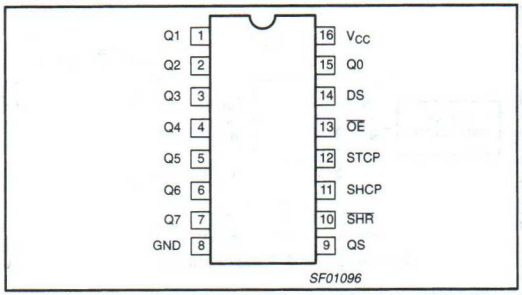
- Low noise, now switching feedthrough current
- Controlled output edge rates
- High impedance PNP base inputs for reduced loading (20μA in High and Low states)
- 8-bit serial-in, parallel-out shift register with storage
- 3-state outputs
- Shift register has direct clear
- Guaranteed shift frequency-DC to 100MHz

DESCRIPTION

The 74F595 contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-State outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct overriding clear, serial input and serial output pins for cascading. Both the shift register and storage register clocks are positive edge-triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

This device uses patented circuitry to control system noise and internal ground bounce. This is done by eliminating switching feedthrough current and controlling both Low-to-High and High-to-Low slew rates.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F595	130MHz	65mA

ORDERING INFORMATION

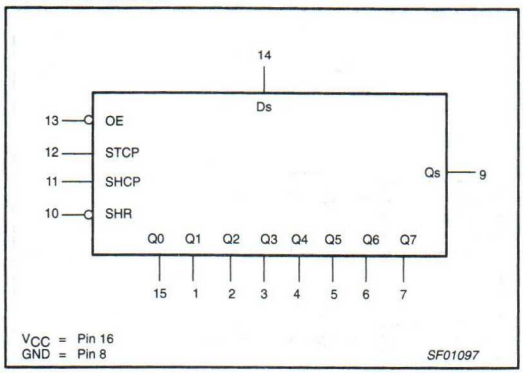
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
16-pin plastic DIP	N74F595N	SOT38-4
16-pin plastic SO	N74F595D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

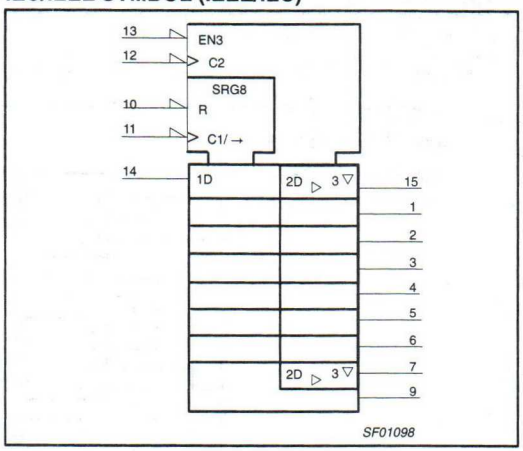
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ds	Serial data input	1.0/0.033	20μA/20μA
SHCP	Shift register clock pulse input (active rising edge)	1.0/0.033	20μA/20μA
STCP	Storage register clock pulse input (active rising edge)	1.0/0.033	20μA/20μA
$\overline{SHR}$	Shift register reset input (active Low)	1.0/0.033	20μA/20μA
$\overline{OE}$	Output Enable input (active Low)	1.0/0.033	20μA/20μA
Qs	Serial expansion output	50/33	1.0mA/20mA
Q0–Q7	Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

LOGIC SYMBOL



IEC/IEEE SYMBOL (IEEE/IEC)

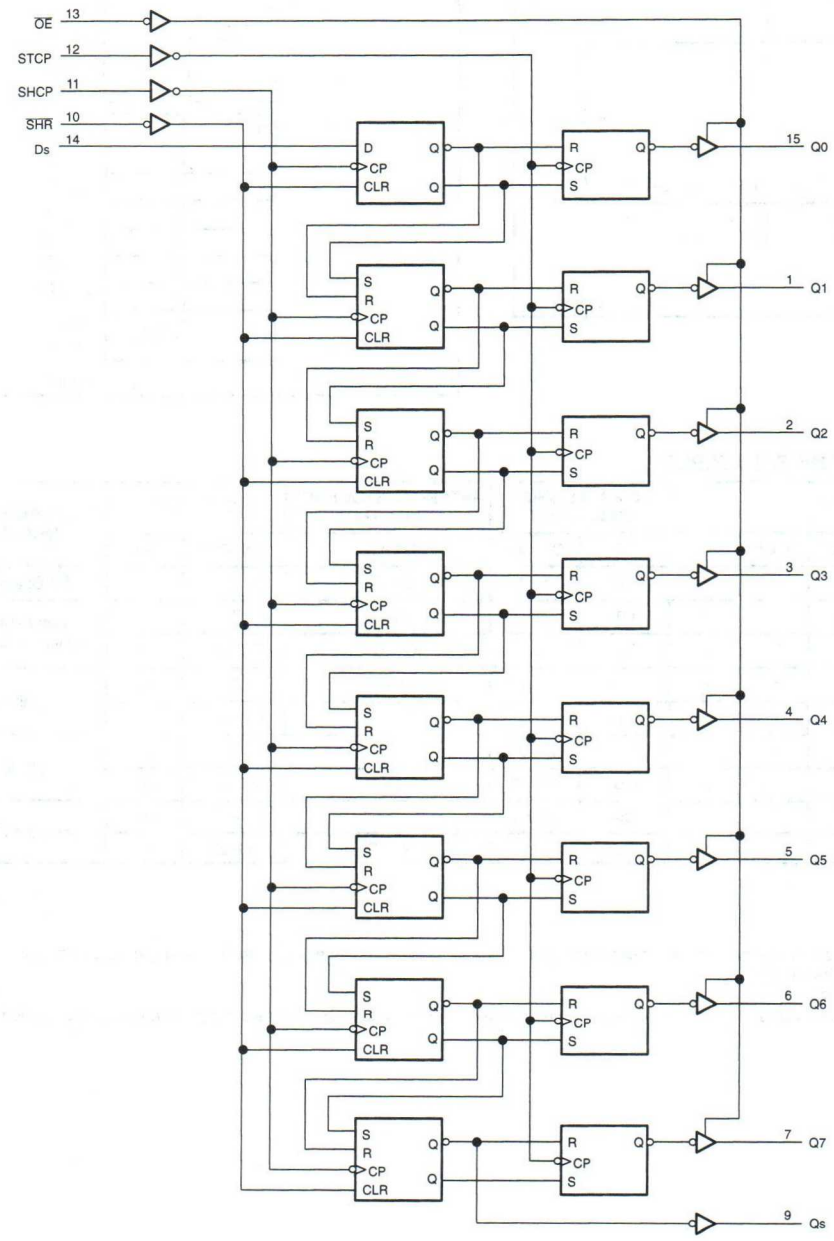


MODE SELECT – FUNCTION TABLE

INPUTS					INTERNAL SHIFT REGISTERS		INTERNAL STORAGE REGISTER	OUTPUTS		OPERATING MODES
$\overline{OE}$	$\overline{SHR}$	SHCP	STCP	Dn	O0	O1–O7	Q0–Q7	Q0–Q7	QS	
H	H	↡	↡	X	O0	O1–O7	Q0–Q7	Z	Q7	No Change
H	L	X	↡	X	L0	L	Q0–Q7	Z	L	Clear shift register, hold latch
L	L	X	↡	X	L0	L	Q0–Q7	Q0–Q7	L	
H	H	↑	↡	ds	Ds	o0–o6	Q0–Q7	Z	o6	Shift
L	H	↑	↡	ds	Ds	o0–o6	Q0–Q7	Q0–Q7	o6	
H	H	↡	↑	X	O0	O1–O7	o0–o7	Z	Q7	Store
L	H	↡	↑	X	O0	O1–O7	o0–o7	o0–o7	Q7	
H	H	↑	↑	ds	Ds	o0–o6	o0–o7*	Z	o6	Store, then Shift
L	H	↑	↑	ds	Ds	o0–o6	o0–o7*	o0–o*	o6	

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance
dn (on)=Lower case letters indicate the state of the referenced input (or output) one setup time prior to the Low-to-High clock transition
↑ = Low-to-High clock transition
↡ = Not a Low-to-High clock transition
* = When clocking both SHCP and STCP simultaneously the Shift Register state will always be one clock pulse ahead of the Storage Register

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

SF01099

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	Qs	40	mA
		Q0–Q7	48	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	Qs			−1	mA
		Q0–Q7			−3	mA
I_{OL}	Low-level output current	Qs			20	mA
		Q0–Q7			24	mA
T_{amb}	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	Qs	V_{CC} = MIN, V_{IL} = MAX, V_{IH}=MIN	I_{OH}=–1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		Q0–Q7		I_{OH} =–3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage	Qs	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL} = 20mA	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
		Q0–Q7		I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					–20	mA
I_{OZH}	Off-state output current, High level of voltage applied	Q0–Q7 only	V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low level of voltage applied	Q0–Q7 only	V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				55	80	mA
		I_{CCL}					70	100	mA
		I_{CCZ}					65	95	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency–SHCP to Qs	Waveform 1	115	135		90		MHz
t_{PLH} t_{PHL}	Propagation delay SHCP to Qs	Waveform 1	6.0 2.5	8.0 4.5	10.5 7.5	5.0 2.5	12.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay STCP to Q0–Q7	Waveform 1	5.5 3.0	8.0 5.0	10.0 8.0	4.5 3.0	13.0 8.5	ns
t_{PHL}	Propagation delay $\overline{SHR}$ to Qs	Waveform 2	3.5	5.5	8.0	3.0	8.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Q0–Q7	Waveform 5 Waveform 6	3.5 3.0	5.5 5.5	9.0 8.5	2.5 2.5	10.5 10.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Q0–Q7	Waveform 5 Waveform 6	2.0 4.0	4.0 6.0	7.0 9.0	1.5 3.0	8.5 10.5	ns

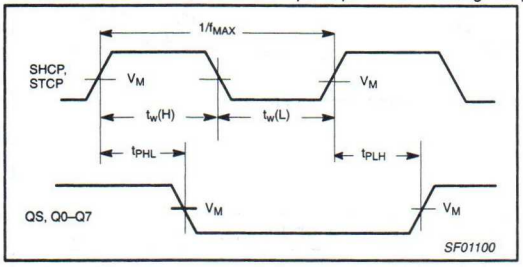
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Ds to SHCP	Waveform 3	2.0 2.0			2.5 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Ds to SHCP	Waveform 3	0 0			0 0		ns
$t_s(L)$	Setup time, Low $\overline{SHR}$ to STCP	Waveform 3	4.5			5.0		ns
$t_s(H)$	Setup time, High SHCP to STCP	Waveform 4	4.5			5.0		ns
$t_W(H)$ $t_W(L)$	SHCP Pulse width, High or Low	Waveform 1	3.5 4.0			4.0 4.0		ns
$t_W(H)$ $t_W(L)$	STCP Pulse width, High or Low	Waveform 1	4.0 3.0			4.0 3.5		ns
$t_W(L)$	$\overline{SHR}$ Pulse width, Low	Waveform 2	3.0			3.0		ns
t_{REC}	Recovery time, $\overline{SHR}$ to SHCP	Waveform 2	3.0			3.0		ns

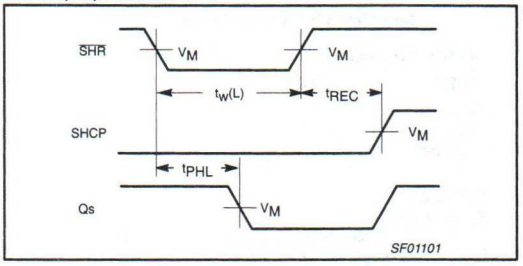
AC WAVEFORMS

For all waveforms, V_M = 1.5V.

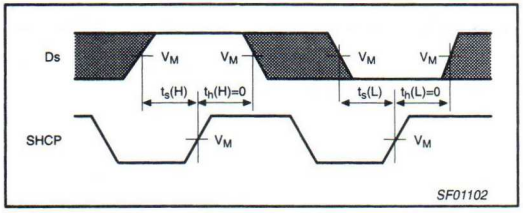
The shaded areas indicate when the input is permitted to change for predictable output performance.



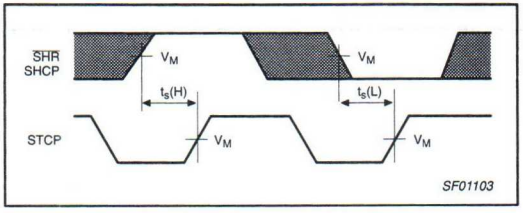
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Widths, and Maximum Clock Frequency



Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay, and Master Reset to Clock Recovery Time



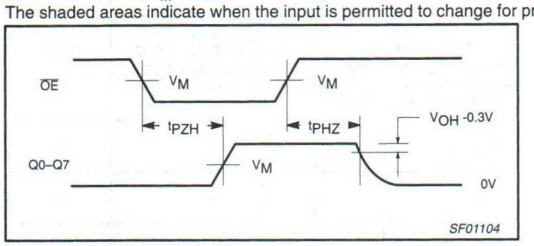
Waveform 3. Data Setup and Hold Times



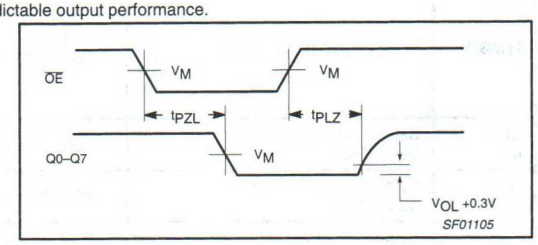
Waveform 4. Setup and Hold Times

AC WAVEFORMS (Continued)

For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

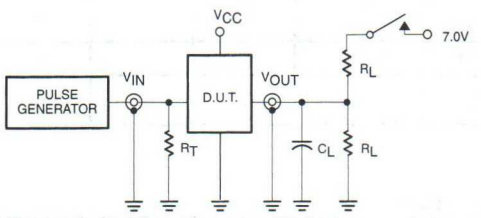


Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

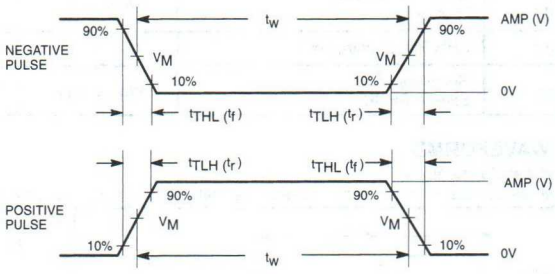


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

8-bit shift register with input storage registers | 74F597

FEATURES

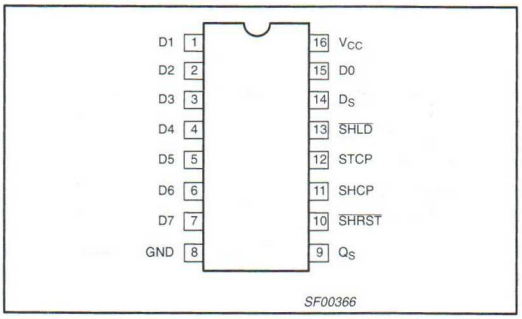
- High impedance PNP base inputs for reduced loading (20μA in High and Low states)
- 8-bit parallel storage register
- 3-State output buffers
- Shift register has asynchronous direct overriding reset
- Shift load $\overline{SHLD}$ is functional when SHCP is Low and locked out when SHCP is High
- Guaranteed shift frequency DC to 105MHz

DESCRIPTION

The 74F597 consists of an 8-bit storage register feeding a parallel-in/serial-in, serial-out 8-bit shift register. The storage register and shift register have separate positive edge triggered clocks. The shift register has asynchronous reset and when SHCP is Low, it has asynchronous load.

The shift register load function has been modified to load when both $\overline{SHLD}$ and SHCP are Low. When SHCP is High the shift register load operation is not performed. Data will be properly shifted on the rising edge of SHCP when $\overline{SHLD}$ is High.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F597	135MHz	42mA

ORDERING INFORMATION

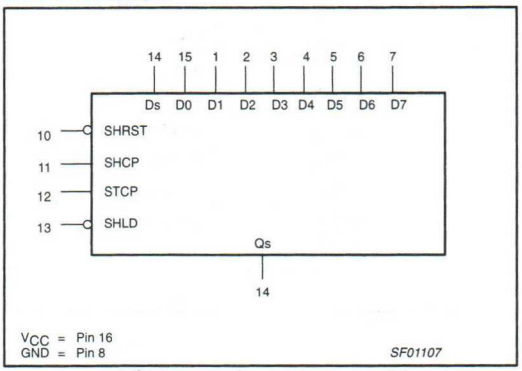
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
16-pin plastic DIP	N74F597N	SOT38-4
16-pin plastic SO	N74F597D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

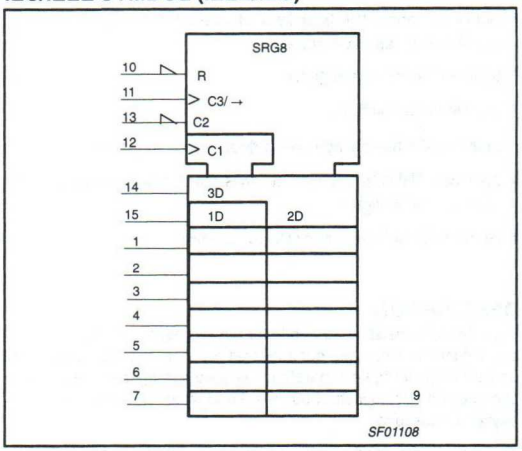
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ds	Serial data input	1.0/0.033	20μA/20μA
D0–D7	Parallel data inputs	1.0/0.033	20μA/20μA
SHCP	Shift register clock pulse input	1.0/0.033	20μA/20μA
STCP	Storage register clock pulse input	1.0/0.033	20μA/20μA
$\overline{SHLD}$	Shift register load input (active Low)	1.0/0.033	20μA/20μA
$\overline{SHRST}$	Shift register reset input (active Low)	1.0/0.033	20μA/20μA
Qs	Serial data output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

LOGIC SYMBOL



IEC/IEEE SYMBOL (IEEE/IEC)

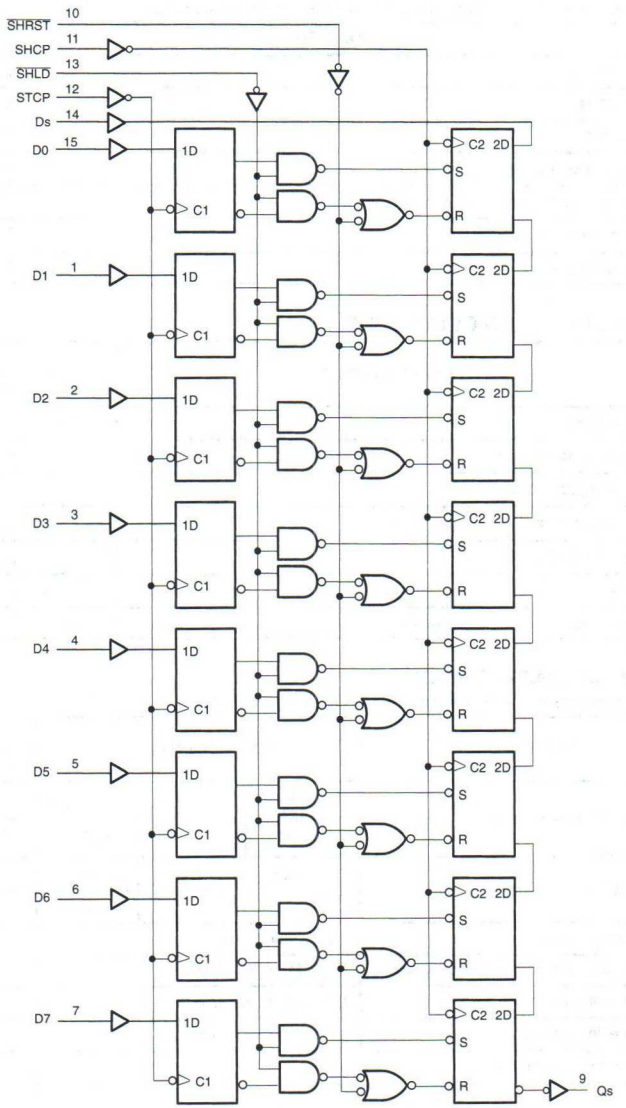


FUNCTION TABLE

INPUTS				OPERATING MODES
STCP	SHCP	$\overline{SHLD}$	$\overline{SHRST}$	
↑	X	X	X	Data loaded to storage registers
↑	L	L	H	Data loaded from inputs to shift register
↨	L	L	H	Data transferred from storage registers to shift registers
X	L	L	L	Invalid logic, state of shift register indeterminate when signals removed
X	X	H	L	Shift register cleared
X	↑	H	H	Shift register clocked, Qn=Qn–1, Q0=Ds
↨	H	X	H	Hold

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
↨ = Not a Low-to-High clock transition

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

SF01109

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX		±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					−20	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				43	65	mA
		I_{CCL}					41	60	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

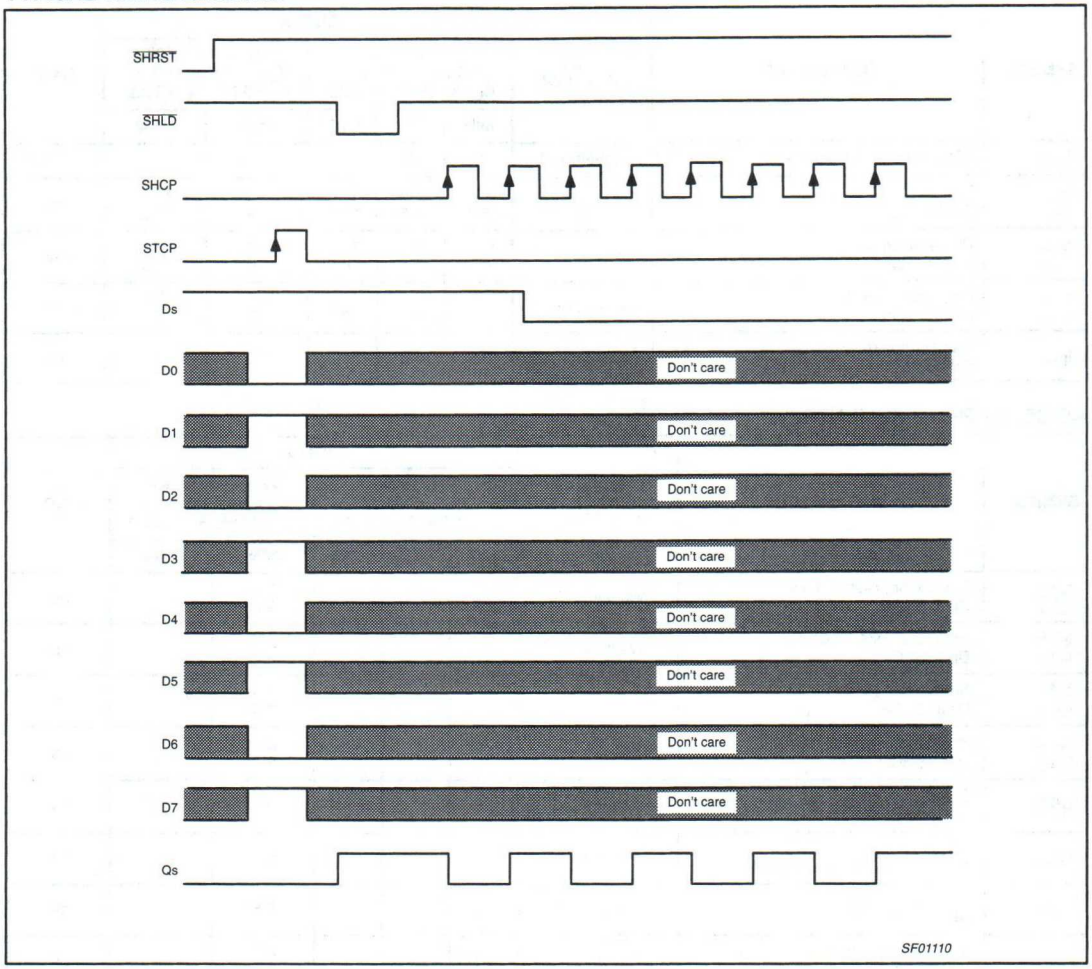
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	120	135		105		MHz
t_{PLH} t_{PHL}	Propagation delay SHCP to Qs	Waveform 1	7.0 6.0	8.5 7.5	11.0 10.0	6.0 5.5	12.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SHLD}$ to Qs	Waveform 1	8.0 6.0	9.5 7.5	12.0 10.0	7.0 5.5	13.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay STCP to Qs	Waveform 1	7.5 8.0	9.5 9.5	11.5 12.0	6.5 7.5	13.0 13.0	ns
t_{PHL}	Propagation delay $\overline{SHRST}$ to Qs	Waveform 2	2.5	5.5	9.0	2.5	9.5	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low Dn to STCP	Waveform 3	1.0 1.5			1.5 2.0		ns
t_h(H) t_h(L)	Hold time, High or Low Dn to STCP	Waveform 3	2.0 2.0			2.0 3.0		ns
t_s(H) t_s(L)	Setup time, High or Low Ds to SHCP	Waveform 3	1.0 1.5			1.0 2.0		ns
t_h(H) t_h(L)	Hold time, High or Low Ds to SHCP	Waveform 3	1.5 2.0			2.0 2.5		ns
t_s(H)	Setup time, High STCP to $\overline{SHLD}$↑	Waveform 4	8.5			9.0		ns
t_h(L)	Hold time, Low STCP to $\overline{SHLD}$↑ (hold mode)	Waveform 3	0.0			0.0		ns
t_s(H)	Setup time, High $\overline{SHLD}$ to SHCP↑	Waveform 3	6.0			6.5		ns
t_W(H) t_W(L)	SHCP Pulse width High or Low	Waveform 1	4.5 4.5			5.5 4.5		ns
t_W(H) t_W(L)	STCP Pulse width High or Low	Waveform 1	4.5 4.5			5.0 4.5		ns
t_W(L)	$\overline{SHRST}$ Pulse width, Low	Waveform 1	4.5			4.5		ns
t_W(L)	$\overline{SHLD}$ Pulse width, Low	Waveform 1	4.5			4.5		ns
t_{REC}	Recovery time, $\overline{SHRST}$ to SHCP	Waveform 2	2.0			2.5		ns

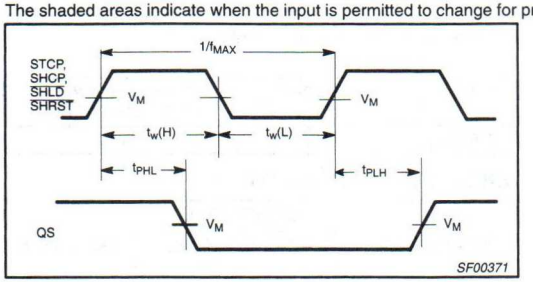
TYPICAL TIMING DIAGRAM



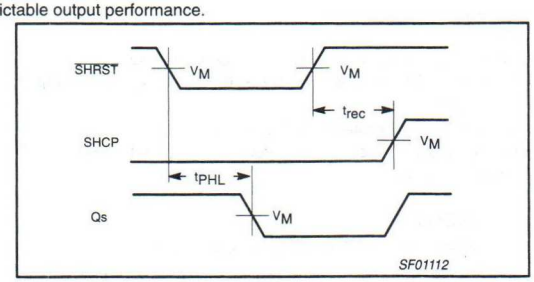
AC WAVEFORMS

For all waveforms, $V_M = 1.5V$.

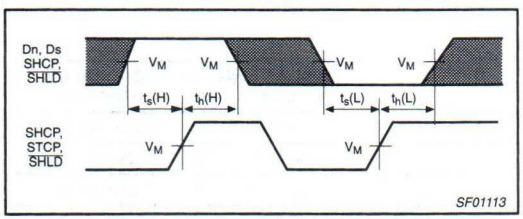
The shaded areas indicate when the input is permitted to change for predictable output performance.



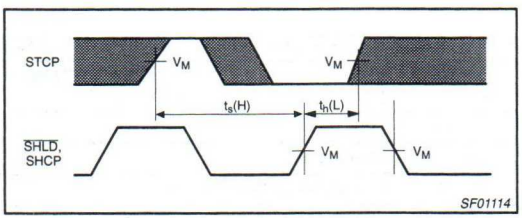
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Widths, and Maximum Clock Frequency, Shift Register Reset and Load Inputs to Serial Data Output



Waveform 2. Propagation Delay, Shift Register Reset and Load Inputs to Serial Data Output, Shift Register Reset and Load Inputs to Shift Register Clock Pulse Input Recovery Time

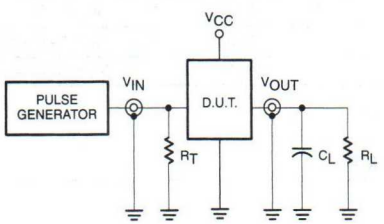


Waveform 3. Setup and Hold Times

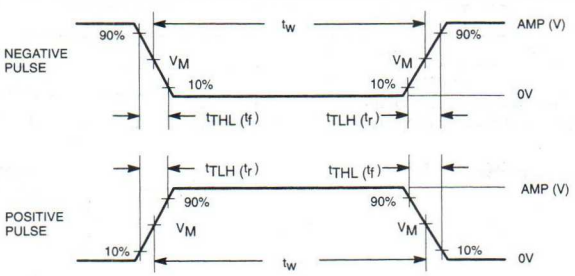


Waveform 4. Setup and Hold Time

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SF00006

8-bit shift register with input storage registers (3-State) 74F598

FEATURES

- High impedance PNP base input for reduced loading (20µA in High and Low states)
- 8–bit parallel storage register
- Shift register has asynchronous direct overriding reset
- Shift load $\overline{SHLD}$ is functional when SHCP is Low and locked out when SHCP is High.
- Guaranteed shift frequency DC to 105MHz
- Parallel 3–State I/O storage register inputs and shift register parallel outputs

DESCRIPTION

The 74F598 consists of an 8–bit storage register feeding a parallel–in/serial–in, parallel–out/serial–out 8–bit shift register. Both the storage register and shift register have positive edge–triggered clocks. The shift register has asynchronous reset and when SHCP is Low, it has asynchronous load.

The shift register load function has been modified to load when both $\overline{SHLD}$ and SHCP are Low. When SHCP is High the shift register load operation is not performed. Data will be properly shifted on the rising edge of SHCP when $\overline{SHLD}$ is High.

TYPE	TYPICAL SHCP f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F598	100MHz	75mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
20–pin plastic DIP	N74F598N	SOT146-1
20–pin plastic SOL	N74F598D	SOT163-1

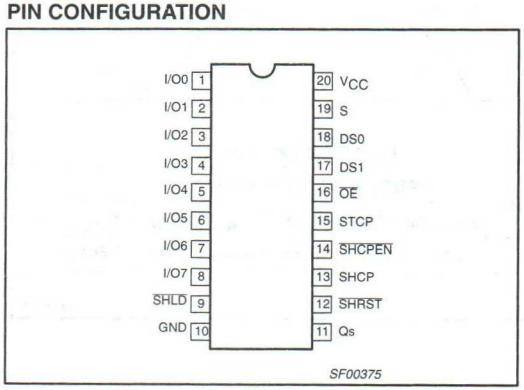
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) High/ Low	LOAD VALUE High/Low
I/On	Parallel data input	1.0/0.033	20µA/20µA
Ds0, Ds1	Serial data inputs	1.0/0.033	20µA/20µA
SHCP	Shift register clock pulse input	1.0/0.033	20µA/20µA
STCP	Storage register clock pulse input	1.0/0.033	20µA/20µA
$\overline{SHCPEN}$	Shift register clock pulse enable input	1.0/0.033	20µA/20µA
$\overline{SHLD}$	Shift register load input (active Low)	1.0/0.033	20µA/20µA
$\overline{SHRST}$	Shift register reset input (active Low)	1.0/0.033	20µA/20µA
S	Serial data select input	1.0/0.033	20µA/20µA
$\overline{OE}$	Output enable input	1.0/0.033	20µA/20µA
Qs	Serial data output	50/33	1.0mA/20mA
I/On	Parallel data outputs	150/40	3.0mA/24mA

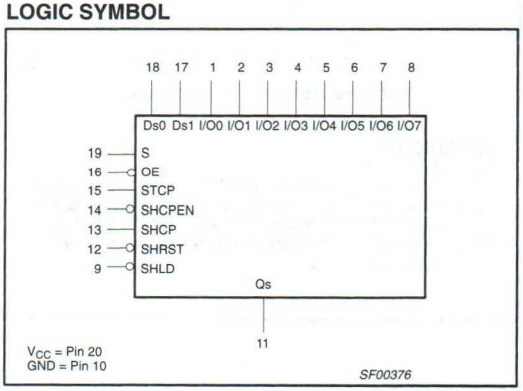
Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

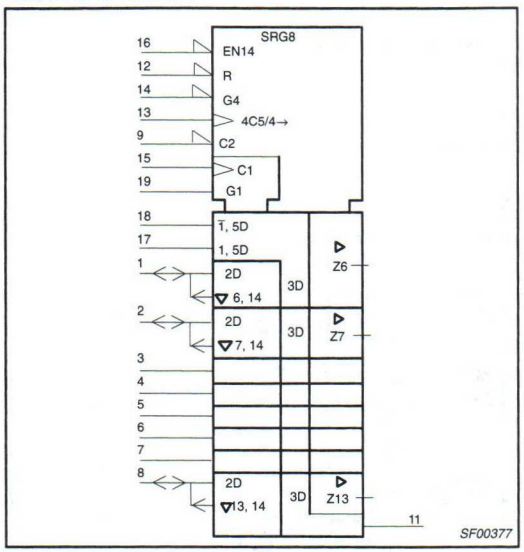
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL



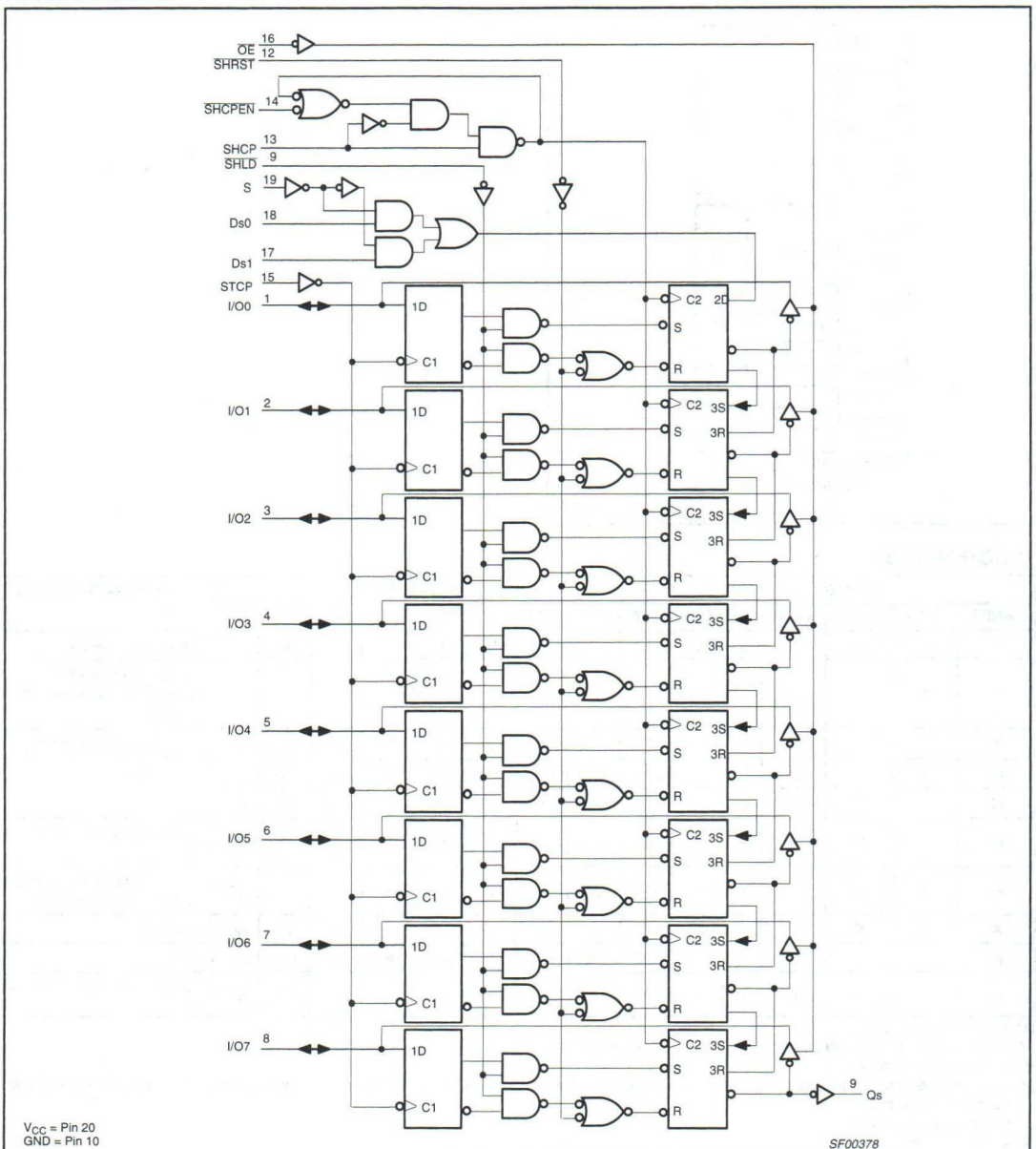
FUNCTION TABLE

INPUTS						INPUTS/OUTPUTS									OPERATING MODE
$\overline{SHRST}$	STCP	SHCP	$\overline{SHLD}$	S	$\overline{OE}$*	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7	Q7	
L	X	L	H	X	L	L	L	L	L	L	L	L	L	L	Clear shift register
L	X	L	L	X	L										Invalid, state of shift register indeterminate when signal is removed
X	↑	X	X	X	H	I0	I1	I2	I3	I4	I5	I6	I7	O7	Load data to storage register
H	X	↑	H	L	L	Ds0	O0	O1	O2	O3	O4	O5	O6	O6	Shift right
H	X	↑	H	H	L	Ds1	O0	O1	O2	O3	O4	O5	O6	O6	
H	↑	L	L	X	H	I0	I1	I2	I3	I4	I5	I6	I7	O7	Load data directly to shift register
H	↕	L	L	X	X	O0	O1	O2	O3	O4	O5	O6	O7	O7	Data transferred from storage register to shift register
X	X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z	NC	3–State
H	↕	X	H	X	X	NC	NC	NC	NC	NC	NC	NC	NC	NC	Hold
H	↕	H	X	X	X	NC	NC	NC	NC	NC	NC	NC	NC	NC	Hold (no storage or shift register load

Notes to function table

D0 – D7 = The level of the steady state inputs to the serial multiplexer.
H = High voltage level
I0 – I7 = The level of the steady state input at the respective I/O terminal is loaded into the flip–flop while the flip–flop outputs (except Q7) are isolated from the I/O terminal.
L = Low voltage level
NC= No change
O0 – O7 = The level of the respective Qn flip–flop prior to the last clock Low–to–High transition
X = Don't care
Z = High impedance "off" state
* = When the $\overline{OE}$ input is High, all I/O terminals are at the High impedance state, sequential operation or cleaning of the register is not affected.
↑ = Low–to–High clock transition
↕ = Not Low–to–High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	Qs	40	mA
		I/O0 – I/O7	48	mA
T_{amb}	Operating free air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current	Qs			–1	mA
		I/O0 – I/O7			–3	mA
I_{OL}	Low–level output current	Qs			20	mA
		I/O0 – I/O7			24	mA
T_{amb}	Operating free air temperature range		0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage	Qs	V_{CC} = MIN, V_{IL} = MAX, V_{IL} = MAX,	I_{OH} = –1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/On	V_{IH} = MIN, V_{IL} = MAX,	I_{OH} = –3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX,		±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX		±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = MAX, V_I = 7.0V					100	µA
		I/On	V_{CC} = MAX, V_I = 5.5V					1	mA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{OZH} + I_{IH}	Off–state output current, High–level voltage applied	I/On only	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{OZL} + I_{IL}	Off–state output current, Low–level voltage applied		V_{CC} = MAX, V_O = 0.5V					–70	µA
I_{OS}	Short–circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				68	100	mA
		I_{CCL}					80	110	mA
		I_{CCZ}					73	105	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

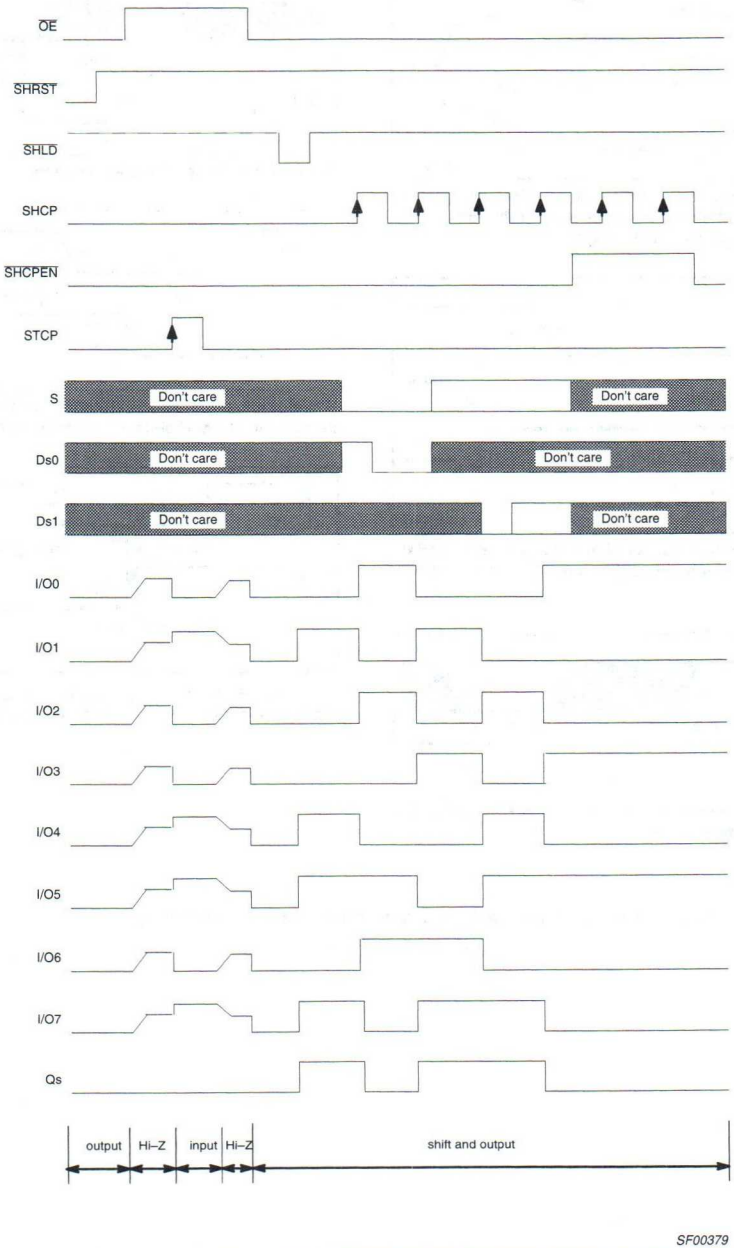
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	SHCP	Waveform 1	85	100		70		MHz
		STCP		140	160		130		
t_{PLH} t_{PHL}	Propagation delay SHCP to Qs		Waveform 1	9.5 6.5	11.5 8.5	14.0 11.5	8.5 6.0	16.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay STCP to Qs ($\overline{SHLD}$ = Low)		Waveform 1	10.0 7.0	11.5 8.5	14.5 11.5	9.0 6.5	16.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SHLD}$ to Qs		Waveform 1	9.0 6.0	11.0 8.0	13.5 10.5	8.0 5.5	15.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay SHCP to I/On		Waveform 1	8.5 5.0	10.5 7.0	13.5 9.5	7.0 4.5	15.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SHLD}$ to I/On		Waveform 1	7.5 6.0	9.5 8.0	12.5 11.0	6.5 6.0	14.5 11.5	ns
t_{PHL}	Propagation delay, $\overline{SHRST}$ to I/On		Waveform 2	6.5	9.0	12.0	6.0	12.5	ns
t_{PHL}	Propagation delay, $\overline{SHRST}$ to Qs		Waveform 2	6.0	7.5	10.5	5.0	11.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low		Waveform 5 Waveform 6	3.5 3.0	5.5 5.0	8.5 7.5	3.0 2.5	9.5 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time to High or Low		Waveform 5 Waveform 6	1.5 4.0	3.5 6.0	6.5 9.0	1.5 4.0	7.5 9.5	ns

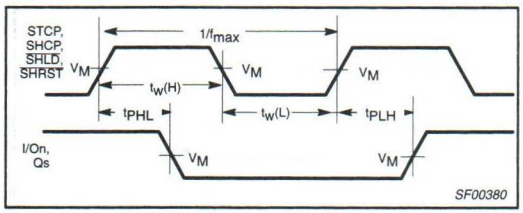
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s (H) t_s (L)	Setup time, High or Low Dsn to SHCP	Waveform 3	0.0 3.5			1.5 4.5		ns
t_h (H) t_h (L)	Hold time, High or Low DSn to SHCP	Waveform 3	0.0 2.5			0.0 3.0		ns
t_s (H) t_s (L)	Setup time, High or Low I/On to STCP	Waveform 3	2.5 2.5			2.5 3.0		ns
t_h (H) t_h (L)	Hold time, High or Low I/On to STCP	Waveform 3	0.0 0.0			1.5 2.0		ns
t_s (H) t_s (L)	Setup time, High or Low S to SHCP	Waveform 3	3.5 3.0			4.0 3.5		ns
t_h (H) t_h (L)	Hold time, High or Low S to SHCP	Waveform 3	2.5 3.0			3.0 3.0		ns
t_s (H)	Setup time, High, STCP to $\overline{SHLD}$	Waveform 4	7.0			8.0		ns
t_h (L)	Hold time, Low, STCP to $\overline{SHLD}$ (hold mode)	Waveform 4	0.0			0.0		ns
t_s (H) t_s (L)	Setup time, High or Low, $\overline{SHCPEN}$ to SHCP	Waveform 3	0.0 2.0			0.0 2.0		ns
t_h (H) t_h (L)	Hold time, High or Low, $\overline{SHCPEN}$ to SHCP	Waveform 3	0.0 4.5			0.0 5.5		ns
t_s (H)	Setup time, High, $\overline{SHLD}$ to SHCP↑	Waveform 3	7.5			8.5		ns
t_w (H) t_w (L)	SHCP Pulse width, High or Low	Waveform 1	5.5 4.0			6.5 4.0		ns
t_w (H) t_w (L)	STCP Pulse width, High or Low	Waveform 1	4.5 4.0			5.5 4.0		ns
t_w (L)	$\overline{SHRST}$ Pulse width, Low	Waveform 1	4.0			4.0		ns
t_w (L)	$\overline{SHLD}$ Pulse width, Low	Waveform 1	4.0			5.0		ns
t_{rec}	Recovery time, $\overline{SHRST}$ to SHCP	Waveform 2	0.0			0.0		ns

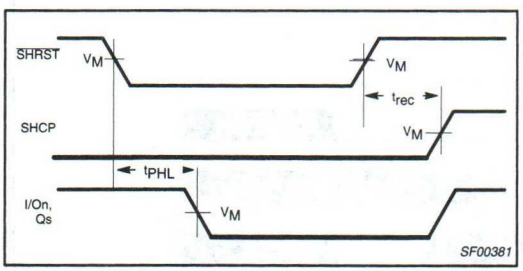
TYPICAL TIMING DIAGRAM



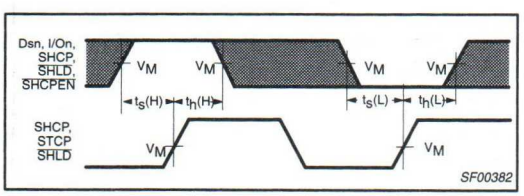
AC WAVEFORMS



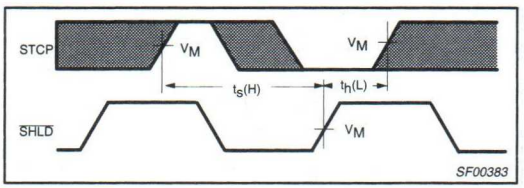
Waveform 1. Propagation delay for clock input to output, clock pulse widths, and maximum clock frequency, shift register reset and load inputs to serial data output



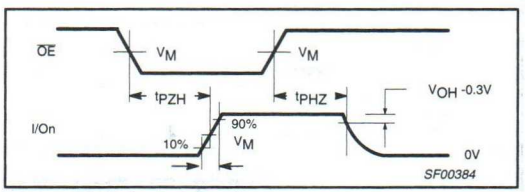
Waveform 2. Propagation delay for shift register reset to serial data output, shift register reset to shift register, shift register input recovery time



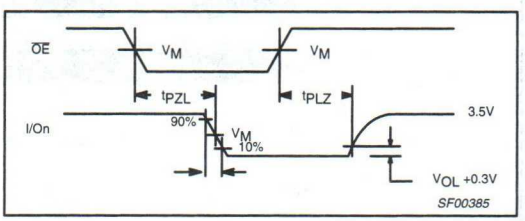
Waveform 3. Setup time and hold times



Waveform 4. Setup time and hold time



Waveform 5. 3-State output enable time to High level, output disable time from High level and transition time to High level

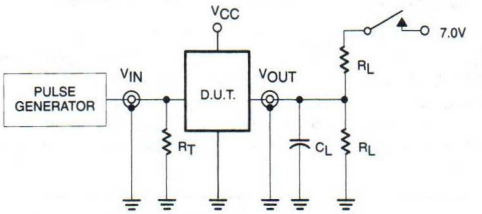


Waveform 6. 3-State output enable time to Low level, output disable time from Low level and transition time to Low level

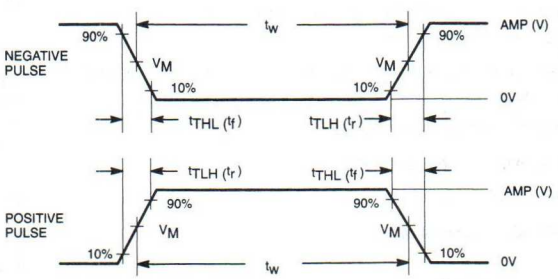
Notes to AC waveforms

1. For all waveforms, $V_M = 1.5V$.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

74F620 Octal Bus Transceiver, Inverting (3-State)
74F623 Octal Bus Transceiver, Non-Inverting (3-State)

FEATURES

- High-impedance NPN base inputs for reduced loading (70μA in High and Low states)
- Ideal for applications which require high output drive and minimal bus loading
- Octal bidirectional bus interface
- 3-State buffer outputs sink 64mA and source 15mA
- 74F620, inverting
- 74F623, non-inverting

DESCRIPTION

The 74F620 is an octal transceiver featuring inverting 3-State bus-compatible outputs in both send and receive directions. The outputs are capable of sinking 64mA and sourcing up to 15mA, providing very good capacitive drive characteristics. The 74F623 is a non-inverting version of the 74F620.

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the Enable inputs ($\overline{OEBA}$ and OEAB). The Enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 74F620 and 74F623 the capability to store data by the simultaneous enabling of $\overline{OEBA}$ and OEAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of bus lines (16 in all) will remain in their last states.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F620	3.5ns	80mA
74F623	4.5ns	105mA

ORDERING INFORMATION

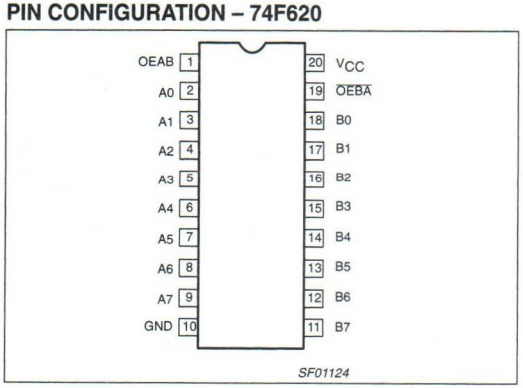
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
20-pin plastic DIP	N74F620N, N74623N	SOT146-1
20-pin plastic SOL	N74F620D, N74623D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

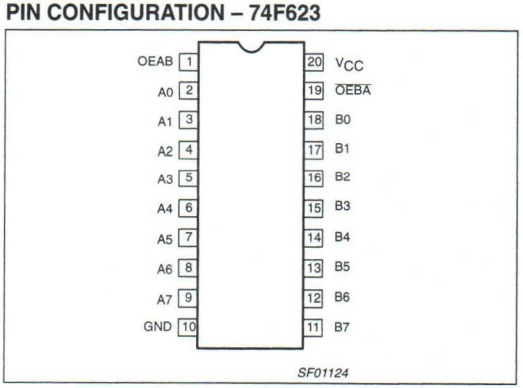
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 - A7, B0 - B7	Data inputs	3.5/1.16	70μA/70μA
$\overline{OEBA}$, OEAB	Output Enable inputs	1.0/0.033	20μA/20μA
A0 - A7	Data outputs	150/40	3mA/24mA
B0 - B7	Data outputs	750/106.7	15mA/64mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

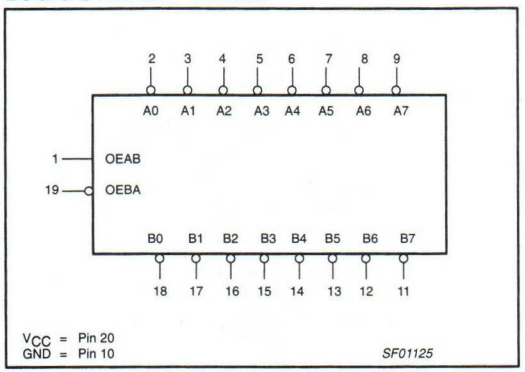
PIN CONFIGURATION – 74F620



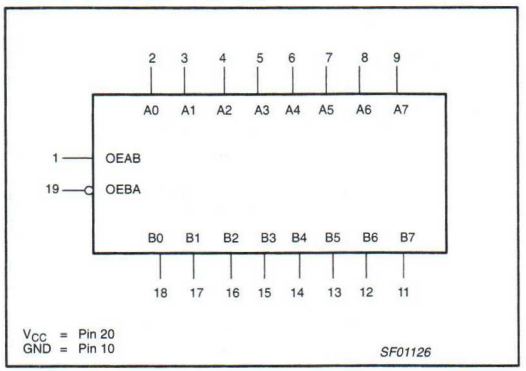
PIN CONFIGURATION – 74F623



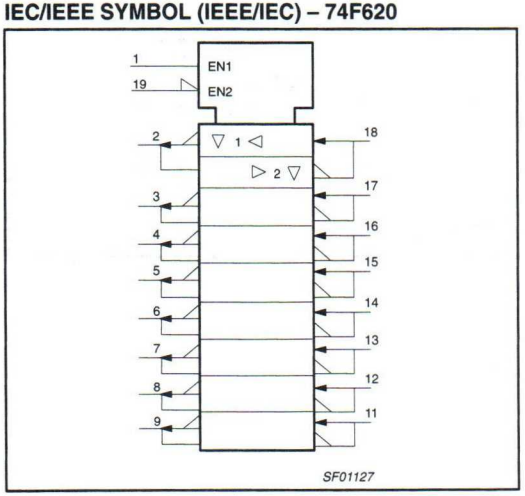
LOGIC SYMBOL – 74F620



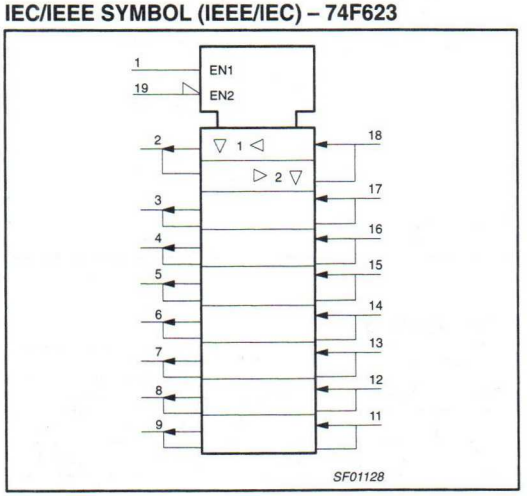
LOGIC SYMBOL – 74F623



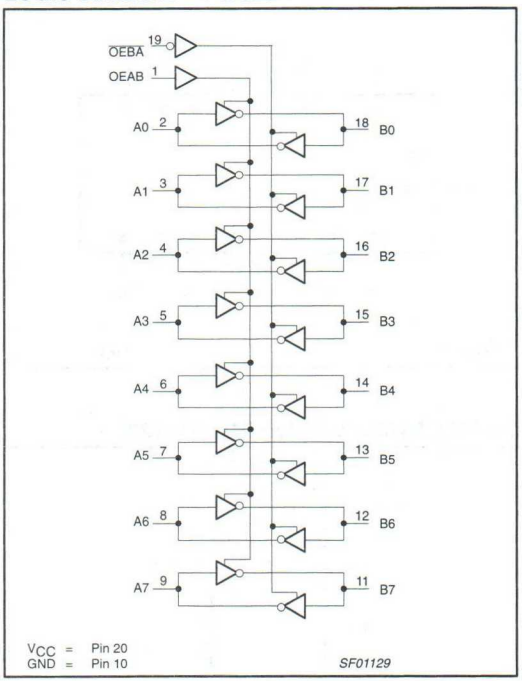
IEC/IEEE SYMBOL (IEEE/IEC) – 74F620



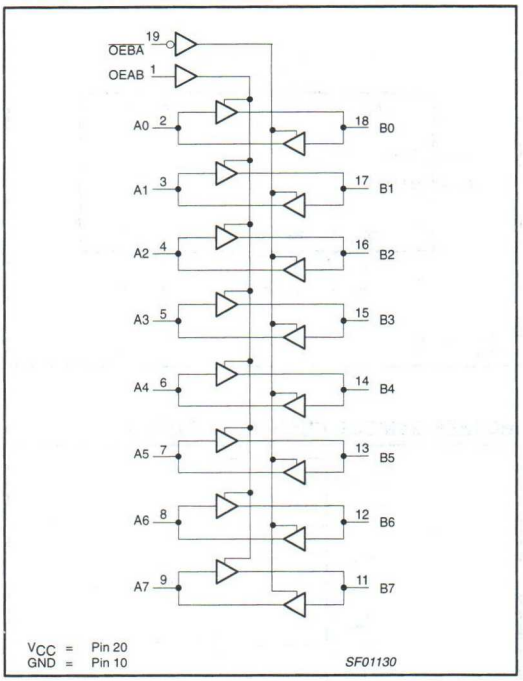
IEC/IEEE SYMBOL (IEEE/IEC) – 74F623



LOGIC DIAGRAM – 74F620



LOGIC DIAGRAM – 74F623



FUNCTION TABLE

INPUTS		OPERATING MODES	
$\overline{OEBA}$	OEAB	74F620	74F623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Z	Z
L	H	$\overline{B}$ data to A bus	B data to A bus
		$\overline{A}$ data to B bus	A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	A0–A7	48	mA
		B0–B7	128	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A0–A7			–3	mA
		B0–B7			–15	mA
I_{OL}	Low-level output current	A0–A7			24	mA
		B0–B7			64	mA
T_{amb}	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	A0–A7 B0–B7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
		B0–B7		I_{OH} = –15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A0–A7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B0–B7		I_{OL} = 48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL} = 64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	$\overline{OEBA}$, OEAB	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		others	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	$\overline{OEBA}$, OEAB only	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{OZH}+I_{IH}	Off-state output current, High-level of voltage applied	A0–A7 B0–B7	V_{CC} = MAX, V_I = 2.7V					70	µA
I_{OZL}+I_{IL}	Off-state output current, Low-level of voltage applied		V_{CC} = MAX, V_I = 0.5V					–70	µA
I_{OS}	Short-circuit output current[3]	A0–A7	V_{CC} = MAX			–60		–150	mA
		B0–B7				–100		–225	mA
I_{CC}	Supply current (total)	74F620 I_{CCH}	V_{CC} = MAX	$\overline{OEBA}$=OEAB=4.5V; A0–A7=GND			70	92	mA
		74F620 I_{CCL}		$\overline{OEBA}$=OEAB=4.5V; A0–A7=4.5V			84	110	mA
		74F620 I_{CCZ}		OEAB=GND; $\overline{OEBA}$=A0–A7=4.5V			84	110	mA
		74F623 I_{CCH}	V_{CC} = MAX	$\overline{OEBA}$=OEAB=4.5V; A0–A7=4.5V			110	140	mA
		74F623 I_{CCL}		$\overline{OEBA}$=OEAB=4.5V; A0–A7=GND			110	140	mA
		74F623 I_{CCZ}		OEAB=GND; $\overline{OEBA}$=A0–A7=4.5V			99	130	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS – 74F620

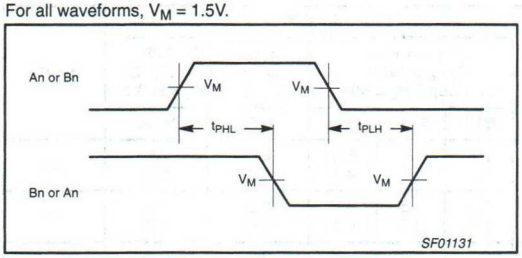
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn	Waveform 2	2.5 1.0	4.5 2.5	6.5 4.5	2.0 1.0	7.5 5.0	ns
t_{PLH} t_{PHL}	Propagation delay Bn to An	Waveform 2	2.5 1.0	4.5 2.5	6.5 4.5	2.0 1.0	7.5 5.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level, $\overline{OEBA}$ to An	Waveform 3 Waveform 4	3.0 4.0	7.5 7.5	10.5 10.5	2.5 3.5	11.5 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level, $\overline{OEBA}$ to An	Waveform 3 Waveform 4	2.5 2.0	4.5 4.5	7.5 7.0	2.0 1.5	8.0 7.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level, OEAB to Bn	Waveform 3 Waveform 4	4.5 4.5	7.5 7.5	10.5 10.0	4.0 4.0	11.5 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level, OEAB to Bn	Waveform 3 Waveform 4	3.0 4.0	6.5 6.5	9.5 9.5	2.5 3.5	10.5 10.5	ns

AC ELECTRICAL CHARACTERISTICS – 74F623

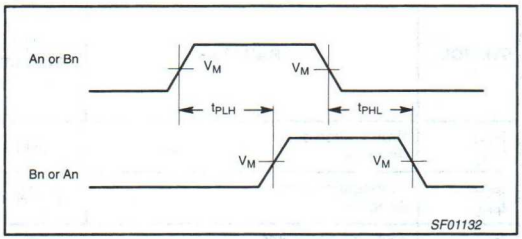
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn	Waveform 1	2.0 3.0	4.0 5.0	5.5 7.0	2.0 2.5	6.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay Bn to An	Waveform 1	2.0 2.5	4.0 4.5	5.5 6.5	2.0 2.5	6.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level, $\overline{OEBA}$ to An	Waveform 3 Waveform 4	5.0 5.0	8.5 7.5	10.5 9.5	5.0 5.0	12.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level, $\overline{OEBA}$ to An	Waveform 3 Waveform 4	2.5 2.5	4.5 4.5	6.5 6.5	2.5 2.5	7.5 7.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level, OEAB to Bn	Waveform 3 Waveform 4	5.0 4.5	8.0 7.0	10.0 9.0	5.0 4.5	11.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level, OEAB to Bn	Waveform 3 Waveform 4	3.0 4.0	6.0 7.0	8.5 9.0	3.0 4.0	10.0 10.0	ns

AC WAVEFORMS

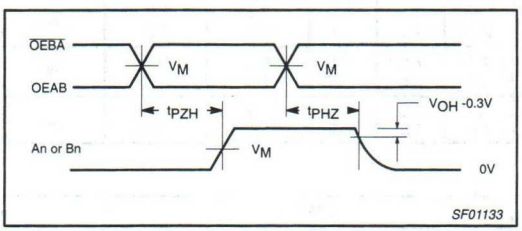
For all waveforms, V_M = 1.5V.



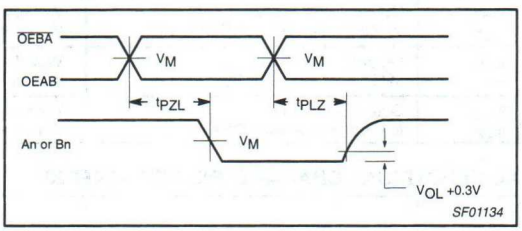
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs

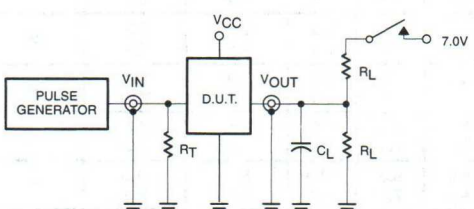


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

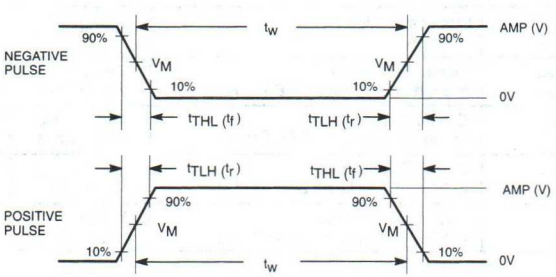


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

Octal bus transceiver, non-inverting (open collector) 74F621

FEATURES

- High-impedance NPN base inputs for reduced loading (20μA in High and Low states)
- Octal bidirectional bus interface
- Open collector outputs sink 64mA
- Non-inverting

DESCRIPTION

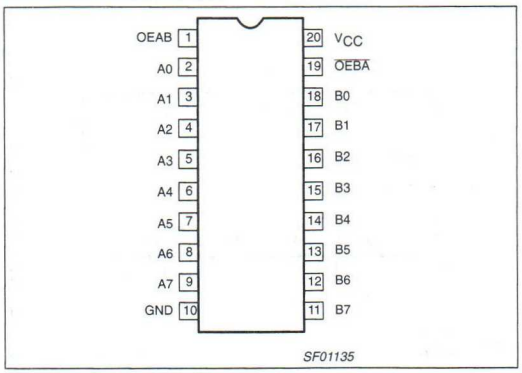
The 74F621 is an octal transceiver featuring non-inverting open collector bus-compatible outputs in both send and receive directions. The outputs are capable of sinking 64mA, providing very good capacitive drive characteristics.

This octal bus transceiver is designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the Enable inputs ($\overline{OEBA}$ and OEAB). The Enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 74F621 the capability to store data by the simultaneous enabling of $\overline{OEBA}$ and OEAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of bus lines (16 in all) will remain in their last states.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F621	8.0ns	105mA

ORDERING INFORMATION

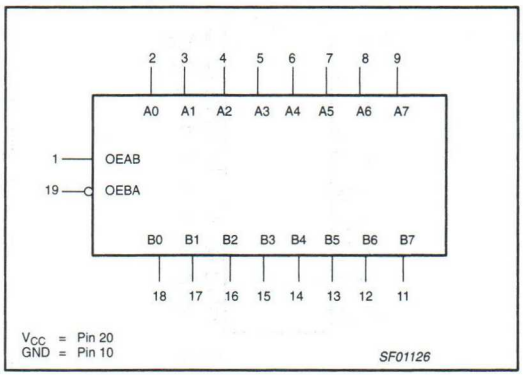
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
20-pin plastic DIP	N74F621N	SOT146-1
20-pin plastic SOL	N74F621D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

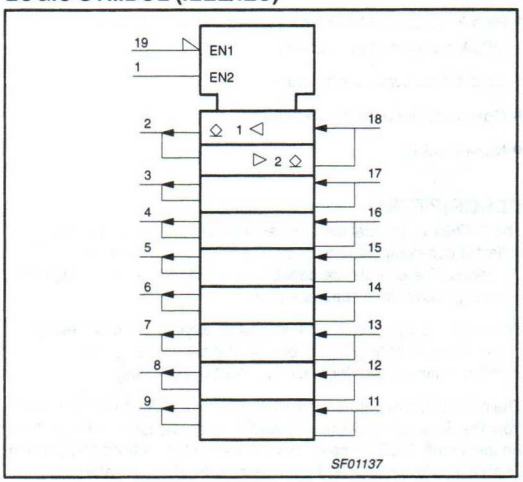
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 - A7, B0 - B7	Data inputs	1.0/0.033	20μA/20μA
$\overline{OEBA}$, OEAB	Output Enable inputs	1.0/0.033	20μA/20μA
A0 - A7	Data outputs	OC/40	OC/24mA
B0 - B7	Data outputs	OC/106.7	OC/64mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state. OC = Open Collector.

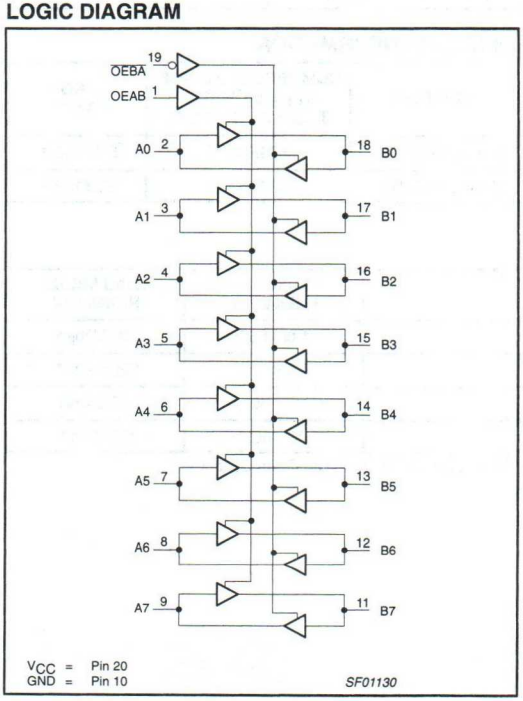
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OPERATING MODES
$\overline{OEBA}$	OEAB	
L	L	B data to A bus
H	H	A data to B bus
H	L	OFF
L	H	B data to A bus
		A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
OFF= High if pull-up resistor is connected to open collector output

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A0–A7	48	mA
		B0–B7	128	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	High-level output current				4.5	V
I_{OL}	Low-level output current	A0–A7			24	mA
		B0–B7			64	mA
T_{amb}	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH}=MIN, V_{OH} = MAX					250	µA
V_{OL}	Low-level output voltage	A0–A7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B0–B7		I_{OL} = 48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL} = 64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	$\overline{OEBA}$, OEAB	V_{CC} = MAX, V_I = 7.0V					100	µA
		others	V_{CC} = 0.0V, V_I = 5.5V					1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					−20	µA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	$\overline{OEBA}$ = OEAB = A0–A7 = 4.5V			105	140	mA
		I_{CCL}		$\overline{OEBA}$ = OEAB = 4.5V, A0–A7 = GND			105	140	mA

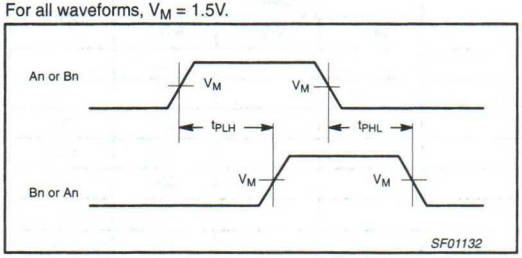
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.

AC ELECTRICAL CHARACTERISTICS

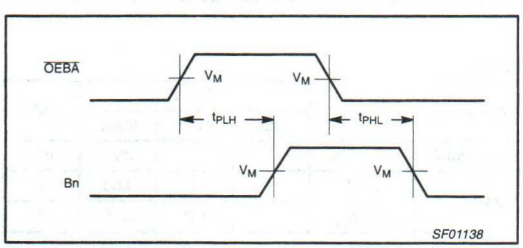
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn	Waveform 1	6.0 4.0	9.5 6.0	12.0 8.0	5.5 3.5	13.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay Bn to An	Waveform 1	6.0 3.5	9.0 5.5	12.0 7.5	5.5 3.0	12.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OEBA}$ to An	Waveform 2	6.0 3.5	10.0 6.5	13.5 10.5	5.5 3.0	14.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay OEAB to Bn	Waveform 3	7.0 3.5	12.0 6.5	15.0 9.5	6.0 3.0	17.0 10.0	ns

AC WAVEFORMS

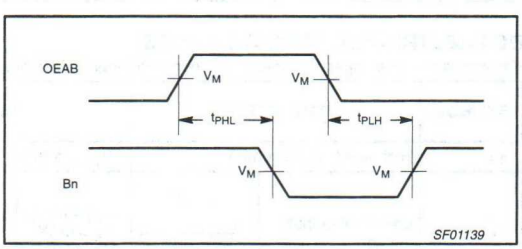
For all waveforms, V_M = 1.5V.



Waveform 1. For Non-Inverting Outputs

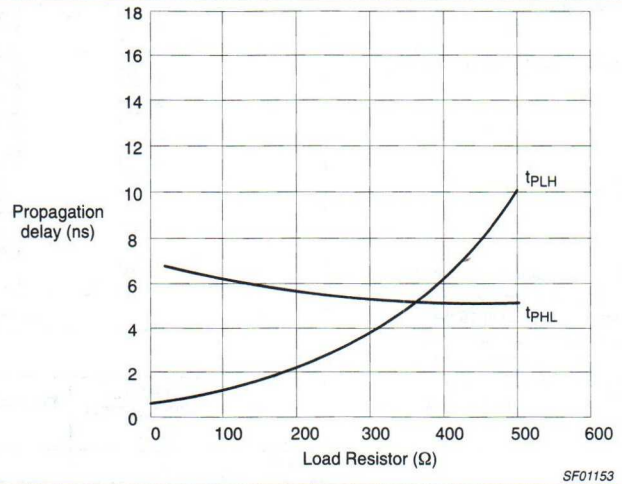


Waveform 2. Propagation Delay, $\overline{OEBA}$ to An



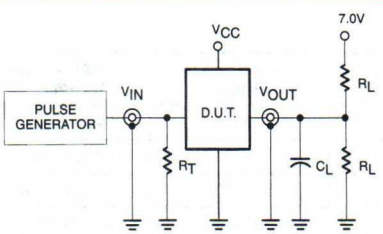
Waveform 3. Propagation Delay, OEAB to Bn

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS

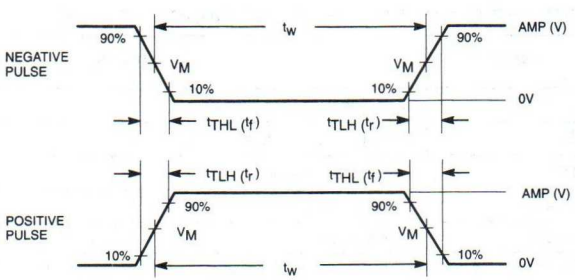


NOTE:
When using open-collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only slight increase in the t_{PHL}. However, if the pull-up resistor is changed, the user must take certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers do not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs



Input Pulse Definition

DEFINITIONS:
R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00027

Octal bus transceiver, inverting (3-State) 74F640

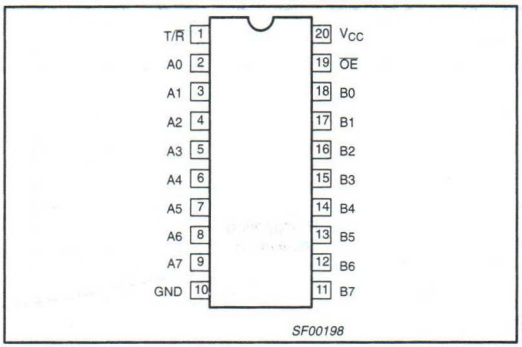
FEATURES

- High-impedance NPN base inputs for reduced loading (70μA in High and Low states)
- Ideal for applications which require high-output drive and minimal bus loading
- Inverting version of 74F245
- Octal bidirectional bus interface
- 3-State outputs sink 64mA and source 15mA

DESCRIPTION

The 74F640 is an octal transceiver featuring inverting 3-State bus compatible outputs in both transmit and receive directions. The B port outputs are capable of sinking 64mA and sourcing 15mA, providing very good capacitive drive characteristics. The device features an Output Enable ($\overline{OE}$) input for easy cascading and Transmit/Receiver (T/$\overline{R}$) input for direction control. The 3-State outputs, B0–B7, have been designed to prevent output bus loading if the power is removed from the device.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F640	3.5ns	78mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
20-pin plastic DIP	N74F640N	SOT146-1
20-pin plastic SOL	N74F640D	SOT163-1

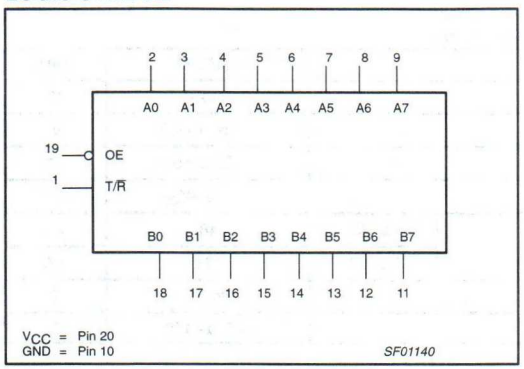
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 - A7, B0 - B7	Data inputs	3.5/0.115	70μA/70μA
$\overline{OE}$	Output Enable input (active Low)	2.0/0.067	40μA/40μA
T/$\overline{R}$	Transmit/Receive input	2.0/0.067	40μA/40μA
A0 - A7	A port outputs	150/40	3.0mA/24mA
B0 - B7	B port outputs	750/106.7	15mA/64mA

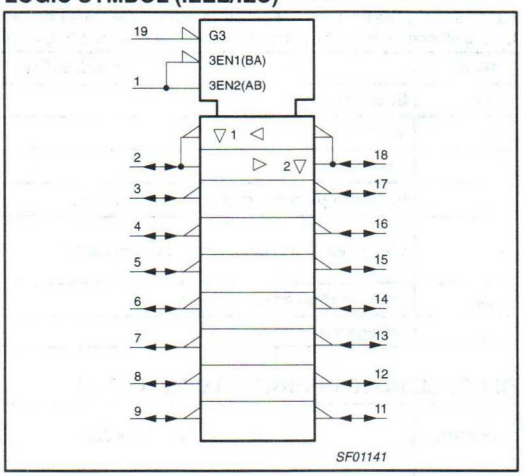
NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

Octal bus transceiver, inverting (3-State) 74F640

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

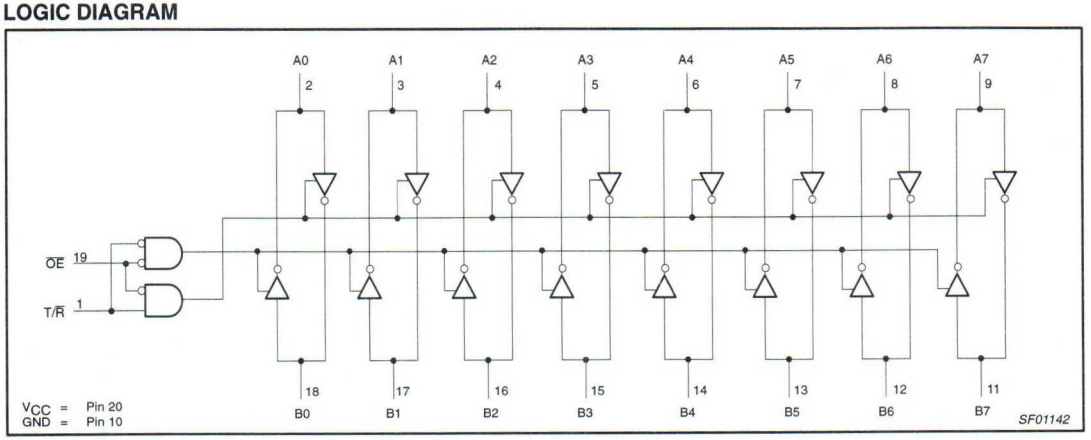


FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B data to Bus $\overline{A}$
L	H	Bus A data to Bus $\overline{B}$
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	A0–A7	48	mA
		B0–B7	128	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	A0–A7			−3	mA
		B0–B7			−15	mA
I_{OL}	Low-level output current	A0–A7			24	mA
		B0–B7			64	mA
T_{amb}	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	A0–A7, B0–B7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
		B0–B7		I_{OH} = –15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A0–A7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B0–B7		I_{OL} = MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	$\overline{OE}$, T/$\overline{R}$	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A0–A7, B0–B7	V_{CC} = 5.5V, V_I = 5.5V					1.0	mA
I_{IH}	High-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 2.7V					40	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					–40	µA
I_{OZH}+I_{IH}	Off-state output current, High level of voltage applied		V_{CC} = MAX, V_I = 2.7V					70	µA
I_{OZL}+I_{IL}	Off-state output current, Low level of voltage applied		V_{CC} = MAX, V_I = 0.5V					–70	µA
I_{OS}	Short-circuit output current[3]	A0–A7	V_{CC} = MAX			–60		–150	mA
		B0–B7				–100		–225	µA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	T/$\overline{R}$ = An = 4.5V, $\overline{OE}$ = GND			66	85	mA
		I_{CCL}		T/$\overline{R}$ = Bn = $\overline{OE}$ = GND			91	120	mA
		I_{CCZ}		T/$\overline{R}$ = Bn = GND, $\overline{OE}$ = 4.5V			78	102	mA

NOTES:

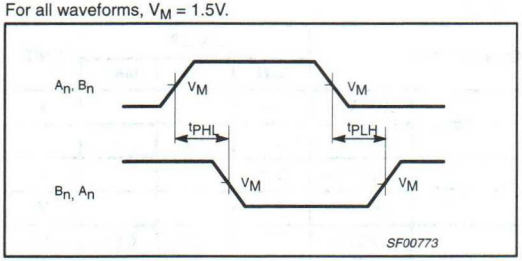
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

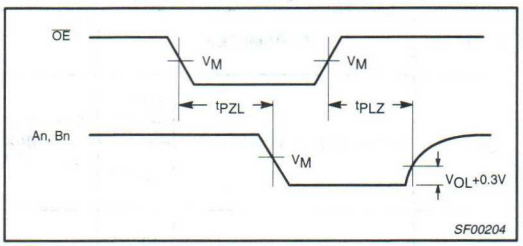
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5V, T_{amb} = +25°C, C_L = 50pF, R_L = 500Ω			V_{CC} = +5V ± 10%, T_{amb} = 0°C to +70°C, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn, Bn to An	Waveform 1	2.0 1.0	4.5 2.5	7.0 5.0	2.0 1.0	8.0 5.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 3 Waveform 2	5.5 5.5	6.5 7.0	10.5 10.5	5.0 5.0	12.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 3 Waveform 2	2.0 2.0	3.5 4.5	6.5 7.0	1.5 2.0	8.0 7.5	ns

AC WAVEFORMS

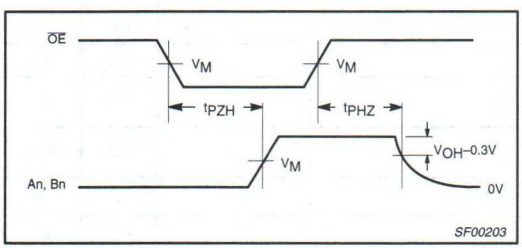
For all waveforms, V_M = 1.5V.



Waveform 1. Propagation Delay for Inverting Outputs

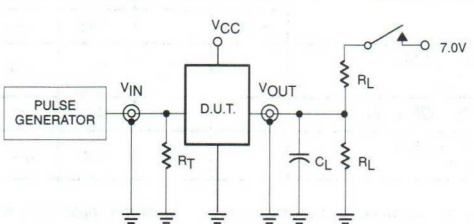


Waveform 2. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

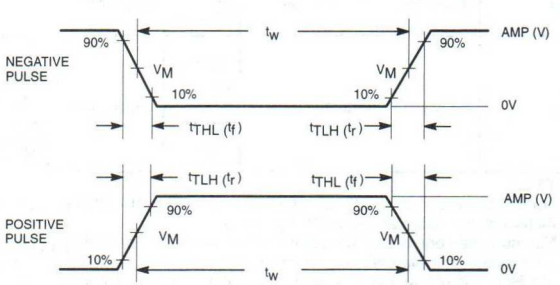


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

Transceivers

74F641/~~74F642~~*

74F641 Octal Bus Transceiver with Common Output Enable, Non-Inverting (Open Collector)
74F642 Octal Bus Transceiver with Common Output Enable, Inverting (Open Collector)

FEATURES

- High-impedance NPN base inputs for reduced loading (20µA in High and Low states)
- Octal bidirectional bus interface
- Common Output Enable for both Transmit and Receive modes
- Open collector outputs sink 64mA
- —74F641, non-inverting
  —74F642, inverting

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
20-pin plastic DIP	N74F641N	SOT146-1
20-pin plastic SOL	N74F641D	SOT163-1

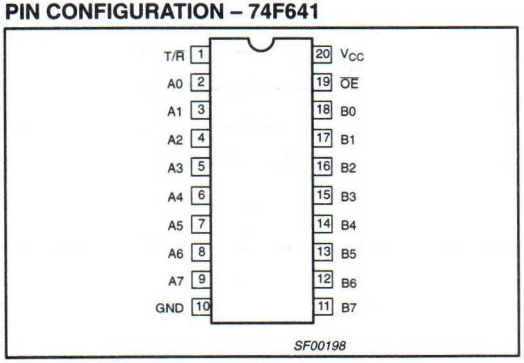
TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F641	8.0ns	69mA
74F642	8.5ns	52mA

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

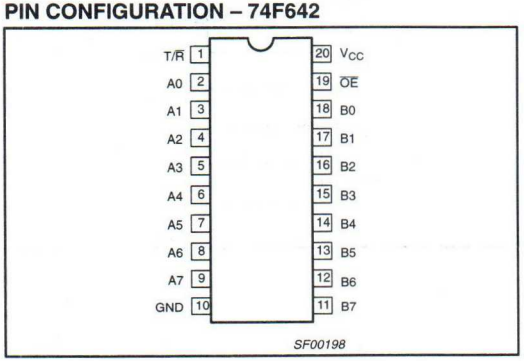
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 - A7, B0 - B7	Data inputs	1.0/0.033	20µA/20µA
T/$\overline{R}$	Transmit/Receive input	2.0/0.067	40µA/40µA
$\overline{OE}$	Output Enable inputs	2.0/0.067	40µA/40µA
A0 - A7	Data outputs	OC/40	OC/24mA
B0 - B7	Data outputs	OC/106.7	OC/64mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state. OC = Open Collector.

PIN CONFIGURATION – 74F641

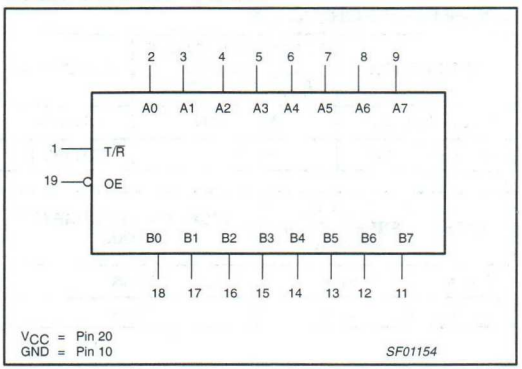


PIN CONFIGURATION – 74F642

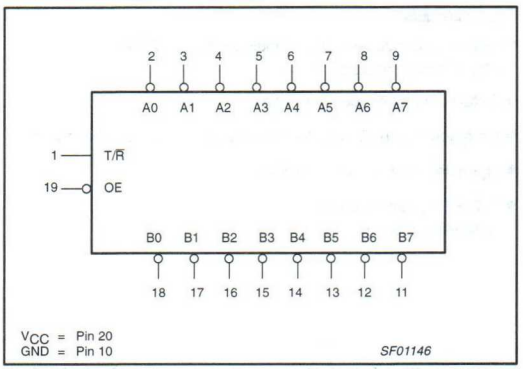


* *Discontinued part. Please see the Discontinued Products List.*

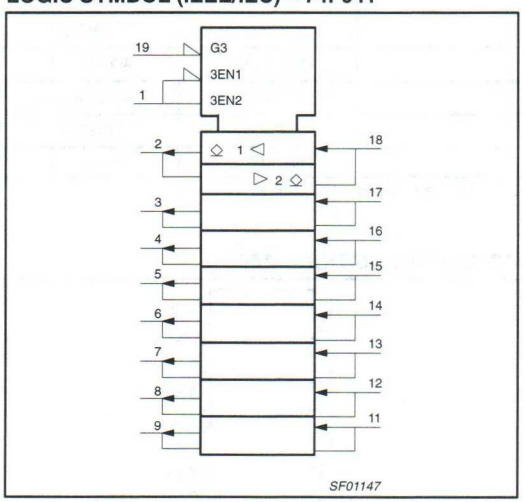
LOGIC SYMBOL – 74F641



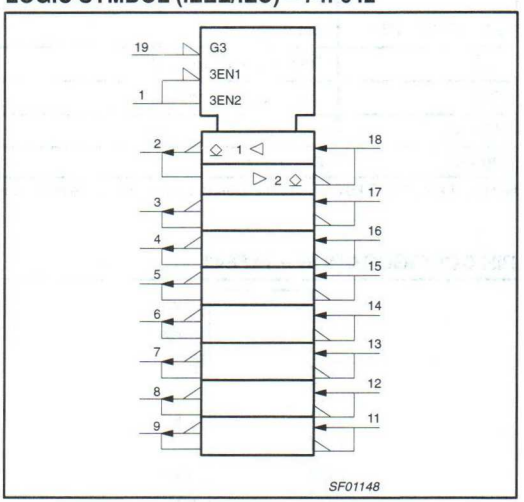
LOGIC SYMBOL – 74F642



LOGIC SYMBOL (IEEE/IEC) – 74F641

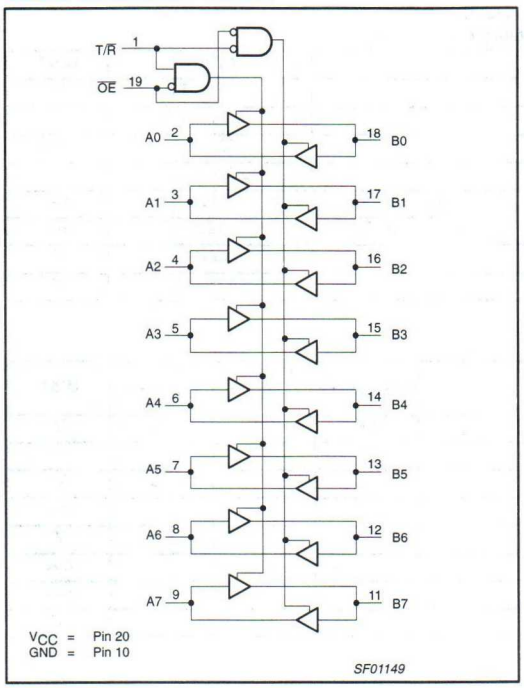


LOGIC SYMBOL (IEEE/IEC) – 74F642

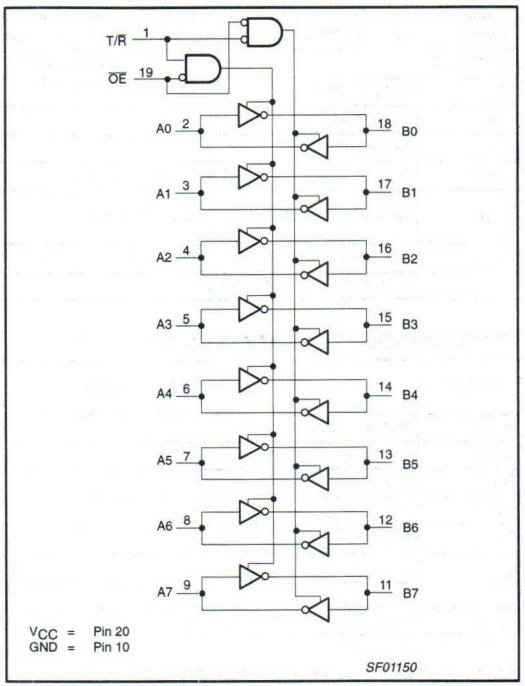


* *Discontinued part. Please see the Discontinued Products List.*

LOGIC DIAGRAM – 74F641



LOGIC DIAGRAM – 74F642



FUNCTION TABLE – 74F641

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	T/$\overline{R}$	An	Bn
L	L	A=B	INPUTS
H	H	INPUTS	B=A
H	X	OFF	OFF

H = High voltage level
L = Low voltage level
X = Don't care
OFF= High if pull-up resistor is connected to open collector output

FUNCTION TABLE – 74F642

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	T/$\overline{R}$	An	Bn
L	L	A=$\overline{B}$	INPUTS
H	H	INPUTS	B=$\overline{A}$
H	X	OFF	OFF

H = High voltage level
L = Low voltage level
X = Don't care
OFF= High if pull-up resistor is connected to open collector output

* *Discontinued part. Please see the Discontinued Products List.*

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	A0–A7	48	mA
		B0–B7	128	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current				4.5	V
I_{OL}	Low-level output current	A0–A7			24	mA
		B0–B7			64	mA
T_{amb}	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX					250	µA
V_{OL}	Low-level output voltage	A0–A7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B0–B7		I_{OL} = 48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL} = 64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	$\overline{T/R}$, $\overline{OE}$	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		An, Bn	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	$\overline{T/R}$, $\overline{OE}$	V_{CC} = MAX, V_I = 2.7V					40	µA
		An, Bn						20	µA
I_{IL}	Low-level input current	$\overline{T/R}$, $\overline{OE}$	V_{CC} = MAX, V_I = 0.5V					−40	µA
		An, Bn						−20	µA
I_{CC}	Supply current (total)	74F641 I_{CCH}	V_{CC} = MAX	An=T/R=4.5, $\overline{OE}$=GND			60	90	mA
		74F641 I_{CCL}		T/R=4.5V, An=$\overline{OE}$=GND			78	120	mA
		74F642 I_{CCH}		An=T/R=$\overline{OE}$=4.5V			37	55	mA
		74F642 I_{CCL}		An=T/R=4.5V, $\overline{OE}$=GND			67	98	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.

** Discontinued part. Please see the Discontinued Products List.*

AC ELECTRICAL CHARACTERISTICS – 74F641

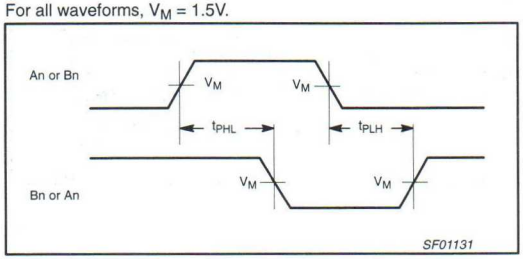
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn	Waveform 2	6.5 4.0	8.5 6.0	11.5 9.5	6.5 4.0	12.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay Bn to An	Waveform 2	6.0 3.5	8.0 5.5	11.5 7.5	6.0 3.5	12.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to An	Waveform 4	7.0 5.0	10.5 7.0	12.5 9.0	7.0 5.0	13.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to Bn	Waveform 4	8.0 3.5	9.0 7.5	12.5 9.5	8.0 5.5	13.5 10.5	ns

AC ELECTRICAL CHARACTERISTICS – 74F642

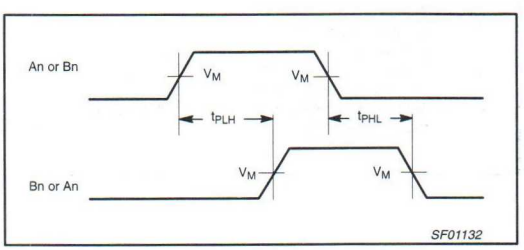
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn	Waveform 1	8.0 2.0	9.0 4.5	12.5 6.5	8.0 2.0	13.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay Bn to An	Waveform 1	7.5 1.5	8.0 4.0	12.0 6.0	7.5 1.5	12.5 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to An	Waveform 3	7.5 6.0	9.0 8.0	12.0 10.5	7.5 6.0	12.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to Bn	Waveform 3	8.0 6.0	9.0 7.0	12.5 10.5	8.0 6.0	13.0 11.0	ns

AC WAVEFORMS

For all waveforms, V_M = 1.5V.



Waveform 1. Propagation Delay for An to Bn or Bn to An (74F642)

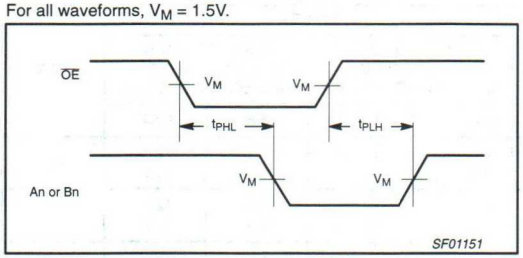


Waveform 2. Propagation Delay for An to Bn or Bn to An (74F641)

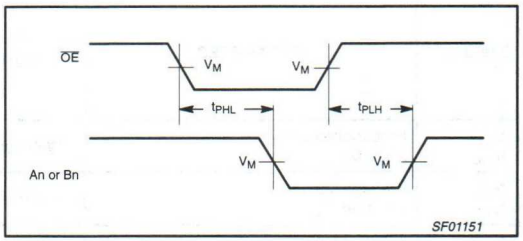
* *Discontinued part. Please see the Discontinued Products List.*

AC WAVEFORMS (Continued)

For all waveforms, V_M = 1.5V.

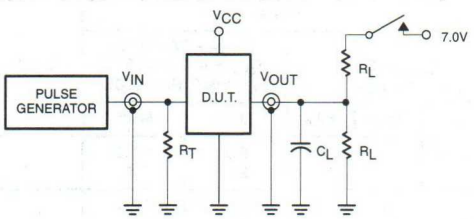


Waveform 3. Propagation Delay for $\overline{OE}$ to An or Bn Outputs (74F642) (Bn or An Inputs in High State)

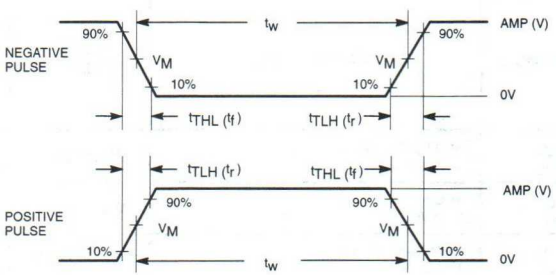


Waveform 4. Propagation Delay for $\overline{OE}$ to An or Bn Outputs (74F641) (Bn or An Inputs in Low State)

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

* *Discontinued part. Please see the Discontinued Products List.*

FEATURES

- Combines 74F245 and two 74F374 type functions in one chip
- High impedance base inputs for reduced loading (70µA in high and low states)
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Choice of non-inverting and inverting data paths
- Controlled ramp outputs for 74F646A/74F648A
- 3-state outputs
- 300 mil wide 24-pin slim dip package

DESCRIPTION

The 74F646/74F646A and 74F648/74F648A transceivers/registers consist of bus transceiver circuits with 3–state outputs, D–type flip–flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes high. Output enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

The select (SAB, SBA) pins determine whether data is stored or transferred through the device in real–time. The DIR determines which bus will receive data when the $\overline{OE}$ is active low. In the isolation mode ($\overline{OE}$ = high), data from bus A may be stored in the B register and/or data from bus B may be stored in the A register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F646/74F648	115MHz	140mA
74F646A/74F648A	185MHz	105mA

ORDERING INFORMATION

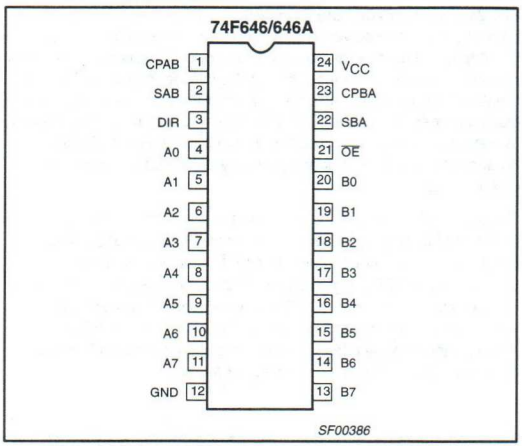
DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
24–pin plastic slim DIP (300mil)	N74F646N, N74F646AN, N74F648N, N74F648AN	SOT222-1
24–pin plastic SOL	N74F646D, N74F646AD, N74F648D, N74F648AD	SOT137-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

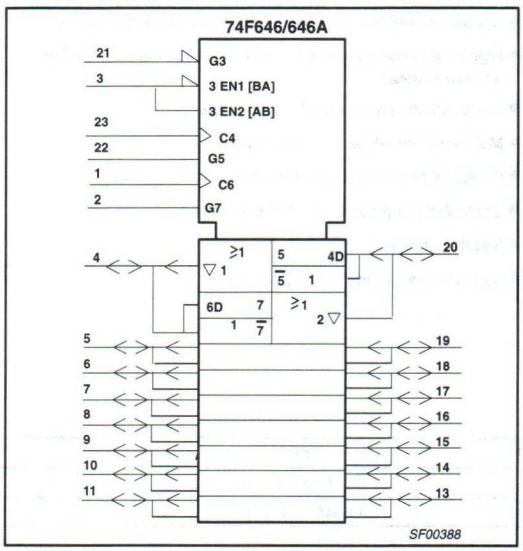
PINS	DESCRIPTION	74F (U.L.) HIGH/ LOW	LOAD VALUE HIGH/ LOW
A0 – A7, B0 – B7	A and B inputs	3.5/0.116	70µA/70µA
CPAB	A–to–B clock input	1.0/0.033	20µA/20µA
CPBA	B–to–A clock input	1.0/0.033	20µA/20µA
SAB	A–to–B select input	1.0/0.033	20µA/20µA
SBA	B–to–A select input	1.0/0.033	20µA/20µA
DIR	Data flow directional control enable input	1.0/0.033	20µA/20µA
$\overline{OE}$	Output enable input	1.0/0.033	20µA/20µA
A0 – A7, B0 – B7	A, B outputs for N74F646A/N74F648A	750/80	15mA/48mA
A0 – A7, B0 – B7	A, B outputs for N74F646/N74F648	750/106.7	15mA/64mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

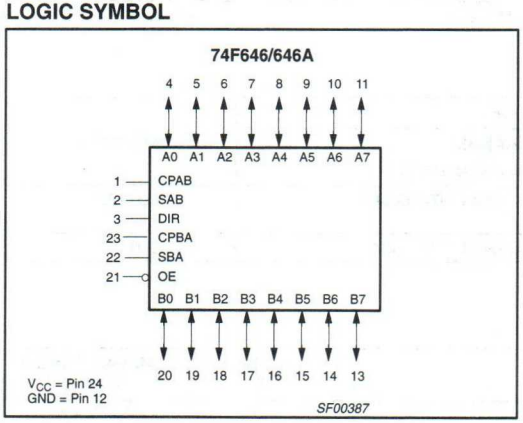
PIN CONFIGURATION



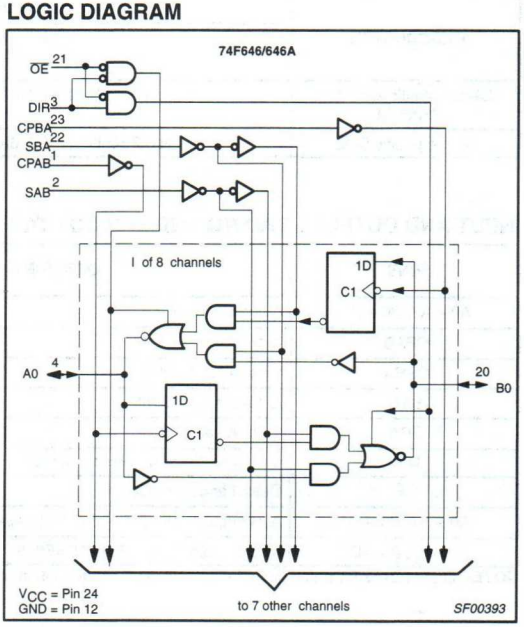
IEC/IEEE SYMBOL



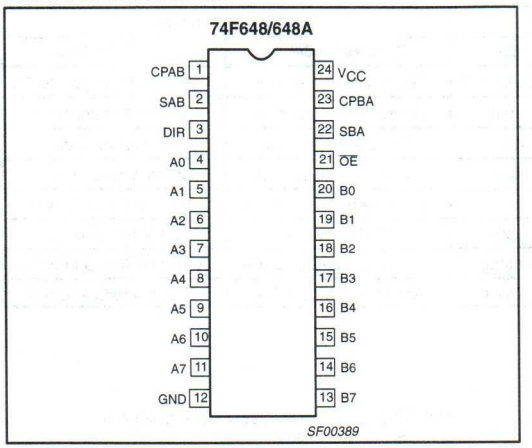
LOGIC SYMBOL



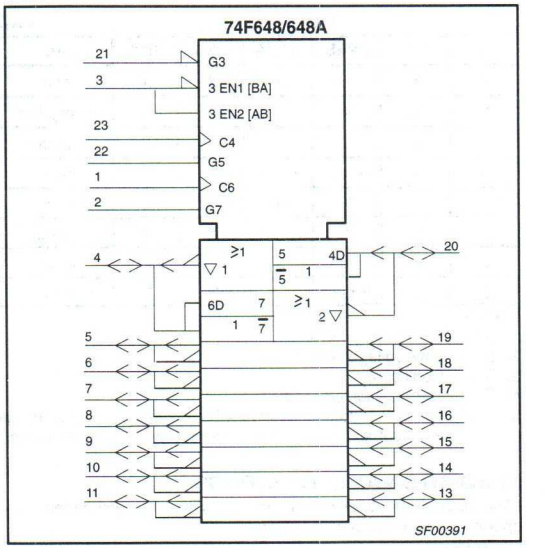
LOGIC DIAGRAM



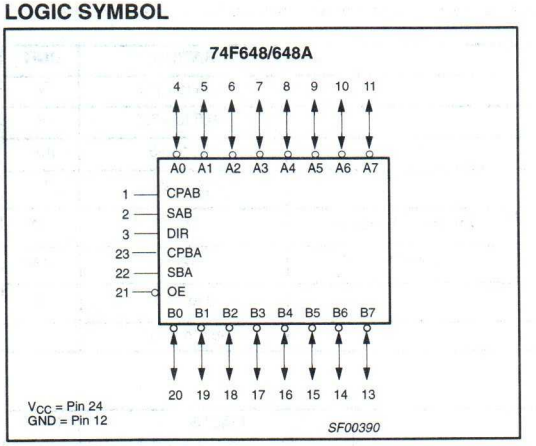
PIN CONFIGURATION



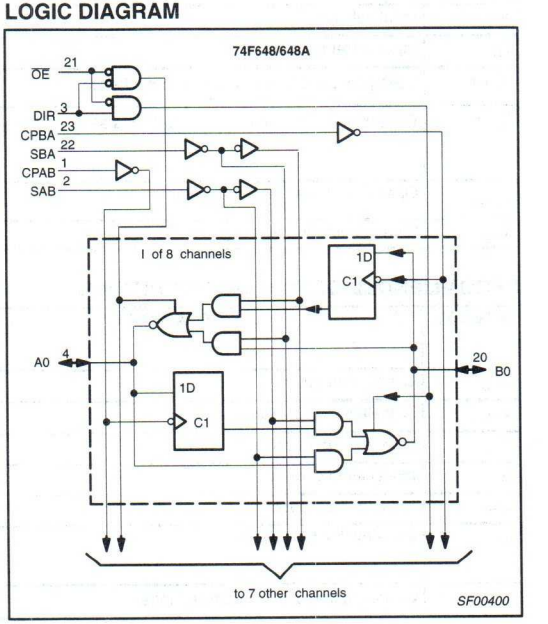
IEC/IEEE SYMBOL



LOGIC SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	An	Bn	74F646/74F646A	74F648/74F648A
X	X	↑	X	X	X	Input	Unspecified*	Store A, B unspecified*	Store A, B unspecified*
X	X	X	↑	X	X	Unspecified*	Input	Store B, A unspecified*	Store B, A unspecified*
H	X	↑	↑	X	X	Input	Input	Store A and B data	Store A and B data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real time B data to A bus	Real time $\overline{B}$ data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus	Stored $\overline{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real time A data to B bus	Real time $\overline{A}$ data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus	Stored $\overline{A}$ data to B bus

NOTES:
1. H = High–voltage level
2. L = Low–voltage level
3. X = Don't care
4. ↑ = Low–to–high clock transition
5. * = The data output function may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low–to–high transition of the clock.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

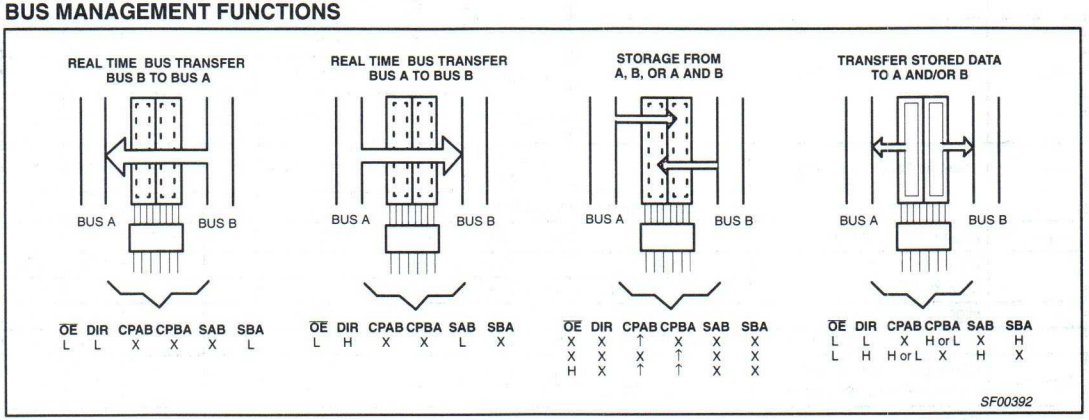
SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	74F646A, 74F648A	72	mA
		74F646, 74F648	128	mA
T_{amb}	Operating free air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current				–15	mA
I_{OL}	Low–level output current	74F646A, 74F648A			48	mA
		74F646, 74F648			64	mA
T_{amb}	Operating free air temperature range		0		+70	°C

The following examples demonstrate the four fundamental bus–management functions that can be performed with the 74F646/646A and 74F648/648A. The select pins determine whether data is stored or transferred through the device in real time. The output enable pins determine the direction of the data flow.

BUS MANAGEMENT FUNCTIONS



DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = –15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	All	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.38	0.55	V
		74F646/74F648 only		I_{OL} = 64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A0–A7, B0–B7	V_{CC} = MAX, V_I = 5.5V					1	mA
I_{IH}	High–level input current	$\overline{OE}$, DIR, CPAB, CPBA, SAB, SBA	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{OZH} + I_{IH}	Off–state output current, high–level voltage applied	A0 – A7, B0 –B7	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{OZL} + I_{IL}	Off–state output current, low–level voltage applied		V_{CC} = MAX, V_O = 0.5V					–70	µA
I_{OS}	Short–circuit output current[3]	74F646, 74F648	V_{CC} = MAX			-100		-225	mA
I_O	Output current[4]	74F646A, 74F648A	V_{CC} = MAX, V_0 = 2.25V			-60		-150	mA
I_{CC}	Supply current (total)	74F646, 74F648	I_{CCH}	V_{CC} = MAX			125	165	mA
			I_{CCL}				160	210	mA
			I_{CCZ}				135	160	mA
		74F646A, 74F648A	I_{CCH}	V_{CC} = MAX			100	145	mA
			I_{CCL}				110	155	mA
			I_{CCZ}				105	155	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type. Unless otherwise specified, V_X = V_{CC} for all test conditions.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_O is tested under conditions that produce current approximately one half of the true short–circuit output current (I_{OS}).

AC ELECTRICAL CHARACTERISTICS FOR 74F646

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	100	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to An or Bn	Waveform 1	5.5 5.5	7.5 8.0	10.0 10.0	5.0 5.0	11.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	Waveform 2	4.0 4.0	6.0 6.5	9.0 8.0	4.0 4.0	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to An or Bn	Waveform 2, 3	5.0 5.0	7.0 6.5	8.5 8.5	4.5 4.5	10.5 9.5	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	5.0 6.5	7.0 8.5	10.0 11.0	4.5 6.0	11.0 12.5	ns
t_{PZH} t_{PZL}	Output enable time DIR to An or Bn	Waveform 5 Waveform 6	4.5 6.0	6.5 8.5	9.0 11.0	4.0 5.5	10.0 12.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	6.5 6.5	9.0 9.0	11.5 11.5	6.0 6.0	12.5 13.5	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to An or Bn	Waveform 5 Waveform 6	5.5 5.5	8.5 8.5	11.0 11.0	4.5 5.0	13.0 12.5	ns

AC SETUP REQUIREMENTS FOR 74F646

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low An or Bn to CPAB or CPBA	Waveform 4	4.5 4.5			5.0 5.0		ns
t_h (H) t_h (L)	Hold time, high or low An or Bn to CPAB or CPBA	Waveform 4	0 0			0 0		ns
t_w (H) t_w (L)	Pulse width, high or low CPAB or CPBA	Waveform 1	4.0 6.0			4.0 6.0		ns

AC ELECTRICAL CHARACTERISTICS FOR 74F648

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	100	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to An or Bn	Waveform 1	5.0 5.0	7.0 7.5	9.5 9.5	4.5 4.5	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	Waveform 3	3.0 4.0	6.0 6.0	8.5 8.5	2.5 3.5	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to An or Bn	Waveform 2,3	4.5 4.5	7.0 6.5	8.5 8.5	4.5 4.5	10.5 9.5	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	4.5 6.0	7.0 8.5	10.0 11.0	4.5 5.5	11.0 12.5	ns
t_{PZH} t_{PZL}	Output enable time DIR to An or Bn	Waveform 5 Waveform 6	4.5 6.0	7.0 8.5	10.0 11.0	4.0 5.5	11.0 12.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	6.0 6.0	9.0 8.5	11.5 12.0	6.0 6.0	12.5 13.5	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to An or Bn	Waveform 5 Waveform 6	5.0 5.0	9.0 9.0	12.5 12.5	4.5 5.0	14.0 14.0	ns

AC SETUP REQUIREMENTS FOR 74F648

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low An or Bn to CPAB or CPBA	Waveform 4	4.0 4.0			5.0 5.0		ns
t_h (H) t_h (L)	Hold time, high or low An or Bn to CPAB or CPBA	Waveform 4	0 0			0 0		ns
t_w (H) t_w (L)	Pulse width, high or low CPAB or CPBA	Waveform 1	3.5 6.5			4.0 7.0		ns

AC ELECTRICAL CHARACTERISTICS FOR 74F646A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	165	185		150		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to An or Bn	Waveform 1	5.5 4.5	7.0 7.0	10.5 9.5	4.5 4.0	11.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	Waveform 2	4.0 2.0	6.0 5.0	9.0 8.0	3.5 2.0	10.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to An or Bn	Waveform 2, 3	4.5 3.5	6.5 8.0	9.5 10.0	4.0 3.0	10.0 11.5	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	3.0 3.0	5.5 5.5	9.0 10.0	2.5 2.5	10.0 10.5	ns
t_{PZH} t_{PZL}	Output enable time DIR to An or Bn	Waveform 5 Waveform 6	3.0 3.5	5.0 6.0	8.0 8.5	3.0 3.0	8.5 9.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	1.5 2.5	4.0 5.5	6.5 8.0	1.0 2.0	8.0 9.5	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to An or Bn	Waveform 5 Waveform 6	2.0 3.0	4.5 5.0	7.5 8.0	1.5 2.0	8.5 8.5	ns

AC SETUP REQUIREMENTS FOR 74F646A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low An or Bn to CPAB or CPBA	Waveform 4	3.5 4.0			4.0 4.5		ns
t_h (H) t_h (L)	Hold time, high or low An or Bn to CPAB or CPBA	Waveform 4	0 0			0 0		ns
t_w (H) t_w (L)	Pulse width, high or low CPAB or CPBA	Waveform 1	3.5 3.5			4.5 4.0		ns

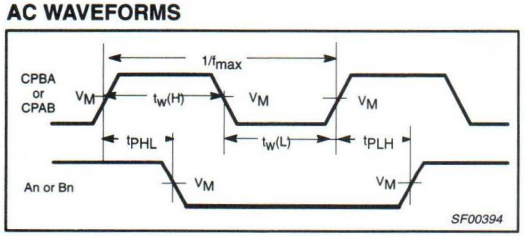
AC ELECTRICAL CHARACTERISTICS FOR 74F648A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	160	185		135		ns
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to An or Bn	Waveform 1	5.0 5.5	7.0 7.5	9.5 10.0	4.5 4.5	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	Waveform 3	2.5 4.0	4.5 6.0	7.5 8.5	2.0 4.0	8.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to An or Bn	Waveform 2, 3	4.0 4.5	7.0 7.0	9.5 9.5	3.5 4.5	11.5 10.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	3.5 4.5	6.5 6.5	10.0 10.0	3.5 4.0	11.0 11.5	ns
t_{PZH} t_{PZL}	Output enable time DIR to An or Bn	Waveform 5 Waveform 6	3.5 4.0	5.5 6.5	8.5 9.5	3.0 4.0	9.0 10.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	2.5 4.0	4.0 6.5	6.5 9.0	2.0 3.5	8.0 10.0	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to An or Bn	Waveform 5 Waveform 6	2.5 2.5	5.0 5.0	8.5 8.0	2.0 3.5	9.0 9.0	ns

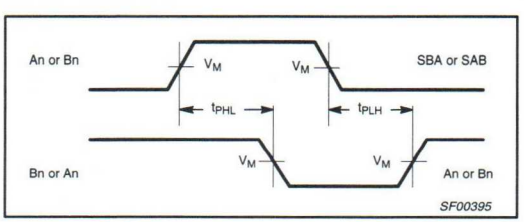
AC SETUP REQUIREMENTS FOR 74F648A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low An or Bn to CPAB or CPBA	Waveform 4	4.0 4.0			4.5 4.5		ns
t_h (H) t_h (L)	Hold time, high or low An or Bn to CPAB or CPBA	Waveform 4	0 0			0 0		ns
t_w (H) t_w (L)	Pulse width, high or low CPAB or CPBA	Waveform 1	3.5 3.5			4.0 3.5		ns

AC WAVEFORMS

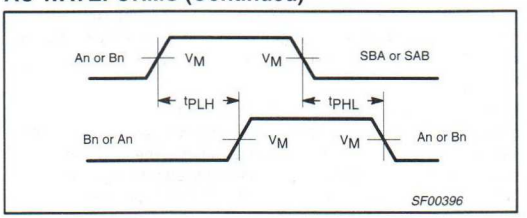


Waveform 1. Propagation delay for clock input to output clock pulse width, and maximum clock frequency

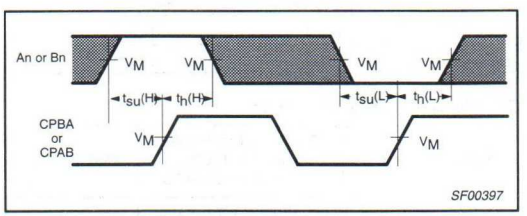


Waveform 2. Propagation delay for An to Bn or Bn to An and SAB or SBA to An or Bn

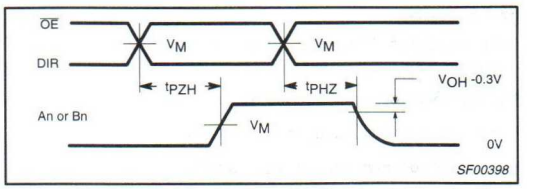
AC WAVEFORMS (Continued)



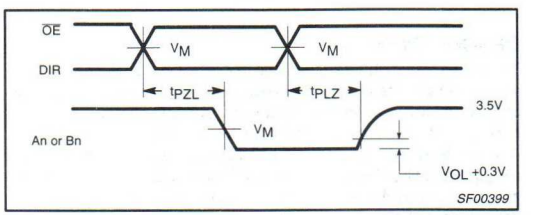
Waveform 3. Propagation delay for An to Bn or Bn to An and SAB or SBA to An or Bn



Waveform 4. Data setup time and hold times



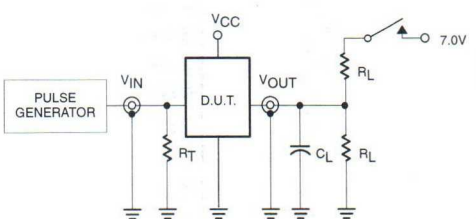
Waveform 5. 3-state output enable time to high level and output disable time from high level



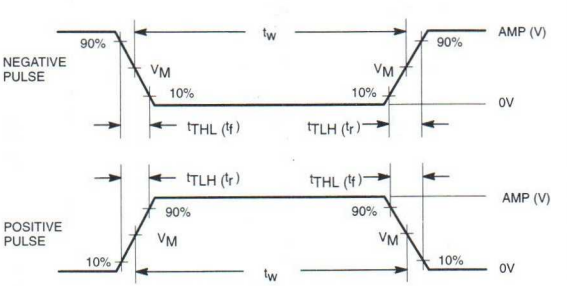
Waveform 6. 3-state output enable time to low level and output disable time from low level

NOTES:
1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

Octal transceivers/registers (open-collector) 74F647/74F649

74F647 Octal Transceiver/Register, Non-inverting (Open Collector)
74F649 Octal Transceiver/Register, Inverting (Open Collector)

FEATURES

- High impedance NPN base inputs for reduced loading (20μA in High and Low states)
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Choice of non-inverting and inverting data paths
- Open Collector outputs
- 300 mil wide 24-pin Slim Dip package

DESCRIPTION

The 74F647 and 74F649 Transceivers/Registers consist of bus transceiver circuits with open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a High logic level. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

The select (SAB, SBA) controls can multiplex stored and real-time (transparent mode) data. The DIR determines which bus will receive data when the Output Enable, $\overline{OE}$ is active Low. In the isolation mode (Output Enable, $\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register.

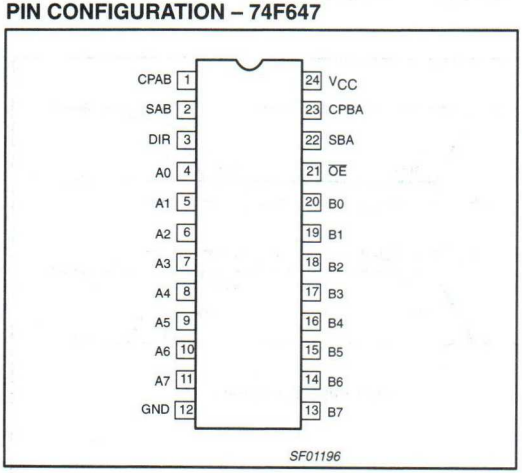
When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time. The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74F647 and 74F649.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F647	65MHz	125mA
74F649	65MHz	125mA

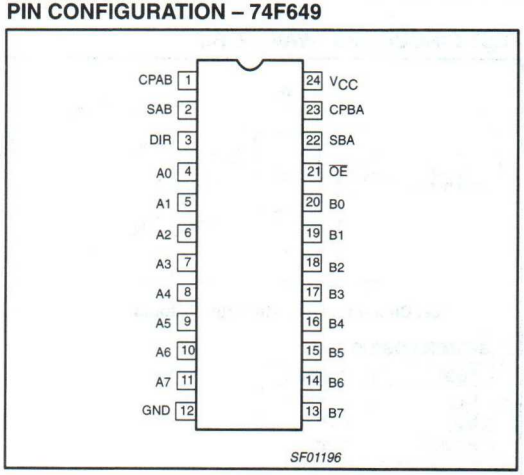
ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
24-pin plastic Slim DIP (300mil)	N74F647N, N74F649N	SOT222-1
24-pin plastic SOL	N74F647D, N74F649D	SOT137-1

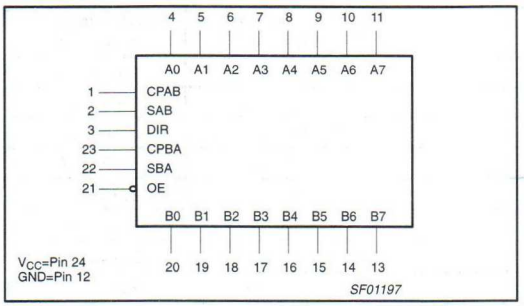
PIN CONFIGURATION – 74F647



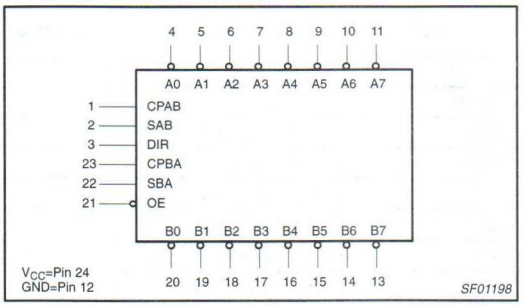
PIN CONFIGURATION – 74F649



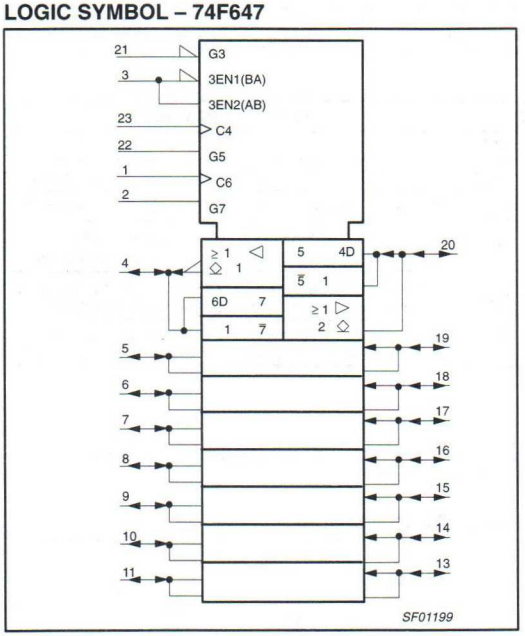
LOGIC SYMBOL – 74F647



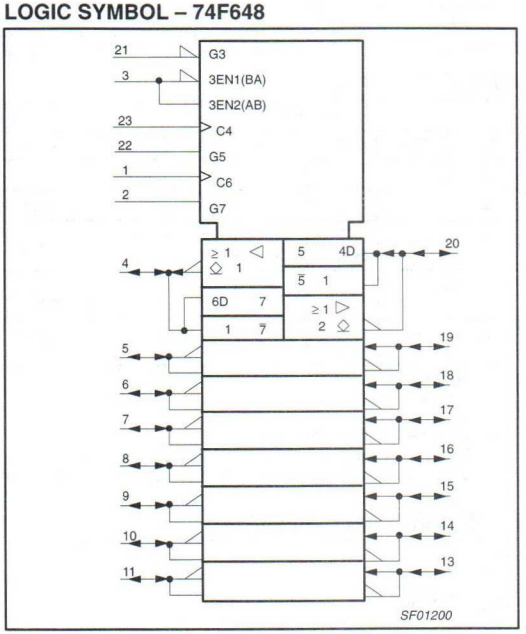
LOGIC SYMBOL – 74F649

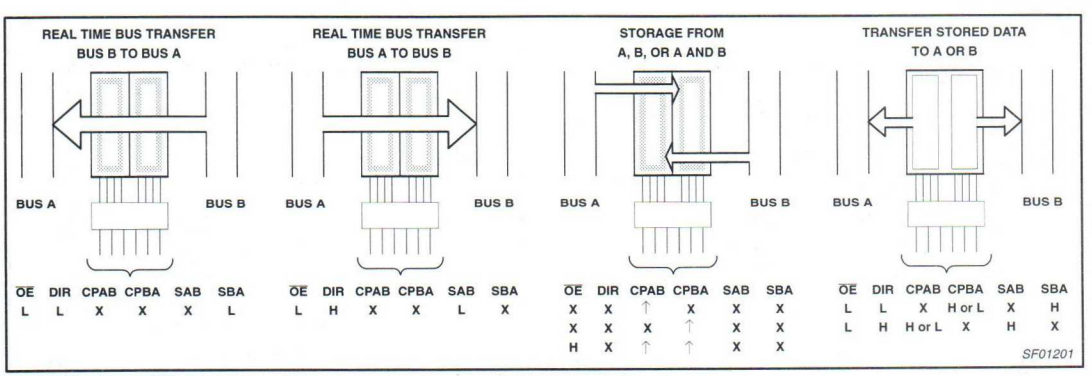


LOGIC SYMBOL – 74F647



LOGIC SYMBOL – 74F648





INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 - A7	A inputs	1.0/0.033	20μA/20μA
B0 - B7	B inputs	1.0/0.033	20μA/20μA
CPAB	A-to-B clock input	1.0/0.033	20μA/20μA
CPBA	B-to-A clock input	1.0/0.033	20μA/20μA
SAB	A-to-B select input	1.0/0.033	20μA/20μA
SBA	B-to-A select input	1.0/0.033	20μA/20μA
DIR	Data flow Directional control enable input	1.0/0.066	20μA/20μA
$\overline{OE}$	Output Enable input	1.0/0.066	20μA/20μA
A0 - A7	A outputs	OC/106.7	OC/64mA
B0 - B7	B outputs	OC/106.7	OC/64mA

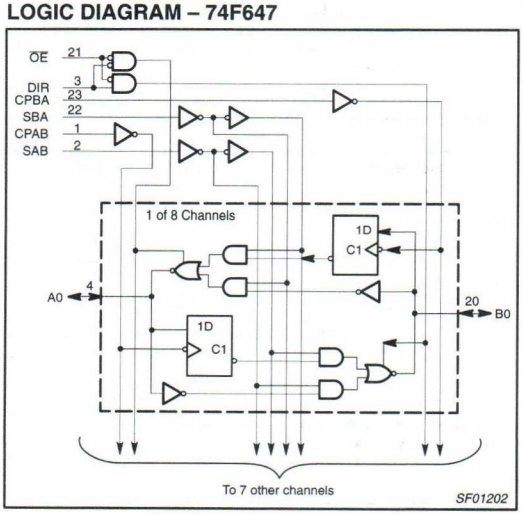
NOTE: One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state. OC = Open Collector

FUNCTION TABLE

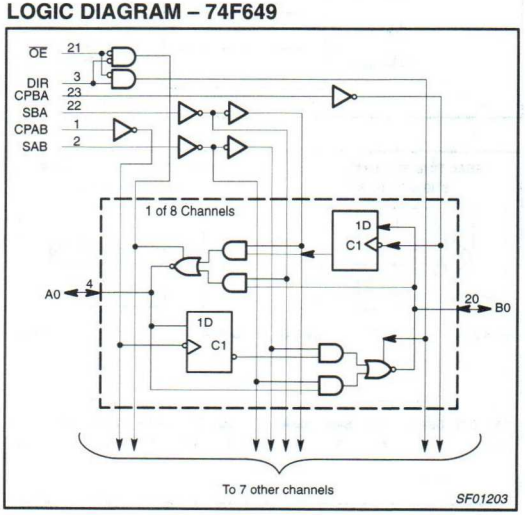
INPUTS						DATA I/O		OPERATING MODE	
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	A0-A7	B0-B7		
X	X	↑	X	X	X	Input	Unspecified*	Store A, B unspecified*	Store A, B unspecified*
X	X	X	↑	X	X	Unspecified*	Input	Store B, A unspecified*	Store B, A unspecified*
H H	X X	↑ H or L	↑ H or L	X X	X X	Input	Input	Store A and B data Isolation, hold storage	Store A and B data Isolation, hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus	Real time B data to A bus Stored B data to A bus
L L	H H	H or L X	X X	L H	X X	Input	Output	Real time A data to B bus Stored A data to B bus	Real time A data to B bus Stored A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* = The data output function may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

LOGIC DIAGRAM – 74F647



LOGIC DIAGRAM – 74F649



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
V_{OH}	High-level output voltage			4.5	V
I_{OL}	Low-level output current			64	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX					250	µA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL} = 48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL} = 64mA	±5%V_{CC}		0.42	0.55	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	Others	V_{CC} = 0.0, V_I = 7.0V					100	µA
		An, Bn	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				105	145	mA
		I_{CCL}					145	200	mA

NOTES:
1. For conditions shown as MIN or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	50	65		40		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA or An	Waveform 1	7.0 5.5	12.0 8.5	15.0 11.0	7.0 5.5	16.5 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	Waveform 2 Waveform 3	7.5 4.0	10.5 7.0	13.5 9.5	7.5 4.0	16.0 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay SBA to An or SAB to Bn	Waveform 2 Waveform 3	7.5 4.0	11.5 7.0	14.5 9.5	7.5 4.0	17.0 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to An or Bn	Waveform 2 Waveform 3	9.0 6.5	13.0 10.0	16.0 12.5	9.0 6.5	18.5 13.5	ns ns
t_{PLH} t_{PHL}	Propagation delay DIR to An or Bn	Waveform 2 Waveform 3	9.0 7.0	13.0 15.0	16.0 18.0	9.0 7.0	18.5 20.0	ns ns

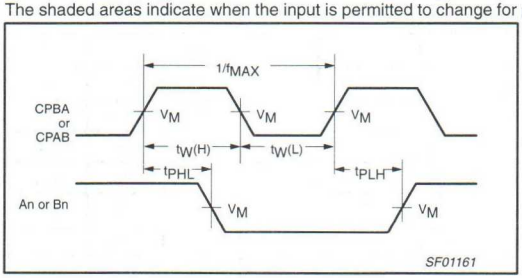
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low An to CPBA or Bn to CPAB	Waveform 4	4.0 4.0			5.0 5.0		ns ns
t_s(H) t_s(L)	Hold time, High or Low An to CPBA or Bn to CPAB	Waveform 4	0 0			0 0		ns ns
t_w(H) t_w(L)	Pulse width, High or Low CPAB or CPBA	Waveform 1	4.5 6.0			4.5 6.5		ns ns

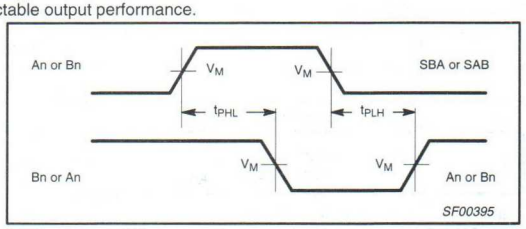
AC WAVEFORMS

For all waveforms, V_M = 1.5V

The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

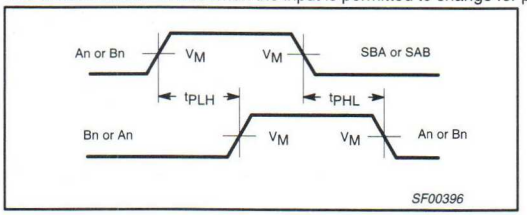


Waveform 2. Propagation Delay, An to Bn or Bn to An and SBA to An or SAB to Bn

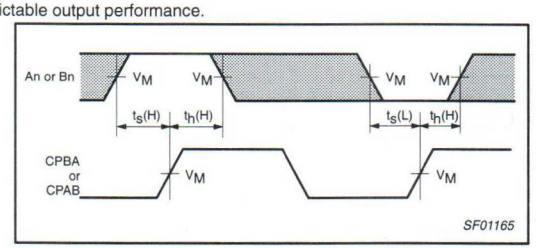
AC WAVEFORMS (Continued)

For all waveforms, V_M = 1.5V

The shaded areas indicate when the input is permitted to change for predictable output performance.

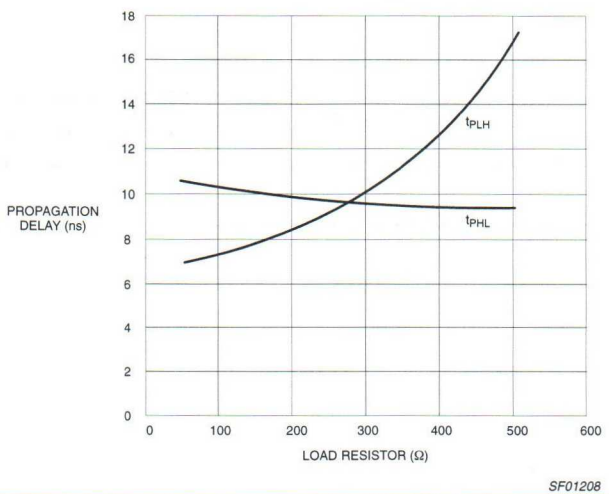


Waveform 3. Propagation Delay, An to Bn or Bn to An and SBA to An or SAB to Bn



Waveform 4. Data Setup and Hold Times

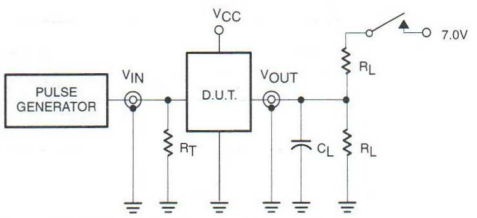
TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS



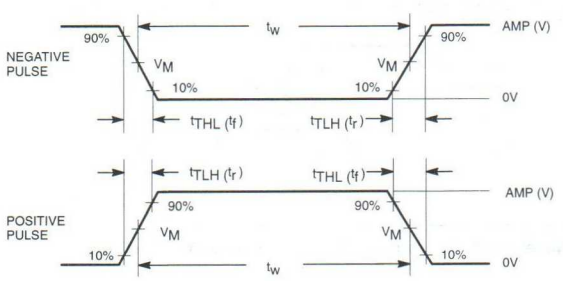
NOTE:

When using open-collector part, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only slight increase in the t_{PHL}. However, if the pull-up resistor is changed, the user must take certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers do not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
Open Collector	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00195

Transceivers/registers

~~74F651/74F652~~*, 74F651A/74F652A

FEATURES

- Combines 74F245 and two 74F374 type functions in one chip
- High impedance base inputs for reduced loading (70μA in high and low states)
- Independent registers for A and B buses
- Multiplexed real–time and stored data
- Choice of non–inverting and inverting data paths
- 3–state outputs
- Industrial temperature range available (–40°C to +85°C) for 74F652A

DESCRIPTION

The 74F651/74F651A and 74F652/74F652A transceivers/registers consist of bus transceiver circuits with 3–state outputs, D–type flip–flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes high. Output enable (OEAB, $\overline{OEBA}$) and select (SAB, SBA) pins are provided for bus management.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT(TOTAL)
74F651/74F652	110MHz	140mA
74F651A/74F652A	175MHz	110mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
24–pin plastic slim DIP (300mil)	N74F651AN, N74F652AN	I74F652AN	SOT222-1
24–pin plastic SOL	N74F651AD, N74F652AD	I74F652AD	SOT137-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

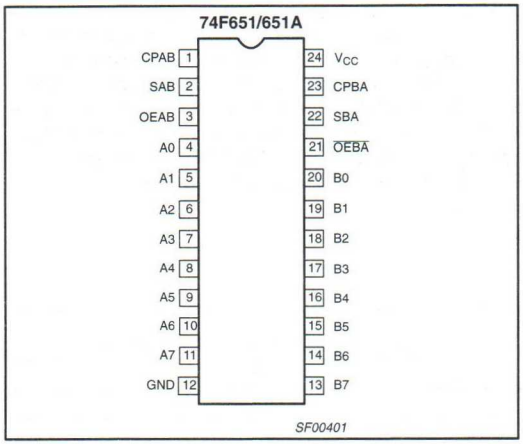
PINS	DESCRIPTION	74F (U.L.) HIGH/ LOW	LOAD VALUE HIGH/ LOW
A0 – A7, B0 – B7	A, B inputs	3.5/0.116	70μA/70μA
CPAB, CPBA	A–to–B, B–to–A clock inputs	1.0/0.033	20μA/20μA
SAB, SBA	A–to–B, B–to–A select inputs	1.0/0.033	20μA/20μA
OEAB, $\overline{OEBA}$	A–to–B, B–to–A output enable inputs	1.0/0.033	20μA/20μA
A0 – A7, B0 – B7	A, B outputs for N74F651, N74F652	750/106.7	15mA/64mA
A0 – A7, B0 – B7	A, B outputs for N74F651A, N74F652A	750/80	15mA/48mA
A0 – A7, B0 – B7	A, B outputs for I74F652A	750/60	15mA/36mA

Note to input and output loading and fan out table

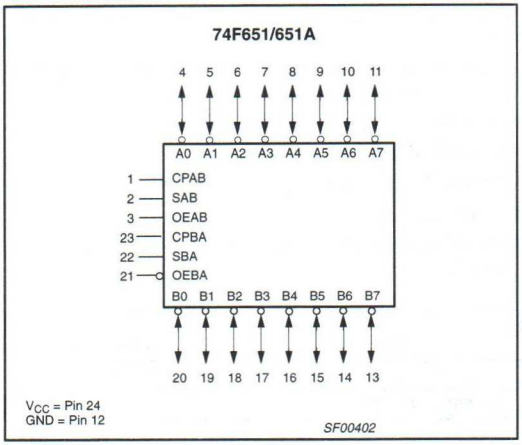
1. One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.

* *Discontinued part. Please see the Discontinued Product List.*

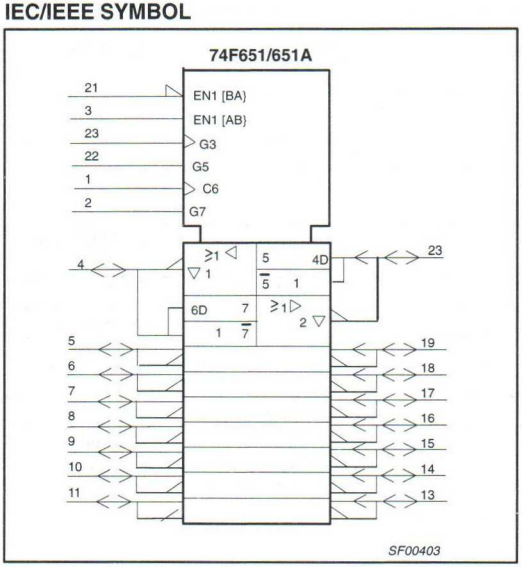
PIN CONFIGURATION



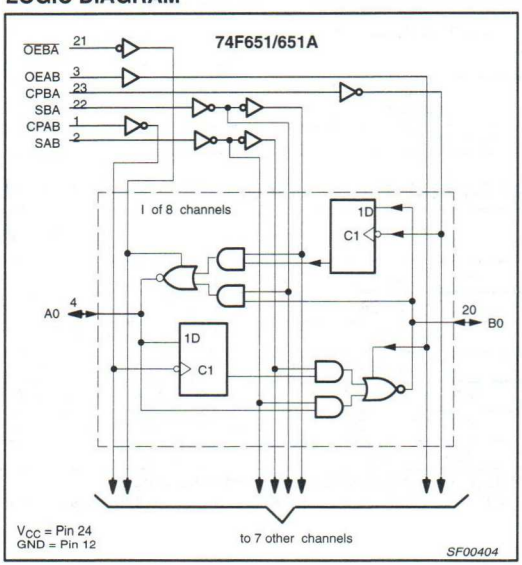
LOGIC SYMBOL



IEC/IEEE SYMBOL

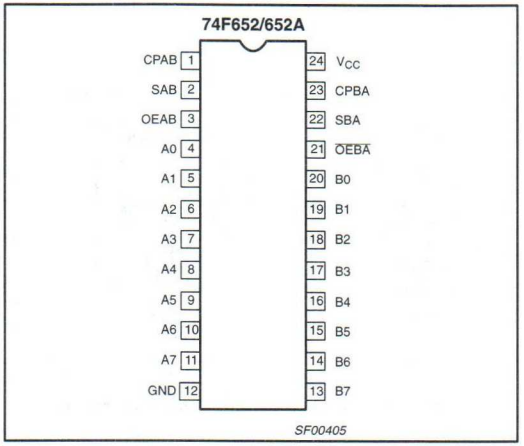


LOGIC DIAGRAM

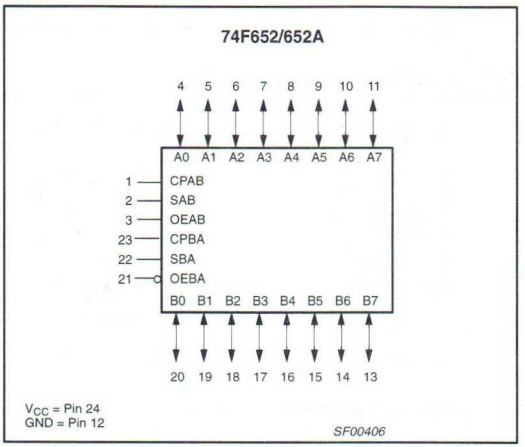


* *Discontinued part. Please see the Discontinued Product List.*

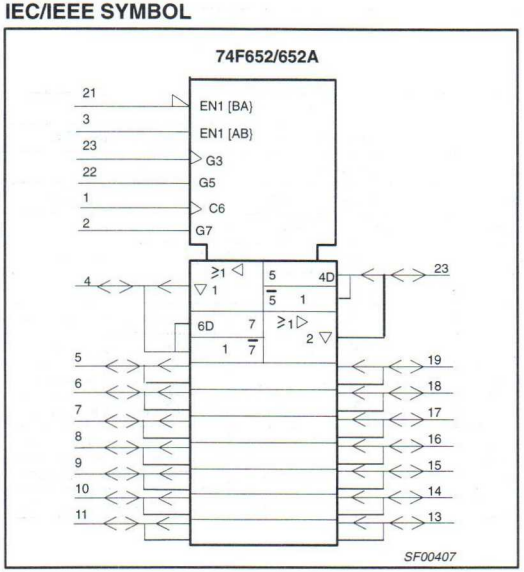
PIN CONFIGURATION



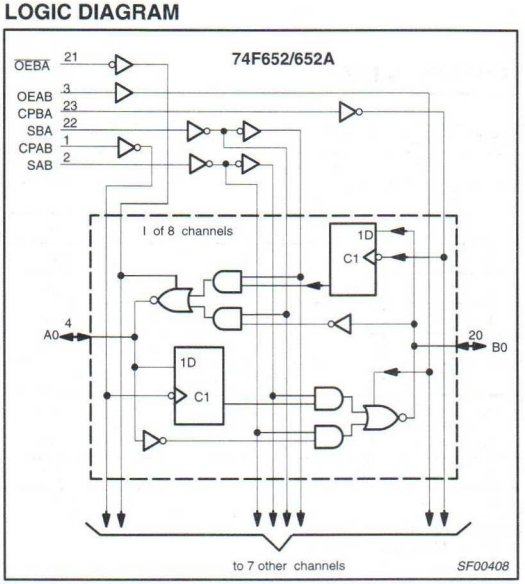
LOGIC SYMBOL



IEC/IEEE SYMBOL



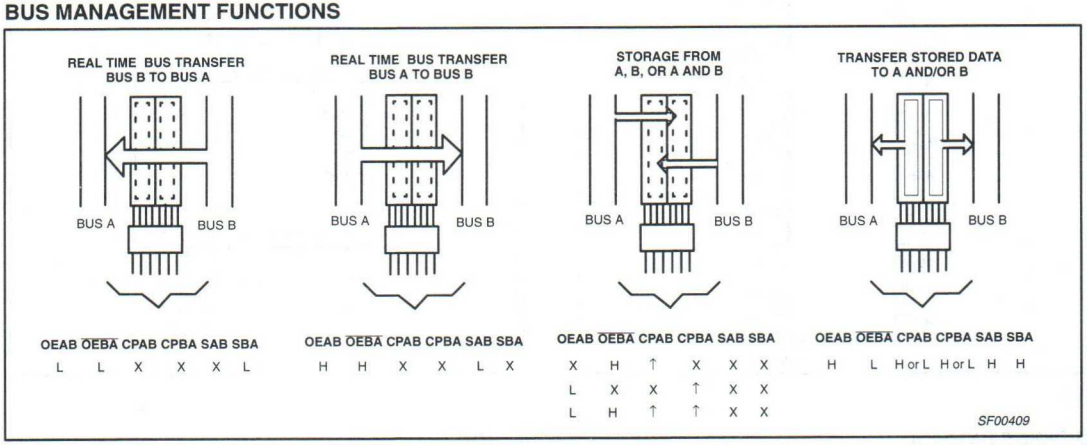
LOGIC DIAGRAM



* *Discontinued part. Please see the Discontinued Product List.*

The following examples demonstrate the four fundamental bus–management functions that can be performed with the 74F651/651A and 74F652/652A. The select pins determine whether data is stored or transferred through the device in real time. The output enable pins determine the direction of the data flow.

BUS MANAGEMENT FUNCTIONS



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	An	Bn	74F651/74F651A	74F652/74F652A
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified*	Store A, hold B	Store A hold B
H	H	↑	↑	L	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Unspecified*	Input	Hold A, store B	Hold A, store B
L	L	↑	↑	X	L	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real time $\overline{B}$ data to A bus	Real time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored $\overline{B}$ data to A bus	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real time $\overline{A}$ data to B bus	Real time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored $\overline{A}$ data to B bus	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ data to B bus	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{B}$ data to A bus	Stored B data to A bus

Notes to function table

1. H = High–voltage level
2. L = Low–voltage level
3. * = The data output function may be enabled or disabled by various signals at the $\overline{OEBA}$ and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low–to–high transition of the clock.
4. ↑ = Low–to–high clock transition
5. X = Don't care

* *Discontinued part. Please see the Discontinued Product List.*

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	74F651, 74F652	128	mA
		74F651A, 74F652A	72	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER			LIMITS			UNIT
				MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5.0	5.5	V
V_{IH}	High–level input voltage			2.0			V
V_{IL}	Low–level input voltage					0.8	V
I_{Ik}	Input clamp current					–18	mA
I_{OH}	High–level output current					–15	mA
I_{OL}	Low–level output current	Commercial range	74F651, 74F652			64	mA
			74F651A, 74F652A			48	mA
		Industrial range (74F652A only)				36	mA
T_{amb}	Operating free air temperature range	Commercial range		0		+70	°C
		Industrial range (74F652A only)		–40		+85	°C

* *Discontinued part. Please see the Discontinued Product List.*

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
				I_{OH} = –15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A0–A7, B0–B7	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High–level input current	OEAB, $\overline{OEBA}$, CPAB, CPBA, SAB, SBA	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{OZH} + I_{IH}	Off–state output current, high–level voltage applied	A0 – A7, B0 –B7	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{OZL} + I_{IL}	Off–state output current, low–level voltage applied		V_{CC} = MAX, V_O = 0.5V					–70	µA
I_{OS}	Short–circuit output current[3]	74F651, 74F652	V_{CC} = MAX			-100		-225	mA
I_O	Output current[4]	74F651A, 74F652A	V_{CC} = MAX, V_0 = 2.25V			-60		-160	mA
I_{CC}	Supply current (total)	74F651, 74F652	I_{CCH}	V_{CC} = MAX			110	155	mA
			I_{CCH}				140[5]	185[5]	mA
			I_{CCL}				155	200	mA
			I_{CCL}				165[5]	240[5]	mA
			I_{CCZ}				130	175	mA
		74F651A, 74F652A	I_{CCH}	V_{CC} = MAX			105	145	mA
			I_{CCL}				115	165	mA
			I_{CCZ}				115	160	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_O is tested under conditions that produce current approximately one half of the true short–circuit output current (I_{OS}).
5. These values are for worst case only. Worst case is defined as all (16) I/O pins selected as outputs. When using worst case conditions thermal mounting is required.

* *Discontinued part. Please see the Discontinued Product List.*

AC ELECTRICAL CHARACTERISTICS FOR 74F651/74F652

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	90	110		80		ns
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to An or Bn	Waveform 1	5.0 5.5	7.0 7.5	10.5 11.0	4.5 5.0	12.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay An or Bn to Bn or An	Waveform 2, 3	3.0 3.0	6.0 6.0	10.0 9.0	2.5 3.0	12.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to An or Bn	Waveform 2, 3	4.0 4.0	7.0 6.5	10.0 9.5	4.0 4.0	12.5 10.0	ns
t_{PZH} t_{PZL}	Output enable time OEAB or $\overline{OEBA}$ to An or Bn	Waveform 7, 8	4.0 6.0	7.0 10.5	10.0 12.0	3.5 5.5	11.0 13.0	ns
t_{PHZ} t_{PLZ}	Output disable time OEAB or $\overline{OEBA}$ to An or Bn	Waveform 7, 8	4.5 4.5	9.5 9.0	13.0 13.0	4.0 4.0	14.5 15.5	ns

AC SETUP REQUIREMENTS FOR 74F651/74F652

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low An or Bn to CPAB or CPBA	Waveform 4	4.0 4.0			5.0 5.0		ns
t_h (H) t_h (L)	Hold time, high or low An or Bn to CPAB or CPBA	Waveform 4	0 0			0 0		ns
t_{su} (H) t_{su} (L)	Setup time, high or low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	5.0 5.0			5.0 5.0		ns
t_h (H) t_h (L)	Hold time, high or low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	0 0			0 0		ns
t_w (H) t_w (L)	Pulse width, high or low CPAB or CPBA	Waveform 1	4.5 6.5			4.5 6.5		ns

Note to AC setup requirements for 74F651/652

1. Setup time is to protect against surge current caused by enabling 16 outputs (64mA per output) simultaneously.

* *Discontinued part. Please see the Discontinued Product List.*

AC ELECTRICAL CHARACTERISTICS FOR 74F651A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	155	175		140		ns
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to An or Bn	Waveform 1	4.5 5.5	7.0 7.5	10.0 10.5	4.0 5.0	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay An or Bn to Bn or An	Waveform 2, 3	2.5 4.0	4.5 6.5	7.5 9.0	2.0 4.0	8.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to An or Bn	Waveform 2, 3	4.0 5.0	7.0 7.0	10.0 10.0	3.5 4.5	12.0 10.0	ns
t_{PZH} t_{PZL}	Output enable time OEAB or $\overline{OEBA}$ to An or Bn	Waveform 7, 8	3.0 3.5	5.0 6.0	8.0 8.5	2.5 3.0	8.5 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time OEAB or $\overline{OEBA}$ to An or Bn	Waveform 7, 8	1.5 2.5	4.0 6.0	7.0 8.5	1.0 2.0	7.5 9.0	ns

AC SETUP REQUIREMENTS FOR 74F651A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low An or Bn to CPAB or CPBA	Waveform 4	3.5 4.0			4.0 4.5		ns
t_h (H) t_h (L)	Hold time, high or low An or Bn to CPAB or CPBA	Waveform 4	0 0			0 0		ns
t_{su} (H) t_{su} (L)	Setup time, high or low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	5.0 5.0			5.0 5.0		ns
t_h (H) t_h (L)	Hold time, high or low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	0 0			0 0		ns
t_w (H) t_w (L)	Pulse width, high or low CPAB or CPBA	Waveform 1	4.5 3.5			4.5 4.0		ns

Note to AC setup requirements for 74F651A

1. Setup time is to protect against surge current caused by enabling 16 outputs (48mA per output) simultaneously.

* *Discontinued part. Please see the Discontinued Product List.*

AC ELECTRICAL CHARACTERISTICS FOR 74F652A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = −40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	155	175		140		140		ns
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to An or Bn	Waveform 1	5.0 5.0	7.5 7.0	10.0 10.0	4.5 4.5	11.5 10.5	4.5 4.5	11.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay An or Bn to Bn or An	Waveform 1	4.0 3.0	6.0 5.0	9.0 8.0	3.5 2.5	10.0 8.5	3.5 2.5	10.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to An or Bn	Waveform 2, 3	4.5 4.0	7.0 8.0	10.0 10.0	4.0 4.0	11.0 11.5	4.0 4.0	11.0 11.5	ns
t_{PZH} t_{PZL}	Output enable time[1] OEAB or $\overline{OEBA}$ to An or Bn	Waveform 7, 8	3.0 3.5	5.0 6.0	8.0 8.5	2.5 3.0	8.5 9.0	2.5 3.0	8.5 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time OEAB or $\overline{OEBA}$ to An or Bn	Waveform 7, 8	1.5 2.5	4.0 6.0	7.0 8.5	1.0 2.0	7.5 9.0	1.0 2.0	7.5 9.0	ns

AC SETUP REQUIREMENTS FOR 74F652A

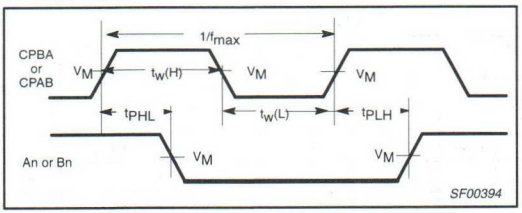
SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = −40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low An or Bn to CPAB or CPBA	Waveform 4	3.5 4.0			4.0 4.5		4.0 4.5		ns
t_h (H) t_h (L)	Hold time, high or low An or Bn to CPAB or CPBA	Waveform 4	0 0			0 0		0 0		ns
t_{su} (H) t_{su} (L)	Setup time, high or low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	5.0 5.0			5.0 5.0		5.0 5.0		ns
t_h (H) t_h (L)	Hold time, high or low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	0 0			0 0		0 0		ns
t_w (H) t_w (L)	Pulse width, high or low CPAB or CPBA	Waveform 1	4.0 3.5			4.5 4.0		4.5 4.0		ns

Note to AC setup requirements for 74F652A

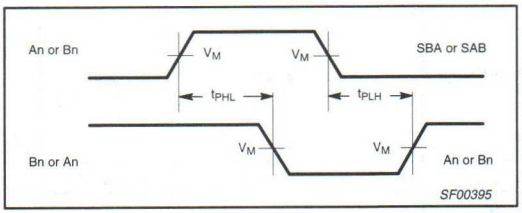
1. Setup time is to protect against surge current caused by enabling 16 outputs (48mA per output) simultaneously.

* *Discontinued part. Please see the Discontinued Product List.*

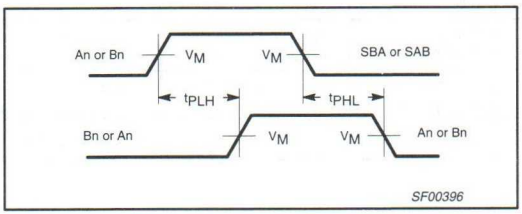
AC WAVEFORMS



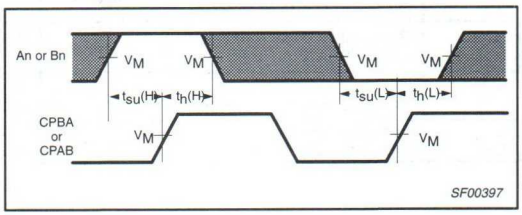
Waveform 1. Propagation delay for clock input to output, clock pulse width, and maximum clock frequency



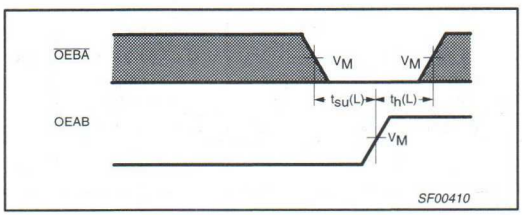
Waveform 2. Propagation delay for An to Bn or Bn to An and SAB or SBA to An or Bn



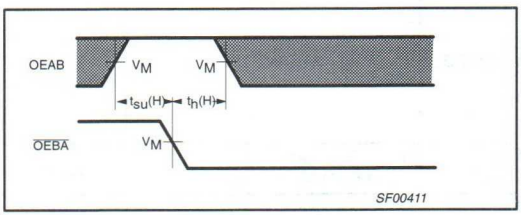
Waveform 3. Propagation delay for An to Bn or Bn to An and SAB or SBA to An or Bn



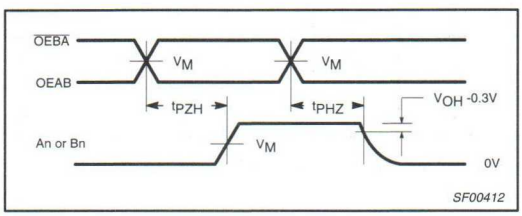
Waveform 4. Data setup time and hold times



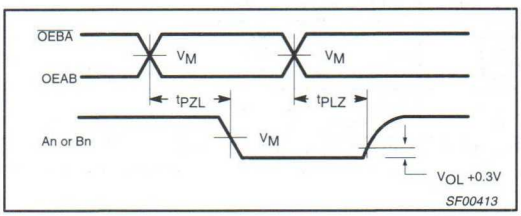
Waveform 5. $\overline{OEBA}$ to OEAB setup time and hold times



Waveform 6. OEAB to $\overline{OEBA}$ setup time and hold times



Waveform 7. 3-state output enable time to high level and output disable time from high level



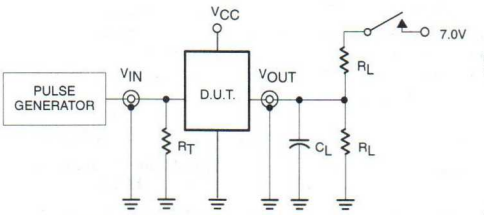
Waveform 8. 3-state output enable time to low level and output disable time from low level

Notes to AC waveforms

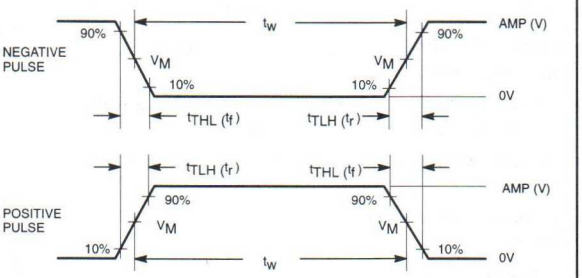
1. For all waveforms, $V_M = 1.5V$.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

* *Discontinued part. Please see the Discontinued Product List.*

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

* *Discontinued part. Please see the Discontinued Product List.*

Buffers/drivers

~~74F655A*~~
74F656A

74F655A Octal buffer/driver with parity, inverting (3-State)
74F656A Octal buffer/driver with parity, non-inverting (3-State)

FEATURES

- Significantly improved AC performance over 74F655 and 74F656
- High impedance NPN base input for reduced loading (40µA in High and Low states)
- Ideal in applications where high output drive and light bus loading are required (I_{IL} is 40µA vs. FAST std of 600µA)
- 74F655A combines 74F240 and 74F280A functions in one package
- 74F656A combines 74F244 and 74F280A functions in one package
- 74F655A Inverting
- 74F656A Non-inverting
- 3-State outputs sink 64mA and source 15mA
- 24-pin plastic Slim DIP (300mil) package
- Inputs on one side and outputs on the other side simplifies PC board layout
- Combined functions reduce part count and enhance system performance
- Industrial temperature range available (–40°C to +85°C)

DESCRIPTION

The 74F655A and 74F656A are octal buffers and line drivers with parity generation/checking designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers. These parts include parity generator/checker to improve PC board density.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F655A	6.5ns	64mA
74F656A	6.5ns	64mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	PKG DWG #
24-pin Plastic Slim DIP (300mil)	N74F656AN	I74F656AN	SOT222-1
24-pin Plastic SOL	N74F656AD	I74F656AD	SOT137-1

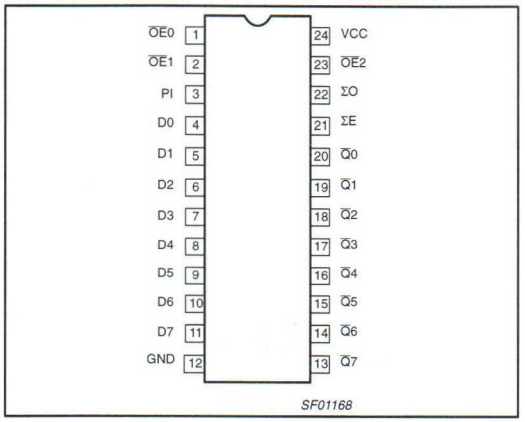
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0–D7	Data inputs	2.0/0.066	40µA/40µA
PI	Parity input	1.0/0.033	20µA/20µA
$\overline{OE}$0, $\overline{OE}$1, $\overline{OE}$2	Output Enable Inputs (active Low)	1.0/0.033	20µA/20µA
ΣE, ΣO	Parity outputs	750/106.7	15mA/64mA
$\overline{Q}$0–$\overline{Q}$7	Data outputs (74F655A)	750/106.7	15mA/64mA
Q0–Q7	Data outputs (74F656A)	750/106.7	15mA/64mA

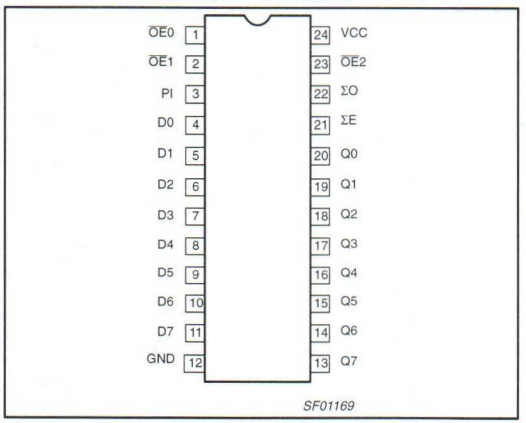
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

* *Discontinued part. Please see the Discontinued Products List.*

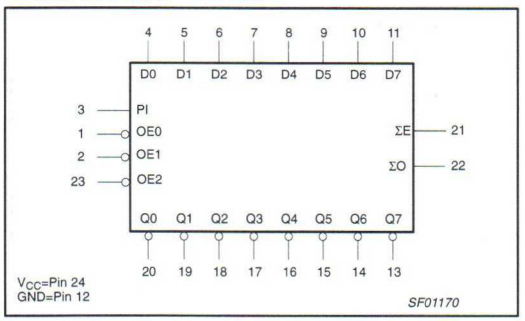
PIN CONFIGURATION – 74F655A



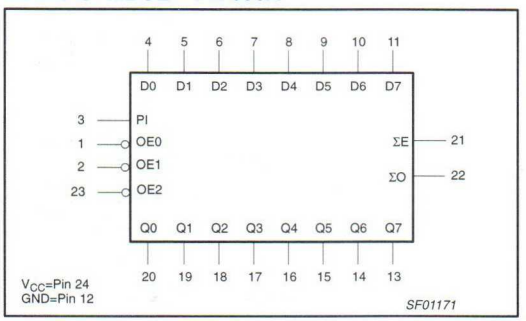
PIN CONFIGURATION – 74F656A



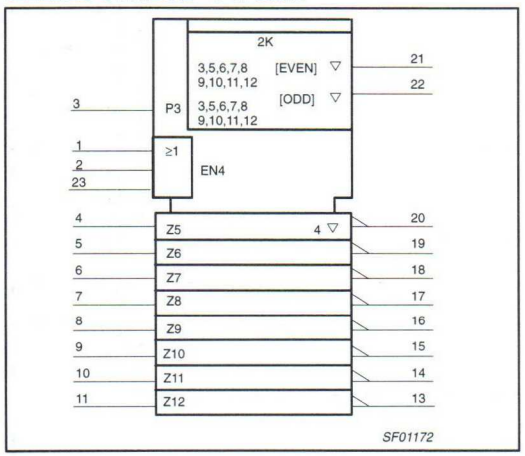
LOGIC SYMBOL – 74F655A



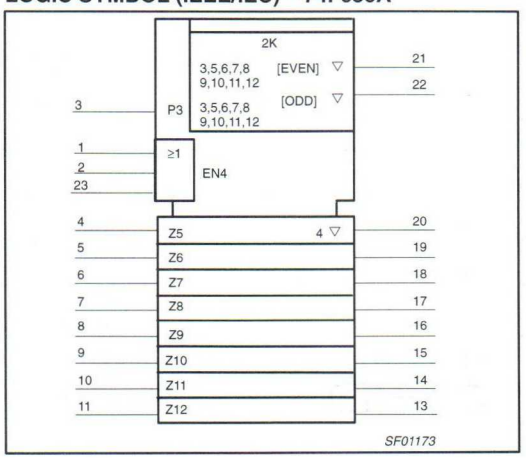
LOGIC SYMBOL – 74F656A



IEEE/IEC SYMBOL – 74F655A

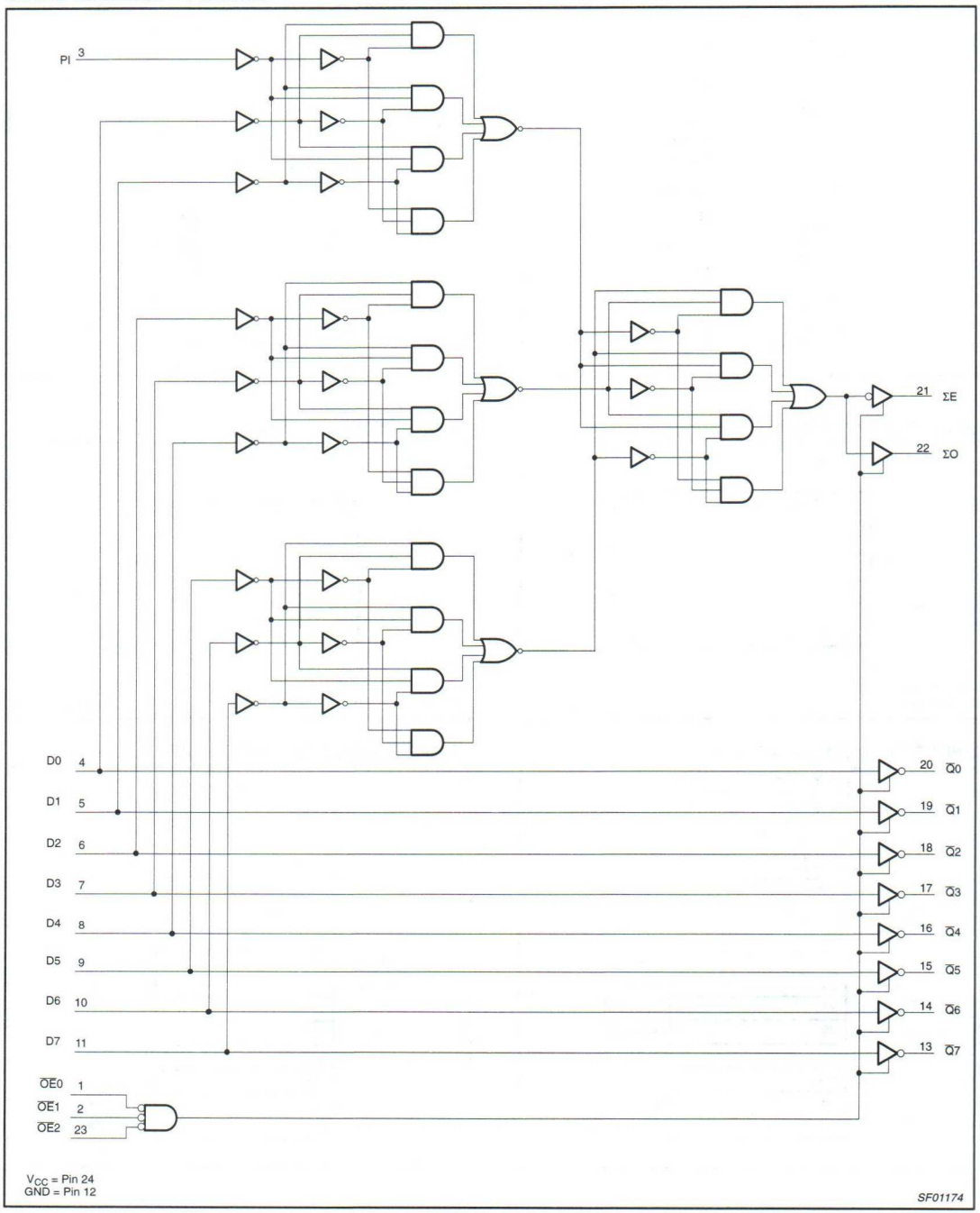


LOGIC SYMBOL (IEEE/IEC) – 74F656A



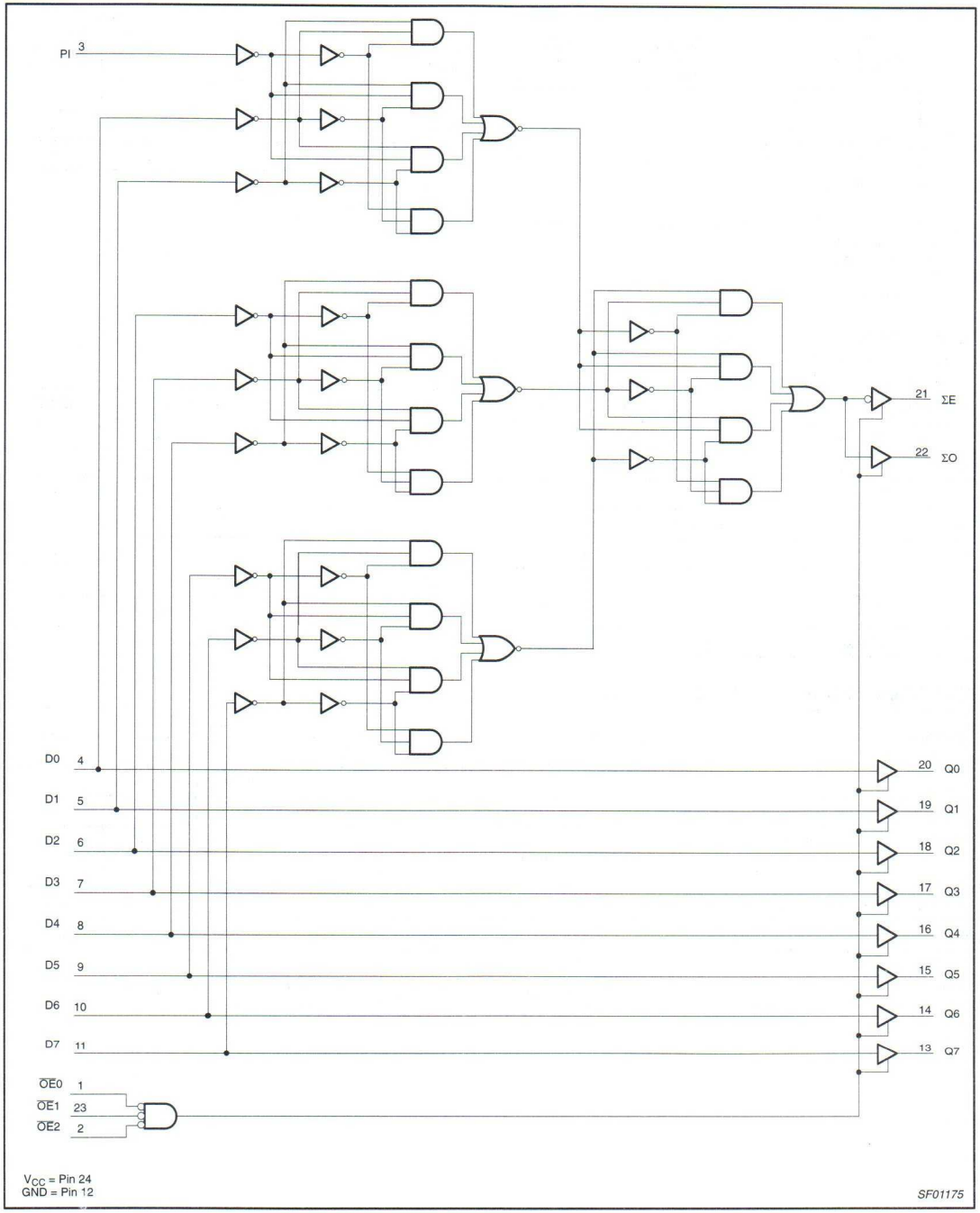
* *Discontinued part. Please see the Discontinued Products List.*

LOGIC DIAGRAM – 74F655A



* *Discontinued part. Please see the Discontinued Products List.*

LOGIC DIAGRAM – 74F656A



* *Discontinued part. Please see the Discontinued Products List.*

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE0}$	$\overline{OE1}$	$\overline{OE2}$	Dn	74F655A	74F656A
				$\overline{Qn}$	Qn
L	L	L	L	H	L
L	L	L	H	L	H
H	X	X	X	Z	Z
X	H	X	X	Z	Z
X	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

FUNCTION TABLE for PARITY OUTPUTS

INPUTS	PARITY OUTPUTS	
Number of inputs, High (PI, D0–D7)	ΣE	Σ0
Even - 0, 2, 4, 6, 8	H	L
Odd - 1, 3, 5, 7, 9	L	H
Any $\overline{OE}$n = High	Z	Z

H = High voltage level
L = Low voltage level
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state		128	mA
T_{amb}	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current				–15	mA
I_{OL}	Low-level output current				64	mA
T_{amb}	Operating free-air temperature range	Commercial range	0		70	°C
		Industrial range	–40		85	°C

** Discontinued part. Please see the Discontinued Products List.*

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.3		V
					I_{OH} = –15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 64mA	±10%V_{CC}			0.55	V
						±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0, V_I = 7.0V					100	µA
I_{IH}	High-level input current	Commercial range	Dn	V_{CC} = MAX, V_I = 2.7V					40	µA
			PI, $\overline{OE}$n						20	µA
		Industrial range	Dn						80	µA
			PI, $\overline{OE}$n						40	µA
I_{IL}	Low-level input current		Dn	V_{CC} = MAX, V_I = 0.5V					–40	µA
			PI, $\overline{OE}$n						–20	µA
I_{OZH}	Off-state current High-level voltage applied			V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state current Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			–100		–225	mA
I_{CC}	Supply current (total)		I_{CCH}	V_{CC} = MAX				50	80	mA
			I_{CCL}					78	110	mA
			I_{CCZ}					83	90	mA

NOTES:

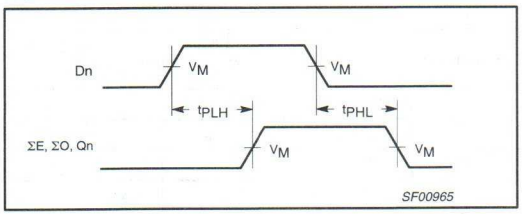
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

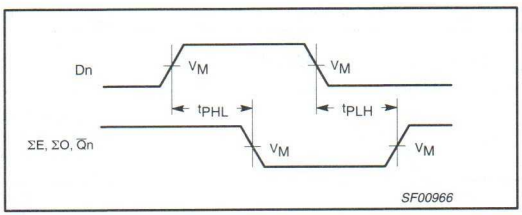
SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS: T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			LIMITS: T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		LIMITS: T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to $\overline{Q}$n	74F655A	Waveform 2	2.0 1.0	4.5 2.5	6.5 4.0	2.0 1.0	7.5 4.5	2.0 1.0	8.5 5.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	74F656A	Waveform 1	2.0 2.5	4.0 5.5	6.5 7.0	2.0 2.5	7.0 7.5	2.0 2.5	8.0 9.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Dn to ΣE, ΣO		Waveform 1, 2	5.5 5.5	10.0 11.0	13.0 14.5	5.5 5.5	14.0 16.5	4.5 5.5	16.5 18.0	ns ns
t_{PZH} t_{PZL}	Output enable time to High or Low level		Waveform 3 Waveform 4	3.5 4.0	7.0 8.0	10.5 11.0	3.5 4.5	11.5 12.0	3.0 4.0	13.0 13.5	ns ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level		Waveform 3 Waveform 4	1.5 2.0	4.5 5.0	8.0 8.0	1.5 2.0	9.0 9.0	1.5 1.5	10.0 10.0	ns ns

* *Discontinued part. Please see the Discontinued Products List.*

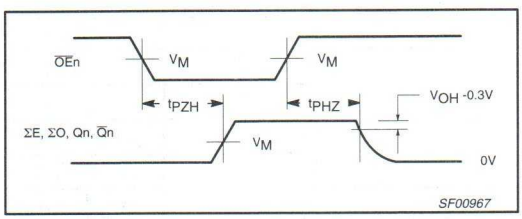
AC WAVEFORMS



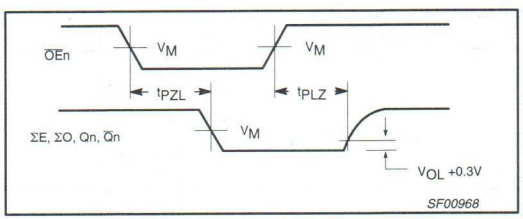
Waveform 1. Propagation Delay, Non-Inverting Outputs



Waveform 2. Propagation Delay, Inverting Outputs

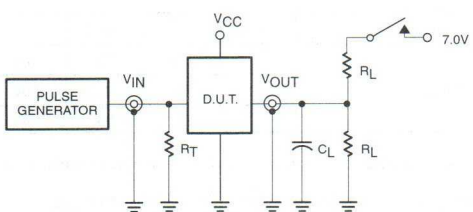


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

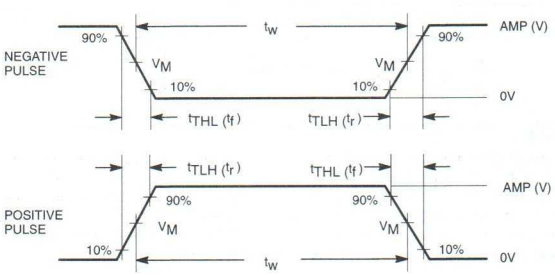


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

* *Discontinued part. Please see the Discontinued Products List.*

Octal transceiver with 8-bit parity generator/checker 74F657

FEATURES

- Combines 74F245 and 74F280A functions in one package
- High impedance base input for reduced loading (70μA in high and low states)
- Ideal in applications where high output drive and light bus loading are required (I_{IL} is 70μA vs FAST std of 600μA)
- 3–state buffer outputs sink 64mA and source 15mA
- Input diodes for termination effects
- 24–pin plastic slim DIP (300mil) package
- Industrial temperature range available (–40°C to +85°C)

DESCRIPTION

The 74F657 is an octal transceiver featuring non–inverting buffers with 3–state outputs and an 8–bit parity generator/checker, and is intended for bus–oriented applications. The buffers have a guaranteed current sinking capability of 24mA at the A ports and 64mA at the B ports. The transmit/receive (T/$\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active high) enables data from A ports to B ports; receive (active low) enables data from B ports to A ports. The output enable ($\overline{OE}$) input disables both the A and B ports by placing them in a high impedance condition when the $\overline{OE}$ input is high.

The parity select (ODD/$\overline{EVEN}$) input gives the user the option of odd or even parity systems.

The parity (PARITY) pin is an output from the generator/checker when transmitting from the port A to B (T/$\overline{R}$ = high) and an input when receiving from port B to A port (T/$\overline{R}$ = low).

When transmitting (T/$\overline{R}$ = high) the parity select (ODD/$\overline{EVEN}$) input is set, then the A port data is polled to determined the number of high bits. The parity (PARITY) output then goes to the logic state determined by the parity select (ODD/$\overline{EVEN}$) setting and by the number of high bits on port A.

For example, if the parity select (ODD/$\overline{EVEN}$) is set low (even parity), and the number of high bits on port A is odd, then the parity (PARITY) output will be high, transmitting even parity. If the number of high bits on port A is even, then the parity (PARITY) output will be low, keeping even parity.

When in receive mode (T/$\overline{R}$ = low) the B port is polled to determine the number of high bits. If parity select (ODD/$\overline{EVEN}$) is low (even parity) and the number of highs on port B is:

(1) odd and the parity (PARITY) input is high, then $\overline{ERROR}$ will be high, significantly no error.

(2) even and the parity (PARITY) input is high, then $\overline{ERROR}$ will be asserted low, indicating an error.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F657	8.0ns	100mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
24–pin plastic slim DIP (300mil)	N74F657N	I74F657N	SOT222-1
24–pin plastic SOL	N74F657D	I74F657D	SOT137-1
24–pin plastic SSOP	N74F657DB	I74F657DB	SOT340-1

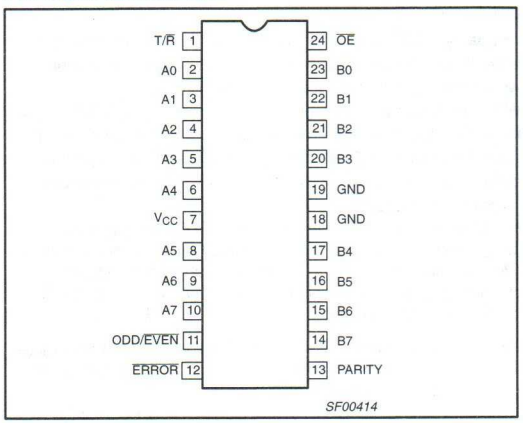
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A7	A ports 3–state inputs	3.5/0.117	70μA/70μA
B0 – B7	B ports 3–state inputs	3.5/0.117	70μA/70μA
PARITY	Parity input	3.5/0.117	70μA/70μA
T/$\overline{R}$	Transmit/receive input	2.0/0.066	40μA/40μA
ODD/$\overline{EVEN}$	Parity select input	1.0/0.033	20μA/20μA
$\overline{OE}$	Output enable input (active low)	2.0/0.066	40μA/40μA
A0 – A7	A ports 3–state outputs	150/40	3.0mA/24mA
B0 – B7	B ports 3–state outputs	750/106.7	15mA/64mA
PARITY	Parity output	750/106.7	15mA/64mA
$\overline{ERROR}$	Error output	750/106.7	15mA/64mA

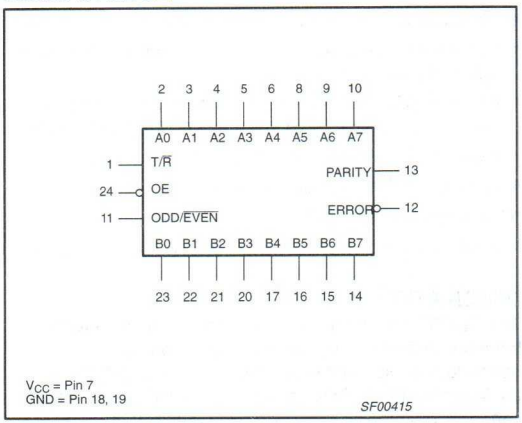
Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.

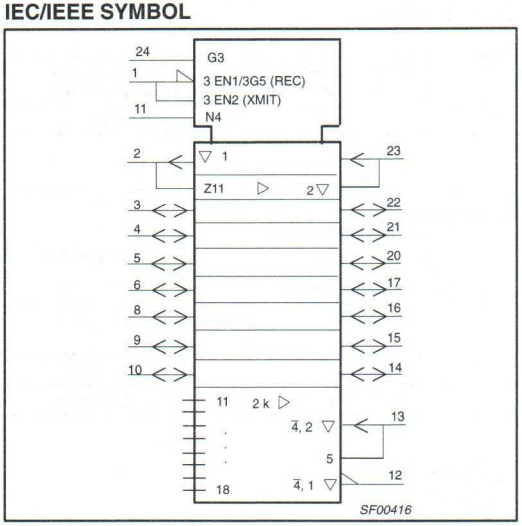
PIN CONFIGURATION



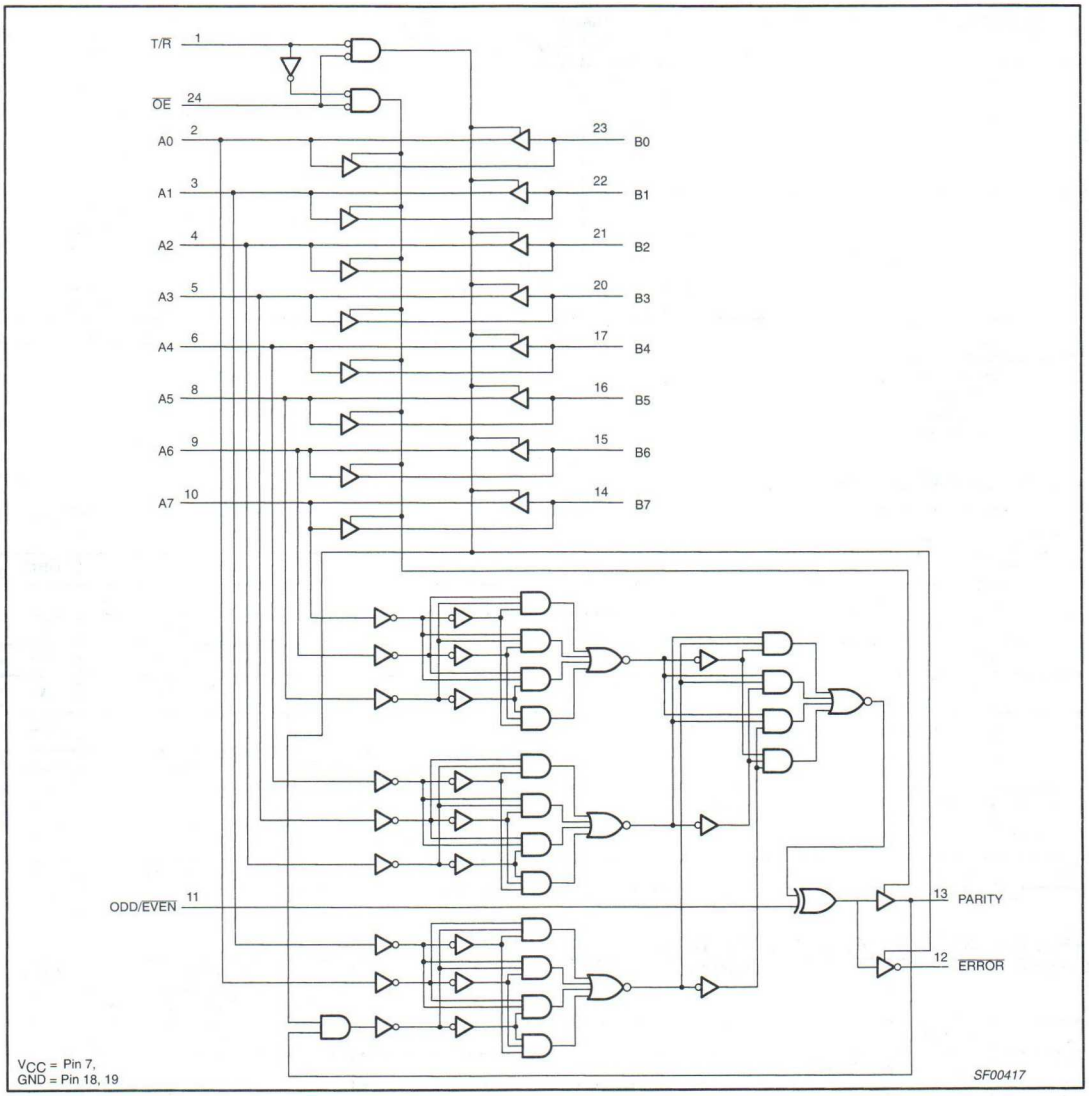
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

NUMBER OF INPUTS THAT ARE HIGH	INPUTS			INPUT/OUTPUT	OUTPUTS	
	$\overline{OE}$	T/$\overline{R}$	ODD/$\overline{EVEN}$	PARITY	$\overline{ERROR}$	OUTPUTS MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	Z

Notes to function table
1. H = High voltage level
2. L = Low voltage level
3. X = Don't care
4. Z = High impedance "'off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	A0 – A7	48	mA
		B0 – B7, PARITY, $\overline{ERROR}$	128	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current	A0 – A7			–3	mA
		B0 – B7, PARITY, $\overline{ERROR}$			–15	mA
I_{OL}	Low–level output current	A0 – A7			24	mA
		B0 – B7, PARITY, $\overline{ERROR}$			64	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage	All outputs	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA[4,5]	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7			V
		B0 – B7, PARITY, $\overline{ERROR}$		I_{OH} = –12mA[5]	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
				I_{OH} = –15mA[4]	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A0 – A7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA[4,5]	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B0 – B7, PARITY, $\overline{ERROR}$		I_{OL} = 48mA[4]	±10%V_{CC}		0.38	0.55	V
				I_{OL} = 48mA[5]	±5%V_{CC}		0.42	0.55	V
				I_{OL} = 64mA[4]	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{OE}$, T/$\overline{R}$, ODD/$\overline{EVEN}$	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A0 – A7	V_{CC} = 5.5V, V_I = 5.5V					2	mA
		B0 – B7						1	mA
I_{IH}	High–level input current	OOD/$\overline{EVEN}$	V_{CC} = MAX, V_I = 2.7V					20[4]	µA
								40[5]	µA
		$\overline{OE}$, T/$\overline{R}$						40[4]	µA
								80[5]	µA
I_{IL}	Low–level input current	OOD/$\overline{EVEN}$	V_{CC} = MAX, V_I = 0.5V					–20	µA
		$\overline{OE}$, T/$\overline{R}$						–40	µA
I_{OZH} + I_{IH}	Off–state output current, high–level voltage applied	A0 – A7, B0 – B7, PARITY	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{OZL} + I_{IL}	Off–state output current, low–level voltage applied		V_{CC} = MAX, V_O = 0.5V					–70	µA
I_{OZH}	Off–state output current, High–level voltage applied	$\overline{ERROR}$	V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off–state output current, low–level voltage applied		V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short circuit output current[3]	A0 – A7	V_{CC} = MAX			-60		-150	mA
		B0 – B7				-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				90	125[4]	mA
							90	135[5]	mA
		I_{CCL}					106	150[4]	mA
							106	160[5]	mA
		I_{CCZ}					98	145	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. For commercial range.
5. For industrial range.

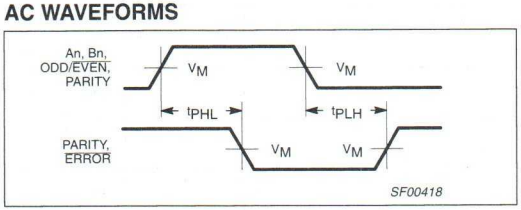
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = −40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	Waveform 2	2.5 3.0	5.5 6.0	7.5 7.5	2.5 3.0	8.0 8.0	2.0 2.5	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay An to PARITY	Waveform 1, 2	7.0 7.0	10.0 10.0	14.0 15.0	7.0 7.0	16.0 16.0	5.5 6.5	16.5 19.0	ns
t_{PLH} t_{PHL}	Propagation delay ODD/$\overline{EVEN}$ to PARITY, $\overline{ERROR}$	Waveform 1, 2	4.5 4.5	7.5 8.0	11.0 11.5	4.5 4.5	12.0 12.5	3.5 4.0	13.0 15.5	ns
t_{PLH} t_{PHL}	Propagation delay Bn to $\overline{ERROR}$	Waveform 1, 2	8.0 8.0	14.0 14.0	20.5 20.5	7.5 7.5	22.5 22.5	7.5 7.5	24.5 25.0	ns
t_{PLH} t_{PHL}	Propagation delay PARITY to $\overline{ERROR}$	Waveform 1, 2	8.0 8.0	11.5 12.0	15.5 15.5	7.5 8.0	16.5 17.0	6.5 6.5	18.5 20.0	ns
t_{PZH} t_{PZL}	Output enable time[1] to high or low level	Waveform 3, 4	3.0 4.0	5.5 7.0	8.0 9.5	3.0 4.0	9.0 11.0	2.0 4.0	9.0 13.0	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level	Waveform 3, 4	2.0 2.0	4.5 4.0	7.5 6.0	2.0 2.0	8.0 6.5	1.0 1.0	8.0 7.5	ns

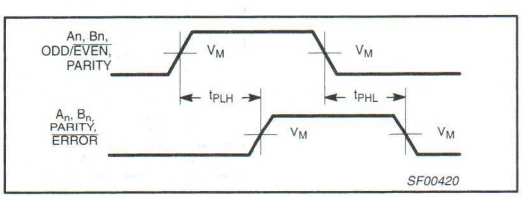
Note to AC electrical characteristics

1. These delay times reflect the 3-state recovery time only and not the signal through the buffers or the parity check circuitry. To assure VALID information at the $\overline{ERROR}$ pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the $\overline{ERROR}$ output. VALID data at the $\overline{ERROR}$ pin ≥ (B to A) + (A to PARITY).

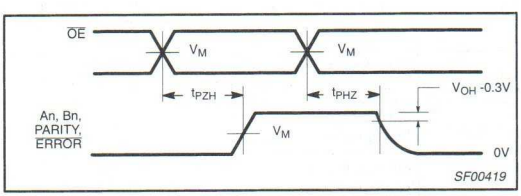
AC WAVEFORMS



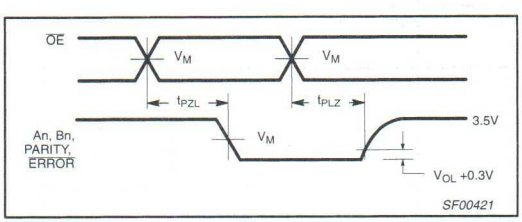
Waveform 1. Propagation delay for inverting outputs



Waveform 2. Propagation delay for non-Inverting outputs



Waveform 3. 3-state output enable time to high level and output disable time from high level

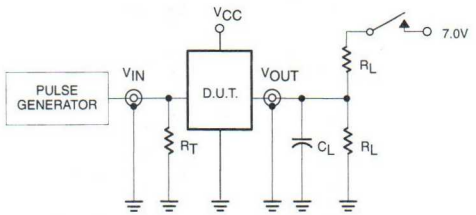


Waveform 4. 3-state output enable time to low level and output disable time from low level

Note to AC waveforms

1. For all waveforms, V_M = 1.5V.

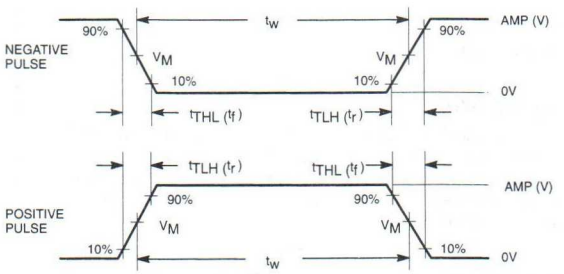
TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open



Input Pulse Definition

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

4 x 4 register file (3-State) — 74F670

FEATURES

- Simultaneous and Independent Read and Write operations
- Expandable to almost any word size and bit length
- 3-State outputs

DESCRIPTION

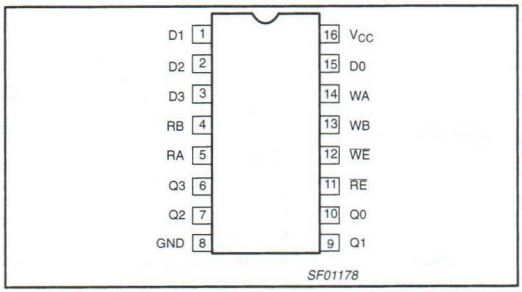
The 74F670 is a 16-bit 3-State Register File organized as 4 words of 4 bits each. Separate Read and Write Address and Enable inputs are available, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four data inputs.

The Write address inputs (WA and WB) determine the location of the stored word. The Write Address inputs should only be changed when the Write Enable input ($\overline{WE}$) is High for conventional operation. When the $\overline{WE}$ is Low, the data is entered into the addressed location.

The addressed location remains transparent to the data while the $\overline{WE}$ is Low. Data supplied at the inputs will be read out in true (non-inverting) form from the 3-State outputs. Data and address inputs are inhibited when the $\overline{WE}$ is High. Direct acquisition of data stored in any of the four registers is made possible by individual Read Address inputs (RA, RB). The addressed word appears at the four outputs when the Read Enable ($\overline{RE}$) is Low. Data outputs are in the high impedance "off" state when the $\overline{RE}$ is High. This permits outputs to be tied together to increase the word capacity to very large numbers.

Up to 128 devices can be stacked to increase the word size to 512 locations by tying the 3-State outputs together. Since the limiting factor for expansion is the output High current, further stacking is possible by tying pullup reisistors to the outputs to increase the I_{OH} current available. Design of the Read Enable signals for the stacked devices must ensure that there is no overlap in the Low levels which cause more than one output to be active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the Enable and address inputs of each device in parallel.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F670	6.5ns	50mA

ORDERING INFORMATION

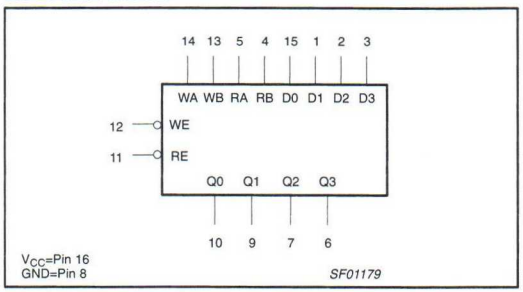
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
16-pin plastic DIP	N74F670N	SOT38-4
16-pin plastic SOL	N74F670D	SOT162-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

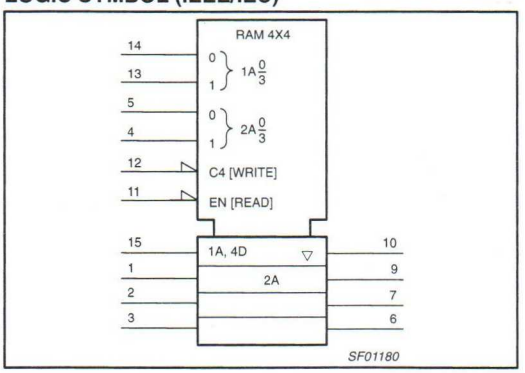
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 - D3	Data inputs	1.0/1.0	20µA/0.6mA
WA, WB	Write address inputs	1.0/1.0	20µA/0.6mA
RA, RB	Read address inputs	1.0/1.0	20µA/0.6mA
$\overline{WE}$	Write Enable inputs	1.0/1.0	20mA/0.6mA
$\overline{RE}$	Read Enable inputs	1.0/1.0	20mA/0.6mA
Q0–Q3	Data output	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



WORD SELECT FUNCTION TABLE

WRITE MODE		READ MODE		OPERATING MODE
WB	WA	RB	RA	Word Selected
L	L	L	L	Word 0
L	H	L	H	Word 1
H	L	H	L	Word 2
H	H	H	H	Word 3

H = High voltage level
L = Low voltage level

WRITE MODE FUNCTION TABLE

INPUTS		INTERNAL LATCHES*	OPERATING MODE
$\overline{WE}$	Dn		
L	L	L	Write data
L	H	H	
H	X	NC	Data latched

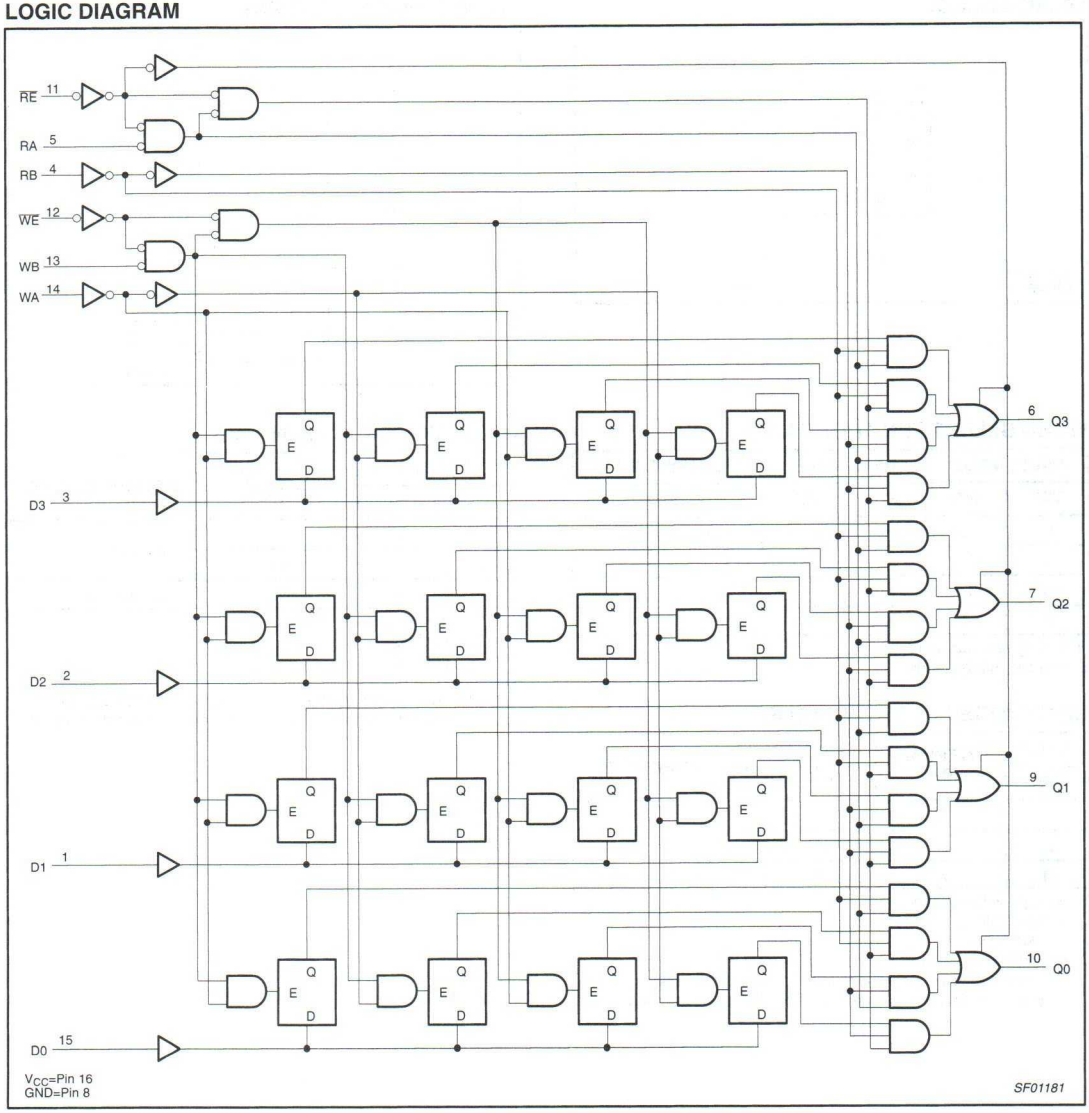
H = High voltage level
L = Low voltage level
NC= No change
X = Don't care
* = The write address (WA and WB) to the "internal latches" must be stabled while $\overline{WE}$ is Low for conventional operation.

READ MODE FUNCTION TABLE

INPUT	INTERNAL LATCHES*	OUTPUT	OPERATING MODE
$\overline{RE}$		Qn	
L	L	L	Read
L	H	H	
H	X	Z	Disabled

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state
* = The selection of "internal latches" by Read Address (RA and RB) are not constrained by $\overline{WE}$ or $\overline{RE}$ operation.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−3	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OZH}	Off state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				−50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			50	70	mA
		I_{CCL}				50	70	mA
		I_{CCZ}				55	80	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb}= +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay RA, RB to Qn	Waveform 3, 4	3.5 4.0	5.5 5.5	9.0 8.5	3.0 3.5	10.0 9.9	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{WE}$ to Qn	Waveform 1, 2	5.0 6.5	7.0 8.5	10.0 11.5	4.5 6.0	11.0 12.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	Waveform 1, 2	3.5 6.0	6.0 8.0	8.5 11.0	3.0 5.5	9.5 12.5	ns ns
t_{PZH} t_{PZL}	$\overline{RE}$ Enable time Qn to High or Low level	Waveform 5 Waveform 6	3.0 4.5	7.0 6.5	12.0 9.0	2.5 4.0	13.0 10.0	ns ns
t_{PHZ} t_{PLZ}	$\overline{RE}$ Disable time Qn to High or Low level	Waveform 5 Waveform 6	2.0 3.0	3.0 5.0	6.5 8.5	1.5 3.0	7.5 8.5	ns ns

AC SETUP REQUIREMENTS

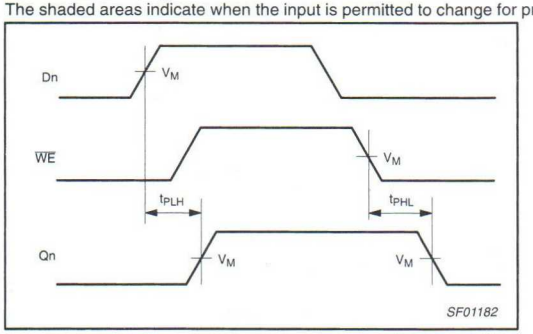
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low Dn to positive going $\overline{WE}$	Waveform 3, 4	1.5 6.0			1.5 7.0		ns ns
t_h(H) t_h(L)	Hold time, High or Low Dn to positive going $\overline{WE}$	Waveform 3, 4	0 1.0			0 1.0		ns ns
t_s(H) t_s(L)	Setup time, High or Low WA, WB to negative going WE[1]	Waveform 3, 4	0 0			0 0		ns ns
t_h(H) t_h(L)	Hold time, High or Low WA, WB to negative going WE[1]	Waveform 3, 4	0 0			0 0		ns ns
t_w(L)	$\overline{WE}$ Pulse width, Low	Waveform 3, 4	6.5			8.5		ns

NOTES:

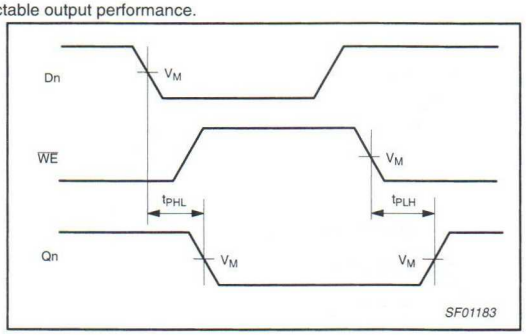
1. Write Address (WA, WB) setup time will protect the data written into the previous address. If protection of data in the previous address is not required, setup time for Write Address to $\overline{WE}$ can be ignored. Any address selection sustained for the final 7ns of the $\overline{WE}$ pulse during hold time for Write Address to $\overline{WE}$ will result in data being written into that location.

AC WAVEFORMS

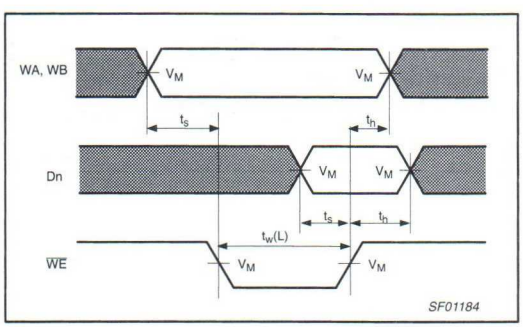
For all waveforms, V_M=1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



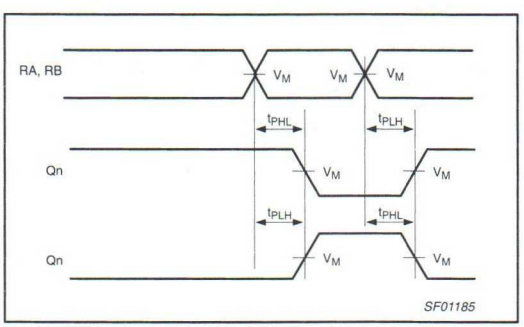
Waveform 1. Propagation Delay, Write Enable and Data to Outptus



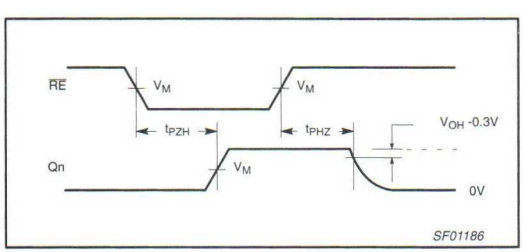
Waveform 2. Propagation Delay, Write Enable and Data to Outputs



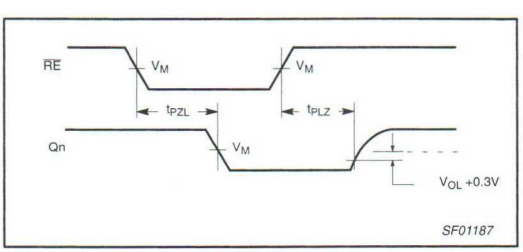
Waveform 3. Setup and Hold Times for Write Address to Write Enable and Data to Write Enable



Waveform 4. Propagation Delays for Read Address to Output

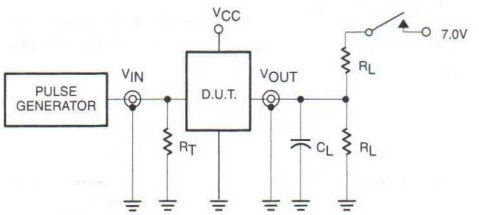


Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

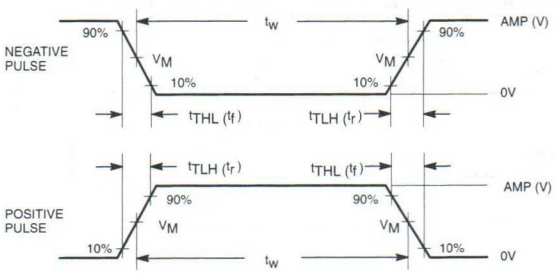


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

16-bit serial/parallel-in, serial-out shift register (3-State) 74F676

FEATURES

- 16-bit parallel-to-serial conversion
- 16-bit serial-in, serial-out
- Chip select control
- Power supply current 48mA typical
- Shift frequency 110MHz tyical
- Available in 300mil-wide 24-pin Slim DIP package

DESCRIPTION

The 74F676 contains 16 flip-flops with provision for synchronous parallel or serial entry and serial output. When the mode (M) input is High, information present on the parallel data (D0–D15) inputs is entered on the falling edge of the clock pulse ($\overline{CP}$) input signal. When M is Low, data is shifted out of the most significant bit position while information present on the serial (SI) input shifts into the least significant bit position. A High signal on the chip select ($\overline{CS}$) input prevents both parallel and serial operations.

The 16 bit shift register operates in one of three modes, as indicated in the shift register Function Table.

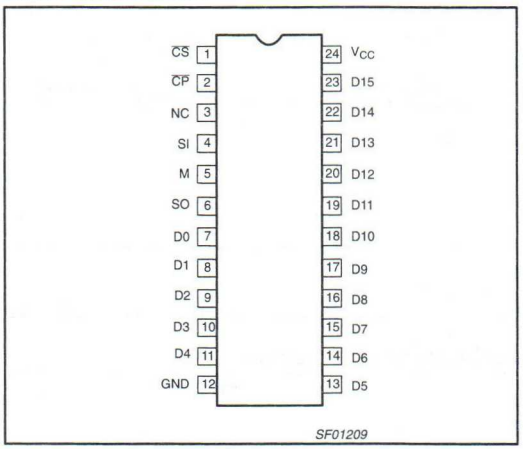
Hold: A High signal on the Chip Select ($\overline{CS}$) input prevents clocking and data is stored in the 16 registers.

Serial load: Data present on the SI pin shifts into the register on the falling edge of $\overline{CP}$. Data enters the Q0 position and shifts toward Q15 on successive clocks finally appearing on the SO pin.

Parallel load: Data present on D0–D15 is entered into the register on the falling edge of $\overline{CP}$. The SO output represents the Q15 register output.

To prevent false clocking, $\overline{CP}$ must be Low during a Low-to-High transition of $\overline{CS}$.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F676	110MHz	48mA

ORDERING INFORMATION

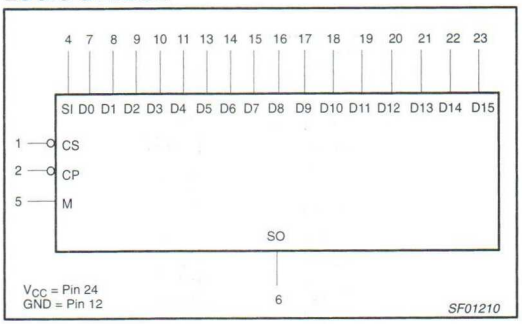
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
24-Pin Plastic Slim DIP (300mil)	N74F676N	SOT222-1
24-Pin Plastic SOL	N74F676D	SOT137-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

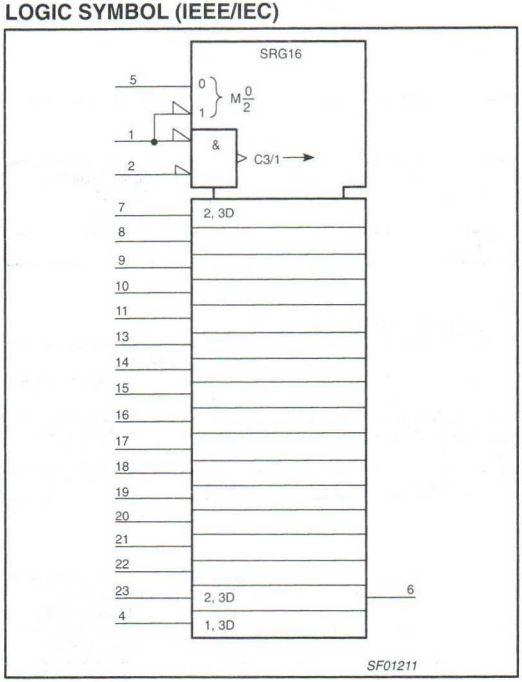
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0–D15	Parallel data inputs	1.0/1.0	20µA/0.6mA
SI	Serial data input	1.0/1.0	20µA/0.6mA
$\overline{CS}$	Chip Select input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CP}$	Clock Pulse input (active falling edge)	1.0/1.0	20µA/0.6mA
M	Mode select input	1.0/1.0	20µA/0.6mA
SO	Serial data output	50/33	1mA/20mA

NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

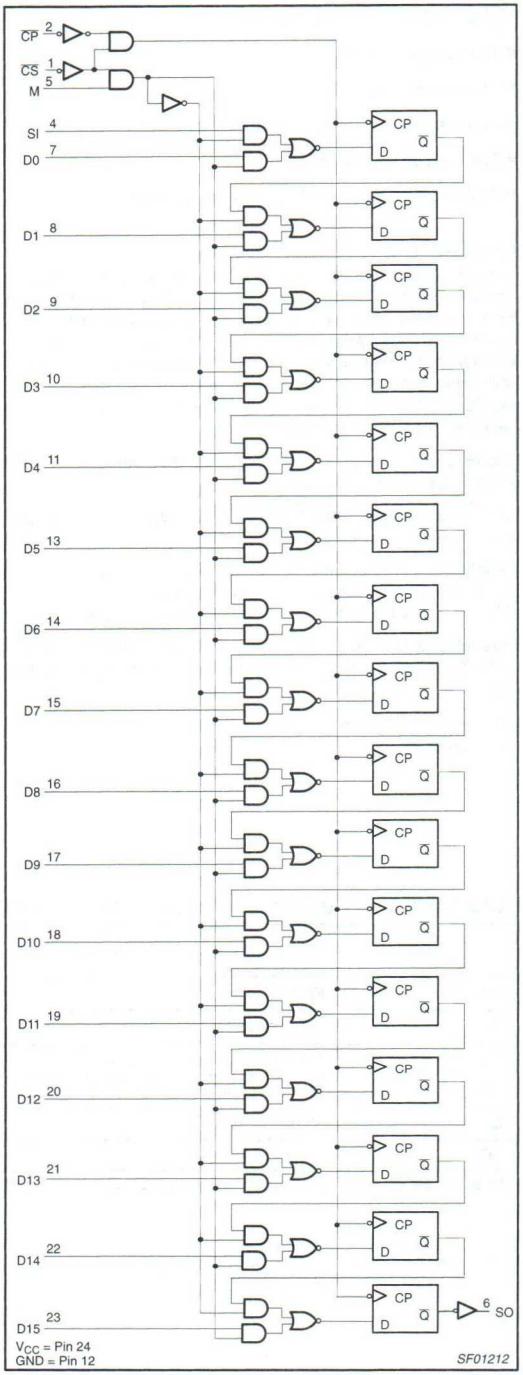


FUNCTION TABLE

CONTROL INPUTS			OPERATING MODE
$\overline{CS}$	M	$\overline{CP}$	
H	X	X	Hold
L	L	↓	Shift/Serial load
L	H	↓	Parallel load

H = High voltage level
L = Low voltage level
X = Don't care
↓ = High-to-Low transition of clock input

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
			±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			48	72	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	100	110		90		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to SO	Waveform 1	4.5 5.0	8.0 7.0	11.0 12.5	4.5 5.0	12.0 13.5	ns ns

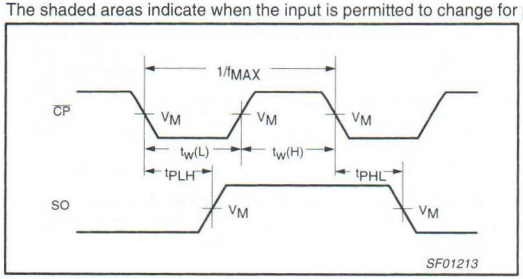
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low SI to $\overline{CP}$	Waveform 2	4.0 4.0			4.0 4.0		ns ns
t_h(H) t_h(L)	Hold time, High or Low SI to $\overline{CP}$	Waveform 2	4.0 4.0			4.0 4.0		ns ns
t_s(H) t_s(L)	Setup time, High or Low Dn to $\overline{CP}$	Waveform 2	3.0 3.0			3.0 3.0		ns ns
t_h(H) t_h(L)	Hold time, High or Low Dn to $\overline{CP}$	Waveform 2	4.0 4.0			4.0 4.0		ns ns
t_s(H) t_s(L)	Setup time, High or Low M to $\overline{CP}$	Waveform 2	8.0 8.0			8.0 8.0		ns ns
t_h(H) t_h(L)	Hold time, High or Low M to $\overline{CP}$	Waveform 2	2.0 2.0			2.0 2.0		ns ns
t_s(L)	Setup time, Low $\overline{CS}$ to $\overline{CP}$	Waveform 2	10.0			10.0		ns
t_h(H)	Hold time, High $\overline{CS}$ to $\overline{CP}$	Waveform 2	10.0			10.0		ns
t_w(H) t_w(L)	$\overline{CP}$ Pulse width, High or Low	Waveform 1	4.0 6.0			4.0 6.0		ns ns

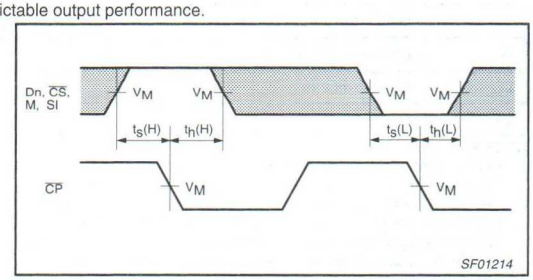
AC WAVEFORMS

For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

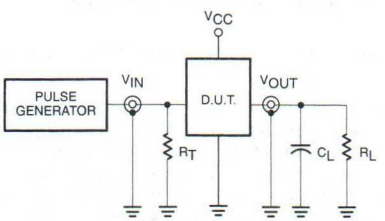


Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

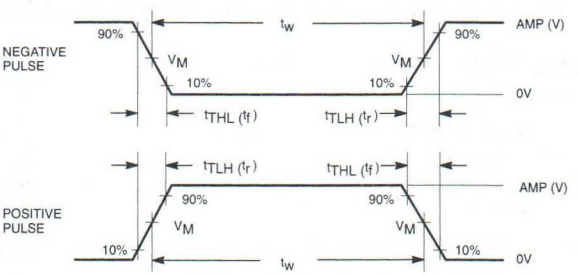


Waveform 2. Setup and Hold Times

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Multiplexers

74F711A/74F711–1/ 74F712A/74F712–1

74F711A Quint 2-to-1 Data Selector Multiplexer (3-State)
74F711-1 Quint 2-to-1 Data Selector Multiplexer with 30Ω Equivalent Output Termination Impedance (3-State)
74F712A Quint 3-to-1 Data Selector Multiplexer
74F712-1 Quint 3-to-1 Data Selector Multiplexer with 30Ω Equivalent Output Termination Impedance

FEATURES for 74F711A/74F711-1

- Consists of five 2-to-1 Multiplexers
- High impedance PNP base inputs for reduced loading (20µA in High and Low states)
- Designed for address multiplexing of dynamic RAM and other applications
- Output inverting/non-inverting option
- 30Ω termination impedance on each output – 74F711-1
- Outputs sink 64mA (74F711A only)

FEATURES for 74F712A/74F712-1

- Consists of five 3-to-1 Multiplexers
- High impedance PNP base inputs for reduced loading (20µA in High and Low states)
- Designed for address multiplexing of dynamic RAM and other applications
- 30Ω termination impedance on each output – 74F712-1
- Outputs sink 64mA (74F712A only)

DESCRIPTION

The 74F711A/74F711-1 consist of five 2-to-1 multiplexers designed for address multiplexing of dynamic RAMs and other multiplexing applications. The 74F711A has a common select (S) input, an Output Enable ($\overline{OE}$) input and an Output Inverting ($\overline{INV}$) input to control the 3-State outputs. The outputs source 15mA and sink 64mA. The 74F711-1 is the same as the 74F711A except that is has a 30Ω termination impedance on each output to reduce line noise and the 3-State outputs sink 5mA.

When the inverting input ($\overline{INV}$) is Low, the input data path is inverted.

To improve speed and noise immunity, V_{CC} and GND side pins are used.

The 74F712A/74F712-1 consist of five 3-to1 multiplexers designed for address multiplexing of dynamic RAMs and other multiplexing applications. The 74F712A has two select (S0, S1) inputs to determine which set of five inputs will be propagated to the five outputs. The outputs source 15mA and sink 64mA. The 74F712-1 is the same as the 74F712A except that it has a 30Ω termination impedance on each output to reduce line noise and the outputs sink 5mA.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F711A	6.0ns	30mA
74F711-1	6.5ns	29mA
74F712A	6.5ns	25mA
74F712-1	6.5ns	25mA

ORDERING INFORMATION

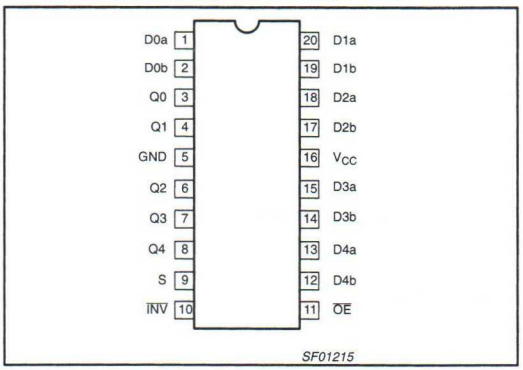
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ± 10% T_{amb} = 0° C to +70°C	PKG DWG #
20-Pin Plastic DIP	N74F711AN, N74F711-1N	SOT146-1
24-Pin Plastic Slim DIP (300 mil)	N74F712AN, N74F712-1N	SOT222-1
20-Pin Plastic SOL	N74F711AD, N74F711-1D	SOT163-1
24-Pin Plastic SOL	N74F712AD, N74F712-1D	SOT137-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

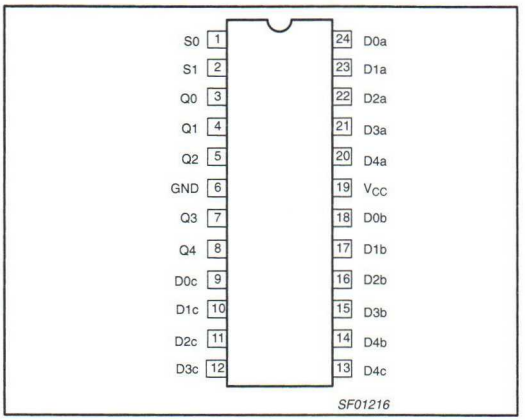
PINS		DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
74F711A/ 74F711-1	Dna, Dnb	Data inputs	1.0/0.066	20µA/40µA
	S	Select input	1.0/0.033	20µA/20µA
	$\overline{OE}$	Output Enable input (active Low)	1.0/0.033	20µA/20µA
	$\overline{INV}$	Output inverting input (active Low)	1.0/0.033	20µA/20µA
	Q0 - Q4	Data outputs for 74F711A	750/106.7	15mA/64mA
	Q0 - Q4	Data outputs for 74F711-1	750/8.33	15mA/5mA
74F712A/ 74F712-1	Dna, Dnb, Dnc	Data inputs	1.0/0.066	20µA/40µA
	S0, S1	Select inputs	1.0/0.033	20µA/20µA
	Q0 - Q4	Data outputs for 74F712A	750/106.7	15mA/64mA
	Q0 - Q4	Data outputs for 74F712-1	750/8.33	15mA/5mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

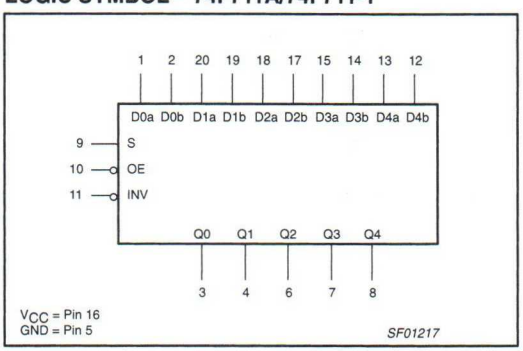
PIN CONFIGURATION – 74F711A/74F711-1



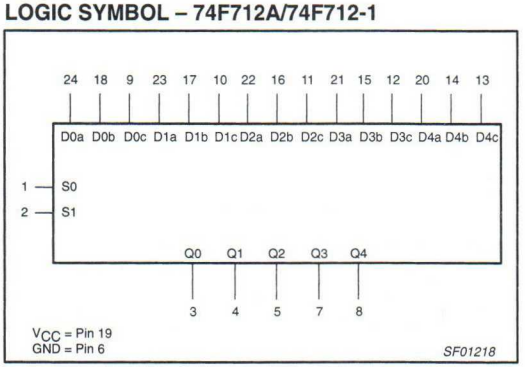
PIN CONFIGURATION – 74F712A/74F712-1



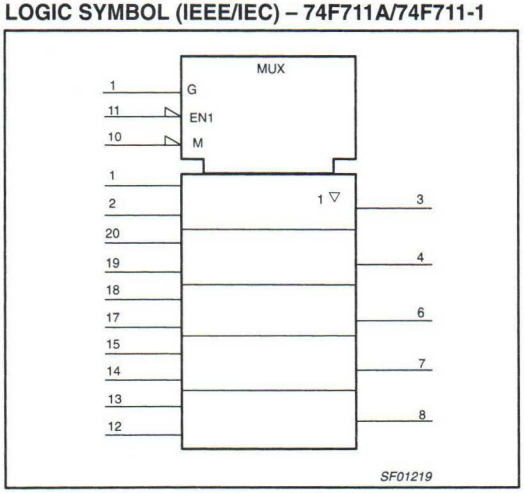
LOGIC SYMBOL – 74F711A/74F711-1



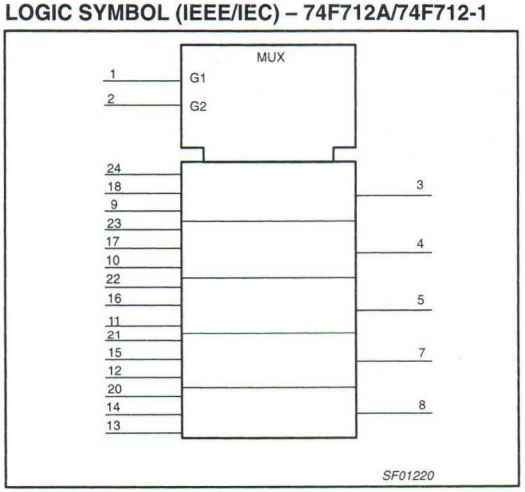
LOGIC SYMBOL – 74F712A/74F712-1



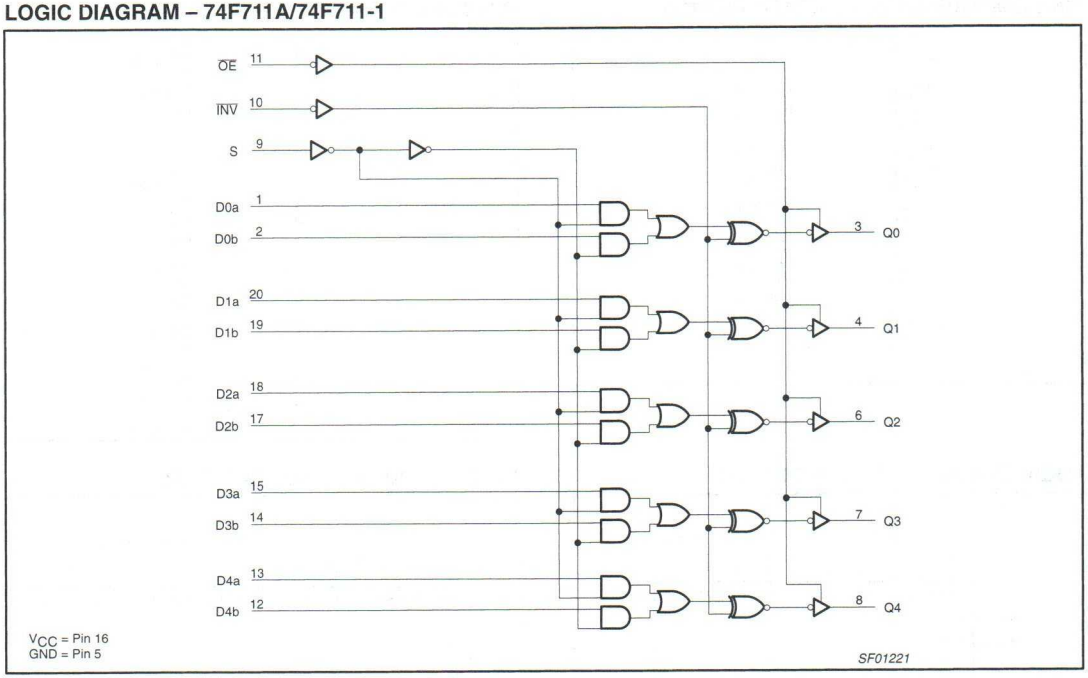
LOGIC SYMBOL (IEEE/IEC) – 74F711A/74F711-1



LOGIC SYMBOL (IEEE/IEC) – 74F712A/74F712-1



LOGIC DIAGRAM – 74F711A/74F711-1

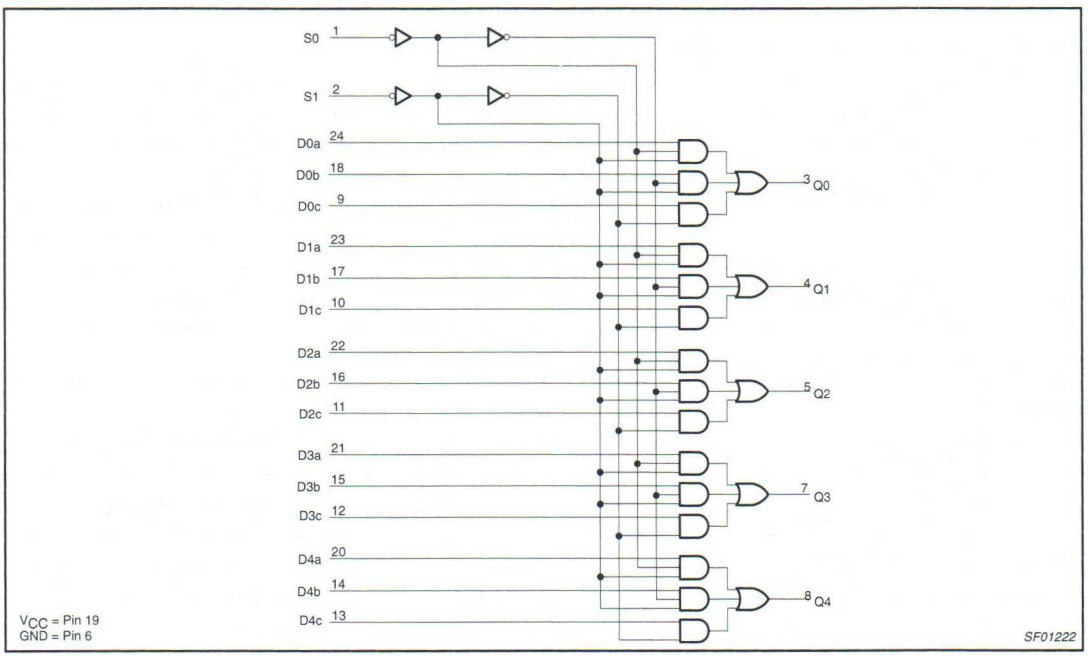


FUNCTION TABLE – 74F711A/74F711-1

INPUTS					OUTPUT
S	INV	OE	Dna	Dnb	Qn
L	L	L	Data a	Data b	$\overline{\text{Data a}}$
H	L	L	Data a	Data b	$\overline{\text{Data b}}$
L	H	L	Data a	Data b	Data a
H	H	L	Data a	Data b	Data b
X	X	H	X	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM – 74F712A/74F712-1



FUNCTION TABLE – 74F712A/74F712-1

INPUTS					OUTPUT
S0	**S1**	**Dna**	**Dnb**	**Dnc**	**Qn**
L	L	Data a	Data b	Data c	Data a
H	L	Data a	Data b	Data c	Data b
X	H	Data a	Data b	Data c	Data c

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	74F711A, 74F712A	96	mA
		74F711-1, 74F712-1	10	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current				–15	mA
I_{OL}	Low-level output current	74F711A, 74F712A			64	mA
		74F711-1, 74F712-1			5	mA
T_{amb}	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = –15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	74F711A/ 74F712A only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.38	0.55	V
					±5%V_{CC}		0.42	0.55	V
		74F711-1/ 74F712-1		I_{OL} = 5mA	±10%V_{CC}		0.38	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	Others	V_{CC} = MAX, V_I = 0.5V					–20	µA
		Dn only						–40	µA
I_{OZH}	Off-state output current High-level voltage applied	74F711A/ 74F711-1 only	V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short-circuit output current[3]	74F711-1/ 74F712-1	V_{CC} = MAX			–60		–150	mA
I_O	Output current[4]	74F711A/ 74F712A	V_{CC} = MAX, V_O = 2.25 V			–60		–150	mA
I_{CC}	Supply current (total)	74F711A	I_{CCH}	V_{CC} = MAX			25	35	mA
			I_{CCL}				33	46	mA
			I_{CCZ}				27	40	mA
		74F711-1	I_{CCH}	V_{CC} = MAX			26	40	mA
			I_{CCL}				33	45	mA
			I_{CCZ}				28	45	mA
		74F712A	I_{CCH}	V_{CC} = MAX			20	27	mA
			I_{CCL}				30	40	mA
		74F712-1	I_{CCH}	V_{CC} = MAX			20	30	mA
			I_{CCL}				29	40	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_O is tested under conditions that produce current approximity one half of the true short-circuit output current (I_{OS}).

AC ELECTRICAL CHARACTERISTICS – 74F711A/74F711-1

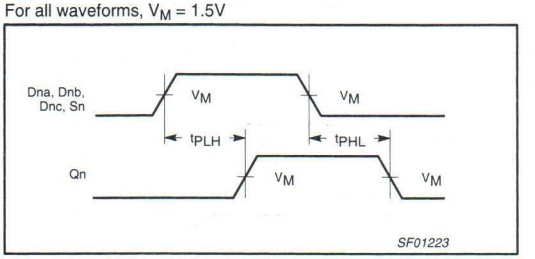
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C V_{CC} = 5V C_L = 50pF, R_L = 500Ω			T_{amb} = 0° C to +70°C V_{CC} = 5V ± 10% C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to Qn	74F711A	Waveform 1, 2	2.5 2.5	5.0 4.0	7.5 7.0	2.0 2.0	8.0 7.5	ns ns
t_{PLH} t_{PHL}	Propagation delay S to Qn		Waveform 1, 3	7.0 5.0	9.0 8.0	12.0 11.0	5.5 4.5	13.5 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{INV}$ to Qn		Waveform 1, 3	6.0 4.0	9.0 8.0	12.5 11.0	5.0 3.5	14.0 11.5	ns ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Qn		Waveform 4 Waveform 5	2.5 2.5	4.0 4.5	6.5 7.0	2.0 2.0	7.0 7.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Qn		Waveform 4 Waveform 5	2.5 3.0	4.0 5.0	7.0 8.0	2.0 2.5	8.0 8.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to Qn	74F711-1	Waveform 1, 2	3.0 2.0	4.5 4.5	7.5 7.5	2.0 2.5	9.0 8.0	ns ns
t_{PLH} t_{PHL}	Propagation delay S, $\overline{INV}$ to Qn		Waveform 1, 3	6.5 4.5	10.0 8.5	13.5 11.5	5.5 4.0	14.5 12.5	ns ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Qn		Waveform 4 Waveform 5	2.5 3.0	4.5 5.0	7.5 7.5	2.0 2.5	9.0 8.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Qn		Waveform 4 Waveform 5	2.0 3.5	4.5 5.5	7.0 8.5	2.0 3.0	8.0 9.5	ns ns

AC ELECTRICAL CHARACTERISTICS – 74F712A/74F712-1

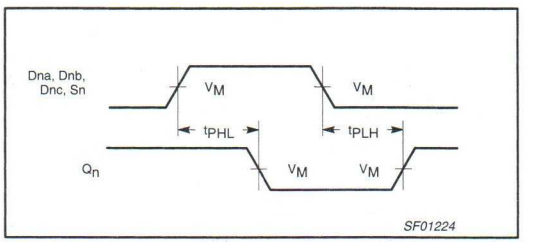
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C V_{CC} = 5V C_L = 50pF, R_L = 500Ω			T_{amb} = 0 to +70°C V_{CC} = 5V ± 10% C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb, Dnc to Qn	74F712A	Waveform 1, 2	2.0 2.0	3.5 3.5	6.5 6.5	2.0 2.0	7.0 7.0	ns ns
t_{PLH} t_{PHL}	Propagation delay S0, S1 to Qn		Waveform 1	6.5 5.0	8.0 7.5	11.5 10.0	5.5 4.5	13.5 11.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb, Dnc to Qn	74F712-1	Waveform 1, 2	2.0 2.0	4.0 4.0	7.0 7.0	2.0 2.0	7.5 7.5	ns ns
t_{PLH} t_{PHL}	Propagation delay S0, S1 to Qn		Waveform 1	7.0 5.5	9.0 7.5	12.0 10.5	6.0 5.5	13.5 11.0	ns ns

AC WAVEFORMS

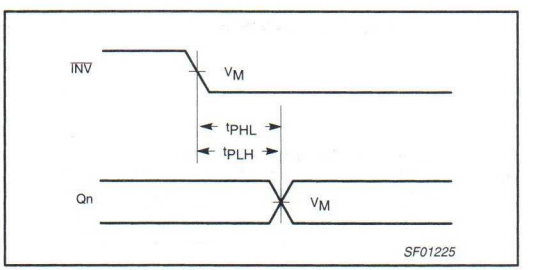
For all waveforms, $V_M = 1.5V$



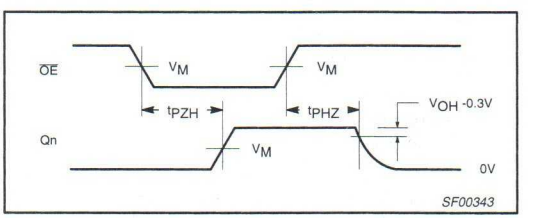
Waveform 1. Propagation Delay for Non-Inverting Output



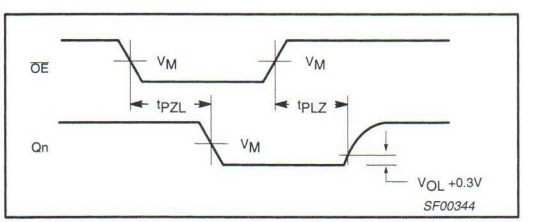
Waveform 2. Propagation Delay for Inverting Output



Waveform 3. Propagation Delay for $\overline{INV}$ to Output

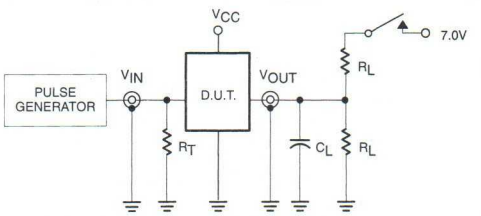


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

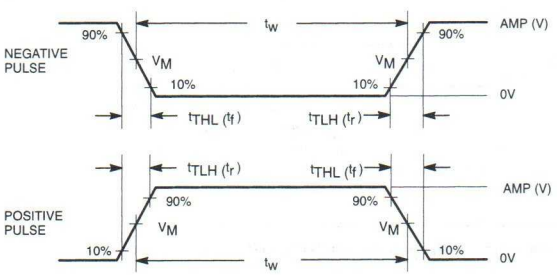


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

Multiplexers

74F723A/74F723–1/ 74F725A/74F725–1

74F723A Quad 3-to-1 Data Selector Multiplexer (3-State)
74F723-1 Quad 3-to-1 Data Selector Multiplexer with 30Ω Equivalent Output Termination Impedance (3-State)
74F725A Quad 4-to-1 Data Selector Multiplexer
74F725-1 Quad 4-to-1 Data Selector Multiplexer with 30Ω Equivalent Output Termination Impedance

FEATURES for 74F723A/74F723-1

- Consists of four 3-to-1 Multiplexers
- High impedance PNP base inputs for reduced loading (20μA in High and Low states)
- Inverting or non-inverting data path capability by an inverting ($\overline{INV}$) input
- Designed for address multiplexing of dynamic RAM and other applications
- Multiple side pins for V_{CC} and GND to reduce lead inductance (improves speed and noise immunity)
- 3-State outputs sink 64mA (74F723A only)
- 30Ω termination impedance on each output – 74F723-1

FEATURES for 74F725A/74F725-1

- Consists of four 4-to-1 Multiplexers
- High impedance PNP base inputs for reduced loading (20μA in High and Low states)
- Equivalent to two 74F253s without 3-State
- Outputs sink 64mA (74F725A only)
- 30Ω termination impedance on each output – 74F725-1

DESCRIPTION

The 74F723A/74F723-1 consist of four 3-to-1 multiplexers designed for address multiplexing of dynamic RAMs and other multiplexing applications. Select (S0, S1) inputs control which line is to be selected, as defined in the Function Table for 74F723A/74F723-1. When the invering input ($\overline{INV}$) is Low, the input data path is inverted.

To improve speed and noise immunity, V_{CC} and GND side pins are used. The 3-State outputs source 15mA and sink 64mA. The 74F723-1 is the same as 74F723A except that it has a 30Ω temination impedance on each output to reduce line noise and the 3-State outputs sink 5mA.

The 74F725A/74F725-1 consist of four 4-to1 multiplexers designed for general multiplexing purpose. The select (S0, S1) inputs control which line is to be selected, as defined in the Function Table for 74F725A/725-1. The outputs source 15mA and sink 64mA. The 74F725-1 is the same as the 74F725A except that it has a 30Ω termination impedance on each output to reduce line noise and the outputs sink 5mA.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F723A	5.5ns	25mA
74F723-1	7.0ns	26mA
74F725A	5.5ns	20mA
74F725-1	6.5ns	20mA

ORDERING INFORMATION

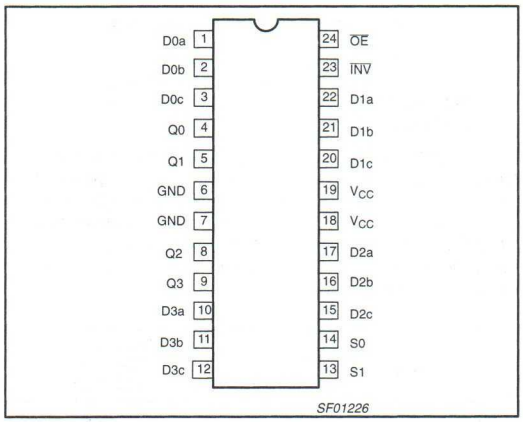
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ± 10% T_{amb} = 0° C to +70°C	PKG DWG #
20-Pin Plastic Slim DIP (300 mil)	N74F723AN, N74F723-1N, N74F725AN, N74F725-1N	SOT222-1
24-Pin Plastic SOL	N74F723AD, N74F723-1D, N74F725AD, N74F725-1D	SOT137-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

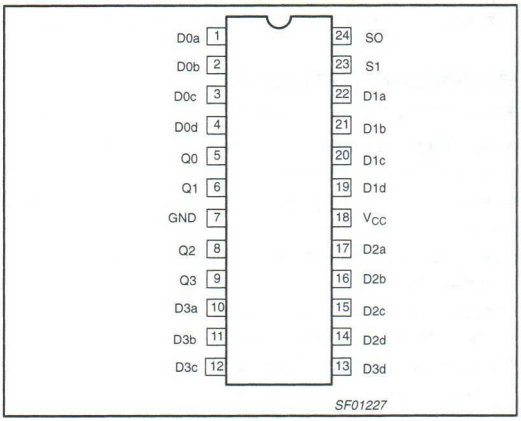
TYPE	PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
74F723A/ 74F723-1	Dna, Dnb, Dnc	Data inputs	1.0/0.066	20μA/40μA
	S0, S1	Select inputs	1.0/0.033	20μA/20μA
	$\overline{OE}$	Output Enable input	1.0/0.033	20μA/20μA
	$\overline{INV}$	Output inverting input	1.0/0.033	20μA/20μA
74F723A	Q0 - Q3	Data outputs for 74F723A	750/106.7	15mA/64mA
74F723-1	Q0 - Q3	Data outputs for 74F723-1	750/8.33	15mA/5mA
74F725A/ 74F725-1	Dna, Dnb, Dnc, Dnd	Data inputs	1.0/0.066	20μA/40μA
	S0, S1	Select inputs	1.0/0.033	20μA/20μA
74F725A	Q0 - Q3	Data outputs	750/106.7	15mA/64mA
74F725-1	Q0 - Q3	Data outputs	750/8.33	15mA/5mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

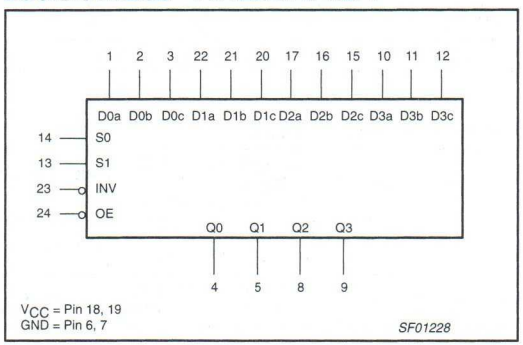
PIN CONFIGURATION – 74F723A/74F723-1



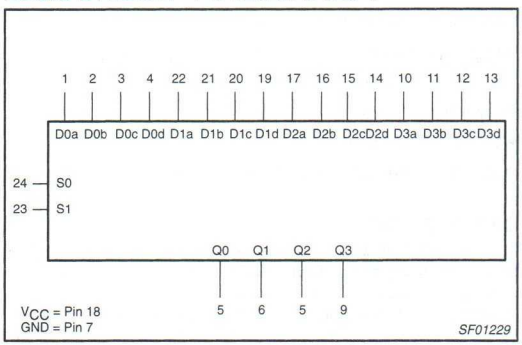
PIN CONFIGURATION – 74F725A/74F725-1



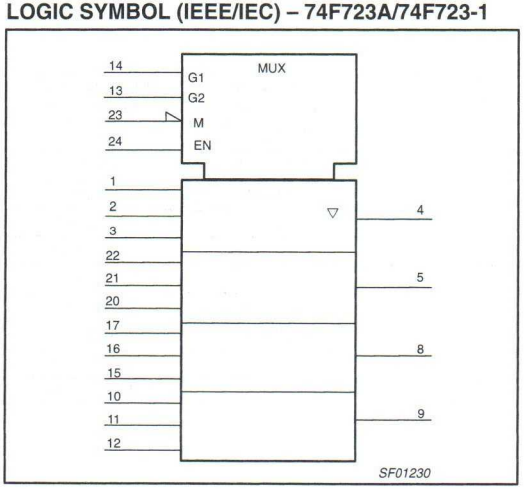
LOGIC SYMBOL – 74F723A/74F723-1



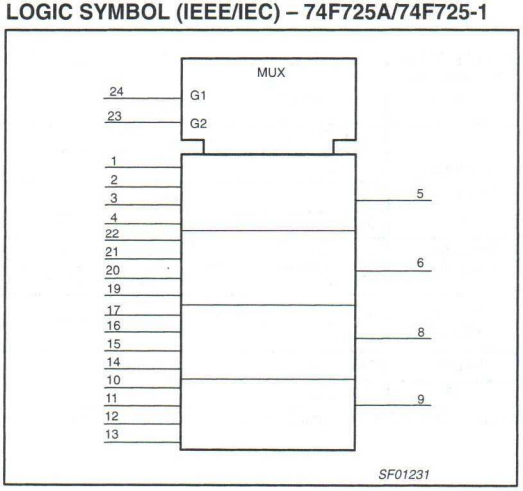
LOGIC SYMBOL – 74F725A/74F725-1



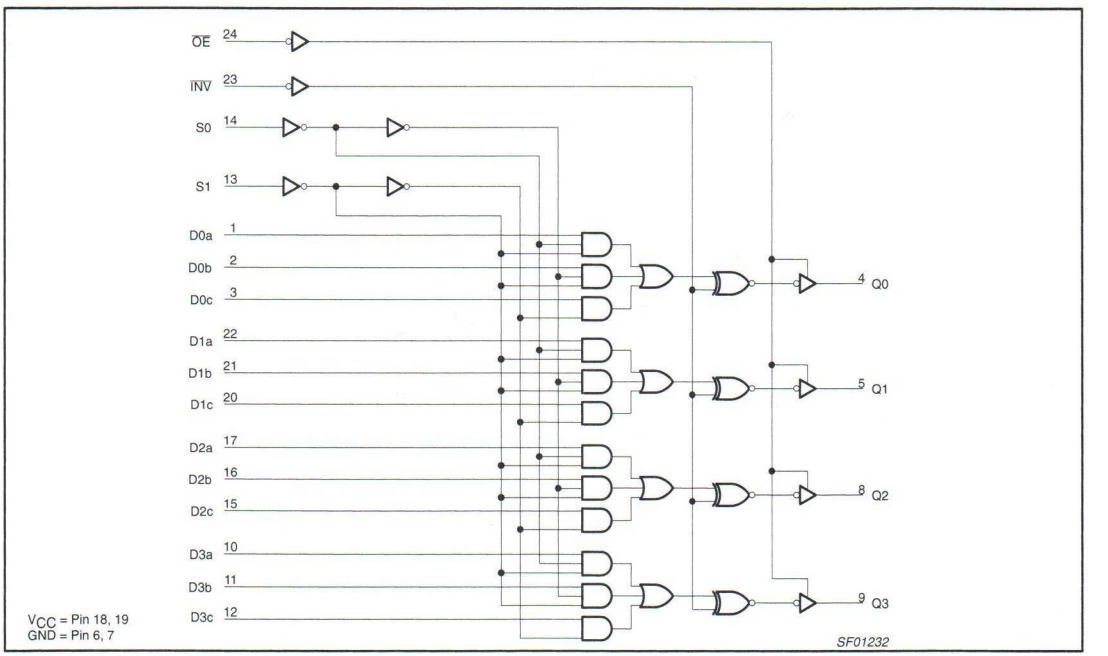
LOGIC SYMBOL (IEEE/IEC) – 74F723A/74F723-1



LOGIC SYMBOL (IEEE/IEC) – 74F725A/74F725-1



LOGIC DIAGRAM – 74F723A/74F723-1

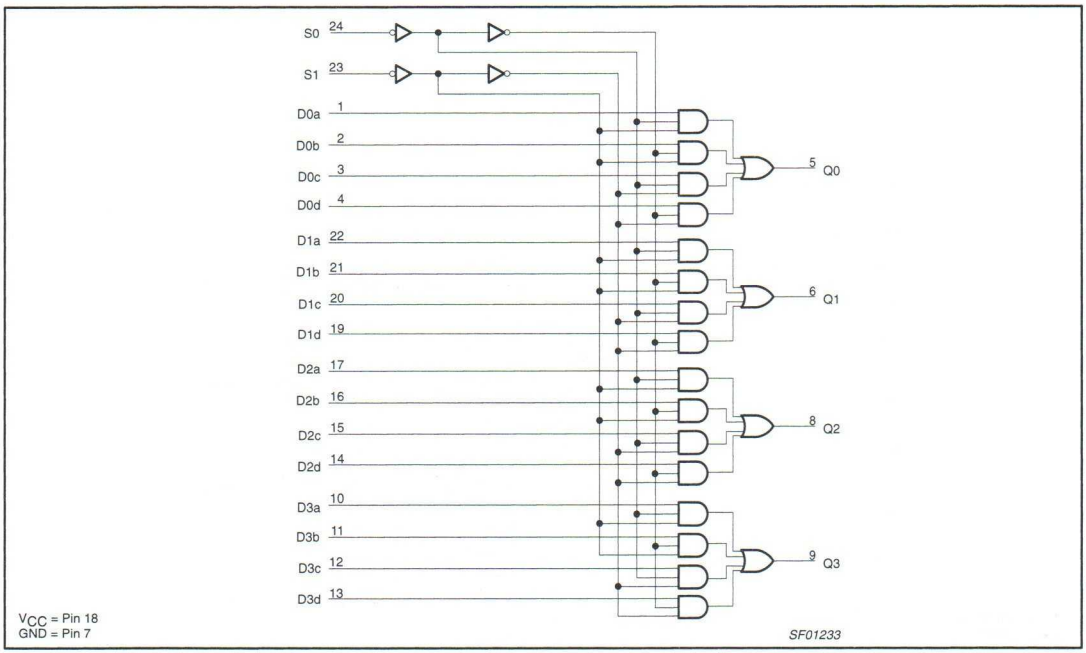


FUNCTION TABLE – 74F723A/74F723-1

INPUTS							OUTPUT
S0	S1	$\overline{INV}$	$\overline{OE}$	Dna	Dnb	Dnc	Qn
L	L	L	L	Data a	Data b	Data c	$\overline{Data\ a}$
L	L	H	L	Data a	Data b	Data c	Data a
H	L	L	L	Data a	Data b	Data c	$\overline{Data\ b}$
H	L	H	L	Data a	Data b	Data c	Data b
X	H	L	L	Data a	Data b	Data c	$\overline{Data\ c}$
X	H	H	L	Data a	Data b	Data c	Data c
X	X	X	H	X	X	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM – 74F725A/74F725-1



FUNCTION TABLE – 74F725A/74F725-1

INPUTS						OUTPUT
S0	S1	Dna	Dnb	Dnc	Dnd	Qn
L	L	Data a	Data b	Data c	Data d	Data a
H	L	Data a	Data b	Data c	Data d	Data b
L	H	Data a	Data b	Data c	Data d	Data c
H	H	Data a	Data b	Data c	Data d	Data d

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	74F723-1, 74F725-1	10	mA
		74F723A, 74F725A	96	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current				–15	mA
I_{OL}	Low-level output current	74F723-1, 74F725-1			5	mA
		74F723A, 74F725A			64	mA
T_{amb}	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = –15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	74F723-1/ 74F725-1	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 5mA	±10%V_{CC}		0.38	0.50	V
					±5%V_{CC}		0.38	0.50	V
		74F723A/ 74F725A		I_{OL} = MAX	±10%V_{CC}		0.38	0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	Others	V_{CC} = MAX, V_I = 0.5V					–20	µA
		Dn only						–40	µA
I_{OZH}	Off-state output current High-level voltage applied	74F723A/ 74F723-1 only	V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short-circuit output current[3]	74F723-1/ 74F725-1	V_{CC} = MAX			–60		–150	mA
I_O	Output current[4]	74F723A/ 74F725A	V_{CC} = MAX, V_O = 2.25V			–60		–150	mA
I_{CC}	Supply current (total)	74F723A	I_{CCH}	V_{CC} = MAX			23	30	mA
			I_{CCL}				29	40	mA
			I_{CCZ}				25	40	mA
		74F723-1	I_{CCH}	V_{CC} = MAX			23	35	mA
			I_{CCL}				29	40	mA
			I_{CCZ}				26	40	mA
		74F725A	I_{CCH}	V_{CC} = MAX			16	25	mA
			I_{CCL}				24	35	mA
		74F725-1	I_{CCH}	V_{CC} = MAX			17	25	mA
			I_{CCL}				25	35	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_O is tested under conditions that produce current approximity one half of the true short-circuit output current (I_{OS}).

AC ELECTRICAL CHARACTERISTICS – 74F723A/74F723-1

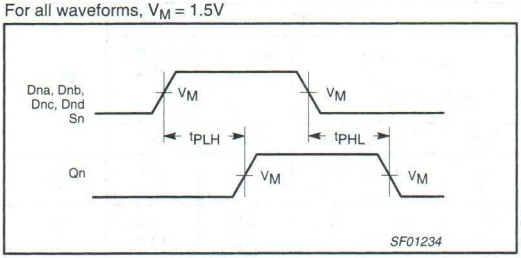
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0° C to +70°C, V_{CC} = 5V ± 10%, C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb, Dnc to Qn	74F723A	Waveform 1, 2	2.5 2.0	5.0 4.5	8.0 7.0	2.0 2.0	8.5 7.5	ns ns
t_{PLH} t_{PHL}	Propagation delay S0, S1, $\overline{INV}$ to Qn		Waveform 1, 3	6.5 4.0	9.0 7.5	12.5 11.0	4.0 3.5	14.0 12.0	ns ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Qn		Waveform 4 Waveform 5	2.0 2.5	4.0 4.5	6.5 7.0	2.0 2.0	7.5 7.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Qn		Waveform 4 Waveform 5	2.5 3.0	4.0 5.0	7.0 7.5	2.0 2.5	7.5 8.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb, Dnc to Qn	74F723-1	Waveform 1, 2	2.5 2.5	6.0 5.0	8.5 8.0	2.5 2.0	9.5 8.0	ns ns
t_{PLH} t_{PHL}	Propagation delay S0, S1, $\overline{INV}$ to Qn		Waveform 1, 3	7.0 5.0	10.0 9.0	14.0 12.5	6.0 4.5	16.0 13.5	ns ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Qn		Waveform 4 Waveform 5	3.0 3.0	4.5 5.0	7.5 7.5	2.5 3.0	8.0 8.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Qn		Waveform 4 Waveform 5	2.5 4.0	4.5 6.0	7.0 8.5	2.0 3.0	8.0 9.5	ns ns

AC ELECTRICAL CHARACTERISTICS – 74F725A/74F725-1

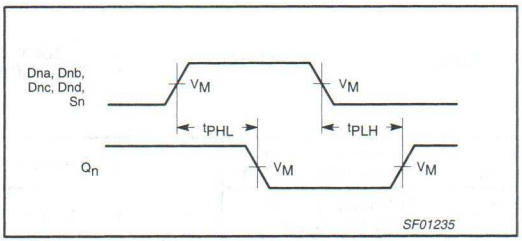
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0 to +70°C, V_{CC} = 5V ± 10%, C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb, Dnc, Dnd to Qn	74F725A	Waveform 1, 2	2.0 2.0	3.5 3.5	6.5 6.5	2.0 2.0	7.0 6.5	ns ns
t_{PLH} t_{PHL}	Propagation delay S0, S1 to Qn		Waveform 1	6.0 5.0	8.5 7.0	11.5 10.0	5.5 4.5	13.5 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb, Dnc, Dnd to Qn	74F725-1	Waveform 1, 2	2.0 2.0	4.0 4.0	7.0 6.5	2.0 2.0	7.5 7.5	ns ns
t_{PLH} t_{PHL}	Propagation delay S0, S1 to Qn		Waveform 1	6.5 5.0	9.0 8.5	12.0 10.5	5.5 5.0	14.0 11.0	ns ns

AC WAVEFORMS

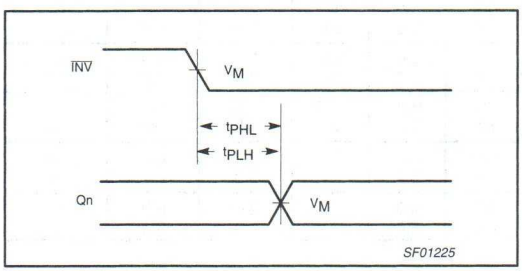
For all waveforms, $V_M = 1.5V$



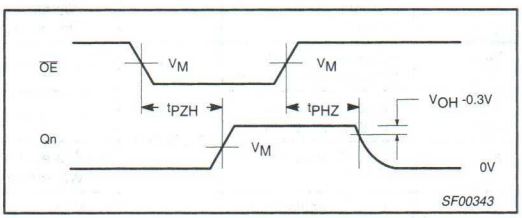
Waveform 1. Propagation Delay for Non-Inverting Output



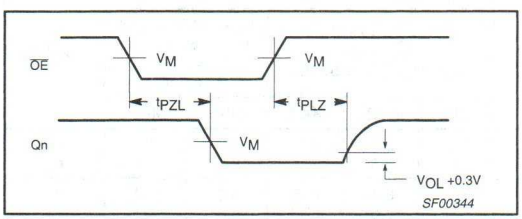
Waveform 2. Propagation Delay for Inverting Output



Waveform 3. Propagation Delay for $\overline{INV}$ to Output

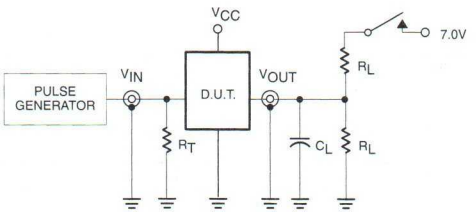


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

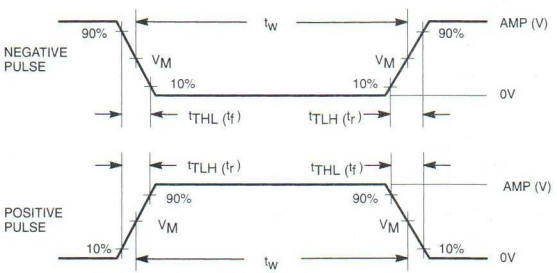


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

74F756 Octal Inverter Buffer (Open Collector)
74F757 Octal Buffer (Open Collector)
74F760 Octal Buffer (Open Collector)

FEATURES

- Octal bus interface
- Open collector versions of 74F240, 74F241 and 74F244

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F756	9.0ns	40mA
74F757	9.0ns	45mA
74F760	9.0ns	45mA

DESCRIPTION

The 74F756, 74F757 and 74F760 are octal buffers that are ideal for driving bus lines of buffer memory address registers. The 74F756 is the open collector version of 74F240, 74F757 is the open collector version of 74F241 and 74760 is the open collector version of 74F244. These devices feature two Output Enables. $\overline{OE}a$ and $\overline{OE}b$ (or OEb for the 74F757), each controlling four of the outputs.

ORDERING INFORMATION

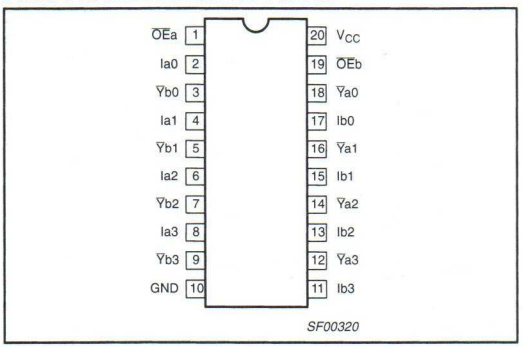
DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
20–pin plastic DIP	N74F756N, N74F757AN, N74F760N	SOT146-1
20–pin plastic SOL	N74F756D, N74F757AD, N74F760D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

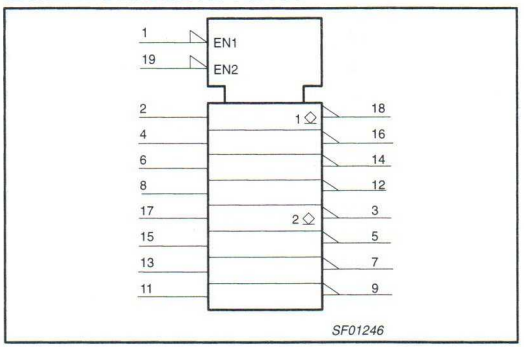
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ian, Ibn	Data inputs	1.0/1.67	20µA/1.0mA
$\overline{OE}a$, $\overline{OE}b$	Output enable input (active Low)	1.0/1.67	20µA/0.2mA
OEb	Output enable input (active High 74F757)	1.0/1.67	20µA/1.0mA
Yan, Ybn	Data outputs (74F757, 74F760)	OC/106.7	OC/64mA
$\overline{Y}an$, $\overline{Y}bn$	Data outputs (74F756)	OC/106.7	OC/64mA

Notes:
One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the Low state.
OC=Open Collector

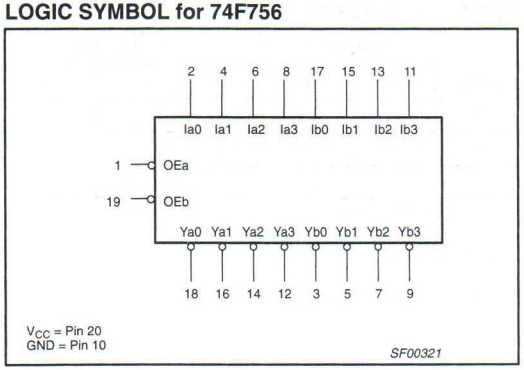
PIN CONFIGURATION for 74F756



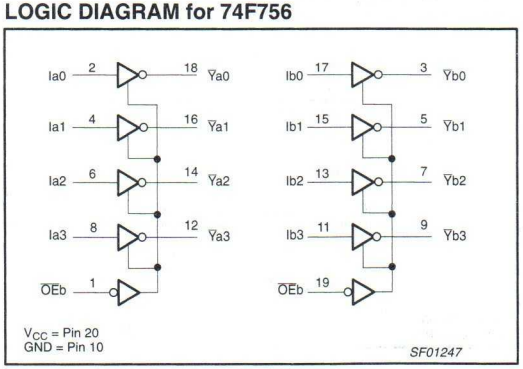
IEC/IEEE SYMBOL for 74F756



LOGIC SYMBOL for 74F756



LOGIC DIAGRAM for 74F756

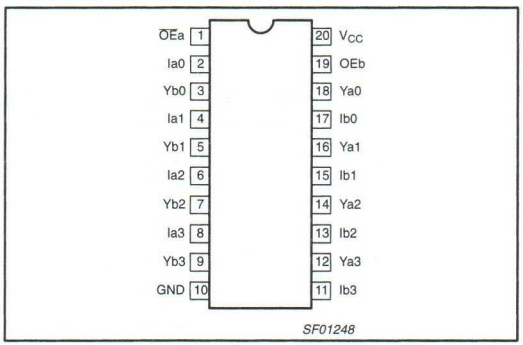


FUNCTION TABLE for 74F756

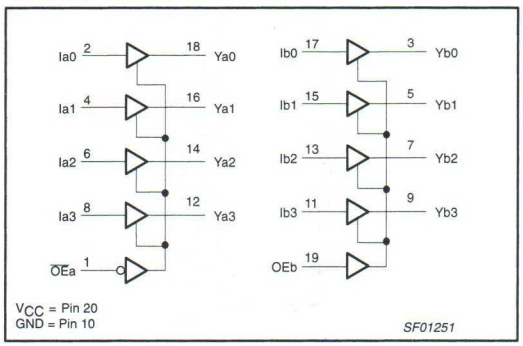
INPUTS				OUTPUTS	
$\overline{OEa}$	Ia	$\overline{OEb}$	Ib	$\overline{Ya}$	$\overline{Yb}$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	H (off)	H (off)

H = High voltage level
L = Low voltage level
X = Don't care

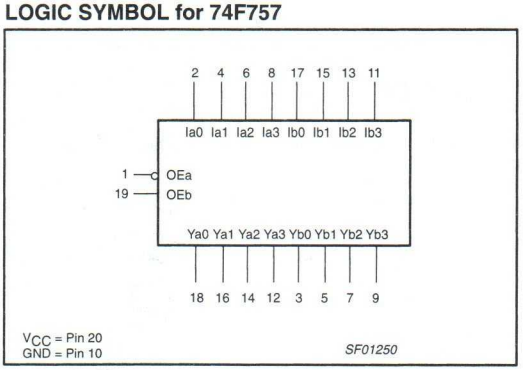
PIN CONFIGURATION for 74F757



LOGIC DIAGRAM for 74F757



LOGIC SYMBOL for 74F757

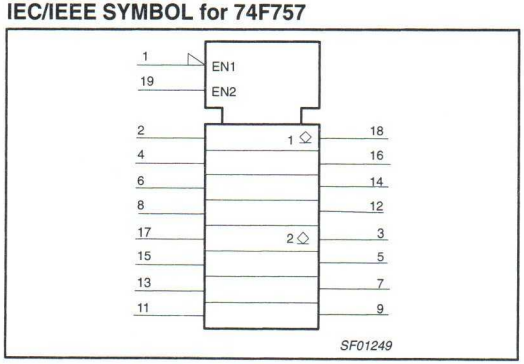


FUNCTION TABLE for 74F757

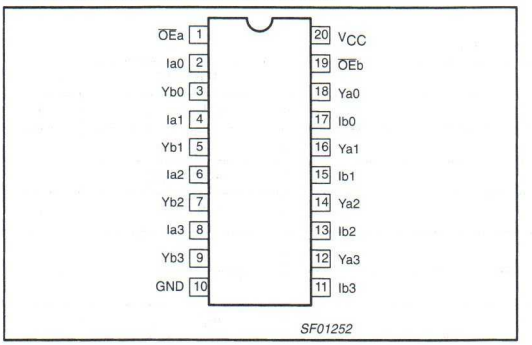
INPUTS				OUTPUTS	
$\overline{OEa}$	Ia	OEb	Ib	Ya	Yb
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	H (off)	H (off)

H = High voltage level
L = Low voltage level
X = Don't care

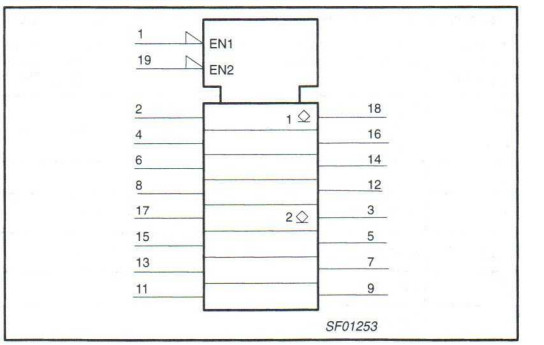
IEC/IEEE SYMBOL for 74F757



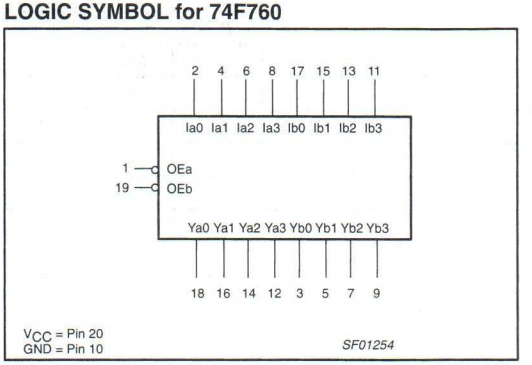
PIN CONFIGURATION for 74F760



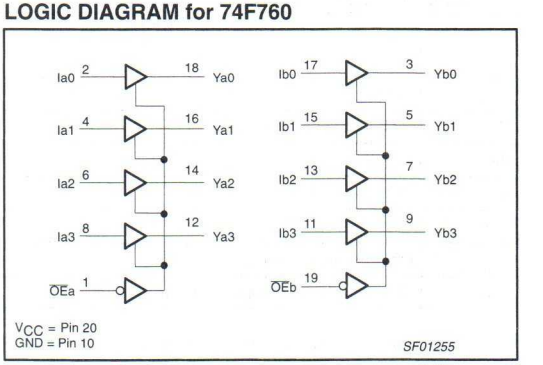
IEC/IEEE SYMBOL for 74F760



LOGIC SYMBOL for 74F760



LOGIC DIAGRAM for 74F760



FUNCTION TABLE for 74F760

INPUTS				OUTPUTS	
$\overline{OE}a$	Ia	$\overline{OE}b$	Ib	Ya	Yb
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	H (off)	H (off)

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
V_{OH}	High-level output voltage			4.5	V
I_{OL}	Low-level output current			64	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							MIN	TYP[2]	MAX	
I_{OH}	High-level output current			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX					250	µA
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL} = 48MAX	±10%V_{CC}		0.38	0.55	V
					I_{OL}= 64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					–1.0	mA
I_{CC}	Supply current (total)	74F756	I_{CCH}	V_{CC} = MAX				20	30	mA
			I_{CCL}					50	70	mA
		74F757	I_{CCH}					30	40	mA
			I_{CCL}					55	80	mA
		74F760	I_{CCH}					25	37	mA
			I_{CCL}					55	80	mA

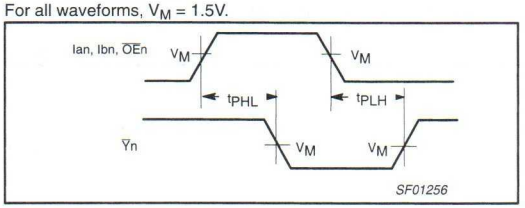
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.

AC ELECTRICAL CHARACTERISTICS

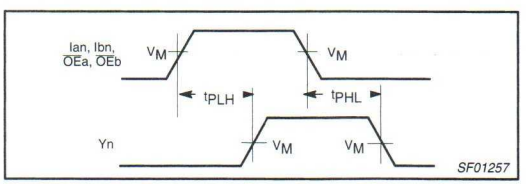
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Ian, Ibn to $\overline{Y}$n	74F756	Waveform 1, 2	8.5 1.0	11.0 3.0	14.0 6.0	8.5 1.0	15.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$n to $\overline{Y}$n		Waveform 1, 2	9.0 5.0	11.5 7.0	14.5 10.0	9.0 4.5	15.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay Ian, Ibn to Yn	74F757	Waveform 1, 2	7.5 3.0	10.5 5.5	13.5 8.5	7.5 3.0	14.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$a or OEb to Yn		Waveform 1, 2	9.0 4.5	10.5 7.0	15.0 10.0	8.5 4.0	16.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay Ian, Ibn to Yn	74F760	Waveform 1, 2	7.5 3.5	10.0 5.5	13.5 8.5	7.5 3.0	14.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$n to Yn		Waveform 1, 2	9.5 5.0	11.5 7.0	14.5 10.5	9.0 4.5	15.0 10.5	ns

AC WAVEFORMS

For all waveforms, V_M = 1.5V.

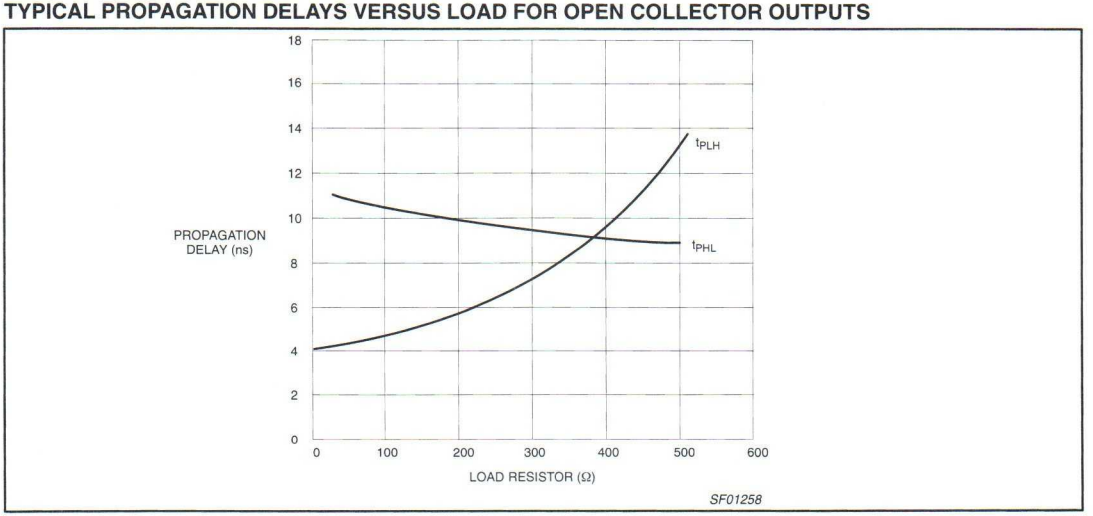


Waveform 1. Propagation Delay for Inverting Outputs



Waveform 2. Propagation Delay for Non-invertIng Outputs

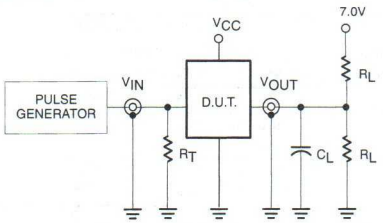
TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS



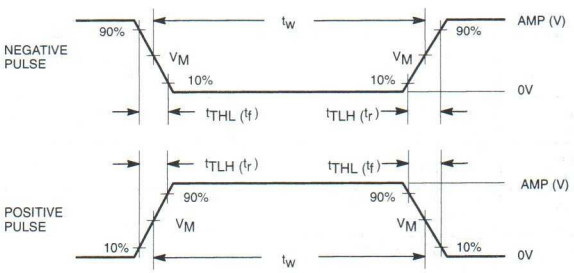
NOTE:

When using open-collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only slight increase in the t_{PHL}. However, if the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers do not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs



Input Pulse Definition

DEFINITIONS:

R_L = Load resistor;
see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00027

Pi–bus transceiver 74F776

FEATURES

- Octal latched transceiver
- Drives heavily loaded backplanes with equivalent load impedances down to 10 ohms
- High drive (100mA) open collector drivers on B port
- Reduced voltage swing (1 volt) produces less noise and reduces power consumption
- High speed operation enhances performance of backplane buses and facilitates incident wave switching
- Compatible with Pi–bus and IEEE 896 Futurebus standards
- Built–in precision band–gap reference provides accurate receiver thresholds and improved noise immunity
- Controlled output ramp and multiple GND pins minimize ground bounce
- Glitch–free power up/power down operation
- Multiple package options
- Industrial temperature range available (–40°C to +85°C)

DESCRIPTION

The 74F776 is an octal bidirectional latched transceiver and is intended to provide the electrical interface to a high performance wired–OR bus. The B port inverting drivers are low–capacitance open collector with controlled ramp and are designed to sink 100mA from 2 volts. The B port inverting receivers have a 100 mV threshold region and a 4ns glitch filter.

The 74F776 B port interfaces to 'Backplane Transceiver Logic' (BTL). BTL features a reduced (1V to 2V) voltage swing for lower power consumption and a series diode on the drivers to reduce capacitive loading. Incident wave switching is employed, therefore BTL propagation delays are short. Although the voltage swing is less for BTL, so is its receiver threshold, therefore noise margins are excellent.

BTL offers low power consumption, low ground bounce, EMI and crosstalk, low capacitive loading, superior noise margin and low propagation delays. This results in a high bandwidth, reliable backplane.

The 74F776 A port has TTL 3–state drivers and TTL receivers with a latch function. A separate high–level control voltage input (V_X) is provided to limit the A side output level to a given voltage level (such as 3.3V). For 5.0V systems, V_X is simply tied to V_{CC}.

The 74F776 has a designed feature to control the B output transitions during power sequencing. There are two possible sequencing, They are as follows:

1. When $\overline{LE}$ = low and $\overline{OEB}$n = low then the B outputs are disabled until the $\overline{LE}$ circuitry takes control. Then the B outputs will follow the A inputs, making a maximum of one transition during power–up (or down).
2. If $\overline{LE}$ = high or $\overline{OEB}$n = high then the B outputs will be disabled during power–up (or down).

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F776	6.5ns	80mA

ORDERING INFORMATION

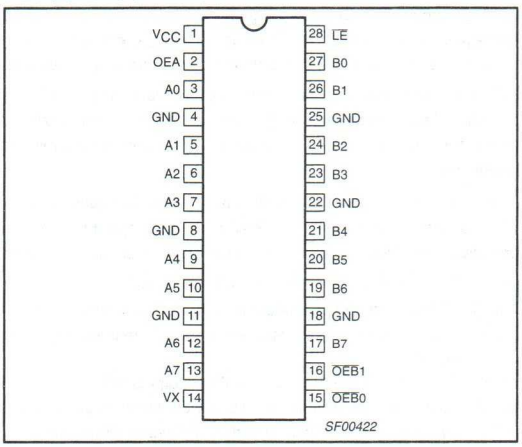
DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
28–pin plastic DIP (600 mil)	N74F776N	I74F776N	SOT117-2
28–pin PLCC	N74F776A	I74F776A	SOT261-2

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

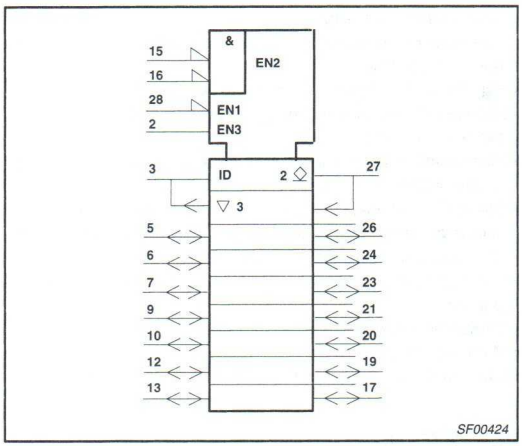
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A7	PNP latched inputs	3.5/0.117	70μA/70μA
B0 – B7	Data inputs with threshold circuitry	5.0/0.167	100μA/100μA
OEA	A output enable input (active high)	1.0/0.033	20μA/20μA
$\overline{OEB0}$, $\overline{OEB1}$	B output enable inputs (active low)	1.0/0.033	20μA/20μA
$\overline{LE}$	Latch enable input (active low)	1.0/0.033	20μA/20μA
A0 – A7	3–state outputs	150/40	3mA/24mA
B0 – B7	Open collector outputs	OC/166.7	OC/100mA

Notes to input and output loading and fan out table
One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.
OC = Open collector.

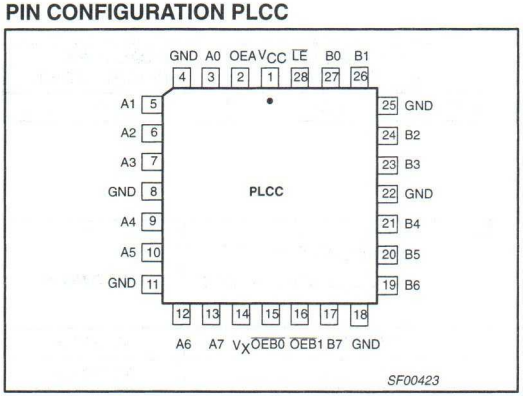
PIN CONFIGURATION



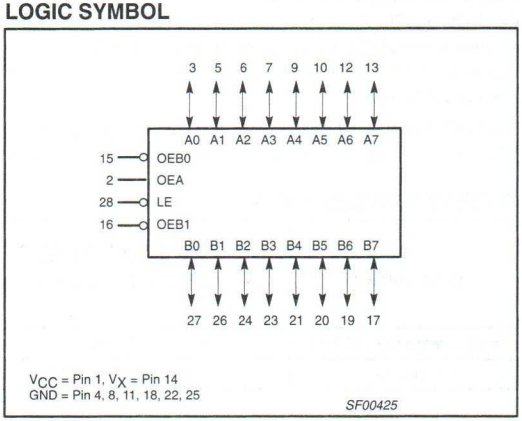
IEC/IEEE SYMBOL



PIN CONFIGURATION PLCC



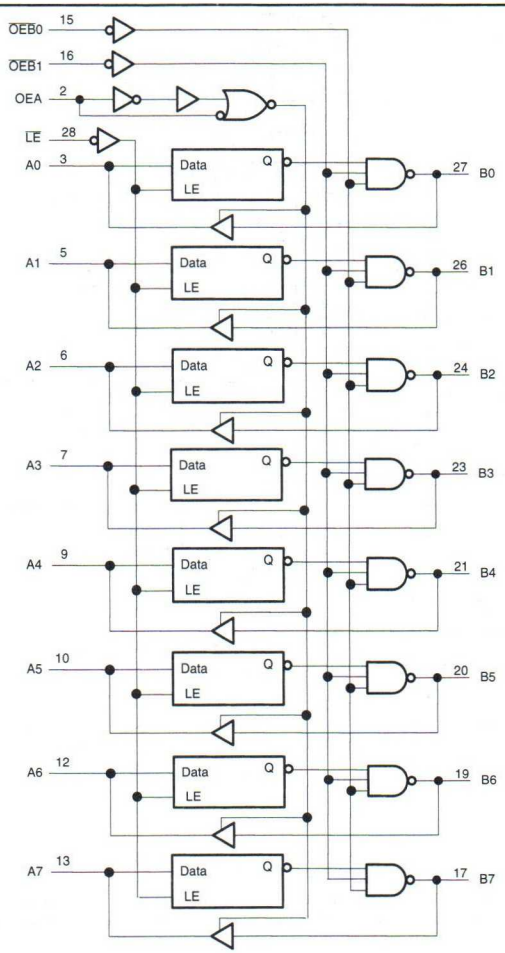
LOGIC SYMBOL



PIN DESCRIPTION

SYMBOL	PINS	TYPE	NAME AND FUNCTION
A0 – A7	3, 5, 6, 7, 9, 10, 12, 13	I/O	PNP latched input/3–state output (with V_X control option)
B0 – B7	27, 26, 24, 23, 21, 20, 19, 17	I/O	Data input with special threshold circuitry to reject noise/ open collector output, high current drive
$\overline{OEB0}$	15	Input	Enables the B outputs when both pins are low
$\overline{OEB1}$	16	Input	
OEA	2	Input	Enables the A outputs when high
$\overline{LE}$	28	Input	Latched when high (a special feature is built in for proper enabling times)
V_X	14	Input	Clamping voltage keeping V_{OH} from rising above V_X ($V_X = V_{CC}$ for normal use)

LOGIC DIAGRAM



V_{CC} = Pin 1, V_X = Pin 14,
GND = Pin 4, 8, 11, 18, 22, 25

SF00426

FUNCTION TABLE

INPUTS						LATCH	OUTPUTS		OPERATING MODE
An	Bn*	$\overline{LE}$	OEA	$\overline{OEB0}$	$\overline{OEB1}$	STATE	An	Bn	
H	X	L	L	L	L	H	Z	Z	A 3–state, data from A to B
L	X	L	L	L	L	L	Z	L	
X	X	H	L	L	L	Qn	Z	Qn	A 3–state, latched data to B
–	–	L	H	L	L	(1)	(1)	(1)	Feedback: A to B, B to A
–	H	H	H	L	L	H (2)	H	Z(2)	Preconditioned latch enabling data transfer from B to A
–	L	H	H	L	L	H (2)	L	Z(2)	
–	–	H	H	L	L	Qn	Qn	Qn	Latch state to A and B
H	X	L	L	H	X	H	Z	Z	B and A 3–state
L	X	L	L	H	X	L	Z	Z	
X	X	H	L	H	X	Qn	Z	Z	
–	H	L	H	H	X	H	H	Z	B 3–state, data from B to A
–	L	L	H	H	X	L	L	Z	
–	H	H	H	H	X	Qn	H	Z	
–	L	H	H	H	X	Qn	L	Z	
H	X	L	L	X	H	H	Z	Z	B and A 3–state
L	X	L	L	X	H	L	Z	Z	
X	X	H	L	X	H	Qn	Z	Z	
–	H	L	H	X	H	H	H	Z	B 3–state, data from B to A
–	L	L	H	X	H	L	L	Z	
–	H	H	H	X	H	Qn	H	Z	
–	L	H	H	X	H	Qn	L	Z	

Notes to function table

H = High voltage level
L = Low voltage level
X = Don't care
– = Input not externally driven
Z = High impedance "off" state
Q_n = High or Low voltage level one setup time prior to the low–to–high $\overline{LE}$ transition.
(1) = Condition will cause a feedback loop path: A to B and B to A.
(2) = The latch must be preconditioned such that B inputs may assume a high or low level while $\overline{OEB0}$ and $\overline{OEB1}$ are low and $\overline{LE}$ is high.
B* = Precaution should be taken to insure the B inputs do not float. If they do they are equal to low state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_X	Threshold control		–0.5 to +7.0	V
V_{IN}	Input voltage	$\overline{OEB}$n, OEA, $\overline{LE}$	–0.5 to +7.0	V
		A0 – A7, B0 – B7	–0.5 to +5.5	V
I_{IN}	Input current		–40 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	A0 – A7	48	mA
		B0 – B7	200	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage	Except B0 – B7	2.0			V
		B0 – B7	1.6			V
V_{IL}	Low–level input voltage	Except B0 – B7			0.8	V
		B0 – B7			1.45	V
I_{Ik}	Input clamp current	Except A0 – A7			–18	mA
		A0 – A7			–40	mA
I_{OH}	High–level output current	A0 – A7			–3	mA
I_{OL}	Low–level output current	A0 – A7			24	mA
		B0 – B7			100	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
I_{OH}	High–level output current	B0 – B7	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
I_{OFF}	Power–off output current	B0 – B7	V_{CC} = 0.0V, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
V_{OH}	High-level output voltage	A0 – A7[4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA, V_X =V_{CC}	2.5		V_{CC}	V
				I_{OH} = –4mA, V_X =3.13V and 3.47V	2.5			V
V_{OL}	Low-level output voltage	A0 – A7[4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 20mA, V_X = V_{CC}			0.50	V
		B0 – B7		I_{OL} = 100mA			1.15	V
				I_{OL} = 4mA	0.40			V
V_{IK}	Input clamp voltage	A0 – A7	V_{CC} = MIN, I_I = I_{IK}				-0.5	V
		Except A0 – A7	V_{CC} = MIN, I_I = I_{IK}				-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEB}$n, OEA, $\overline{LE}$	V_{CC} = 0.0V, V_I = 7.0V				100	µA
		A0 – A7, B0 – B7	V_{CC} = MAX, V_I = 5.5V				1	mA
I_{IH}	High–level input current	$\overline{OEB}$n, OEA, $\overline{LE}$	V_{CC} = MAX, V_I = 2.7V, Bn –An =0V				20	µA
		B0 – B7	V_{CC} = MAX, V_I = 2.1V				100	µA
I_{IL}	Low–level input current	$\overline{OEB}$n, OEA, $\overline{LE}$	V_{CC} = MAX, V_I = 0.5V				–20	µA
		B0 – B7	V_{CC} = MAX, V_I = 0.3V				–100	µA
I_{OZH} + I_{IH}	Off state output current, high level voltage applied	A0 – A7	V_{CC} = MAX, V_O = 2.7V				70	µA
I_{OZL} + I_{IL}	Off state output current, low level voltage applied	A0 – A7	V_{CC} = MAX, V_O = 0.5V				–70	µA
I_X	High–level control current		V_{CC} = MAX, V_X = V_{CC}, $\overline{LE}$ = OEA = $\overline{OEB}$n = 2.7V, A0 – A7 = 2.7V, B0 – B7 = 2.0V,		–100		100	µA
			V_{CC} = MAX, V_X = 3.13 & 3.47V, $\overline{LE}$ = OEA = 2.7V, $\overline{OEB}$n = A0 – A7 = 2.7V, B0 – B7 = 2.0V,		–10		10	µA
I_{OS}	Short circuit output current[3]	A0 – A7 only	V_{CC} = MAX, Bn = 1.8V, OEA = 2.0V, $\overline{OEB}$n = 2.7V		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			65	100	mA
		I_{CCL}	V_{CC} = MAX, V_{IL} = 0.5V			100	145	mA
		I_{CCZ}				75	100	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type. Unless otherwise specified, V_X = V_{CC} for all test conditions.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are for V_{IH} =1.8v and V_{IL} = 1.3V.

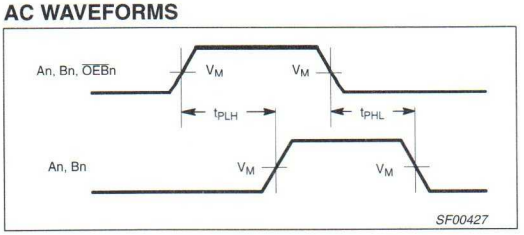
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Bn to An	Waveform 1	5.5 4.5	8.0 6.0	12.0 9.0	5.5 4.5	12.0 9.0	5.5 4.5	12.0 9.0	ns
t_{PZH} t_{PZL}	Output enable time to high or low, OEA to An	Waveform 3, 4	8.0 8.5	10.5 11.0	13.5 13.5	7.5 8.0	15.0 15.5	7.5 8.0	15.5 15.5	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low, OEA to An	Waveform 3, 4	2.0 2.0	3.5 4.5	6.0 7.0	1.5 2.0	6.5 7.5	1.5 2.0	6.5 7.5	ns
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_D = 30pF, R_U = 9Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_D = 30pF, R_U = 9Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_D = 30pF, R_U = 9Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn	Waveform 1	3.0 3.0	5.0 4.5	7.0 7.5	2.5 2.5	8.0 8.5	2.0 2.5	9.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}$ to Bn	Waveform 1	3.5 3.5	5.0 5.0	8.0 8.0	3.0 2.5	9.0 9.0	2.5 2.5	9.5 9.5	ns
t_{PLH} t_{PHL}	Enable/disable time $\overline{OEB}$n to An	Waveform 1	3.0 3.5	4.5 5.5	7.0 9.0	2.5 3.5	8.0 10.0	2.5 3.5	8.5 10.5	ns
t_{TLH} t_{THL}	Transition time, B port 1.3V to 1.7V, 1.7V to 1.3V	Test Circuit and Waveforms	0.5 0.5	2.0 2.0	4.5 4.5	0.5 0.5	5.0 4.5	0.5 0.5	5.0 4.5	ns

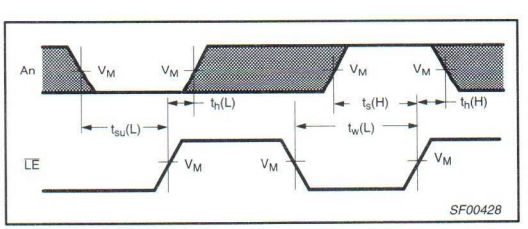
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low An to $\overline{LE}$	Waveform 2	3.5 4.5			4.5 5.0		4.5 5.0		ns
t_h(H) t_h(L)	Hold time, high or low An to $\overline{LE}$	Waveform 2	0.0 0.0			0.0 0.0		0.0 0.0		ns
t_w (L)	$\overline{LE}$ pulse width, low	Waveform 2	4.0			5.0		5.0		ns

AC WAVEFORMS

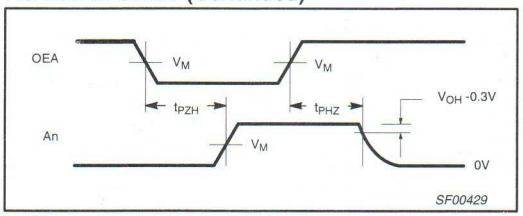


Waveform 1. Propagation delay for data to output

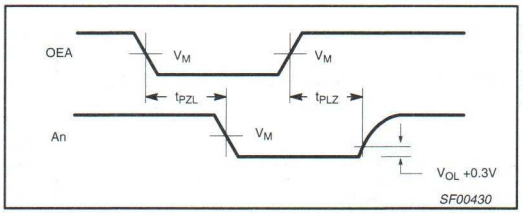


Waveform 2. Data setup and hold times and $\overline{LE}$ pulse width

AC WAVEFORMS (Continued)



Waveform 3. 3-state output enable time to high level and output disable time from high level



Waveform 4. 3-state output enable time to low level and output disable time from low level

Notes to AC waveforms

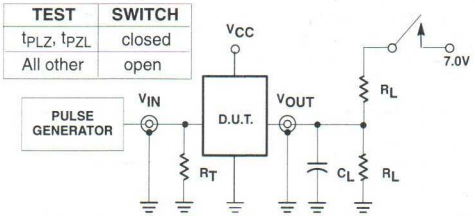
For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

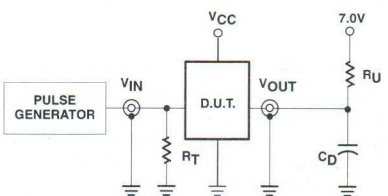
TEST CIRCUIT AND WAVEFORMS

SWITCH POSITION

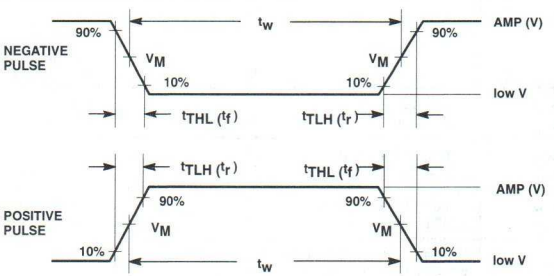
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test circuit for 3–State outputs on A port



Test circuit for outputs on B port



Input pulse definition

family	INPUT PULSE REQUIREMENTS						
	amplitude	Low V	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
A port	3.0V	0.0V	1.5V	1MHz	500ns	2.5ns	2.5ns
B port	2.0V	1.0V	1.0V	1MHz	500ns	4.0ns	4.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_U = Pull up resistor; see AC electrical characteristics for value.
C_D = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SF00431

Triple bidirectional latched bus transceiver (3–State + Open Collector) 74F777

FEATURES

- Latching transceiver
- High drive Open Collector output current with minimum output swing
- Compatible with Test Mode (TM) bus specification
- Controlled output ramp
- Multiple package options
- Industrial temperature range available (–40°C to +85°C)

DESCRIPTION

The 74F777 is a triple bidirectional latched bus transceiver and is intended to provide the electrical interface to a high performance wired–OR bus. This bus has a loaded characteristics impedance range of 20 to 50 ohms and is terminated on each end with a 30 to 40 ohm resistor.

The 74F777 is a triple bidirectional transceiver with Open Collector B and 3–State A port output drivers. A latch function is provided for the A port signals. The B port output driver is designed to sink 100mA from 2 volts to minimize crosstalk and ringing on the bus.

A separate output threshold clamp voltage (V_X) is provided to prevent the A port output High level from exceeding future high density processor supply voltage levels. For 5 volt systems, V_X is simply tied to V_{CC}.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F777	7.0ns	45mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
20–pin plastic DIP (300 mil)	N74F777N	I74F777N	SOT146-1
20–pin PLCC	N74F777A	I74F777A	SOT380-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

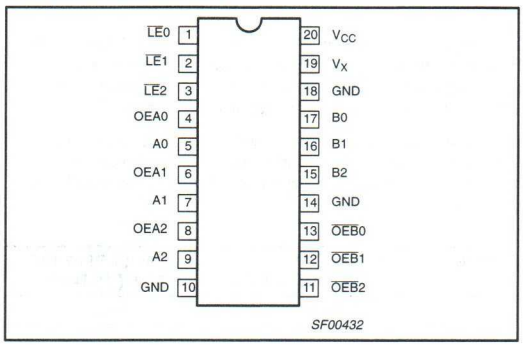
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A2	PNP latched inputs	3.5/0.117	70µA/70µA
B0 – B2	Data inputs with threshold circuitry	5.0/0.167	100µA/100µA
OEA0 – OEA2	A output enable inputs (active–High)	1.0/0.033	20µA/20µA
$\overline{OEB0}$ – $\overline{OEB2}$	B output enable inputs (active–Low)	1.0/0.033	20µA/20µA
$\overline{LE0}$ – $\overline{LE2}$	Latch enable inputs (active–Low)	1.0/0.033	20µA/20µA
A0 – A2	3–State outputs	150/40	3mA/24mA
B0 – B2	Open Collector outputs	OC/166.7	OC/100mA

Note to input and output loading and fan out table

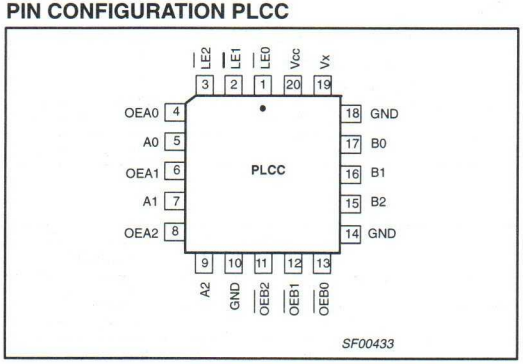
One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.
OC = Open Collector.

Triple bidirectional latched bus transceiver (3–State + Open Collector) 74F777

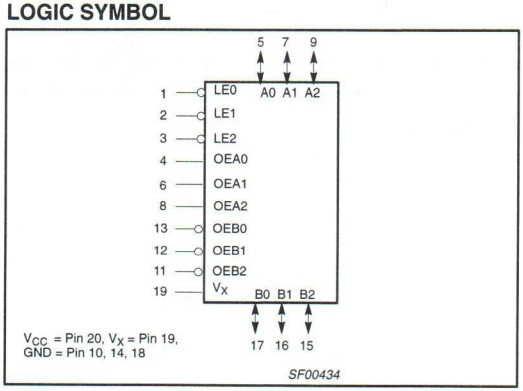
PIN CONFIGURATION



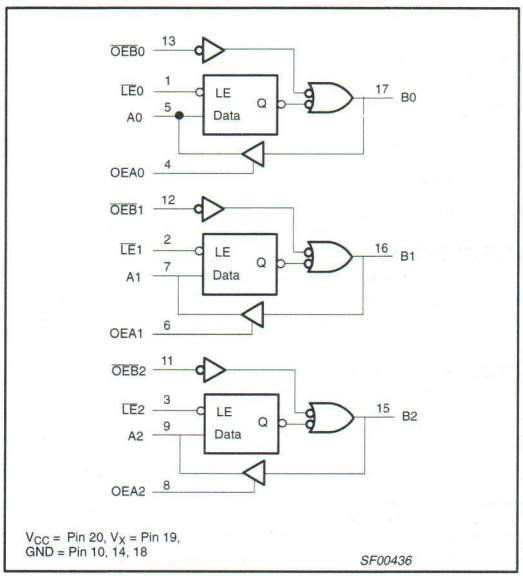
PIN CONFIGURATION PLCC



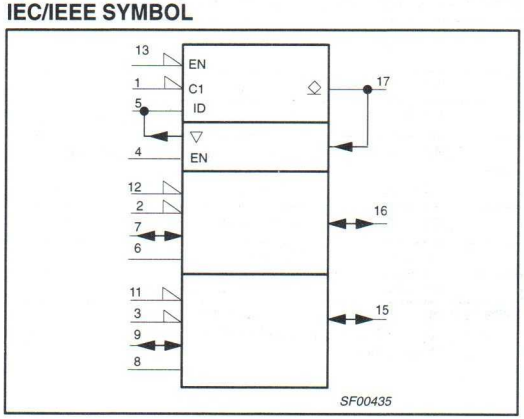
LOGIC SYMBOL



LOGIC DIAGRAM



IEC/IEEE SYMBOL



FUNCTION TABLE

INPUTS					LATCH	OUTPUTS		OPERATING MODE
An	Bn*	$\overline{LE}$n	OEAn	$\overline{OEB}$n	STATE	An	Bn	
H	X	L	L	L	H	Z	H**	A 3-State, data from A to B
L	X	L	L	L	L	Z	L	
X	X	H	L	L	Qn	Z	Qn	A 3-State, latched data to B
–	–	L	H	L	(1)	(1)	(1)	Feedback: A to B, B to A
–	H	H	H	L	H (2)	H	Z(2)	Preconditioned latch enabling
–	L	H	H	L	H (2)	L	Z(2)	data transfer from B to A
–	–	H	H	L	Qn	Qn	Qn	Latch state to A and B
H	X	L	L	H	H	Z	Z	
L	X	L	L	H	L	Z	Z	B and A 3–State
X	X	H	L	H	Qn	Z	Z	
–	H	L	H	H	H	H	Z	
–	L	L	H	H	L	L	Z	B 3-State, data from B to A
–	H	H	H	H	Qn	H	Z	
–	L	H	H	H	Qn	L	Z	

Notes to function table Qn

H = High voltage level
L = Low voltage level
X = Don't care
– = Input not externally driven
Z = High impedance (off) state
Q_n = High or Low voltage level one setup time prior to the Low–to–High $\overline{LE}$ transition.
(1) = Condition will cause a feedback loop path: A to B and B to A.
(2) = The latch must be preconditioned such that B inputs may assume a High or Low level while $\overline{OEB}$0 and $\overline{OEB}$1 are Low and $\overline{LE}$ is High.
B_n* =Precaution should be taken to insure the B inputs do not float. If they do they are equal to Low state.
H**= Goes to level of pull-up voltage.
Each latch is independent. The latches may be run in any combination of modes.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_X	Threshold control		–0.5 to +7.0	V
V_{IN}	Input voltage	$\overline{OEB}$n, OEAn, $\overline{LE}$n	–0.5 to +7.0	V
		A0 – A2, B0 – B2	–0.5 to +5.5	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in	A0 – A2	48	mA
	Low output state	B0 – B2	200	mA
T_{amb}	Operating free air	Commercial range	0 to +70	°C
	temperature range	Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage	Except B0 – B2	2.0			V
		B0 – B2	1.6			V
V_{IL}	Low–level input voltage	Except B0 – B2			0.8	V
		B0 – B2			1.43	V
I_{Ik}	Input clamp current	Except A0 – A2			–18	mA
		A0 – A2			–40	mA
I_{OH}	High–level output current	Except A0 – A2			–3	mA
I_{OL}	Low–level output current	A0 – A2			24	mA
		B0 – B2			100	mA
T_{amb}	Operating free–air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
I_{OH}	High–level output current	B0 – B2	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
I_{OFF}	Power–off output current	B0 – B2	V_{CC} = 0.0V, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
V_{OH}	High-level output voltage	A0 – A2[4]	V_{CC} = MIN,	I_{OH} = –3mA, V_X = V_{CC}	2.5		V_{CC}	V
			V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –4mA, V_X = 3.13V and 3.47V	2.5		V_X	V
V_{OL}	Low-level output voltage	A0 – A2[4]	V_{CC} = MIN,	I_{OL} = 20mA, V_X = V_{cc}			0.50	V
		B0 – B2	V_{IL} = MAX,	I_{OL} = 100mA			1.15	V
			V_{IH} = MIN	I_{OL} = 4mA	0.40			V
V_{IK}	Input clamp voltage	A0 – A2	V_{CC} = MIN, I_I = I_{IK}				-0.5	V
		Except A0 – A2	V_{CC} = MIN, I_I = I_{IK}				-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEB}$n, OEAn, $\overline{LE}$n	V_{CC} = MAX, V_I = 7.0V				100	µA
		A0 – A2, B0 – B2	V_{CC} = MAX, V_I = 5.5V				1	mA
I_{IH}	High–level input current	$\overline{OEB}$n, OEAn, $\overline{LE}$n	V_{CC} = MAX, V_I = 2.7V, Bn – An = 0V				20	µA
		B0 – B2	V_{CC} = MAX, V_I = 2.1V				100	µA
I_{IL}	Low–level input current	$\overline{OEB}$n, OEAn $\overline{LE}$n	V_{CC} = MAX, V_I = 0.5V				–20	µA
		B0 – B2	V_{CC} = MAX, V_I = 0.3V				–100	µA
I_{OZH} + I_{IH}	Off–state output current, High level voltage applied	A0 – A2	V_{CC} = MAX, V_O = 2.7V				70	µA
I_{OZL} + I_{IL}	Off–state output current, Low level voltage applied	A0 – A2	V_{CC} = MAX, V_I = 0.5V				–70	µA
I_X	High level control current		V_{CC} = MAX, V_X = V_{CC}, $\overline{LE}$ = OEAn = $\overline{OEB}$n = 2.7V, A0 – A2 = 2.7V, B0 – B2 = 2.0V,		–100		100	µA
			V_{CC} = MAX, V_X = 3.13 & 3.47V, $\overline{LE}$ = OEAn = 2.7V, $\overline{OEB}$n = A0 – A2 = 2.7V, B0 – B2 = 2.0V		–10		10	µA
I_{OS}	Short circuit output current[3]	A0 – A2 only	V_{CC} = MAX, Bn = 1.8V, OEAn = 2.0V, $\overline{OEB}$n = 2.7V		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			40	60	mA
		I_{CCL}	V_{CC} = MAX, V_{IL} = 0.5V			55	80	mA
		I_{CCZ}	V_{CC} = MAX, V_{IL} = 0.5V			45	67	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type. Unless otherwise specified, V_X =V_{CC} for all test condition.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are for V_{IH} =1.8v and V_{IL} = 1.3V.

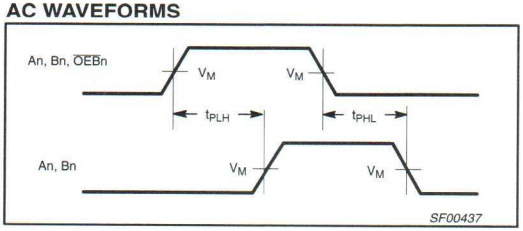
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS							UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 30pF, R_L = 9Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 30pF, R_L = 9Ω		T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ±10%, C_L = 30pF, R_L = 9Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Bn to An	Waveform 1	8.5 7.5	10.5 9.5	13.0 12.0	8.0 7.5	14.5 12.5	8.0 7.5	14.5 12.5	ns
t_{PZH} t_{PZL}	Output enable time to High or Low OEAn to An	Waveform 3, 4	8.0 9.0	10.0 11.0	13.0 14.0	7.0 8.0	14.5 15.5	7.0 8.0	14.5 15.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low OEAn to An	Waveform 3, 4	1.5 1.5	3.0 3.0	6.0 6.0	1.0 1.0	6.5 6.0	1.0 1.0	6.5 6.0	ns
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS							UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_D= 30pF, R_U = 9Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_D = 30pF, R_U = 9Ω		T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ±10%, C_D= 30pF, R_U = 9Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn	Waveform 1	3.0 5.0	4.5 6.5	7.0 9.0	2.5 4.5	8.0 10.0	2.5 4.5	8.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}$n to Bn	Waveform 1	3.5 5.5	5.5 7.5	8.0 10.5	3.0 5.0	9.0 11.5	3.0 5.0	9.0 11.5	ns
t_{PLH} t_{PHL}	Enable/disable time $\overline{OEB}$n to An	Waveform 1	3.0 6.0	5.0 8.0	7.5 10.5	3.0 5.5	8.0 12.0	3.0 5.5	8.0 12.0	ns
t_{TLH} t_{THL}	Transition time, B port 1.3V to 1.7V, 1.7V to 1.3V	Test Circuits and Waveforms	0.5 0.5	4.0 2.0	4.5 4.5	0.5 0.5	7.0 4.5	0.5 0.5	7.0 4.5	ns

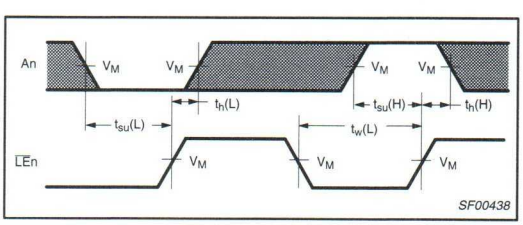
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_D= 30pF, R_U = 9Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_D = 30pF, R_U = 9Ω		T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ±10%, C_D= 30pF, R_U = 9Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time An to $\overline{LE}$n	Waveform 2	4.0 4.5			4.5 4.5		4.5 4.5		ns
t_h (H) t_h (L)	Hold time An to $\overline{LE}$n	Waveform 2	0.0 0.0			0.0 0.0		0.0 0.0		ns
t_w (L)	$\overline{LE}$n pulse width, Low	Waveform 2	5.5			6.5		6.5		ns

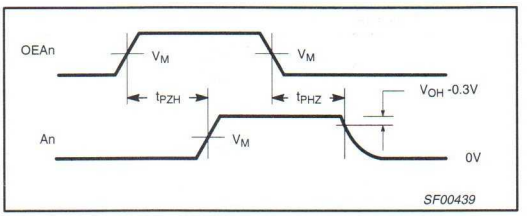
AC WAVEFORMS



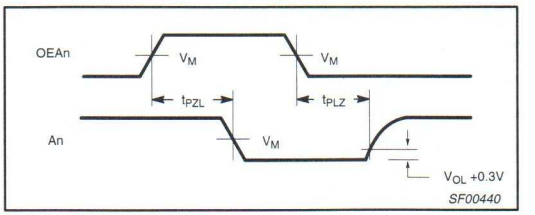
Waveform 1. Propagation delay, data to output and enable/disable time $\overline{OEB}$n to Bn



Waveform 2. Data set-up and hold times and $\overline{LE}$ pulse width



Waveform 3. 3-State output enable time to High level and output disable time from High level



Waveform 4. 3-State output enable time to Low level and output disable time from Low level

Notes to AC waveforms

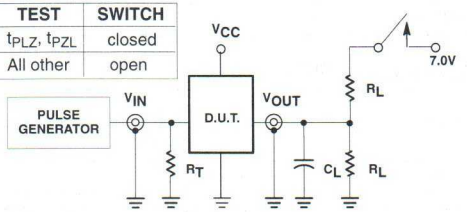
For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

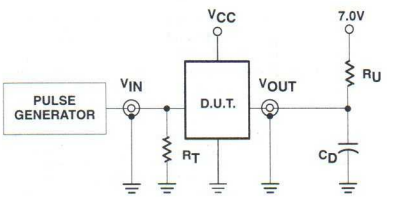
TEST CIRCUITS AND WAVEFORMS

SWITCH POSITION

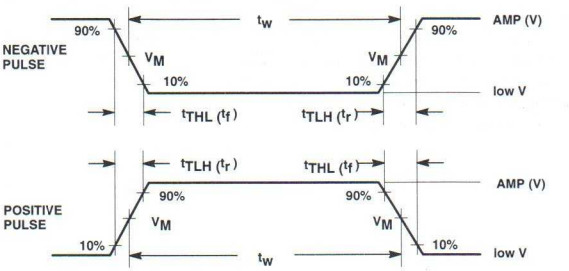
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test circuit for 3–State outputs on A port



Test circuit for outputs on B port



Input pulse definition

family	INPUT PULSE REQUIREMENTS						
	amplitude	Low V	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
A port	3.0V	0.0V	1.5V	1MHz	500ns	2.5ns	2.5ns
B port	2.0V	1.0V	1.0V	1MHz	500ns	4.0ns	4.0ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_U = Pull up resistor; see AC electrical characteristics for value.

C_D = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

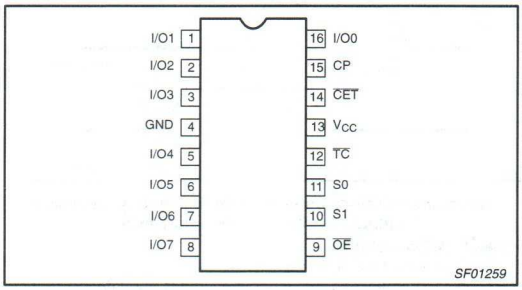
SF00431

8-bit bidirectional binary counter (3-State) 74F779

FEATURES

- Multiplexed 3-State I/O ports for bus oriented applications
- Built-in look-ahead carry capability
- Center power pins to reduce effects of package inductance
- Count frequency 145MHz typical
- Supply current 90mA typical
- See 74F269 for 24-pin separate I/O port version
- See 74F579 for 20-pin version
- See 74F1779 for extended function version of the 74F799

PIN CONFIGURATION



DESCRIPTION

The 74F779 is a fully synchronous 8-stage Up/Down Counter with multiplexed 3-State I/O ports for bus-oriented applications. All control functions (hold, count up, count down, synchronous load) are controlled by two mode pine (S0, S1). The device also features carry look-ahead for easy cascading. All state changes are initiated by the rising edge of the clock. When $\overline{CET}$ is High the data outputs are held in their current state and $\overline{TC}$ is held High. The $\overline{TC}$ output is not recommended for use as a clock or asynchronous reset due to the possibility of decoding spikes.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F779	145MHz	90mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
16-Pin Plastic DIP	N74F779N	SOT38-4
16-Pin Plastic SOL	N74F779D	SOT 162-1

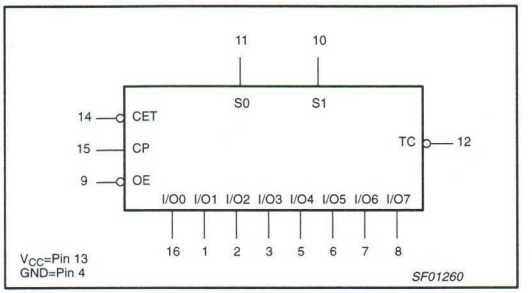
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I/On	Data inputs	3.5/1.0	70µA/0.6mA
	Data outputs	150/40	3.0mA/24mA
S0, S1	Select inputs	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{TC}$	Terminal Count output (active Low)	50/33	1.0mA/20mA

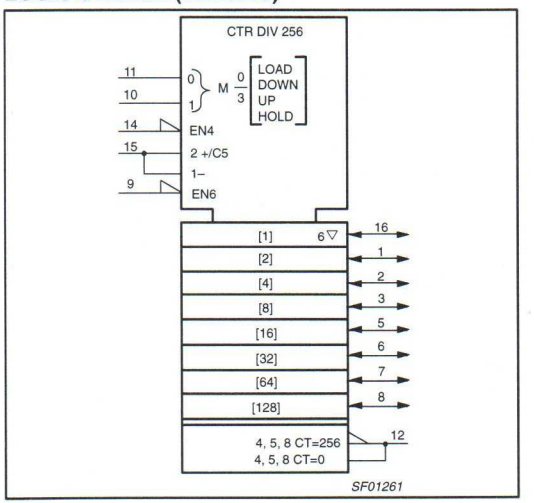
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

8-bit bidirectional binary counter (3-State) 74F779

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

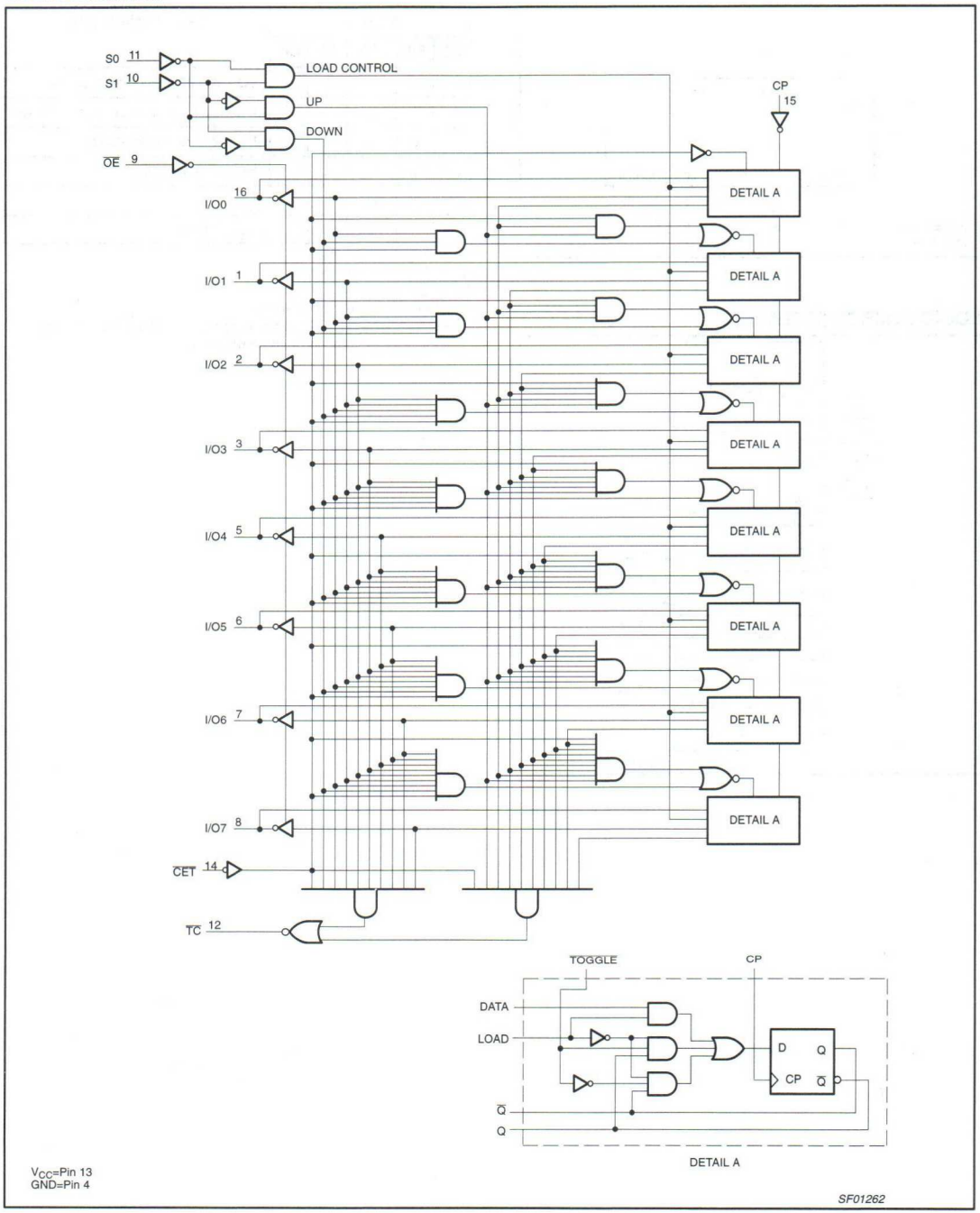


FUNCTION TABLE

INPUTS					OPERATING MODE
S1	S0	$\overline{CET}$	$\overline{OE}$	CP	
X	X	X	H	X	I/O0 to I/O7 in High impedance
X	X	X	L	X	Flip-flop outputs appear on I/O lines
L	L	X	H	↑	Parallel load all flip-flops
(not LL)		H	X	↑	Hold ($\overline{TC}$ held High)
H	L	L	X	↑	Count up
L	H	L	X	↑	Count down

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
(not LL) = S0 and S1 should never be Low voltage level at the same time in the hold mode only.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	$\overline{TC}$	40	mA
		I/On	48	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	$\overline{TC}$			−1	mA
		I/On			−3	mA
I_{OL}	Low-level output current	$\overline{TC}$			20	mA
		I/On			24	mA
T_{amb}	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	$\overline{TC}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/On	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	I/On	V_{CC} = 5.5V, V_I = 5.5V					1	mA
		others	V_{CC} = 5.5V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	except I/On	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					–0.6	mA
$I_{IH}+I_{OZH}$	Off-state output current High-level voltage applied	I/On	V_{CC} = MAX, V_O = 2.7V					70	µA
$I_{IL}+I_{OZL}$	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					–600	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				82	116	mA
		I_{CCL}					91	128	mA
		I_{CCZ}					97	136	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	125	145		115		MHz
t_{PLH} t_{PHL}	Propagation delay CP to I/On	Waveform 1	4.5 5.5	7.0 8.0	10.5 10.5	4.5 5.5	11.0 11.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	4.5 4.5	7.0 7.0	9.0 9.0	4.5 4.5	10.0 10.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 2	3.0 3.0	4.5 5.5	6.5 7.5	2.5 2.5	7.5 8.0	ns ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 4 Waveform 5	2.5 4.5	4.5 6.5	7.0 9.0	2.5 4.5	8.0 9.5	ns ns
t_{PHZ} t_{PLZ}	Output Enable time from High or Low level	Waveform 4 Waveform 5	1.0 1.0	3.0 4.0	6.5 7.0	1.0 1.0	8.0 8.0	ns ns

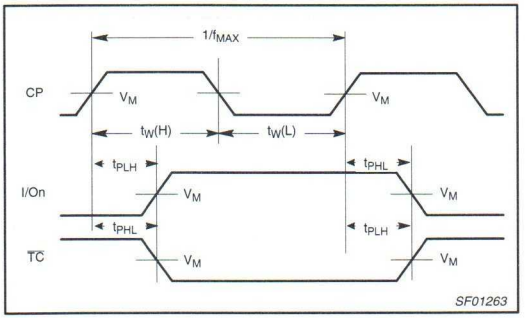
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_n to CP	Waveform 3	5.0 5.0			5.0 5.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n to CP	Waveform 3	1.0 1.0			1.0 1.0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CET}$ to CP	Waveform 3	5.0 5.5			5.0 6.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CET}$ to CP	Waveform 3	0 0			0 0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low Sn to CP	Waveform 3	8.0 8.0			8.5 8.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Sn to CP	Waveform 3	0 0			0 0		ns ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.0 4.0			4.0 4.0		ns ns

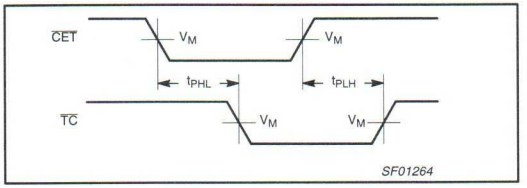
AC WAVEFORMS

For all waveforms, V_M = 1.5V.

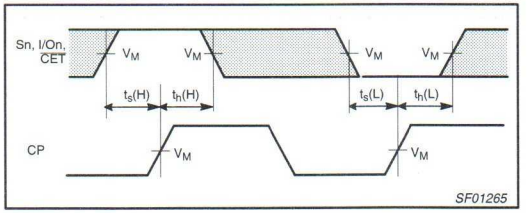
The shaded areas indicate when the input is permitted to change for predictable output performance.



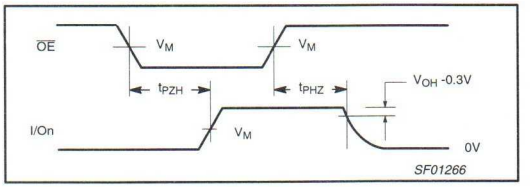
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



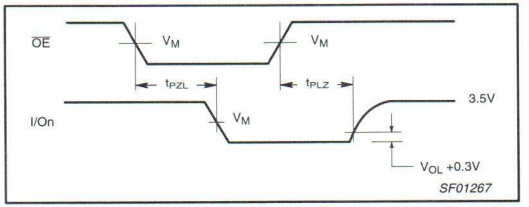
Waveform 2. Propagation Delay $\overline{CET}$ Input to Terminal Count Output



Waveform 3. Data Setup and Hold Times

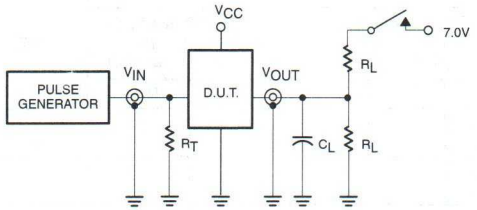


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

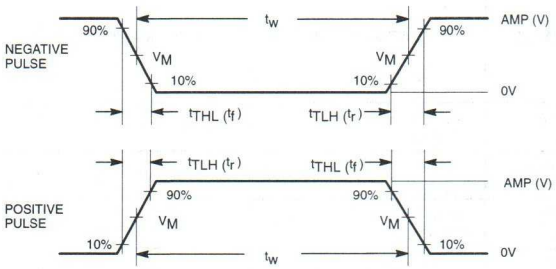


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

4-bit asynchronous bus arbiter 74F786

FEATURES

- Arbitrates between 4 asynchronous inputs
- Separate grant output for each input
- Common output enable
- On board 4 input AND gate
- Metastable–free outputs
- Industrial temperature range available (–40°C to +85°C)

DESCRIPTION

The 74F786 is an asynchronous 4–bit arbiter designed for high speed real–time applications. The priority of arbitration is determined on a first–come first–served basis. Separate bus grant ($\overline{BG}$n) outputs are available to indicate which one of the request inputs is served by the arbitration logic. All $\overline{BG}$n outputs are enabled by a common enable ($\overline{EN}$) pin. In order to generate a bus request signal a separate 4 input AND gate is provided which may also be used as an independent AND gate. Unused bus request ($\overline{BR}$) inputs may be disabled by tying them high.

The 74F786 is designed so that contention between two or more request signals will not glitch or display a metastable condition. In this situation an increase in the $\overline{BR}$n to $\overline{BG}$n t_{PHL} may be observed. A typical 74F786 has an h = 6.6ns, t = 0.41ns and To = 5µsec.

Where:

h = Typical propagation delay through the device and t and To are device parameters derived from test results and can most nearly be defined as:

t = A function of the rate at which a latch in a metastable state resolves that condition.

To = A function of the measurement of the propensity of a latch to enter a metastable state. To is also a very strong function of the normal propagation delay of the device.

For further information, please refer to the 74F786 application notes.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F786	6.6ns	55mA

ORDERING INFORMATION

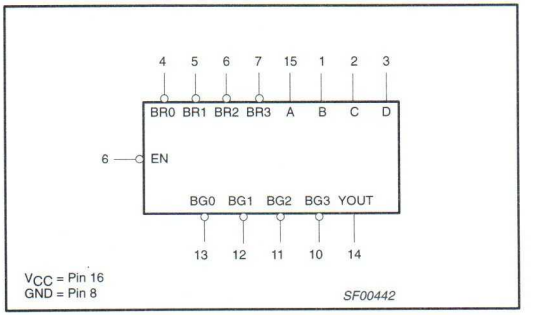
DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
16–pin plastic DIP	N74F786N	I74F786N	SOT 38-4
16–pin plastic SO	N74F786D	I74F786D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

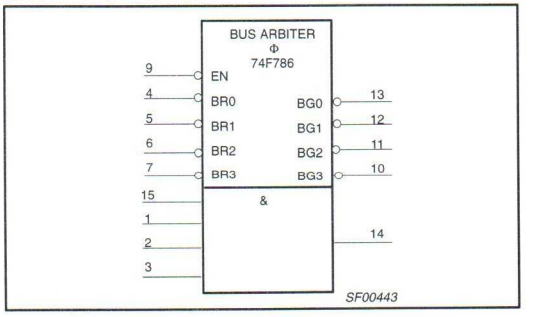
PINS	DESCRIPTION	74F (U.L.) HIGH/ LOW	LOAD VALUE HIGH/ LOW
$\overline{BR}$0 – $\overline{BR}$3	Bus request inputs (active low)	1.0/3.0	20µA/1.8mA
A, B, C, D	AND gate inputs	1.0/1.0	20µA/0.6mA
$\overline{EN}$	Common bus grant output enable input (active low)	1.0/1.0	20µA/0.6mA
YOUT	AND gate output	150/40	3.0mA/24mA
$\overline{BG}$0 – $\overline{BG}$3	Bus grant outputs (active low)	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

LOGIC SYMBOL



IEC/IEEE SYMBOL



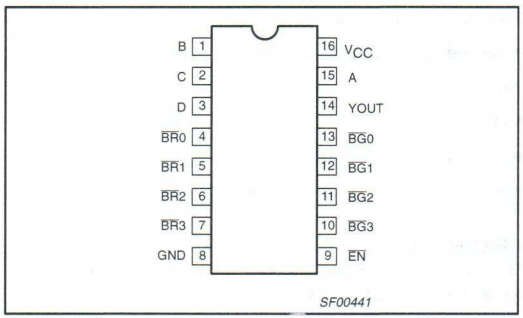
4-bit asynchronous bus arbiter 74F786

FUNCTIONAL DESCRIPTION

The $\overline{BR}$n inputs have no inherent priority. The arbiter assigns priority to the incoming requests as they are received, therefore, the first $\overline{BR}$ asserted will have the highest priority. When a bus request is received its corresponding bus grant becomes active, provided that $\overline{EN}$ is low. If additional bus requests are made during this time they are queued. When the first request is removed, the arbiter services the bus request with the next highest priority. Removing a request while a previous request is being serviced can cause a grant to be changed when arbitrating between three or four requests. For that reason, the user should not remove ungranted requests when arbitrating between three or four requests. This does not apply to arbitration between two requests.

If two or more $\overline{BR}$n inputs are asserted at precisely the same time, one of them will be selected at random, and all $\overline{BG}$n outputs will be held in the high state until the selection is made. This guarantees that an erroneous $\overline{BG}$n will not be generated even though a metastable condition may occur internal to the device. When the $\overline{EN}$ is in the high state the $\overline{BG}$n outputs are forced high.

PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	PINS	TYPE	NAME	FUNCTION
$\overline{BR}0 - \overline{BR}3$	4, 5, 6, 7	Input	Bus request inputs (active low)	The logic of this device arbitrates between these four inputs. Unused inputs should be tied high.
A, B, C, D	15, 1, 2, 3	Input	Inputs of the 4–input AND gate	
$\overline{EN}$	9	Input	Enable input	When low it enables the $\overline{BG}0 - \overline{BG}3$ outputs.
$\overline{BG}0 - \overline{BG}3$	13, 12, 11, 10	Output	Bus grant outputs (active low)	These outputs indicate the selected bus request. $\overline{BG}0$ corresponds to $\overline{BR}0$, $\overline{BG}1$ to $\overline{BR}1$, etc.
YOUT	14	Output	Output of the 4–input AND gate	
GND	8	Ground	ground (0V)	
V_{CC}	16	Power	Positive supply voltages	

ARBITER FUNCTION TABLE

INPUTS					OUTPUTS			
$\overline{EN}$	$\overline{BR0}$	$\overline{BR1}$	$\overline{BR2}$	$\overline{BR3}$	$\overline{BG0}$	$\overline{BG1}$	$\overline{BG2}$	$\overline{BG3}$
L	1	X	X	X	L	H	H	H
L	X	1	X	X	H	L	H	H
L	X	X	1	X	H	H	L	H
L	X	X	X	1	H	H	H	L
H	X	X	X	X	H	H	H	H

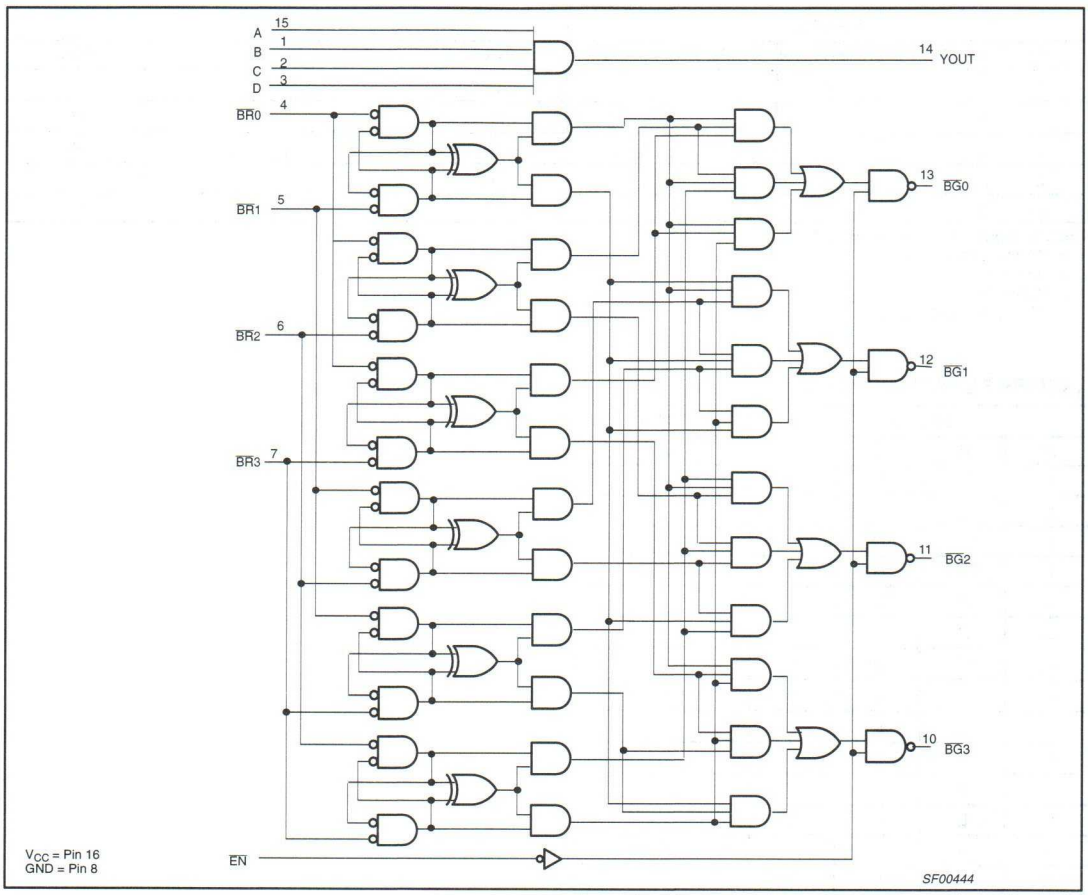
Notes to mode selection function table
H = High–voltage level
L = Low–voltage level
X = Don't care
1 = First of inputs to go low

ARBITER FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	YOUT
L	L	L	L	L
L	L	L	H	L
L	L	H	L	L
L	L	H	H	L
L	H	L	L	L
L	H	L	H	L
L	H	H	L	L
L	H	H	H	L
H	L	L	L	L
H	L	L	H	L
H	L	H	L	L
H	L	H	H	L
H	H	L	L	L
H	H	L	H	L
H	H	H	L	L
H	H	H	H	H

Notes to AND function table
H = High–voltage level
L = Low–voltage level

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		48	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IN}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current				–1	mA
I_{OL}	Low–level output current				24	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High–level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OH} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN		±5%V_{CC}	2.7	3.3		V
V_{OL}	Low–level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN		±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current	A – D, $\overline{EN}$	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
		$\overline{BR}n$						-1.8	mA
I_{OS}	Short–circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX				55	80	mA

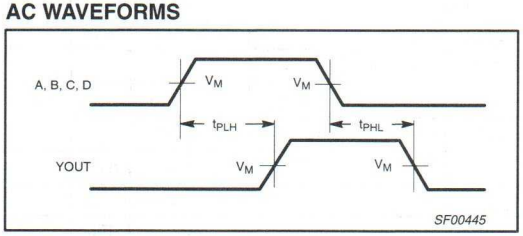
Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

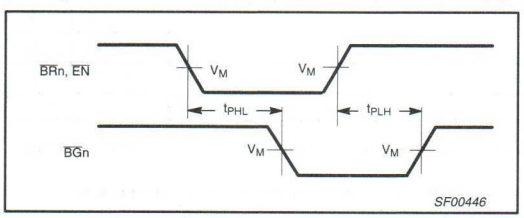
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay, A, B, C, D to YOUT	Waveform 1	2.5 2.5	4.5 4.5	7.5 7.5	2.0 2.5	8.5 7.5	2.0 2.5	8.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay, $\overline{BR}$n to $\overline{BG}$n	Waveform 2	5.0 4.5	7.0 6.5	10.0 9.5	4.5 4.0	10.5 10.0	4.5 4.0	10.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay, $\overline{EN}$ to $\overline{BG}$n	Waveform 2	3.0 2.5	5.0 4.5	8.0 7.5	2.5 2.5	8.5 8.0	2.5 2.5	8.5 8.0	ns
t_{PHL}	Propagation delay, $\overline{BR}$a to $\overline{BG}$b	Waveform 2	5.0	7.0	10.0	4.5	10.5	4.5	10.5	ns

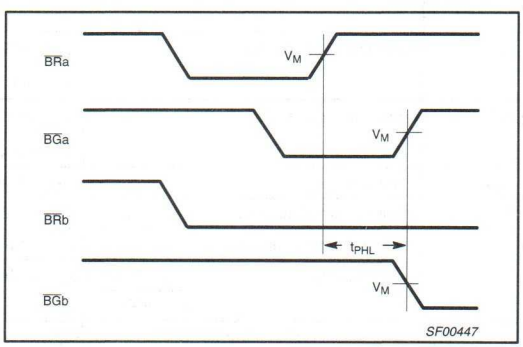
AC WAVEFORMS



Waveform 1. Propagation delay for AND gate to output



Waveform 2. Propagation delay for bus request or enable to bus grant output

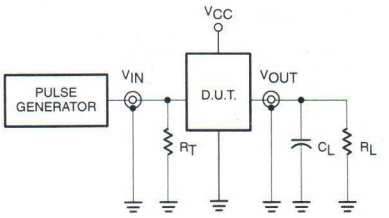


Waveform 3. Propagation delay for bus request to bus grant output

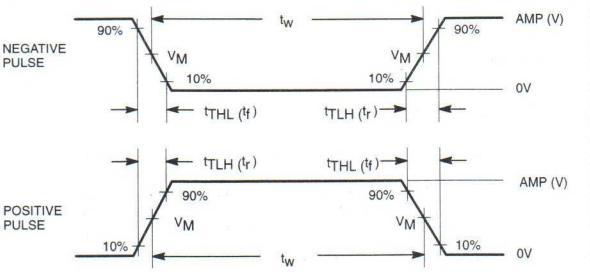
Notes to AC waveforms

1. For all waveforms, V_M = 1.5V.
2. a and b represents any of the bus requests or grants. $\overline{BG}$a low–to–high transition and the $\overline{BG}$b high–to–low transition occur simultaneously.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor;
see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Hex 2-input NAND drivers | 74F804/1804

FEATURES

- High capacitive drive capability
- Choice of configuration
  Corner V_{CC} and GND – 74F804
  Center V_{CC} and GND – 74F1804
- Typical propagation delay of 2.5ns

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F804	2.5ns	9mA
74F1804	2.5ns	9mA

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

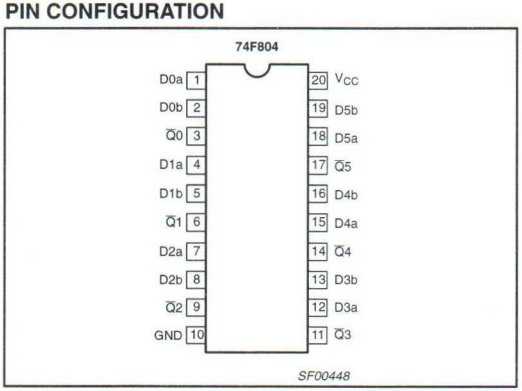
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna – Dnb	Data inputs	1.0/0.033	20μA/20μA
$\overline{Q}0$ – $\overline{Q}5$	Data outputs	2400/80	48mA/48mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.

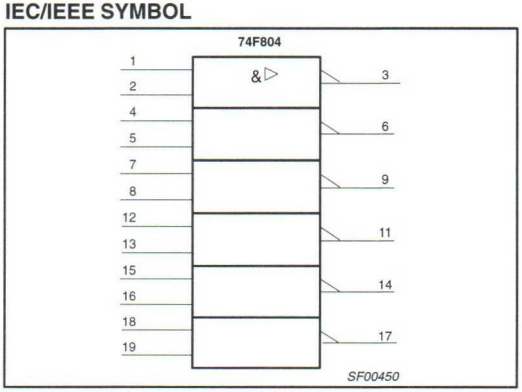
ORDERING INFORMATION

DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
20–pin plastic DIP	N74F804N, N74F1804N	SOT146-1
20–pin plastic SOL	N74F804D, N74F1804D	SOT163-1

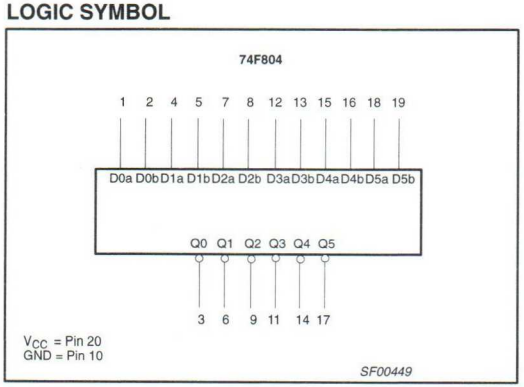
PIN CONFIGURATION



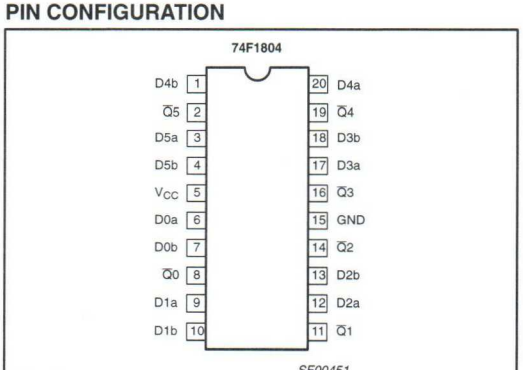
IEC/IEEE SYMBOL



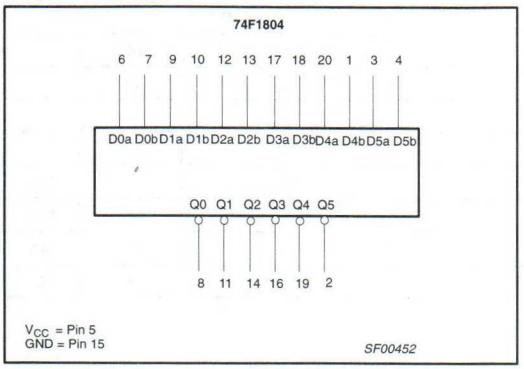
LOGIC SYMBOL



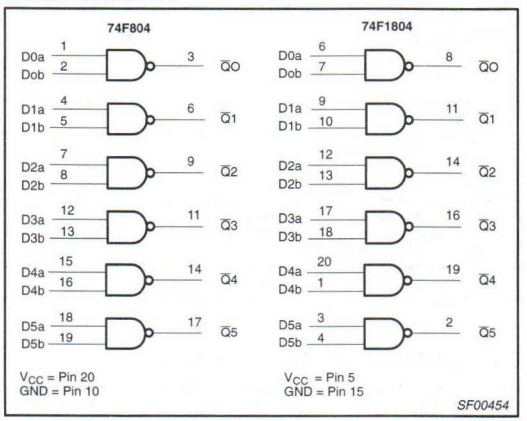
PIN CONFIGURATION



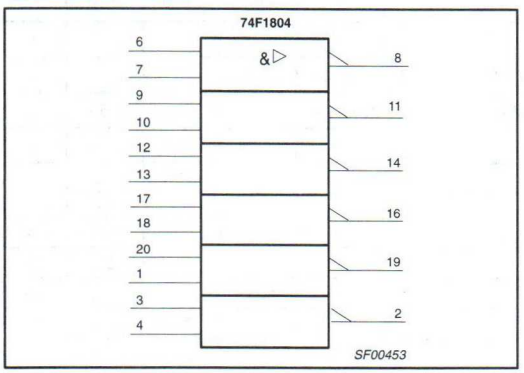
LOGIC SYMBOL



LOGIC DIAGRAM



IEC/IEEE SYMBOL



FUNCTION TABLE

INPUTS		OUTPUT
Da	**Db**	**$\overline{Q}$**
H	H	L
L	X	H
X	L	H

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	96	mA
T_{amb}	Operating free–air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–48	mA
I_{OL}	Low–level output current			48	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.0			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.38	0.55	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.38	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				-20	µA
I_O	Output current[3]		V_{CC} = MAX		-60		-160	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		2.0	3.0	mA
		I_{CCL}	V_{CC} = MAX	V_{IN} = 4.5V		15	20	mA

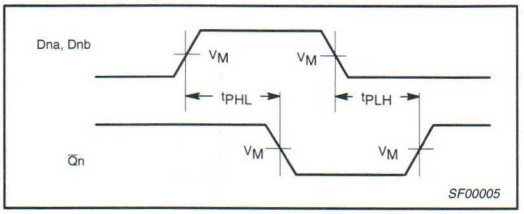
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short–circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

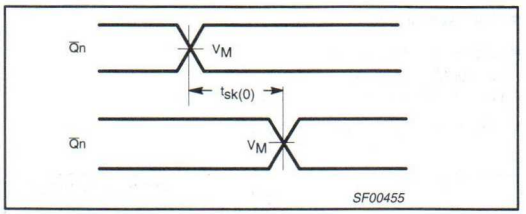
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to $\overline{Q}$n	Waveform 1	1.0 1.0	2.0 3.0	4.0 4.5	1.0 1.0	4.0 5.0	ns
$t_{sk(o)}$	Output skew[1,2]	Waveform 2			1.5		1.5	ns

NOTES:
1. [t_{PN} actual – t_{PM} actual] for any output compared to any other output where N and M are either LH or HL.
2. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

AC WAVEFORMS



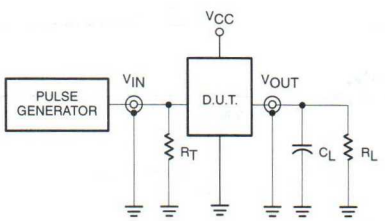
Waveform 1. Propagation delay for inverting outputs



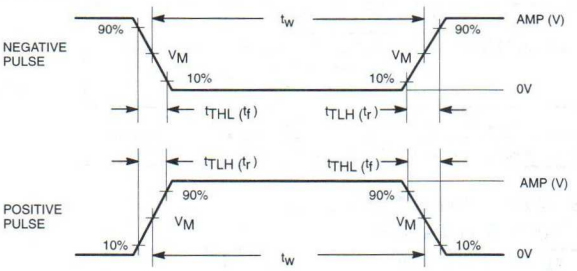
Waveform 2. Output skew

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Hex 2-input NOR drivers | 74F805/74F1805

FEATURES

- High capacitive drive capability
- Choice of configuration
  Corner V_{CC} and GND – 74F805
  Center V_{CC} and GND – 74F1805
- Typical propagation delay of 2.3ns

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F805	2.3ns	10mA
74F1805	2.3ns	10mA

ORDERING INFORMATION

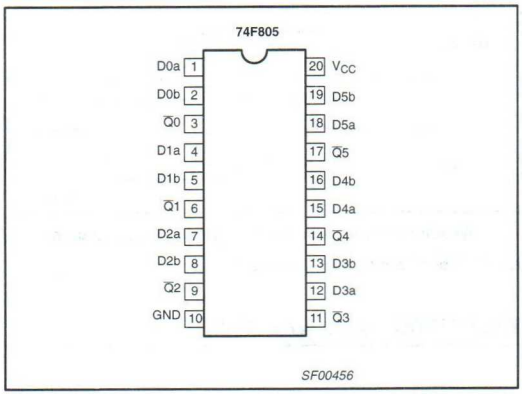
DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
20–pin plastic DIP	N74F805N, N74F1805N	SOT146-1
20–pin plastic SOL	N74F805D, N74F1805D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

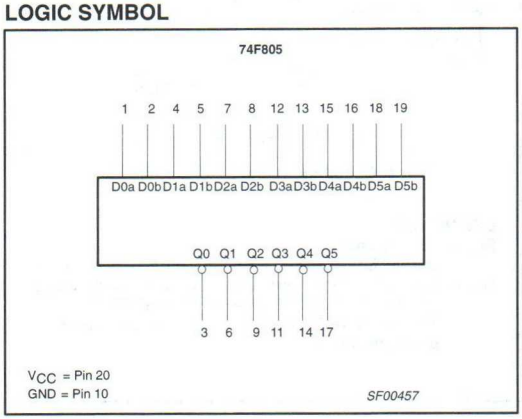
PINS	DESCRIPTION	74F (U.L.) HIGH/ LOW	LOAD VALUE HIGH/LOW
Dna – Dnb	Data inputs	1.0/0.033	20µA/20µA
$\overline{Q}0 – \overline{Q}5$	Data outputs	2400/80	48mA/48mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

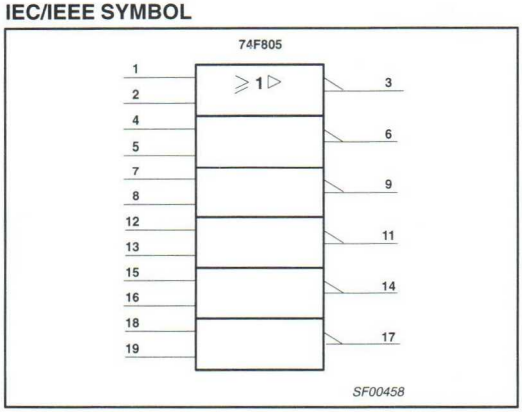
PIN CONFIGURATION



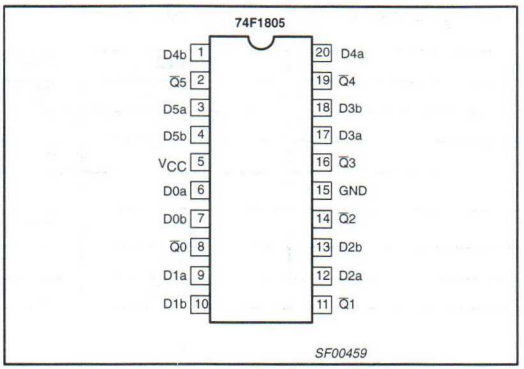
LOGIC SYMBOL



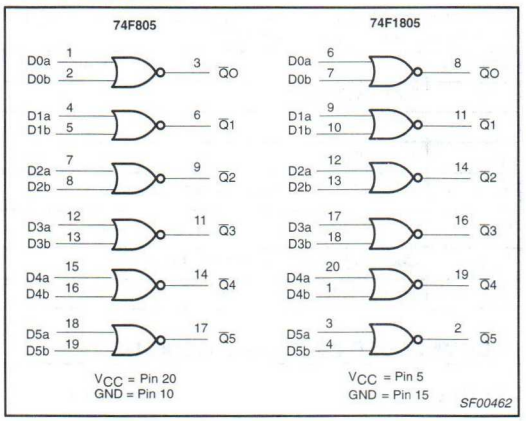
IEC/IEEE SYMBOL



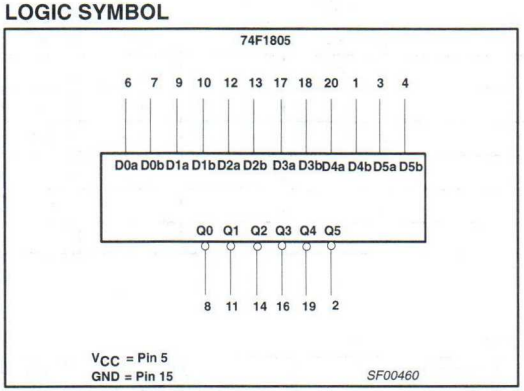
PIN CONFIGURATION



LOGIC DIAGRAM



LOGIC SYMBOL



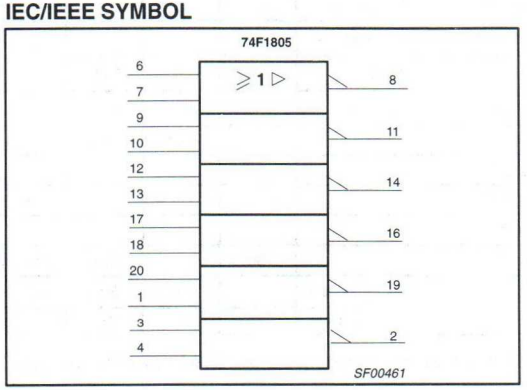
FUNCTION TABLE

INPUTS		OUTPUT
Dna	Dnb	$\overline{Q}n$
H	X	L
X	H	L
L	L	H

Notes to function table

H = High voltage level
L = Low voltage level
X = Don't care

IEC/IEEE SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	96	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–48	mA
I_{OL}	Low–level output current			48	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.0			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.38	0.55	V
			V_{IH} = MIN, I_{OI} = MAX	±5%V_{CC}		0.38	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				-20	µA
I_O	Output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		3.0	5.0	mA
		I_{CCL}		V_{IN} = 4.5V		17	25	mA

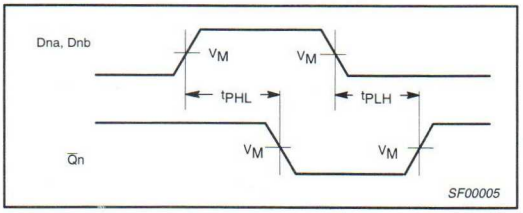
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short–circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

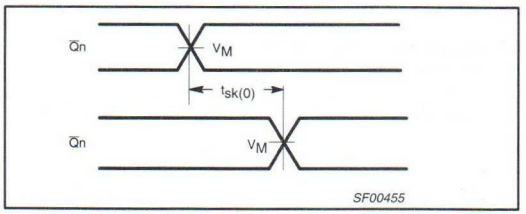
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to $\overline{Q}$n	Waveform 1	1.0 1.0	2.0 2.5	4.0 4.5	1.0 1.0	4.0 4.5	ns
$t_{sk(o)}$	Output skew[1,2]	Waveform 2			1.5		1.5	ns

NOTES:
1. [t_{PN} actual – t_{PM} actual] for any output compared to any other output where N and M are either LH or HL.
2. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

AC WAVEFORMS



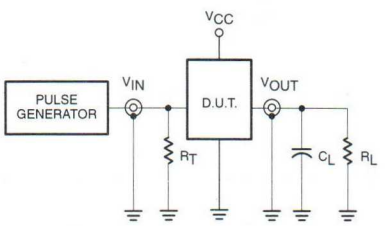
Waveform 1. Propagation delay for inverting output



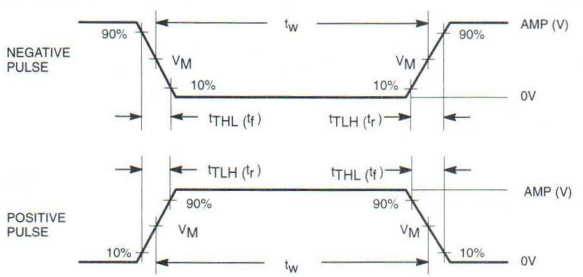
Waveform 2. Output skew

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SF00006

Hex 2-input AND drivers | 74F808/74F1808

FEATURES

- High capacitive drive capability
- Choice of configuration
  Corner V_{CC} and GND – 74F808
  Center V_{CC} and GND – 74F1808
- Typical propagation delay of 4.0ns
- Superior ground noise characteristics (implemented using output edge rate control)
- Increased source and sink current (64mA)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F808	4.0ns	24mA
74F1808	4.0ns	24mA

ORDERING INFORMATION

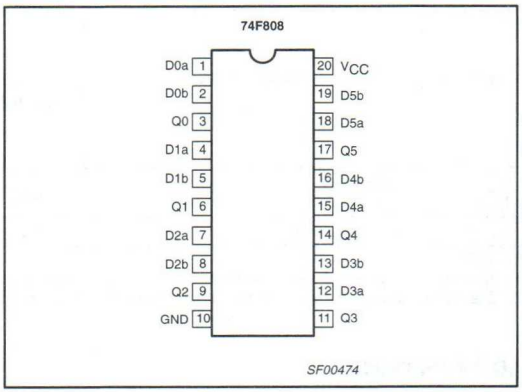
DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
20–pin plastic DIP	N74F808N, N74F1808N	SOT 146-1
20–pin plastic SOL	N74F808D, N74F1808D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

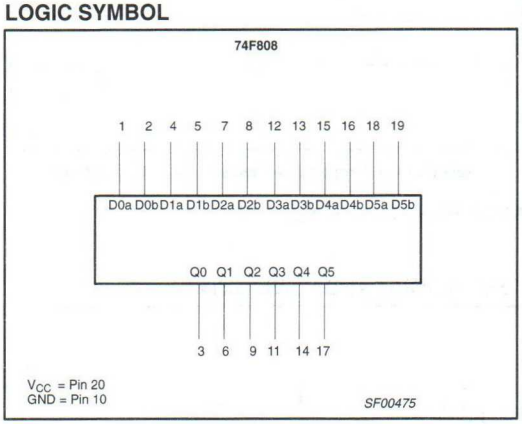
PINS	DESCRIPTION	74F (U.L.) HIGH/ LOW	LOAD VALUE HIGH/LOW
Dna – Dnb	Data inputs	1.0/0.033	20μA/20μA
Q0 – Q5	Data outputs	3200/106.	64mA/64mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.

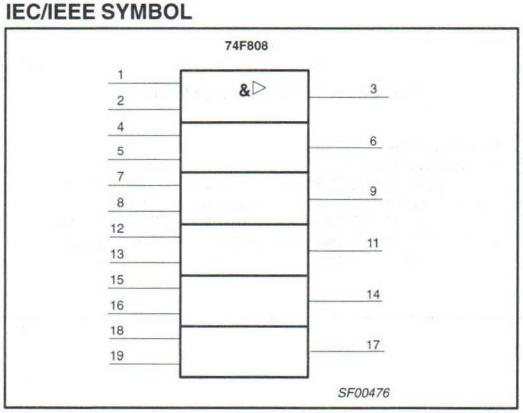
PIN CONFIGURATION



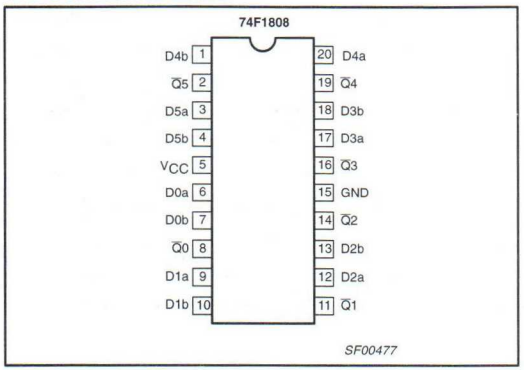
LOGIC SYMBOL



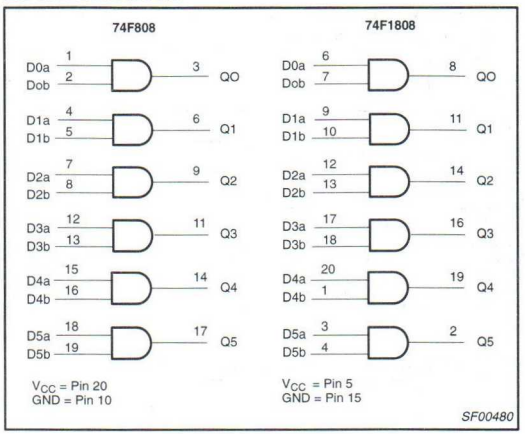
IEC/IEEE SYMBOL



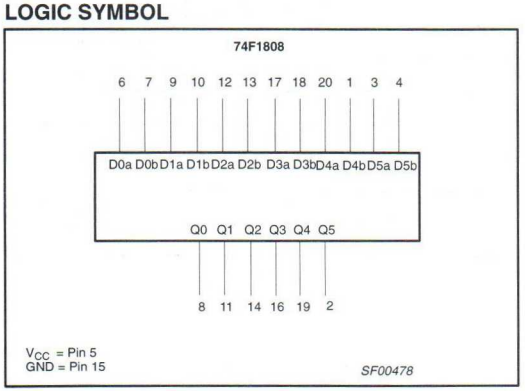
PIN CONFIGURATION



LOGIC DIAGRAM



LOGIC SYMBOL



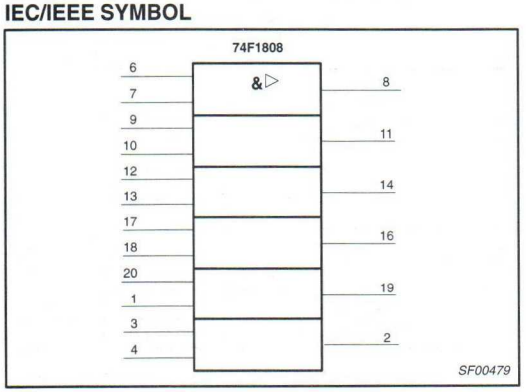
FUNCTION TABLE

INPUTS		OUTPUT
Da	Db	Q
H	H	H
L	X	L
X	L	L

NOTES:

H = High voltage level
L = Low voltage level
X = Don't care

IEC/IEEE SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	96	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–64	mA
I_{OL}	Low–level output current			64	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.0			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.38	0.55	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.38	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				-20	µA
I_O	Output current[3]		V_{CC} = MAX		-60		-180	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		19	27	mA
		I_{CCL}		V_{IN} = 4.5V		30	42	mA

NOTES:

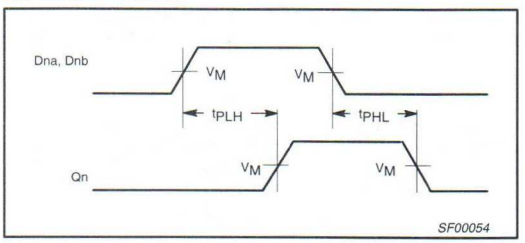
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short–circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

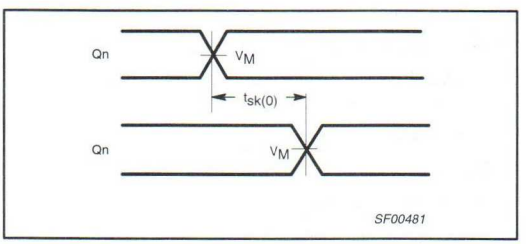
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to Qn	Waveform 1	2.0 2.0	4.5 3.5	6.3 6.0	2.0 1.5	6.8 6.5	ns
$t_{sk(o)}$	Output skew[1,2]	Waveform 2			2.5		3.0	ns

NOTES:
1. [t_{PN} actual – t_{PM} actual] for any output compared to any other output where N and M are either LH or HL.
2. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

AC WAVEFORMS



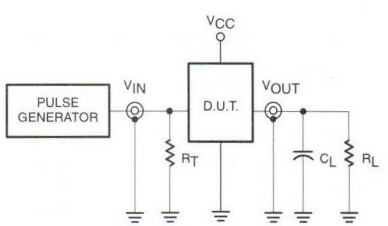
Waveform 1. Propagation delay for inverting outputs



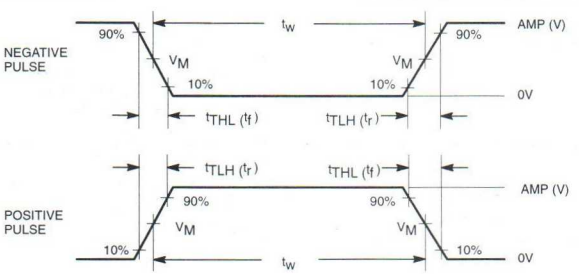
Waveform 2. Output skew

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor;
see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Bus interface registers | 74F821/822/823/824/825/826

74F821 10-bit bus interface register, non-inverting (3-State)
74F822 10-bit bus interface register, inverting (3-State)
74F823 9-bit bus interface register, non-inverting (3-State)
74F824 9-bit bus interface register, inverting (3-State)
74F825 8-bit bus interface register, non-inverting (3-State)
74F826 8-bit bus interface register, inverting (3-State)

FEATURES

- High speed parallel registers with positive edge-triggered D-type flip-flops
- High performance bus interface buffering for wide data/address paths or busses carrying parity
- High impedance PNP base inputs for reduced loading (20μA in high and low states)
- I_{IL} is 20μA vs 1000μA for AM29821 series
- Buffered control inputs to reduce AC effects
- Ideal where high speed, light loading, or increased fan-in as required with MOS microprocessor
- Positive and negative over-shoots are clamped to ground
- 3-State outputs glitch free during power-up and power-down
- Slim Dip 300 mil package
- Broadside pinout compatible with AMD AM 29821-29826 series
- Outputs sink 64mA and source 24mA
- Industrial temperature range available (–40°C to +85°C) for 74F823

DESCRIPTION

The 74F821 series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of busses carrying parity.

The 74F821/74F822 are buffered 10-bit wide versions of the popular 74F374/74F534 functions.

The 74F822 is the inverted output version of 74F821.

The 74F823 and 74F824 are 9-bit wide buffered registers with clock enable ($\overline{CE}$) and master reset ($\overline{MR}$) which are ideal for parity bus interfacing in high microprogrammed systems.

The 74F824 is the inverted version of 74F823.

The 74F825 and 74F826 are 8-bit buffered registers with all the 74F823/74F824 controls plus output enable ($\overline{OE}0$, $\overline{OE}1$, $\overline{OE}2$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. They are ideal for uses as an output port requiring high I_{OL}/I_{OH}.

The 74F826 is the inverted version of 74F825.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F821, 74F822	180MHz	75mA
74F823, 74F824	180MHz	70mA
74F825, 74F826	180MHz	65mA

ORDERING INFORMATION

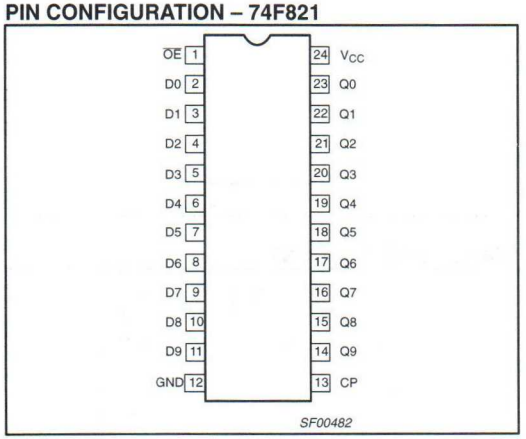
DESCRIPTION	ORDER CODE		PKG. DWG. #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
24-pin plastic slim DIP (300mil)	N74F821N, N74F822N, N74F823N, N74F824N, N74F825N, N74F826N	I74F823N	SOT222-1
24-pin plastic SOL	N74F821D, N74F822D, N74F823D, N74F824D, N74F825D, N74F826D	I74F823D	SOT137-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

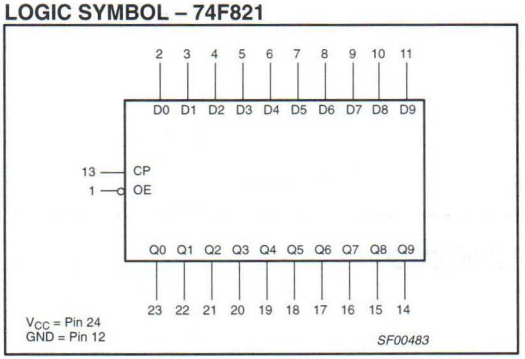
PINS		DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
74F821 74F822	Dn	Data inputs	1.0/1.0	20μA/0.6mA
	CP	Clock input	1.0/1.0	20μA/0.6mA
	$\overline{OE}$	Output enable input (active low)	1.0/3.0	20μA/1.8mA
	Qn, $\overline{Qn}$	Data outputs	1200/106.7	24mA/64mA
74F823 74F824	Dn	Data inputs	1.0/1.0	20μA/0.6mA
	CP	Clock input	1.0/1.0	20μA/0.6mA
	$\overline{CE}$	Clock enable input (active low)	1.0/3.0	20μA/1.8mA
	$\overline{MR}$	Master reset input (active low)	1.0/3.0	20μA/1.8mA
	$\overline{OE}$	Output enable input (active low)	1.0/3.0	20μA/1.8mA
	Qn, $\overline{Qn}$	Data outputs	1200/106.7	24mA/64mA
74F825 74F826	Dn	Data inputs	1.0/1.0	20μA/0.6mA
	CP	Clock input	1.0/1.0	20μA/0.6mA
	$\overline{CE}$	Clock enable input (active low)	1.0/3.0	20μA/1.8mA
	$\overline{MR}$	Master reset input (active low)	1.0/3.0	20μA/1.8mA
	$\overline{OE}$	Output enable input (active low)	1.0/3.0	20μA/1.8mA
	Qn, $\overline{Qn}$	Data outputs	1200/106.7	24mA/64mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.

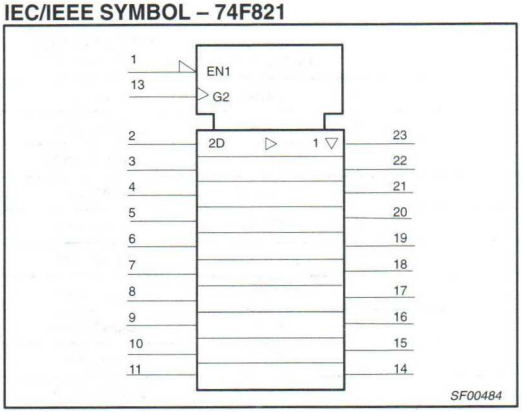
PIN CONFIGURATION – 74F821



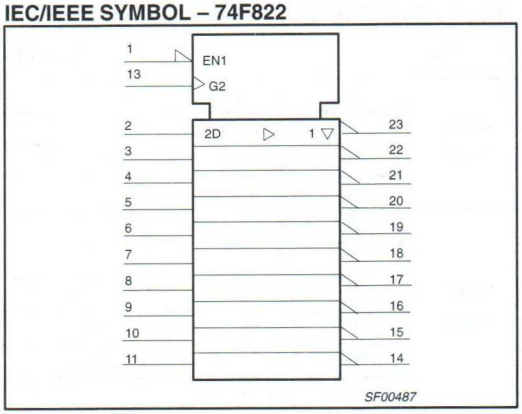
LOGIC SYMBOL – 74F821



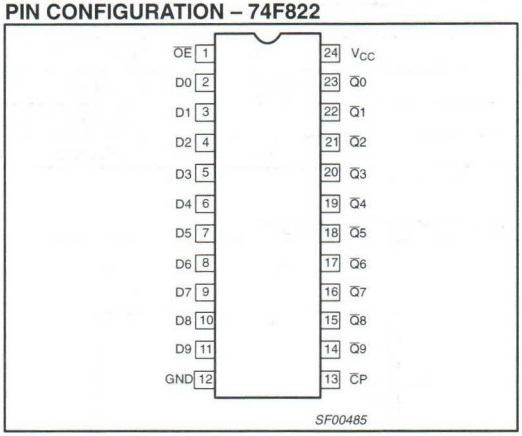
IEC/IEEE SYMBOL – 74F821



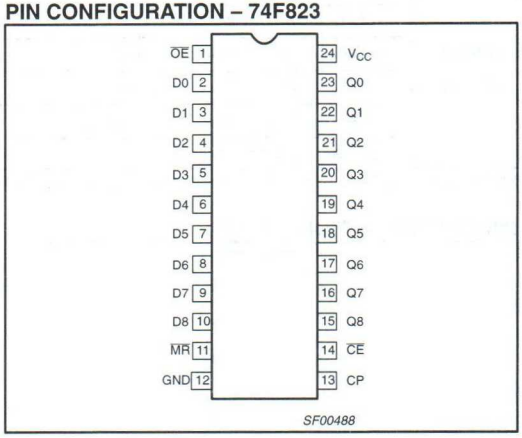
IEC/IEEE SYMBOL – 74F822



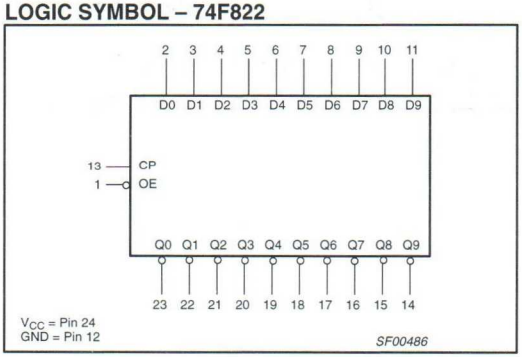
PIN CONFIGURATION – 74F822



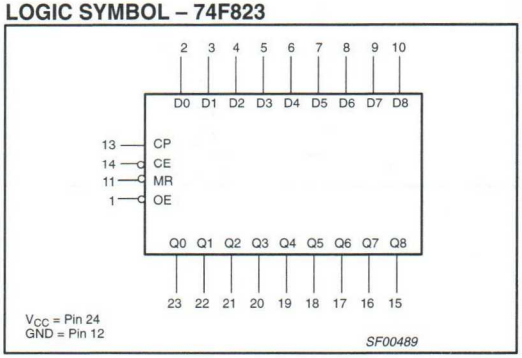
PIN CONFIGURATION – 74F823



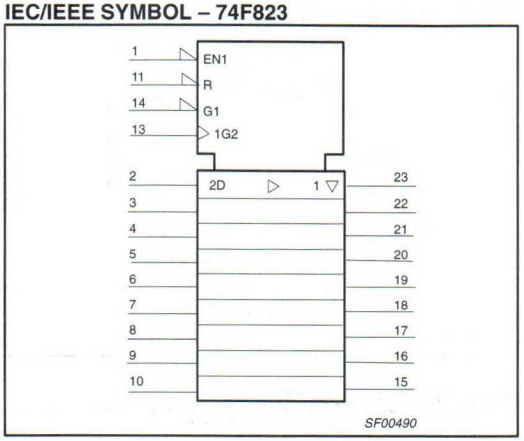
LOGIC SYMBOL – 74F822



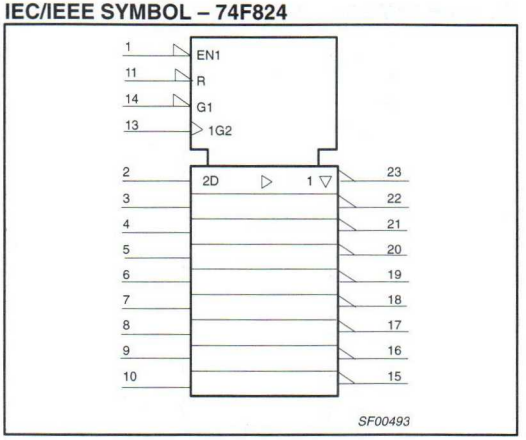
LOGIC SYMBOL – 74F823



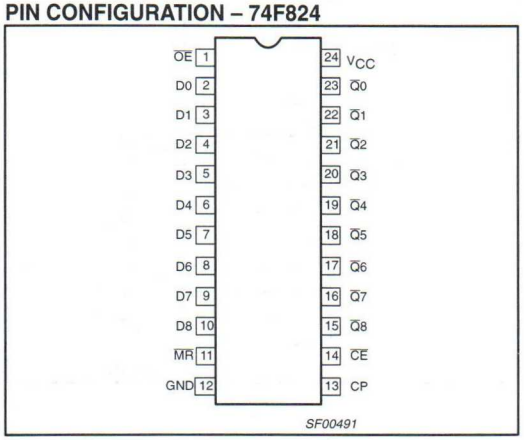
IEC/IEEE SYMBOL – 74F823



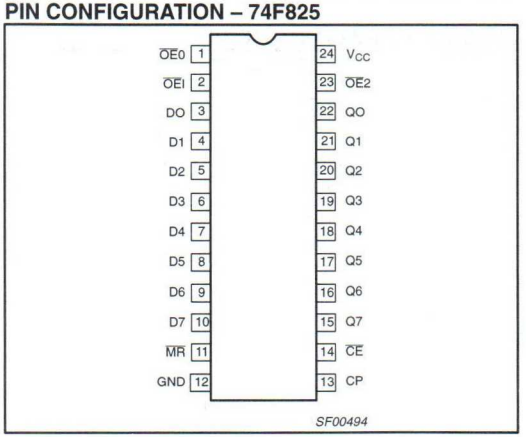
IEC/IEEE SYMBOL – 74F824



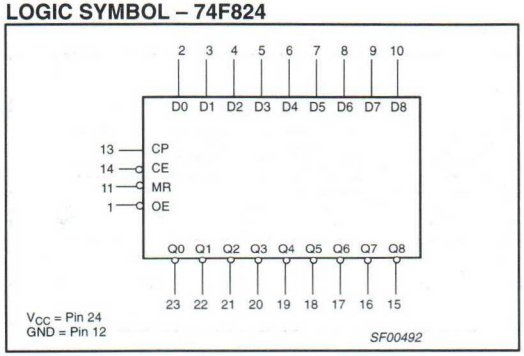
PIN CONFIGURATION – 74F824



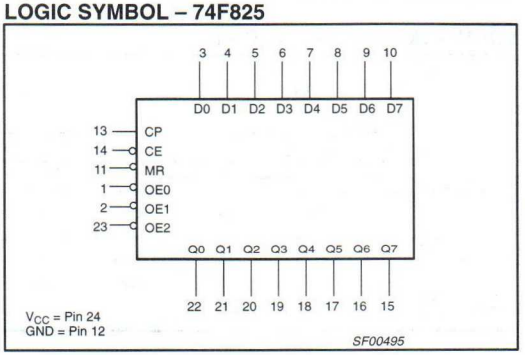
PIN CONFIGURATION – 74F825



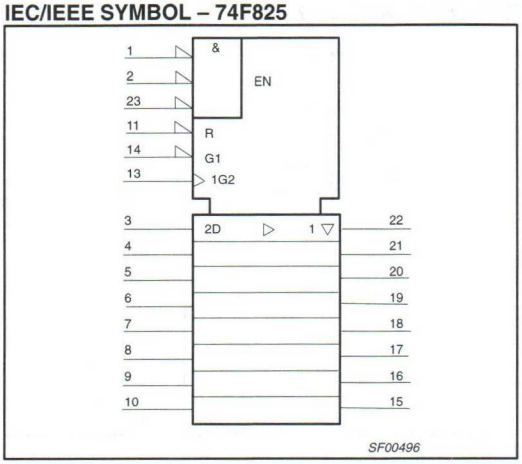
LOGIC SYMBOL – 74F824



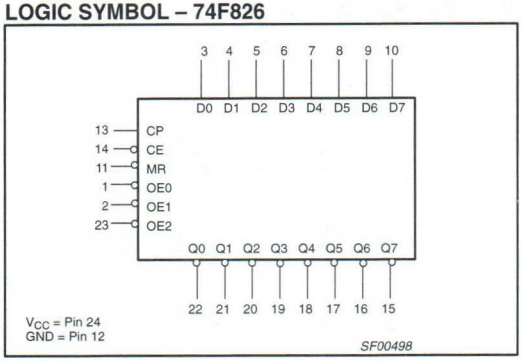
LOGIC SYMBOL – 74F825



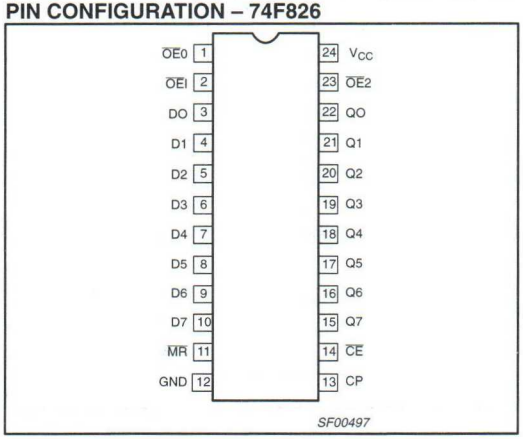
IEC/IEEE SYMBOL – 74F825



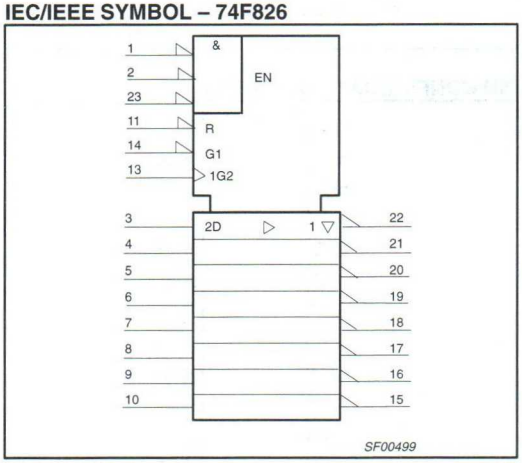
LOGIC SYMBOL – 74F826



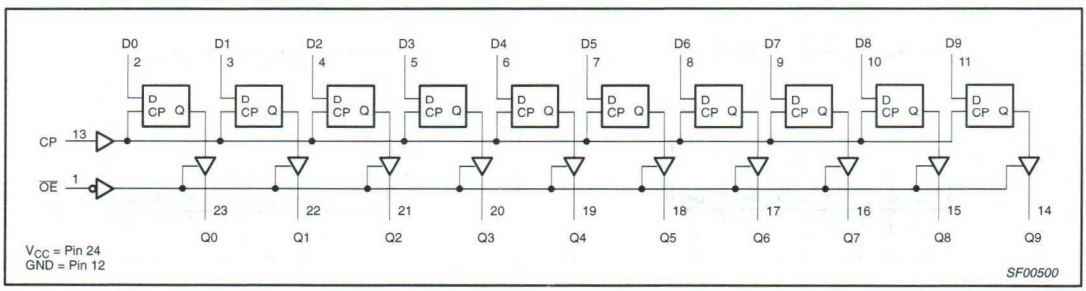
PIN CONFIGURATION – 74F826



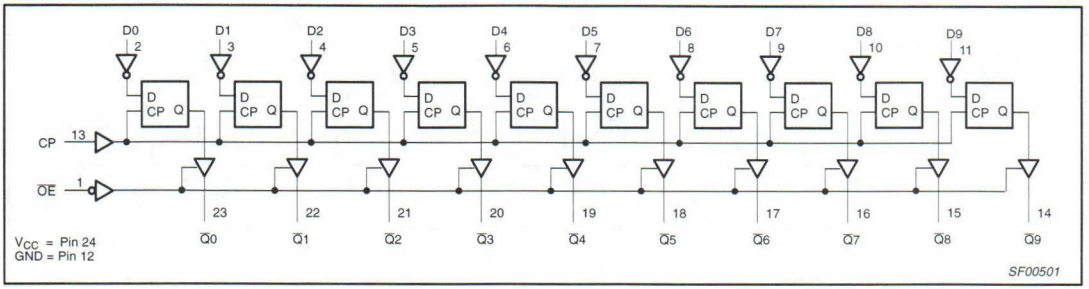
IEC/IEEE SYMBOL – 74F826



LOGIC DIAGRAM FOR 74F821



LOGIC DIAGRAM FOR 74F822

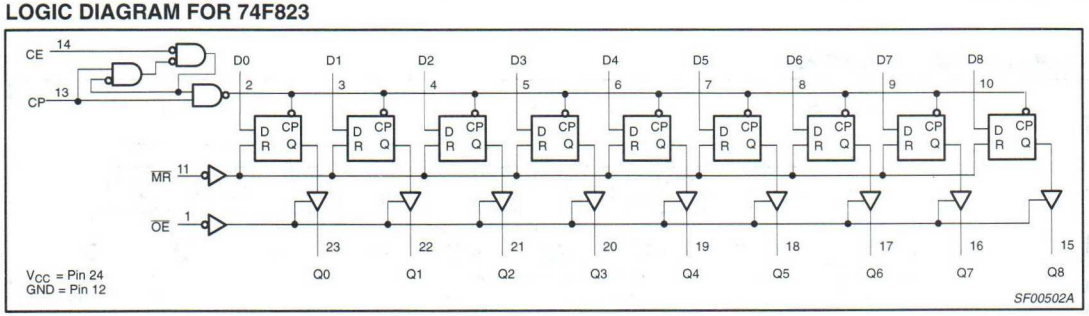


FUNCTION TABLE FOR 74F821 AND 74F822

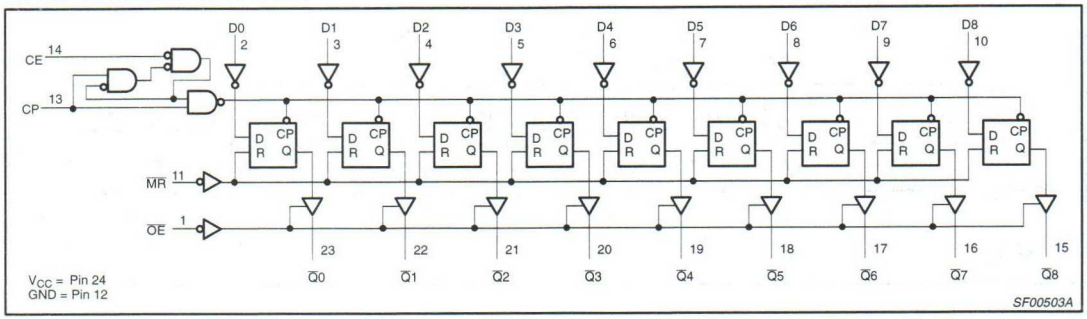
INPUTS			OUTPUTS		OPERATING MODE
			74F821	74F822	
$\overline{OE}$	CP	Dn	Q	$\overline{Q}$	
L	↑	l	L	H	Load and read data
L	↑	h	H	L	
L	↕	X	NC	NC	Hold
H	X	X	Z	Z	High impedance

H = High-voltage level
h = High state must be present one setup time before the low-to-high clock transition
L = Low-voltage level
l = Low state must be present one setup time before the low-to-high clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-high clock transition
↕ = Not low-to-high clock transition

LOGIC DIAGRAM FOR 74F823



LOGIC DIAGRAM FOR 74F824

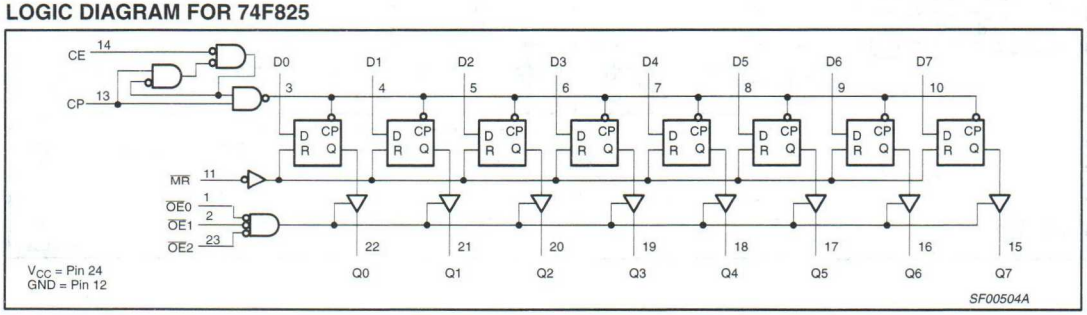


FUNCTION TABLE for 74F823 and 74F824

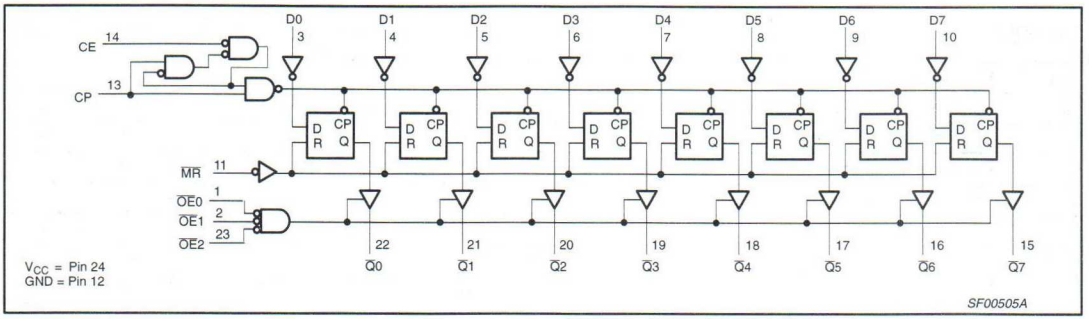
INPUTS					OUTPUTS		OPERATING MODE
					74F823	74F824	
$\overline{OE}$	$\overline{MR}$	$\overline{CE}$*	CP	Dn	Q	$\overline{Q}$	
L	L	X	X	X	L	L	Clear
L	H	L	↑	h	H	L	Load and read data
L	H	L	↑	l	L	H	
L	H	H	X	X	NC	NC	Hold
H	X	X	X	X	Z	Z	High impedance

H = High-voltage level
h = High state must be present one setup time before the low-to-high clock transition
L = Low-voltage level
l = Low state must be present one setup time before the low-to-high clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
* = Since $\overline{CE}$ input is sensitive to very short (<3ns) high-to-low-to-high going spikes while CP is high, users should avoid the use of decoders or other potentially glitch prone device on the $\overline{CE}$ input.
↑ = Low-to-high clock transition

LOGIC DIAGRAM FOR 74F825



LOGIC DIAGRAM FOR 74F826



FUNCTION TABLE FOR 74F825 AND 74F826

INPUTS					OUTPUTS		OPERATING MODE
					74F825	74F826	
$\overline{OE}n$	$\overline{MR}$	$\overline{CE}$*	CP	Dn	Q	$\overline{Q}$	
L	L	X	X	X	L	L	Clear
L	H	L	↑	h	H	L	Load and read data
L	H	L	↑	l	L	H	
L	H	H	X	X	NC	NC	Hold
H	X	X	X	X	Z	Z	High impedance

H = High-voltage level
h = High state must be present one setup time before the low-to-high clock transition
L = Low-voltage level
l = Low state must be present one setup time before the low-to-high clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
* = Since $\overline{CE}$ input is sensitive to very short (<3ns) high-to-low-to-high going spikes while CP is high, users should avoid the use of decoders or other potentially glitch prone device on the $\overline{CE}$ input.
↑ = Low-to-high clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		128	mA
T_{amb}	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current				–24	mA
I_{OL}	Low–level output current				64	mA
T_{amb}	Operating free-air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –15mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.4			V
					I_{OH} = –24mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}			0.55	V
						±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High–level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current			V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{OZH}	Off–state output current, high–level voltage applied			V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off–state output current, low–level voltage applied			V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short–circuit output current[3]			V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	74F821, 74F822	I_{CCH}	V_{CC} = MAX				75	105	mA
			I_{CCL}					75	105	mA
			I_{CCZ}					75	115	mA
		74F823, 74F824	I_{CCH}	V_{CC} = MAX				65	100	mA
			I_{CCL}					70	105	mA
			I_{CCZ}					75	110	mA
		74F825, 74F826	I_{CCH}	V_{CC} = MAX				60	85	mA
			I_{CCL}					60	90	mA
			I_{CCZ}					65	95	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS FOR 74F821/74F822/74F824/74F825/74F826

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency		Waveform 1	150	180		140		ns
t_{PLH} t_{PHL}	Propagation delay CP to Qn or $\overline{Qn}$	74F821, 74F825, 74F826	Waveform 1	4.0 4.0	6.5 6.0	8.5 8.5	4.0 3.5	9.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Qn}$	74F822, 74F824	Waveform 1	4.5 4.5	6.5 6.5	9.0 9.0	4.5 4.5	10.0 9.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn or $\overline{Qn}$	74F824 74F825, 74F826	Waveform 2	3.0	5.0	8.0	3.0	8.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$n to Qn or $\overline{Qn}$		Waveform 4 Waveform 5	2.0 3.0	4.5 5.0	8.0 8.0	2.0 2.5	9.0 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$n to Qn or $\overline{Qn}$		Waveform 4 Waveform 5	1.5 1.5	3.5 3.5	6.5 6.5	1.5 1.5	7.5 7.5	ns

AC SETUP REQUIREMENTS FOR 74F821/74F822/74F824/74F825/74F826

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low Dn to CP		Waveform 3	1.0 1.0			1.0 1.0		ns
t_h (H) t_h (L)	Hold time, high or low Dn to CP		Waveform 3	2.0 2.0			2.0 2.0		ns
t_w (H) t_w (L)	CP Pulse width, high or low		Waveform 1	3.5 3.5			4.0 4.0		ns
t_{su} (H) t_{su} (L)	Setup time, high or low, $\overline{CE}$ to CP	74F824, 74F825, 74F826	Waveform 3	0.0 2.0			0.0 2.0		ns
t_h (H) t_h (L)	Hold time, high or low $\overline{CE}$ to CP		Waveform 3	0.0 3.0			0.0 3.5		ns
t_w (L)	$\overline{MR}$ Pulse width, low		Waveform 2	4.5			4.5		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP		Waveform 2	2.5			2.5		ns

AC ELECTRICAL CHARACTERISTICS FOR 74F823

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	150	180		140		130		ns
t_{PLH} t_{PHL}	Propagation delay CP to Qn or $\overline{Q}$n	Waveform 1	4.0 4.0	6.5 6.0	8.5 8.5	4.0 3.5	9.5 9.0	4.0 3.5	10.0 9.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn or $\overline{Q}$n	Waveform 2	3.0	5.0	8.0	3.0	8.0	3.0	8.5	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$n to Qn or $\overline{Q}$n	Waveform 4 Waveform 5	2.0 3.0	4.5 5.0	8.0 8.0	2.0 2.5	9.0 9.0	2.0 2.5	11.0 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$n to Qn or $\overline{Q}$n	Waveform 4 Waveform 5	1.5 1.5	3.5 3.5	6.5 6.5	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns

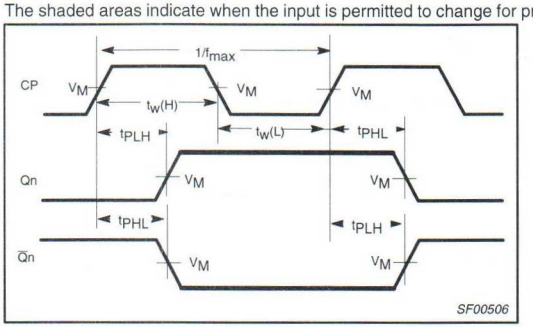
AC SETUP REQUIREMENTS FOR 74F823

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low Dn to CP	Waveform 3	1.0 1.0			1.0 1.0		2.0 1.5		ns
t_h (H) t_h (L)	Hold time, high or low Dn to CP	Waveform 3	2.0 2.0			2.0 2.0		2.5 2.0		ns
t_w (H) t_w (L)	CP Pulse width, high or low	Waveform 1	3.5 3.5			4.0 4.0		4.0 4.0		ns
t_{su} (H) t_{su} (L)	Setup time, high or low, $\overline{CE}$ to CP	Waveform 3	0.0 2.0			0.0 2.0		0.0 2.0		ns
t_h (H) t_h (L)	Hold time, high or low $\overline{CE}$ to CP	Waveform 3	0.0 3.0			0.0 3.5		1.5 4.0		ns
t_w (L)	$\overline{MR}$ Pulse width, low	Waveform 2	4.5			4.5		4.5		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 2	2.5			2.5		2.5		ns

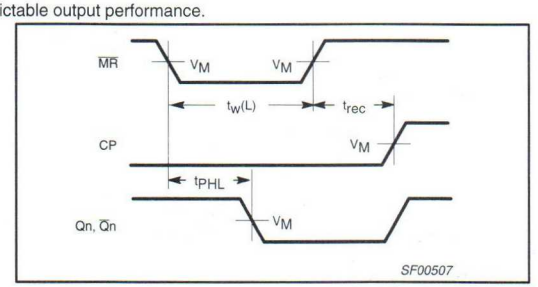
AC WAVEFORMS

For all waveforms, $V_M = 1.5V$.

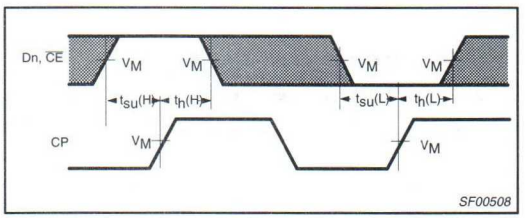
The shaded areas indicate when the input is permitted to change for predictable output performance.



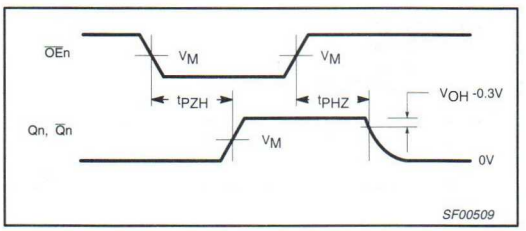
Waveform 1. Propagation delay for clock input to output, clock pulse width, and maximum clock frequency



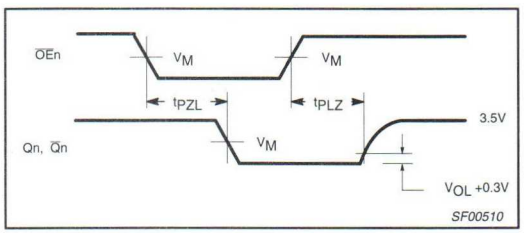
Waveform 2. Master reset pulse width, master reset to output delay and master reset to clock recovery time



Waveform 3. Data setup time and hold times

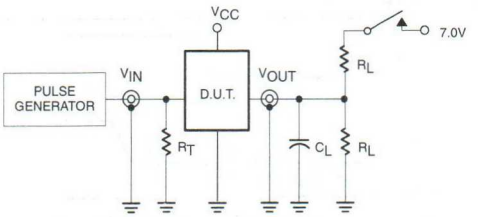


Waveform 4. 3-State output enable time to high level and output disable time from high level

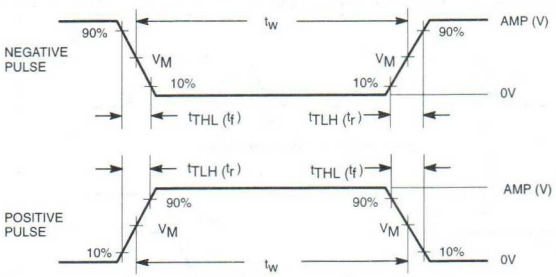


Waveform 5. 3-State output enable time to low level and output disable time from low level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

74F827 10-bit buffer/line driver, non-inverting (3-State)
74F828 10-bit buffer/line driver, inverting (3-State)

FEATURES

- High impedance NPN base inputs for reduced loading (20μA in High and Low states)
- I_{IL} is 20μA vs FAST family spec of 600μA and 1000μA for AMD 29827/29828 series
- Ideal where high speed, light bus loading and increased fan-in are required
- Controlled rise and fall times to minimize ground bounce
- Glitch free power-up in 3-State
- Flow through pinout architecture for microprocessor oriented applications
- Outputs sink 64mA
- 74F827 available in SSOP type II package

DESCRIPTION

The 74F827 and 74F828 10-Bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NOR Output Enables ($\overline{OE0}$, $\overline{OE1}$) for maximum control flexibility.

The 74F827 and 74F828 are functionally and pin compatible to AMD AM29827 and AM29828. The 74F828 is an inverting version of 74F827.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F827	6.0ns	60mA
74F828	6.0ns	55mA

ORDERING INFORMATION

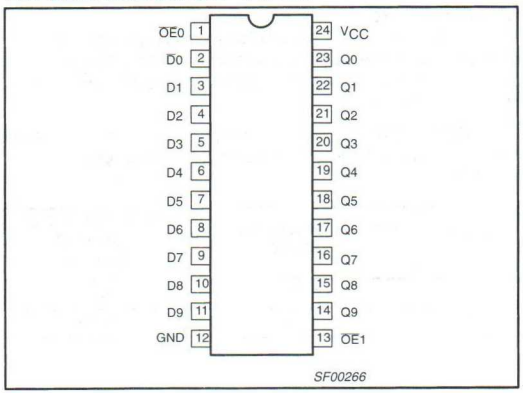
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C	DRAWING NUMBER
24-Pin Plastic DIP (300 mil)	N74F827N, N74F828N	SOT222-1
24-Pin Plastic SOL	N74F827D, N74F828D	SOT137-1
24-Pin Plastic SSOP Type II	N74F827DB	SOT340-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

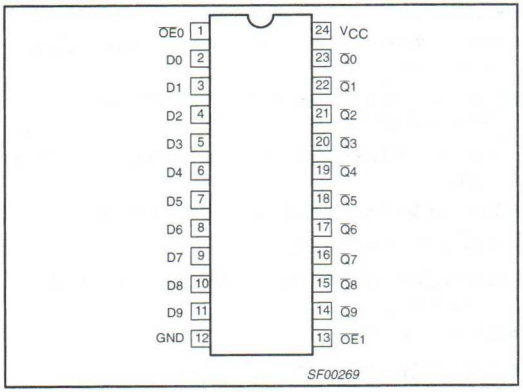
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0-D9	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE0}$-$\overline{OE1}$	Output enable inputs (active Low)	1.0/0.033	20μA/20μA
Q0-Q9	Data outputs (74F827)	1200/106.7	24mA/64mA
$\overline{Q0}$-$\overline{Q9}$	Data outputs (74F828)	1200/106.7	24mA/64mA

NOTES:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6 mA in the Low state.

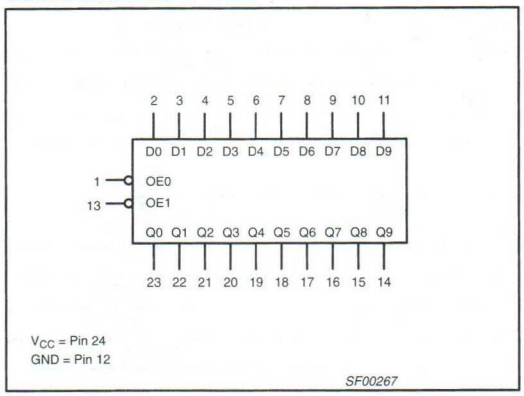
PIN CONFIGURATION - 74F827



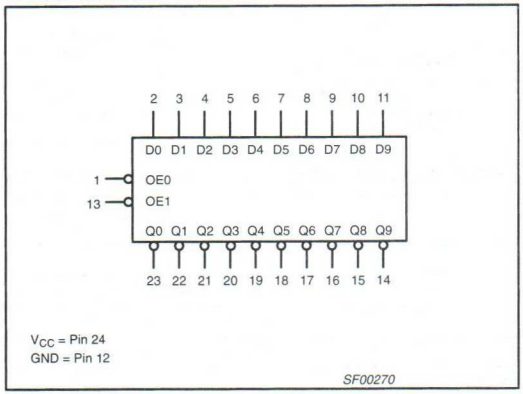
PIN CONFIGURATION - 74F828



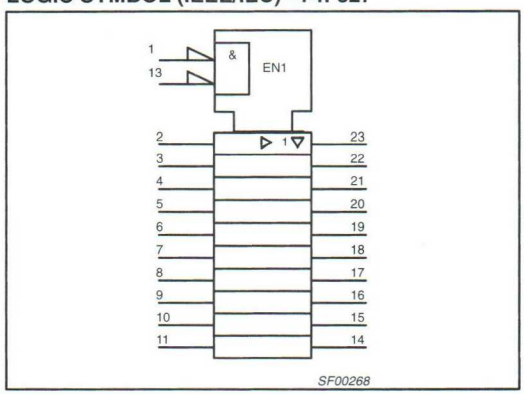
LOGIC SYMBOL - 74F827



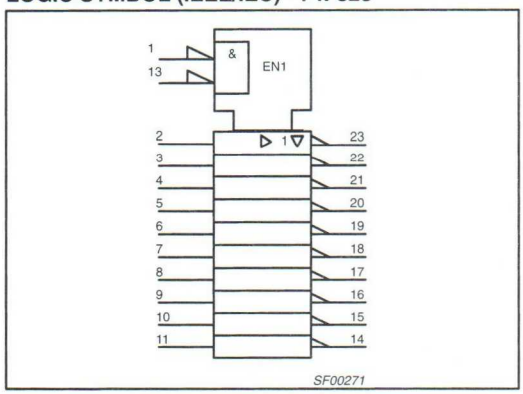
LOGIC SYMBOL - 74F828



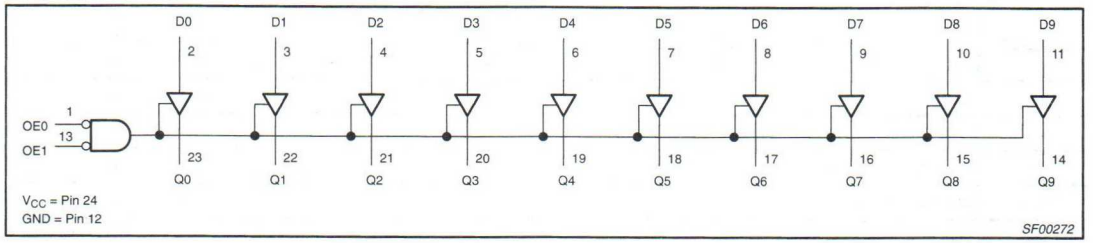
LOGIC SYMBOL (IEEE/IEC) - 74F827



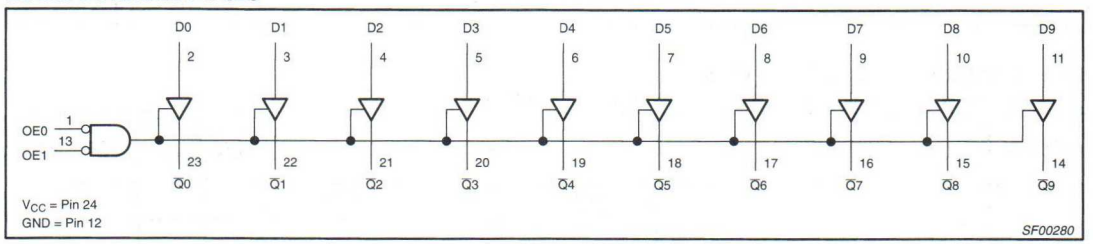
LOGIC SYMBOL (IEEE/IEC) - 74F828



LOGIC DIAGRAM 74F827



LOGIC DIAGRAM 74F828



FUNCTION TABLE

INPUTS		OUTPUTS		OPERATING MODE
		74F827	74F828	
$\overline{OE}n$	Dn	Qn	$\overline{Q}n$	
L	L	L	H	Transparent
L	H	H	L	Transparent
H	X	Z	Z	High impedance

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to + 70	°C
T_{stg}	Storage temperature range	–65 to + 150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			64	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –15mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.4	3.3		V
				V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –24mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}			0.55	V
						±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{OZH}	Off-state output current, High voltage applied			V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low voltage applied			V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short circuit output current[3]			V_{CC} = MAX			–100		–225	mA
I_{CC}	Supply current (total)	74F827	I_{CCH}	V_{CC} = MAX				50	70	mA
			I_{CCL}					70	100	mA
			I_{CCZ}					60	90	mA
		74F828	I_{CCH}	V_{CC} = MAX				30	45	mA
			I_{CCL}					65	85	mA
			I_{CCZ}					55	70	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at one time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC CHARACTERISTICS

SYMBOL	PARAMETER			LIMITS					UNIT
				T_{amb} = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_{amb} = 0 °C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74F827	Waveform 1	2.0 2.0	5.5 4.5	8.5 8.5	2.0 2.0	9.0 9.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_n$ to Q_n		Waveform 3 Waveform 4	5.0 4.0	8.0 6.0	12.0 10.5	4.5 4.0	14.0 11.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_n$ to Q_n		Waveform 3 Waveform 4	2.5 2.5	5.0 5.0	8.0 8.0	2.0 2.0	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	74F828	Waveform 2	2.0 1.0	6.0 3.0	8.5 7.0	2.0 1.0	9.5 8.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_n$ to $\overline{Q}_n$		Waveform 3 Waveform 4	6.0 5.0	8.0 7.0	11.5 10.5	5.5 4.5	14.0 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_n$ to $\overline{Q}_n$		Waveform 3 Waveform 4	2.5 1.5	5.0 4.0	8.5 7.0	2.0 1.5	9.0 8.0	ns

AC CHARACTERISTICS

for 1 Output switching with C_L = 300pF and R_L = 500Ω load

SYMBOL	PARAMETER			LIMITS					UNIT
				T_{amb} = +25°C V_{CC} = 5V C_L = 300pF R_L = 500Ω			T_{amb} = 0 °C to +70°C V_{CC} = 5V ±10% C_L = 300pF R_L = 500Ω		
				MIN	Typ	Max	MIN	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74F827	Waveform 1		9.5 7.5	13.0 10.0		14.0 11.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_n$ to Q_n		Waveform 3 Waveform 4		15.0 9.5	20.0 13.0		21.0 14.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_n$ to Q_n		Waveform 3 Waveform 4		15.0 9.5	19.0 13.5		20.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	74F828	Waveform 2		10.0 6.0	13.0 9.0		14.0 10.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_n$ to $\overline{Q}_n$		Waveform 3 Waveform 4		15.5 10.5	19.0 13.0		21.0 14.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_n$ to $\overline{Q}_n$		Waveform 3 Waveform 4		15.0 10.0	18.0 13.0		20.0 14.5	ns

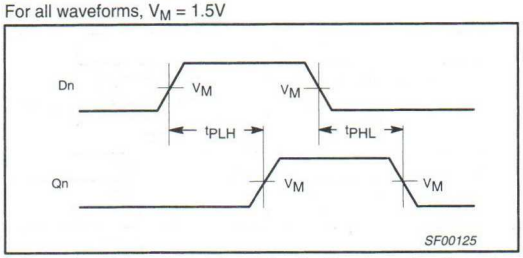
AC CHARACTERISTICS

for 10 Outputs switching with C_L = 300pF and R_L = 500Ω load

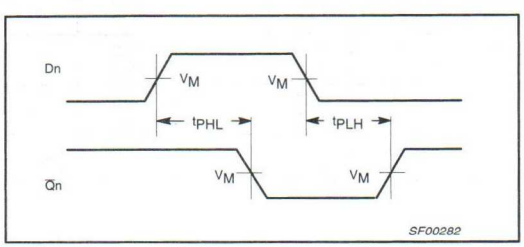
SYMBOL	PARAMETER			LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0 °C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				MIN	Typ	Max	MIN	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74F827	Waveform 1		12.0 14.0	16.0 17.0		17.0 18.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_n$ to Q_n		Waveform 3 Waveform 4		15.0 17.0	20.0 21.0		21.0 21.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_n$ to Q_n		Waveform 3 Waveform 4		15.0 12.5	19.0 15.5		20.0 16.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	74F828	Waveform 2		10.0 10.0	17.0 13.5		18.0 14.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_n$ to $\overline{Q}_n$		Waveform 3 Waveform 4		18.0 15.0	21.0 18.0		23.0 19.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_n$ to $\overline{Q}_n$		Waveform 3 Waveform 4		16.5 11.5	19.5 14.5		22.5 15.0	ns

AC WAVEFORMS

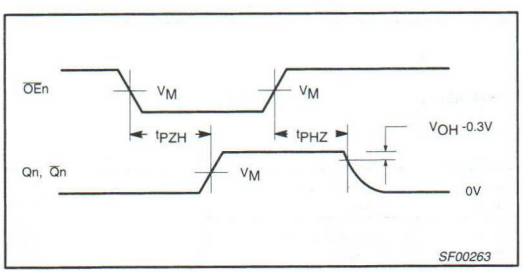
For all waveforms, V_M = 1.5V



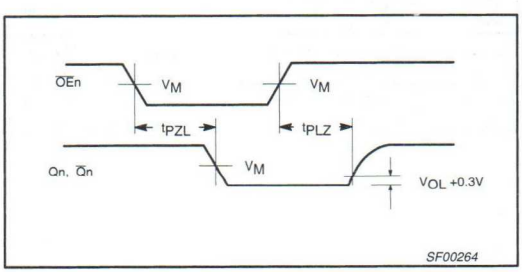
Waveform 1. Propagation Delay for Non-Inverting Output



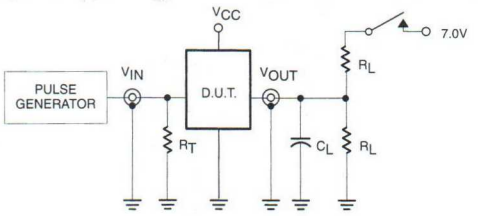
Waveform 2. Propagation Delay for Inverting Output



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



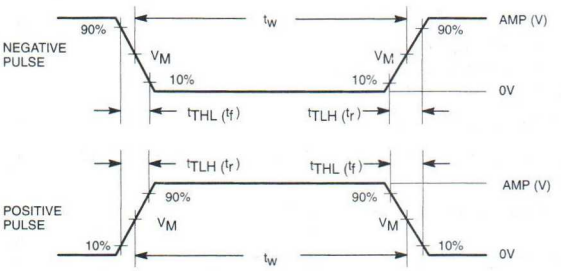
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



Test Circuit for Open Collector Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open



Input Pulse Definition

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

Hex 2-input OR drivers | 74F832/74F1832

FEATURES

- High capacitive drive capability
- Choice of configuration
  Corner V_{CC} and GND – 74F832
  Center V_{CC} and GND – 74F1832
- Typical propagation delay of 3.5ns
- Superior ground noise characteristics (implemented using output edge rate control)
- Increased source and sink current (64mA)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F832	3.5ns	26mA
74F1832	3.5ns	26mA

ORDERING INFORMATION

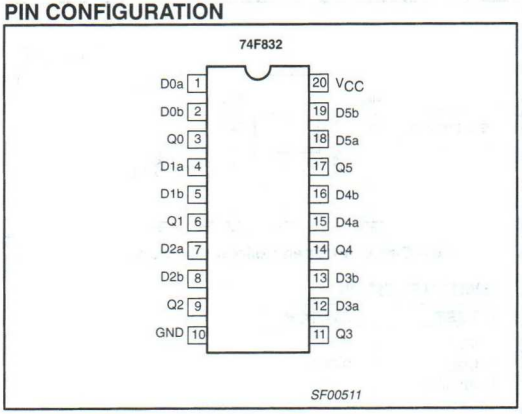
DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
20–pin plastic Dual In-line Package	N74F832N, N74F1832N	SOT146-1
20–pin plastic Small Outline Large	N74F832D, N74F1832D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

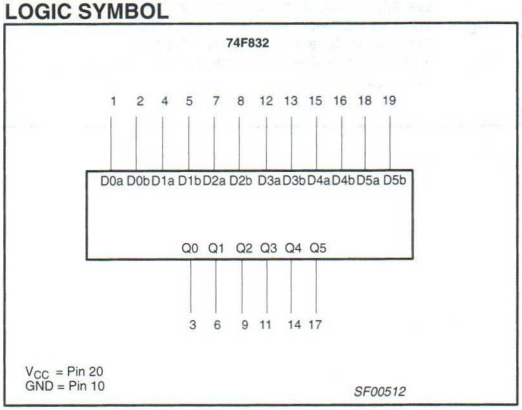
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna – Dnb	Data inputs	1.0/0.033	20µA/20µA
Q0 – Q5	Data outputs	3200/106.7	64mA/64mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

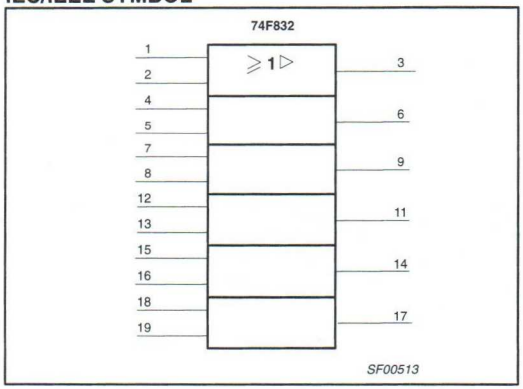
PIN CONFIGURATION



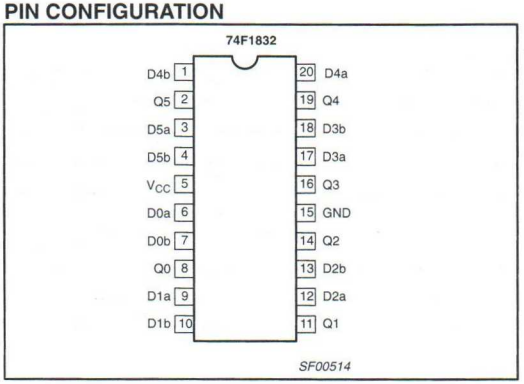
LOGIC SYMBOL



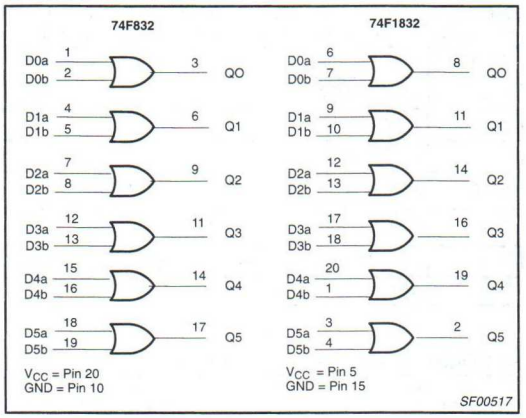
IEC/IEEE SYMBOL



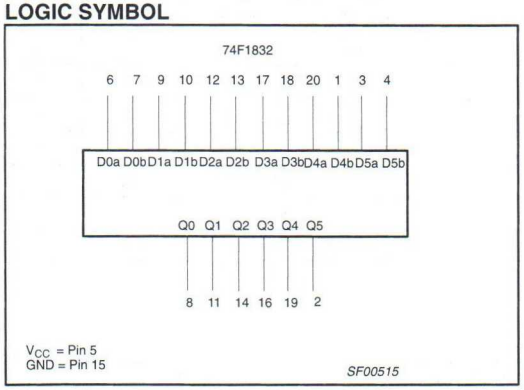
PIN CONFIGURATION



LOGIC DIAGRAM



LOGIC SYMBOL

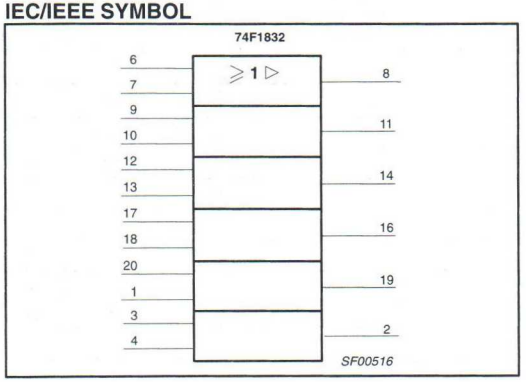


FUNCTION TABLE

INPUTS		OUTPUT
Dna	**Dnb**	**Qn**
H	X	H
X	H	H
L	L	L

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

IEC/IEEE SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	96	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–64	mA
I_{OL}	Low–level output current			64	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.0			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.38	0.55	V
			V_{IH} = MIN, I_{OI} = MAX	±5%V_{CC}		0.38	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				-20	µA
I_O	Output current[3]		V_{CC} = MAX		-60		-180	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		21	30	mA
		I_{CCL}		V_{IN} = 4.5V		31	44	mA

NOTES:

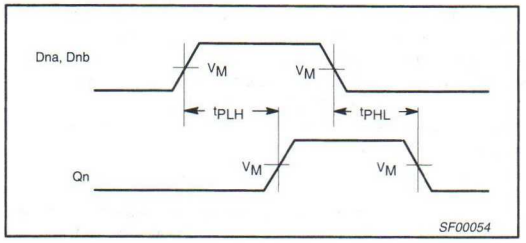
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short–circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

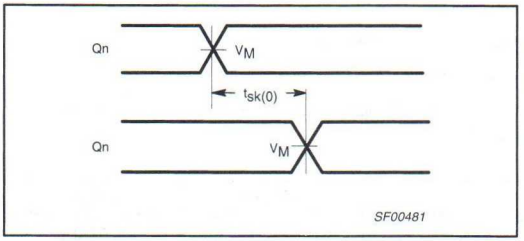
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to Qn	Waveform 1	2.0 2.0	4.0 3.5	6.0 6.0	2.0 1.5	6.5 6.5	ns
$t_{sk(o)}$	Output skew[1, 2]	Waveform 2			2.0		2.5	ns

NOTES:
1. $|t_{PN}$ actual – t_{PM} actual $|$ for any output compared to any other output where N and M are either LH or HL.
2. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

AC WAVEFORMS



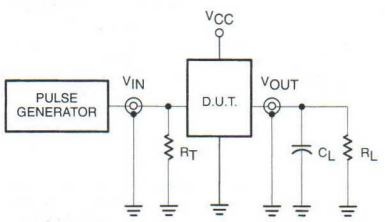
Waveform 1. Propagation delay for inverting output



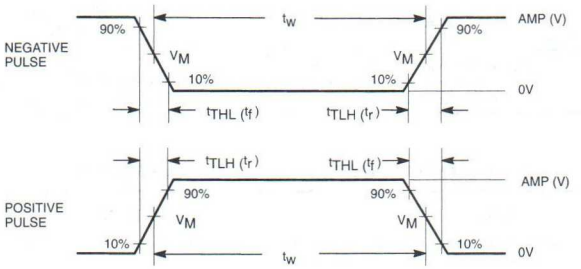
Waveform 2. Output skew

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor;
see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Bus interface latches

74F841/74F842/74F843/ ~~74F844*~~/74F845/74F846

74F841/74F842 10-bit bus interface latches, non-inverting/inverting (3-State)
74F843/74F844 9-bit bus interface latches, non-inverting/inverting (3-State)
74F845/74F846 8-bit bus interface latches, non-inverting/inverting (3-State)

FEATURES

- High speed parallel latches
- Extra data width for wide address/data paths or buses carrying parity
- High impedance NPN base input structure minimizes bus loading
- IIL is 20μA vs 1000A for AM29841 series
- Buffered control inputs to reduce AC effects
- Ideal where high speed, light loading, or increased fan-in are required as with MOS microprocessors
- Positive and negative over-shoots are clamped to ground
- 3-State outputs glitch free during power-up and power-down
- 48mA sink current
- Slim Dip 300 mil package
- Broadside pinout
- Pin-for-pin and function compatible with AMD AM29841-846 series

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F841, 74F842	5.5ns	60mA
74F843, 74F845	5.5ns	75mA
74F844, 74F846	6.2ns	60mA

DESCRIPTION

The 74F841–74F846 bus interface latch series are designed to provide extra data width for wider address/data paths of buses carrying parity.

The 74F841–74F846 series are funcitonally an pin compatible to the AMD AM29841–AM29846 series.

The 74F841 consists of ten D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is High. This allows asynchronous operation, as the output transition follows the data in transition. On the LE High-to-Low transition, the data that meets the setup and hold time is latched.

Data appears on the bus when the Output Enable ($\overline{OE}$) is Low. When $\overline{OE}$ is High the output is in the High-impedance state.

The 74F842 is the inverted output version of the 74F841.

The 74F843 consists of nine D-type latches with 3-State outputs. In addition to the LE and $\overline{OE}$ pins, the 74F843 has a Master Reset ($\overline{MR}$) pin and Preset ($\overline{PRE}$) pin. These pins are ideal for parity bus interfacing in high performance systems. When $\overline{MR}$ is Low, the outputs are Low if $\overline{OE}$ is Low. When $\overline{MR}$ is High, data can be entered into the latch. When $\overline{PRE}$ is Low, the outputs are High, if $\overline{OE}$ is Low, $\overline{PRE}$ overrides $\overline{MR}$.

The 74F844 is the inverted output version of the 74F843.

The 74F845 consists of eight D-type latches with 3-State outputs. In addition to the LE, $\overline{OE}$, $\overline{MR}$ and $\overline{PRE}$ pins, the 74F845 has two addtitional $\overline{OE}$ pins making a total of three Output Enables ($\overline{OE}$0, $\overline{OE}$1, $\overline{OE}$2) pins.

The multiple Ouptut Enables ($\overline{OE}$0, $\overline{OE}$1, $\overline{OE}$2) allow multi-user control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$.

The 74F846 is the inverted output version of the 74F845.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_{amb} = 0°C to +70°C	PACKAGE DRAWING NUMBER
24–pin plastic Slim DIP (300 mil)	N74F841N, N74F842N, N74F843N, N74F845N, N74F846N	SOT222-1
24–pin plastic SOL	N74F841D, N74F842D, N74F843D, N74F845D, N74F846D	SOT137-1

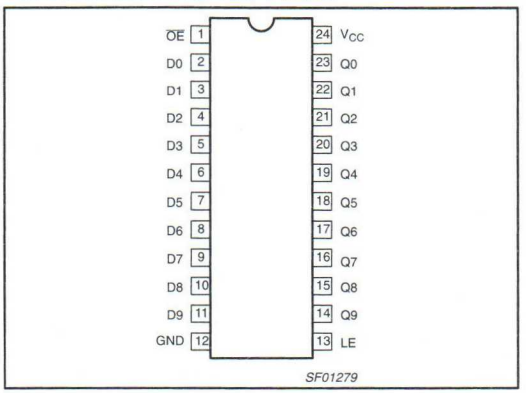
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dn	Data inputs	1.0/0.033	20μA/20μA
LE	Latch Enable input	1.0/0.033	20μA/20μA
$\overline{OE}$, $\overline{OE}$n	Output Enable input (active Low)	1.0/0.033	20μA/20μA
$\overline{MR}$	Master Reset input (active Low)	1.0/0.033	20μA/20μA
$\overline{PRE}$	Preset input (active Low)	1.0/0.033	20μA/20μA
Qn	Data outputs	1200/80	24mA/48mA
$\overline{Q}$n	Data outputs	1200/80	24mA/48mA

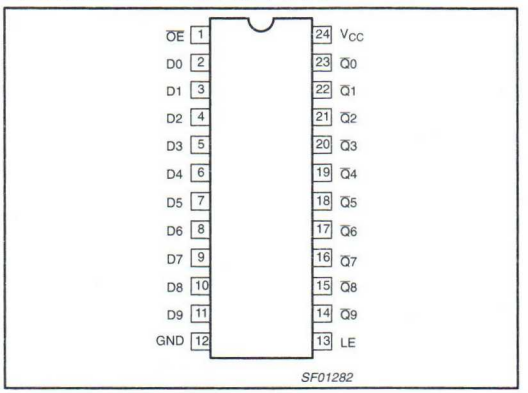
NOTE: One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

** Discontinued part. Please see the Discontinued Products List.*

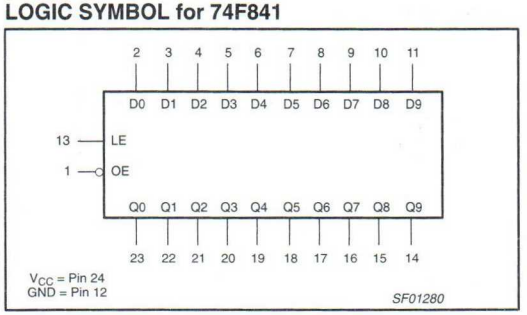
PIN CONFIGURATION for 74F841



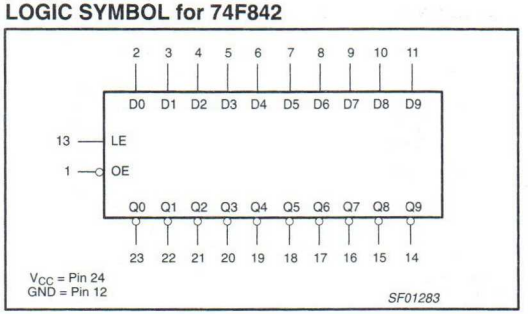
PIN CONFIGURATION for 74F842



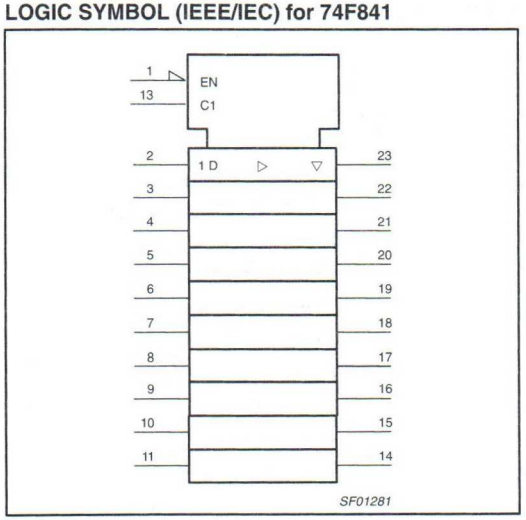
LOGIC SYMBOL for 74F841



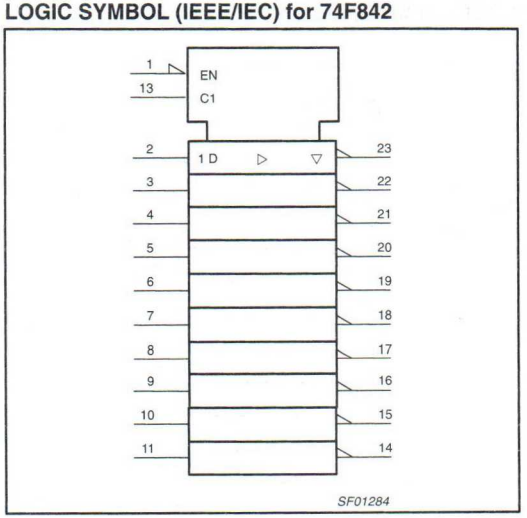
LOGIC SYMBOL for 74F842



LOGIC SYMBOL (IEEE/IEC) for 74F841

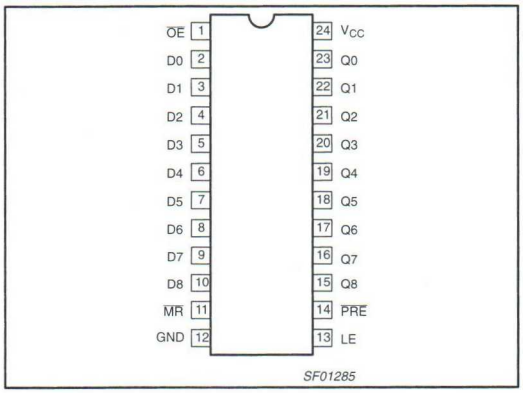


LOGIC SYMBOL (IEEE/IEC) for 74F842

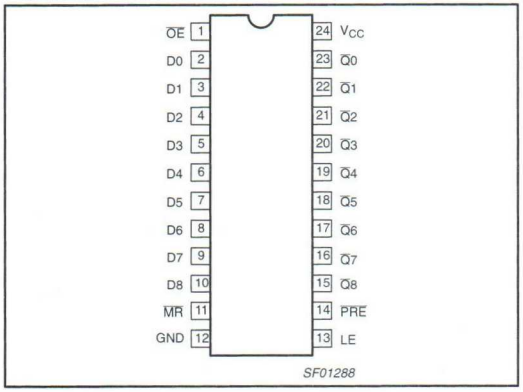


** Discontinued part. Please see the Discontinued Products List.*

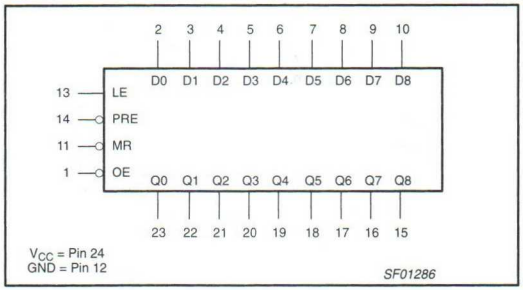
PIN CONFIGURATION for 74F843



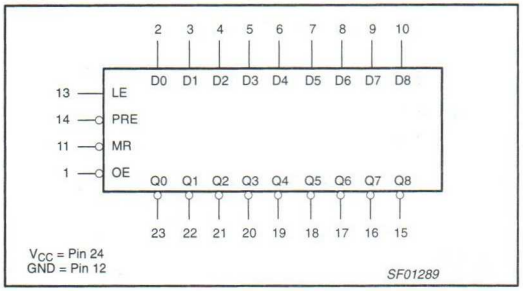
PIN CONFIGURATION for 74F844



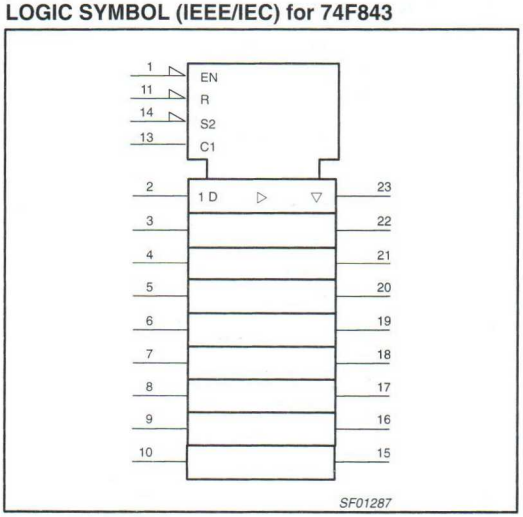
LOGIC SYMBOL for 74F843



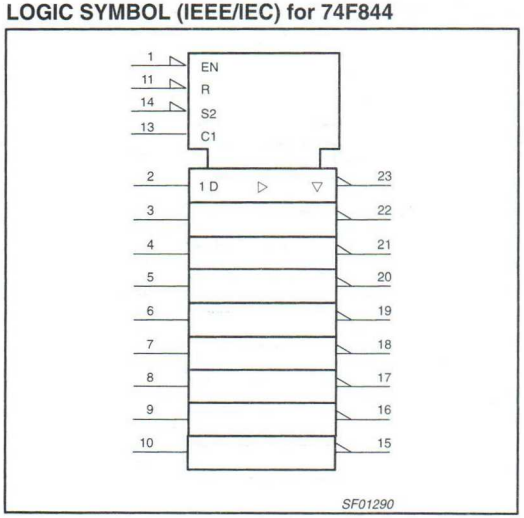
LOGIC SYMBOL for 74F844



LOGIC SYMBOL (IEEE/IEC) for 74F843

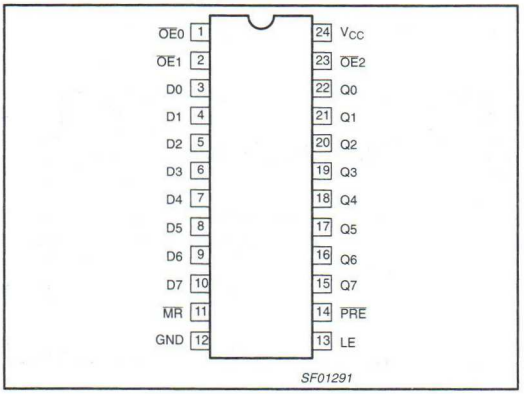


LOGIC SYMBOL (IEEE/IEC) for 74F844

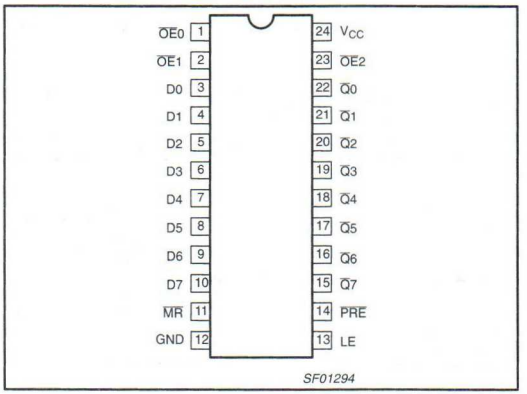


** Discontinued part. Please see the Discontinued Products List.*

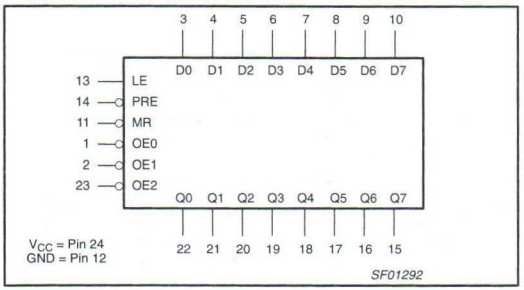
PIN CONFIGURATION for 74F845



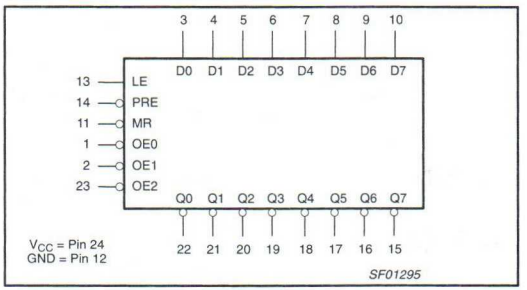
PIN CONFIGURATION for 74F846



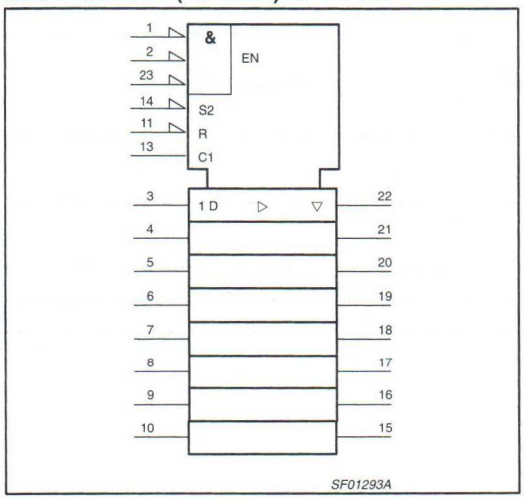
LOGIC SYMBOL for 74F845



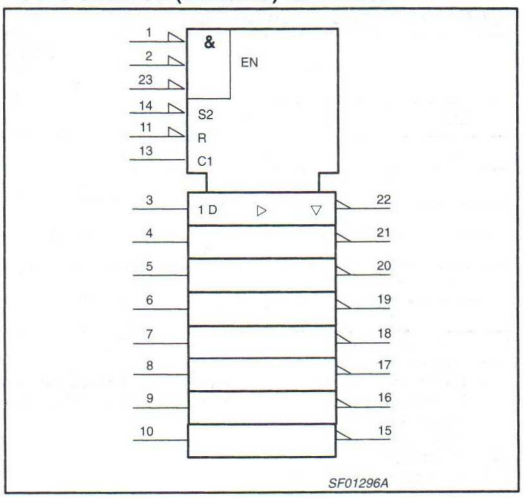
LOGIC SYMBOL for 74F846



LOGIC SYMBOL (IEEE/IEC) for 74F845

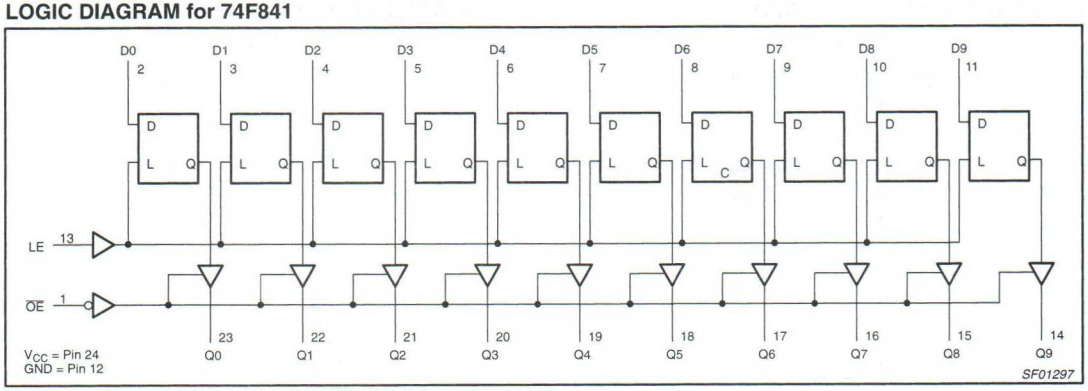


LOGIC SYMBOL (IEEE/IEC) for 74F846

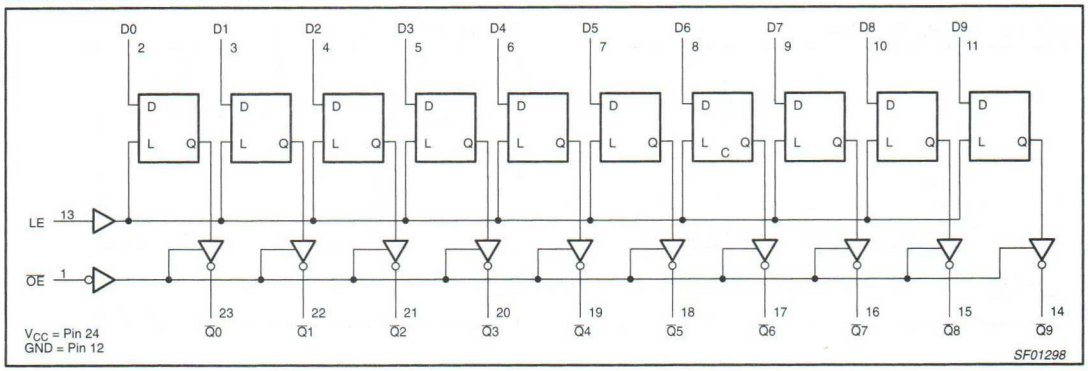


** Discontinued part. Please see the Discontinued Products List.*

LOGIC DIAGRAM for 74F841



LOGIC DIAGRAM for 74F842



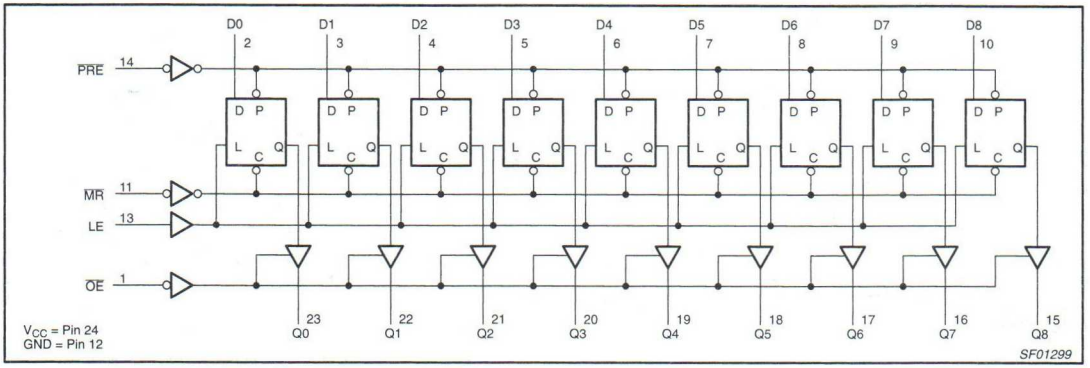
FUNCTION TABLE for 74F841 and 74F842

INPUTS			OUTPUTS		OPERATING MODE
			74F841	74F842	
$\overline{OE}$	LE	Dn	Qn	$\overline{Qn}$	
L	H	L	L	H	Transparent
L	H	H	H	L	
L	↓	l	L	H	Latched
L	↓	h	H	L	
H	X	X	Z	Z	High Impedance
L	L	X	NC	NC	Hold

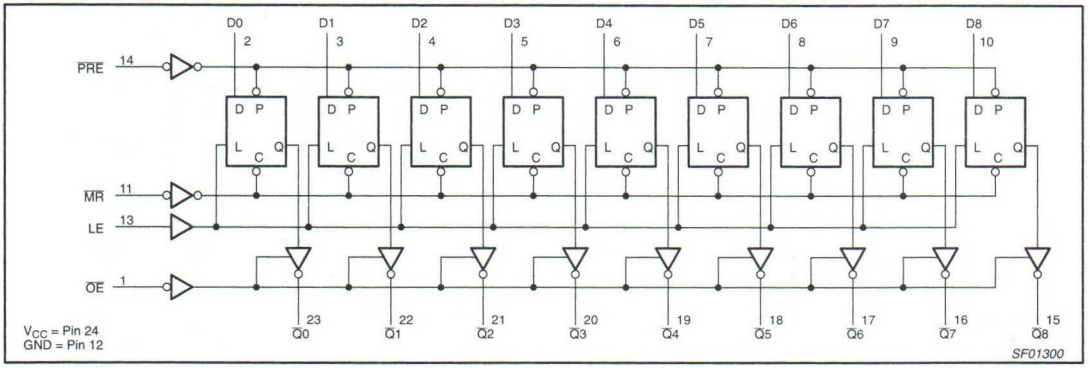
H = High voltage level
L = Low voltage level
h = High state one setup time before the High-to-Low LE transition
l = Low state one setup time before the High-to-Low LE transition
↓ = High-to-Low transition
X = Don't care
NC= No change
Z = High impedance "off" state

** Discontinued part. Please see the Discontinued Products List.*

LOGIC DIAGRAM for 74F843



LOGIC DIAGRAM for 74F844



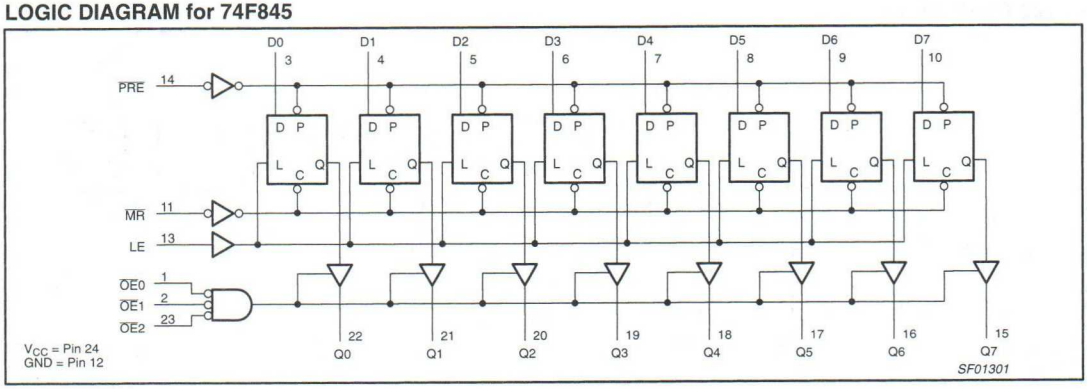
FUNCTION TABLE for 74F843 and 74F844

INPUTS					OUTPUTS		OPERATING MODE
					74F843	74F844	
$\overline{OE}$	$\overline{PRE}$	$\overline{MR}$	LE	Dn	Qn	$\overline{Qn}$	
L	L	X	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	H	H	H	L	L	H	Transparent
L	H	H	H	H	H	L	
L	H	H	↓	l	L		Latched
L	H	H	↓	h	H		
H	X	X	X	X	Z	Z	High Impedance
L	H	H	L	X	NC	NC	Hold

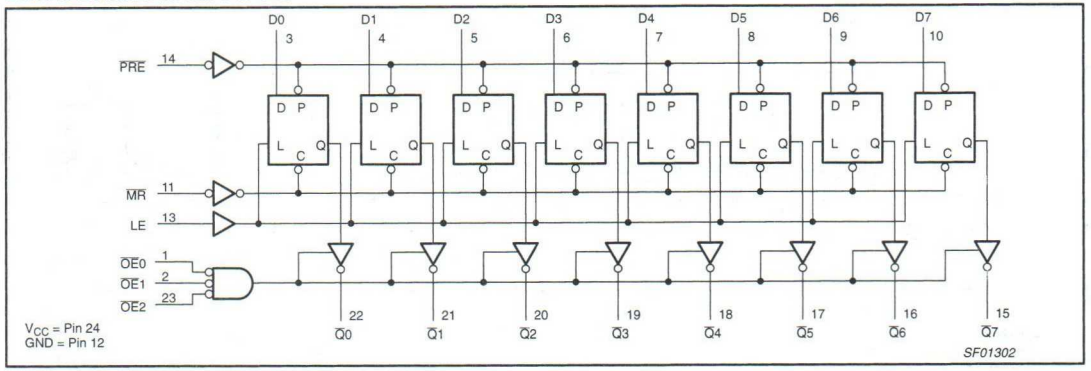
H = High voltage level
L = Low voltage level
h = High state one setup time before the High-to-Low LE transition
l = Low state one setup time before the High-to-Low LE transition
↓ = High-to-Low transition
X = Don't care
NC= No change
Z = High impedance "off" state

** Discontinued part. Please see the Discontinued Products List.*

LOGIC DIAGRAM for 74F845



LOGIC DIAGRAM for 74F846



FUNCTION TABLE for 74F845 and 74F846

INPUTS					OUTPUTS		OPERATING MODE
					74F845	74F846	
$\overline{OE}$	$\overline{PRE}$	$\overline{MR}$	LE	Dn	Qn	$\overline{Qn}$	
L	L	X	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	H	H	H	L	L	H	Transparent
L	H	H	H	H	H	L	
L	H	H	↓	l	L	H	Latched
L	H	H	↓	h	H	L	
H	X	X	X	X	Z	Z	High Impedance
L	H	H	L	X	NC	NC	Hold

H = High voltage level
L = Low voltage level
h = High state one setup time before the High-to-Low LE transition
l = Low state one setup time before the High-to-Low LE transition
↓ = High-to-Low transition
X = Don't care
NC= No change
Z = High impedance "off" state

** Discontinued part. Please see the Discontinued Products List.*

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	84	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			48	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

** Discontinued part. Please see the Discontinued Products List.*

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –15mA	±10%V_{CC}	2.2			V
				±5%V_{CC}	2.2	3.3		V
			I_{OH} = –24mA	±10%V_{CC}	2.0			V
				±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 32mA	±10%V_{CC}		0.38	0.55	V
			I_{OL} = 48mA	±5%V_{CC}		0.38	0.55	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low-level voltage applied	V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			–100		–225	mA
I_{CC}	Supply current (total)	74F841	I_{CCH}	V_{CC} = MAX		50	65	mA
			I_{CCL}			60	80	mA
			I_{CCZ}			70	92	mA
		74F842	I_{CCH}	V_{CC} = MAX		40	60	mA
			I_{CCL}			65	90	mA
			I_{CCZ}			60	90	mA
		74F843 74F845	I_{CCH}	V_{CC} = MAX		65	90	mA
			I_{CCL}			75	100	mA
			I_{CCZ}			85	115	mA
		74F844 74F846	I_{CCH}	V_{CC} = MAX		50	70	mA
			I_{CCL}			70	95	mA
			I_{CCZ}			70	95	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

** Discontinued part. Please see the Discontinued Products List.*

AC ELECTRICAL CHARACTERISTICS for 74F841/74F842

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	74F841	Waveform 1, 2	2.0 2.5	4.0 4.5	7.5 7.5	2.0 2.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay LE to Qn	74F841	Waveform 1, 2	4.5 4.0	6.5 6.0	9.5 9.0	4.0 3.5	10.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay Dn to $\overline{Qn}$	74F842	Waveform 1, 2	3.5 3.0	5.5 5.0	8.5 8.0	4.5 4.0	9.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay LE to $\overline{Qn}$	74F842	Waveform 1, 2	5.0 4.5	7.0 6.5	10.0 9.0	3.0 3.0	10.5 9.5	ns
t_{PZH} t_{PZL}	Output enable time High or Low-level $\overline{OE}$n to Qn or $\overline{Qn}$		Waveform 5 Waveform 6	2.5 4.0	4.5 6.0	8.0 9.5	2.0 3.0	8.5 10.5	ns
t_{PHZ} t_{PLZ}	Output disable time High or Low-level $\overline{OE}$n to Qn or $\overline{Qn}$		Waveform 5 Waveform 6	1.0 1.0	4.5 5.0	8.0 8.0	1.0 1.0	8.5 8.5	ns

AC SETUP REQUIREMENTS for 74F841/74F842

SYMBOL	PARAMETER		TEST CONDITION	LIMITS				UNIT
				T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω		T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low Dn to LE		Waveform 4	0.0 0.0		1.0 1.0		ns
t_h(H) t_h(L)	Hold time, High or Low Dn to LE	74F841	Waveform 4	2.5 3.0		3.0 4.0		ns
t_w(H)	LE pulse width, High	74F841	Waveform 4	3.5		4.0		ns
t_h(H) t_h(L)	Hold time, High or Low Dn to LE	74F842	Waveform 4	3.0 3.5		3.5 4.5		ns
t_w(H)	LE pulse width, High	74F842	Waveform 4	3.0		3.0		ns

** Discontinued part. Please see the Discontinued Products List.*

AC ELECTRICAL CHARACTERISTICS for 74F843/74F845

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	Waveform 1, 2	2.0 2.5	4.5 4.5	7.5 8.0	2.0 2.5	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay LE to Qn	Waveform 1, 2	4.5 4.0	6.5 6.0	9.5 8.5	4.5 4.0	10.0 8.5	ns
t_{PLH}	Propagation delay $\overline{PRE}$ to Qn	Waveform 3	3.5	5.5	8.5	3.0	9.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn	Waveform 3	2.0	4.5	7.5	2.0	8.0	ns
t_{PZH} t_{PZL}	Output enable time High or Low-level $\overline{OE}$n to Qn	Waveform 5 Waveform 6	2.5 4.0	4.5 6.0	7.5 9.5	2.0 3.0	8.0 10.5	ns
t_{PHZ} t_{PLZ}	Output disable time High or Low-level $\overline{OE}$n to Qn	Waveform 5 Waveform 6	1.0 1.0	4.5 5.0	8.0 8.0	1.0 1.0	8.5 8.5	ns

AC SETUP REQUIREMENTS for 74F843/74F845

SYMBOL	PARAMETER	TEST CONDITION	LIMITS				UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω		T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low Dn to LE	Waveform 4	1.0 1.0		0.0 0.0		ns
t_h(H) t_h(L)	Hold time, High or Low Dn to LE	Waveform 4	3.0 4.0		3.0 4.0		ns
t_w(H)	LE pulse width, High	Waveform 4	3.0		3.0		ns
t_w(L)	$\overline{PRE}$ pulse width, Low	Waveform 3	4.0		5.0		ns
t_w(H)	$\overline{MR}$ pulse width, Low	Waveform 3	4.0		5.0		ns
t_{REC}	$\overline{PRE}$ recovery time	Waveform 3	0.0		0.0		ns
t_{REC}	$\overline{MR}$ recovery time	Waveform 3	3.5		4.5		ns

** Discontinued part. Please see the Discontinued Products List.*

AC ELECTRICAL CHARACTERISTICS for 74F844/74F846

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to $\overline{Q}$n	Waveform 1, 2	3.5 3.0	5.5 5.0	8.5 8.0	3.0 3.0	9.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay LE to $\overline{Q}$n	Waveform 1, 2	5.0 4.5	7.0 6.5	10.0 9.0	5.0 4.5	10.5 9.5	ns
t_{PLH}	Propagation delay $\overline{PRE}$ to $\overline{Q}$n	Waveform 3	3.5	5.5	8.5	3.0	9.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to $\overline{Q}$n	Waveform 3	5.0	7.0	10.0	4.5	10.5	ns
t_{PZH} t_{PZL}	Output enable time High or Low-level $\overline{OE}$n to $\overline{Q}$n	Waveform 5 Waveform 6	2.5 4.0	5.0 6.0	7.5 9.5	2.0 3.0	8.0 10.5	ns
t_{PHZ} t_{PLZ}	Output disable time High or Low-level $\overline{OE}$n to $\overline{Q}$n	Waveform 5 Waveform 6	1.0 1.0	4.5 5.0	8.0 8.0	1.0 1.0	8.5 8.5	ns

AC SETUP REQUIREMENTS for 74F844/74F846

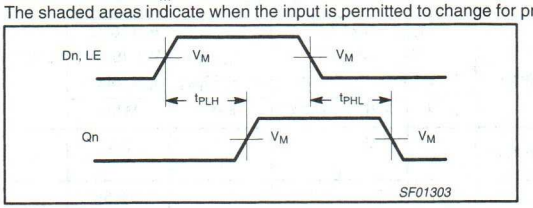
SYMBOL	PARAMETER	TEST CONDITION	LIMITS				UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω		T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low Dn to LE	Waveform 4	0.0 0.0		0.0 0.0		ns
t_h(H) t_h(L)	Hold time, High or Low Dn to LE	Waveform 4	3.0 4.0		3.0 4.0		ns
t_w(H)	LE pulse width, High	Waveform 4	3.0		3.0		ns
t_w(L)	$\overline{PRE}$ pulse width, Low	Waveform 3	4.0		5.0		ns
t_w(H)	$\overline{MR}$ pulse width, Low	Waveform 3	4.0		5.0		ns
t_{REC}	$\overline{PRE}$ recovery time	Waveform 3	0.0		0.0		ns
t_{REC}	$\overline{MR}$ recovery time	Waveform 3	3.5		4.5		ns

** Discontinued part. Please see the Discontinued Products List.*

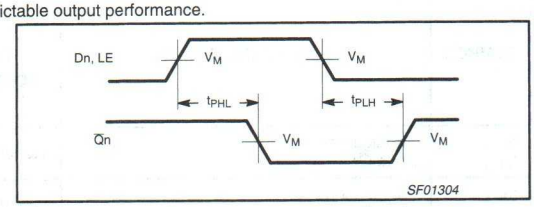
AC WAVEFORMS

For all waveforms, $V_M = 1.5V$.

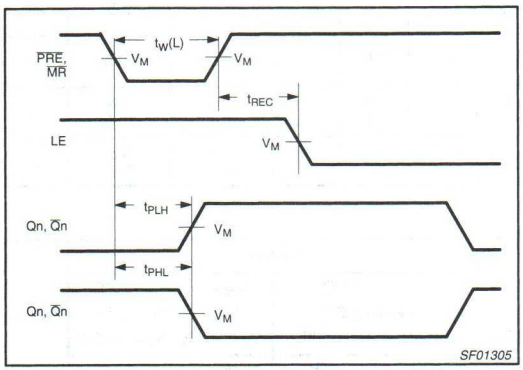
The shaded areas indicate when the input is permitted to change for predictable output performance.



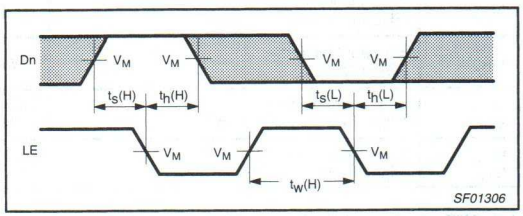
Waveform 1. Propagation Delay, Non-Inverting Path



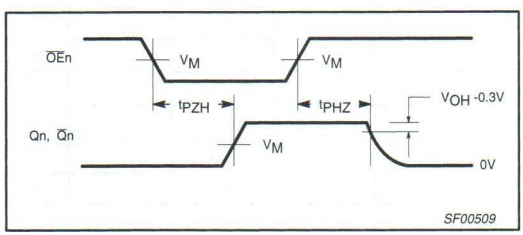
Waveform 2. Propagation Delay, Inverting Path



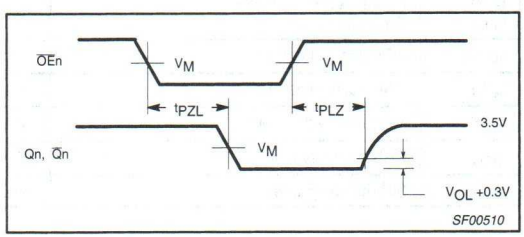
Waveform 3. Master Reset and Preset Pulse Width, Master Reset and Preset to Output Delay, and Master Reset and Preset to Latch Enable Recovery Time



Waveform 4. Data Setup and Hold Times



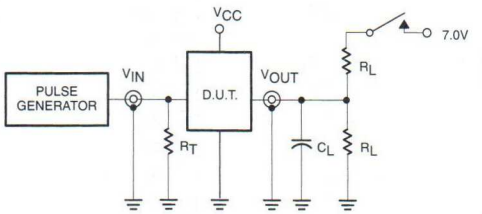
Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



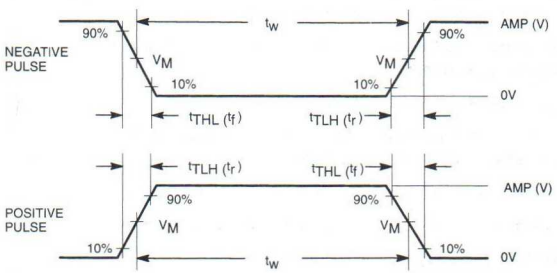
Waveform 6. 3-State Output Enable Time to Low Level and Output Disable time from Low Level

** Discontinued part. Please see the Discontinued Products List.*

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

** Discontinued part. Please see the Discontinued Products List.*

Bus transceivers (3-State)

~~74F861*~~, ~~74F862*~~, 74F863, ~~74F864*~~

FEATURES

- Provide high performance bus interface buffering for wide data/address paths or buses carrying parity
- High impedance NPN base inputs for reduced loading (20µA in High and Low states)
- I_{IL} is 20µA vs. 1000µA for AM29861 series
- Buffered control inputs for light loading, or increased fan-in as required with MOS microprocessors
- Positive and negative over-shoots are clamped to ground
- 3-State outputs glitch free during power-up and power-down
- Slim dual In-line (DIP) 300mil package
- Broadside pinout compatible with AMD AM29861–29864
- Outputs sink 64mA

DESCRIPTION

The 74F861 series bus transceivers provide high performance bus interface buffering for wide data/address paths of buses carrying parity. The 74F863/864 9-bit bus transceivers have NOR-ed transmit and receive output enables for maximum control flexibility.

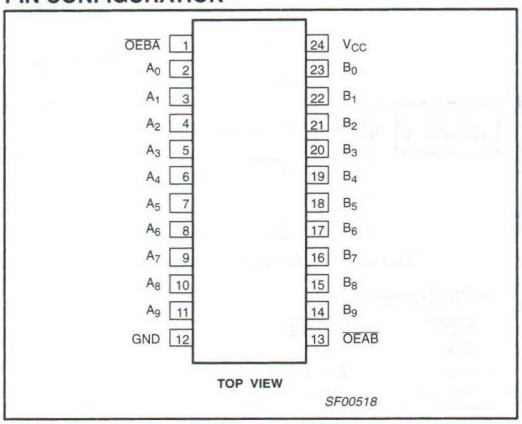
TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F861, 74F862	6.0ns	150mA
74F863, 74F864	6.0ns	115mA

ORDERING INFORMATION

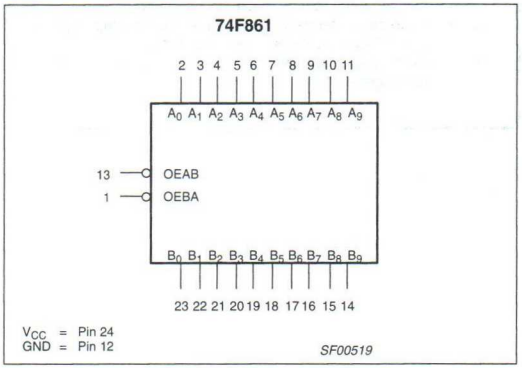
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C	PKG DWG #
24-pin Plastic Slim Dual In-line (300mil) Package	74F863N	SOT222-1
24-pin Plastic Small Outline Large[1]	74F863D	SOT137-1

NOTE:
1. Thermal mounting techniques are recommended. See SMD Process Applications for a discussion of thermal considerations for surface mounted devices.

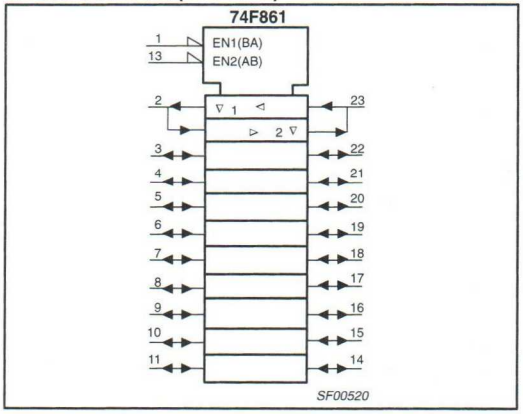
PIN CONFIGURATION



LOGIC SYMBOL

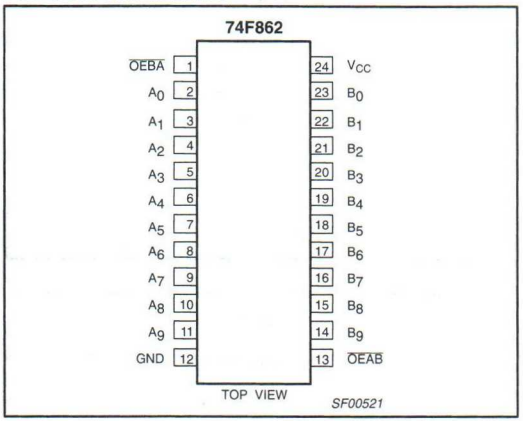


LOGIC SYMBOL (IEEE/IEC)

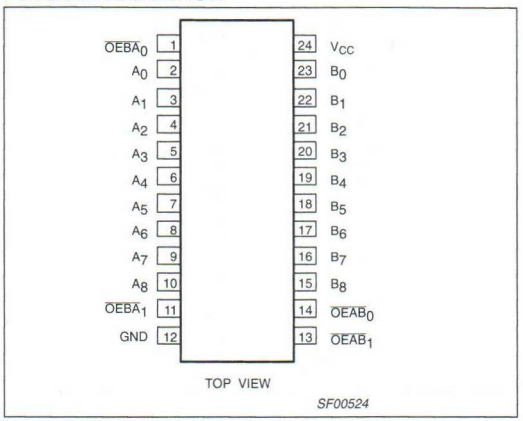


* *Discontinued part. Please see the Discontinued Products List.*

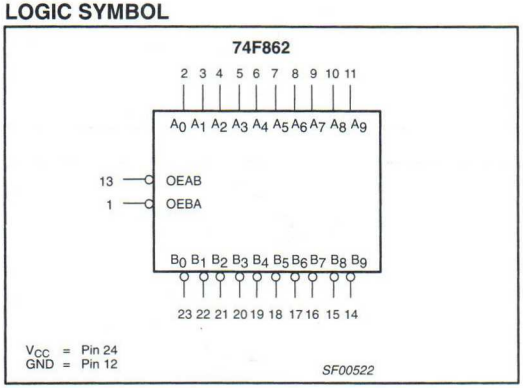
PIN CONFIGURATION



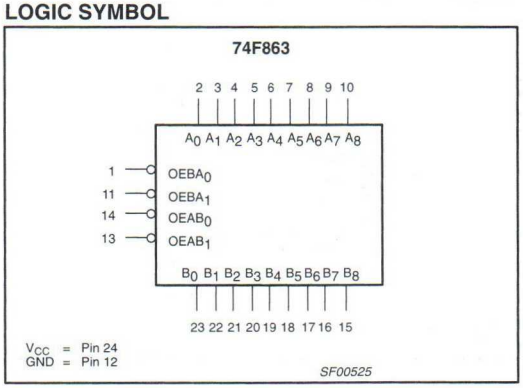
PIN CONFIGURATION



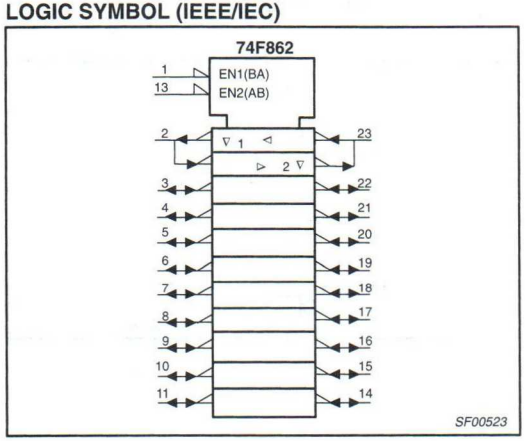
LOGIC SYMBOL



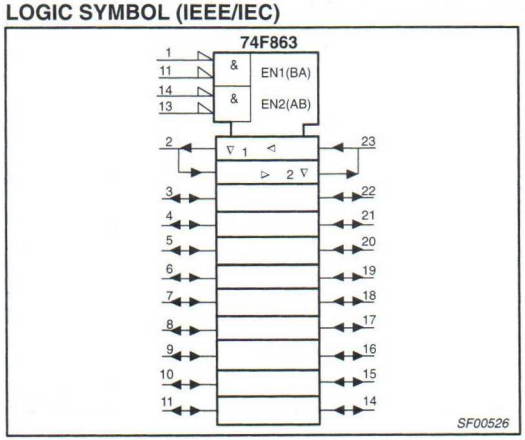
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

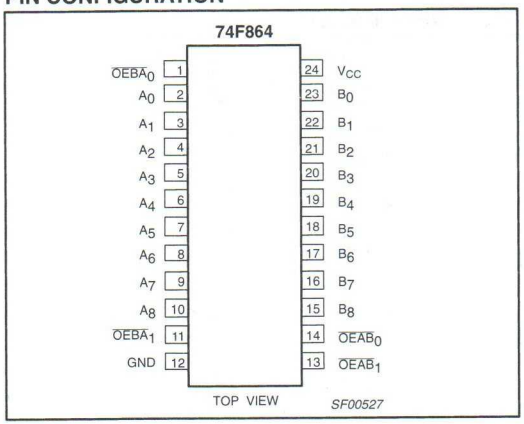


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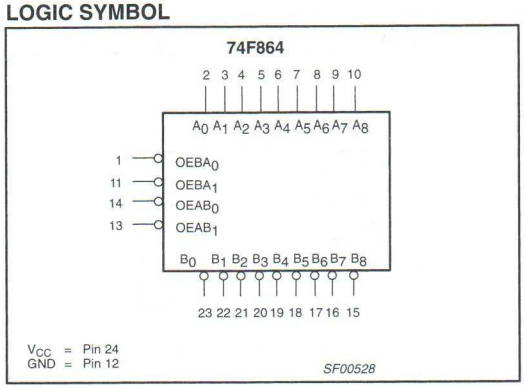


* *Discontinued part. Please see the Discontinued Products List.*

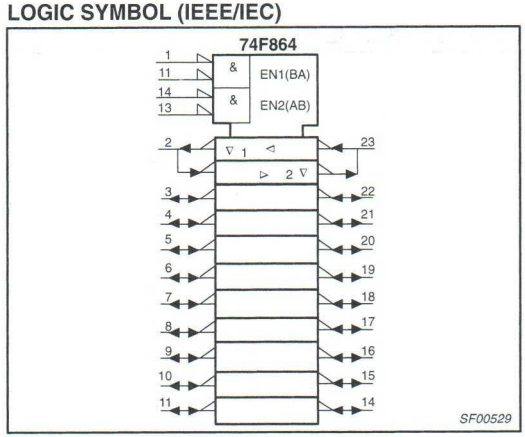
PIN CONFIGURATION



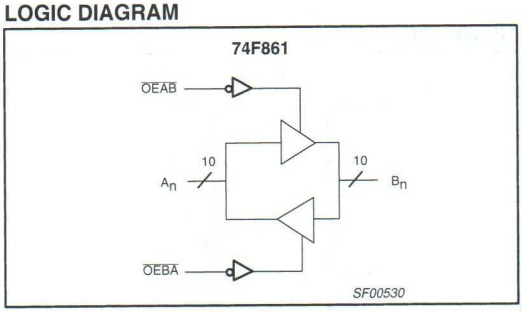
LOGIC SYMBOL

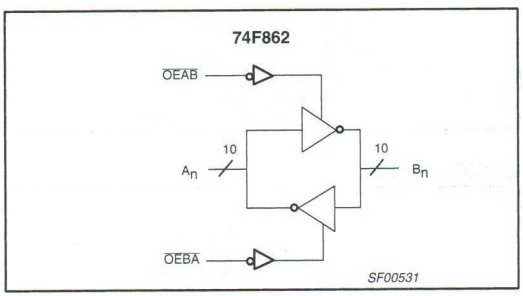


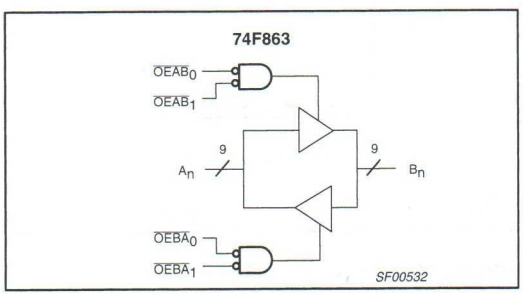
LOGIC SYMBOL (IEEE/IEC)

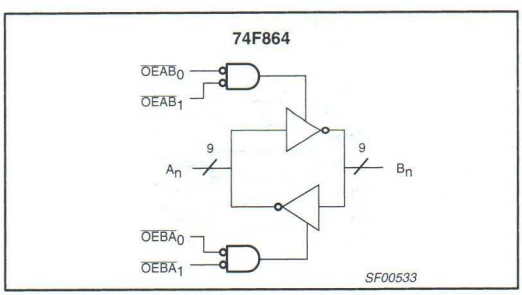


LOGIC DIAGRAM









* *Discontinued part. Please see the Discontinued Products List.*

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS		DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
74F861 74F862	$A_0 - A_9$	Data transmit inputs	3.5/0.117	70μA/70μA
	$B_0 - B_9$	Data receive inputs	3.5/0.117	70μA/70μA
	$\overline{OEBA}$	Transmit output enable input	1.0/0.033	20μA/20μA
	$\overline{OEAB}$	Receive output enable input	1.0/0.033	20μA/20μA
	$A_0 - A_9$	Data transmit outputs	1200/106.7	24mA/64mA
	$B_0 - B_9$	Data receive outputs	1200/106.7	24mA/64mA
74F863 74F864	$A_0 - A_9$	Data transmit inputs	3.5/0.117	70μA/70μA
	$B_0 - B_9$	Data receive inputs	3.5/0.117	70μA/70μA
	$\overline{OEBA}_n$	Transmit output enable input	1.0/0.033	20μA/20μA
	$\overline{OEAB}_n$	Receive output enable input	1.0/0.033	20μA/20μA
	$A_0 - A_9$	Data transmit outputs	1200/106.7	24mA/64mA
	$B_0 - B_9$	Data receive outputs	1200/106.7	24mA/64mA

NOTE: One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

FUNCTION TABLE FOR 74F861 AND 74F862

INPUTS		OPERATING MODES	
$\overline{OEAB}$	$\overline{OEBA}$	74F861	74F862
L	H	A data to B bus	A data to B bus
H	L	B bus to A data	B bus to A data
H	H	Z	Z

H = High voltage level
L = Low voltage level
Z = High impedance "off" state

FUNCTION TABLE FOR 74F863 AND 74F864

INPUTS				OPERATING MODES	
$\overline{OEAB}_0$	$\overline{OEAB}_1$	$\overline{OEBA}_0$	$\overline{OEBA}_1$	74F863	74F864
L L	L L	H X	X H	A data to B bus	A data to B bus
H X	X H	L L	L L	B bus to A data	B bus to A data
H	H	H	H	Z	Z

H = High voltage level
L = Low voltage level
Z = High impedance "off" state

* *Discontinued part. Please see the Discontinued Products List.*

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-24	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

** Discontinued part. Please see the Discontinued Products List.*

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage			V_{CC}=MIN, V_{IL}=MAX, V_{IH}=MIN	I_{OH}=-15mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.4	3.3		V
				V_{CC}=MIN, V_{IL}=MAX, V_{IH}=MIN	I_{OH}=-24mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC}=MIN, V_{IL}=MAX, V_{IH}=MIN	I_{OL}=-48mA	±10%V_{CC}		0.38	0.55	V
					I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEAB}$, $\overline{OEBA}$ $\overline{OEAB_n}$, $\overline{OEBA_n}$		V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A_n, B_n		V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{IH} + I_{OZH}	Off-state output current High-level voltage applied		A_n, B_n	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{IL} + I_{OZL}	Off-state output current Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V					-70	µA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			-100		-225	mA
I_{CC}	A_n, B_n Supply current total	74F861 74F863	I_{CCH}	V_{CC} = MAX				145	195	mA
			I_{CCL}					140	195	mA
			I_{CCZ}					165	220	mA
		74F862 74F864	I_{CCH}	V_{CC} = MAX				90	130	mA
			I_{CCL}					120	170	mA
			I_{CCZ}					130	160	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

** Discontinued part. Please see the Discontinued Products List.*

AC ELECTRICAL CHARACTERISTICS

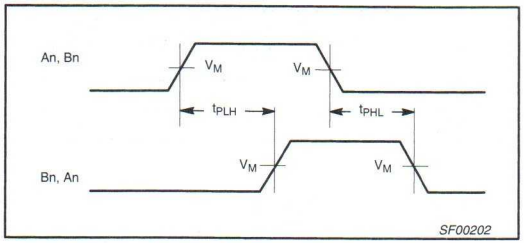
SYMBOL	PARAMETER	TEST CONDITION	74F861, 74F863					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay A_n or B_n	Waveform 1	4.0 3.0	6.0 5.0	9.0 8.0	3.5 2.5	10.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n or A_n	Waveform 1	4.0 2.5	6.0 5.0	9.0 8.0	3.5 2.5	10.0 9.0	ns
t_{PZH} t_{PZL}	Output Enable time High or Low level $\overline{OEBA}_n$ to A_n	Waveform 3 Waveform 4	6.0 4.0	8.0 6.0	11.5 10.0	5.0 4.0	13.0 11.0	ns
t_{PZH} t_{PZL}	Output Enable time High or Low level $\overline{OEAB}_n$ to B_n	Waveform 3 Waveform 4	6.0 4.0	8.0 6.0	11.0 10.0	5.0 4.0	13.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time High or Low level $\overline{OEBA}_n$ to A_n	Waveform 3 Waveform 4	3.5 2.5	5.5 5.0	9.0 8.5	3.0 2.0	9.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable time High or Low level $\overline{OEAB}_n$ to B_n	Waveform 3 Waveform 4	3.5 2.5	5.5 4.5	8.5 8.5	3.0 2.0	9.5 9.5	ns

AC ELECTRICAL CHARACTERISTICS

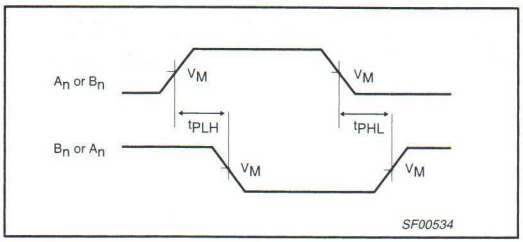
SYMBOL	PARAMETER	TEST CONDITION	74F862, 74F864					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay A_n or B_n	Waveform 2	4.0 1.5	6.0 3.5	9.0 6.5	3.0 1.5	10.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n or A_n	Waveform 2	4.0 1.5	6.0 3.5	9.0 6.5	3.5 1.5	10.0 7.0	ns
t_{PZH} t_{PZL}	Output Enable time High or Low level $\overline{OEBA}_n$ to A_n	Waveform 3 Waveform 4	6.5 6.0	8.5 7.5	12.0 12.0	5.5 5.0	13.5 14.0	ns
t_{PZH} t_{PZL}	Output Enable time High or Low level $\overline{OEAB}_n$ to B_n	Waveform 3 Waveform 4	6.5 6.0	8.5 7.5	12.0 12.0	5.5 5.0	13.5 14.0	ns
t_{PHZ} t_{PLZ}	Output Disable time High or Low level $\overline{OEBA}_n$ to A_n	Waveform 3 Waveform 4	3.0 2.5	5.0 4.0	8.5 8.5	2.5 2.0	9.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time High or Low level $\overline{OEAB}_n$ to B_n	Waveform 3 Waveform 4	3.0 2.5	5.0 4.0	8.5 8.5	2.5 2.0	9.5 9.0	ns

* *Discontinued part. Please see the Discontinued Products List.*

AC WAVEFORMS

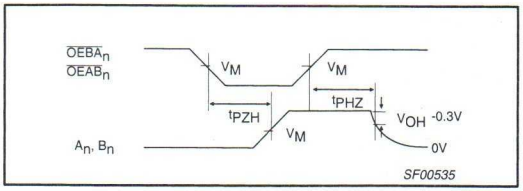


Waveform 1. Propagation Delay for Non-inverting Output

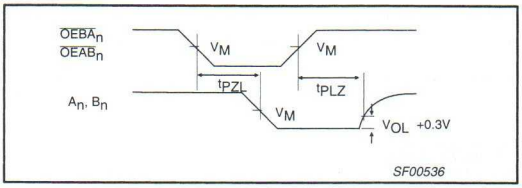


Waveform 2. Propagation Delay for Inverting Output

NOTE: For all waveforms, V_M = 1.5V.

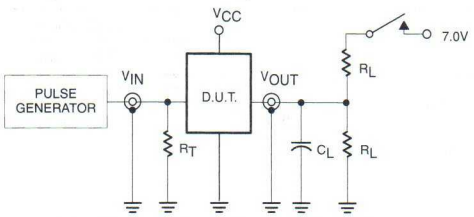


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

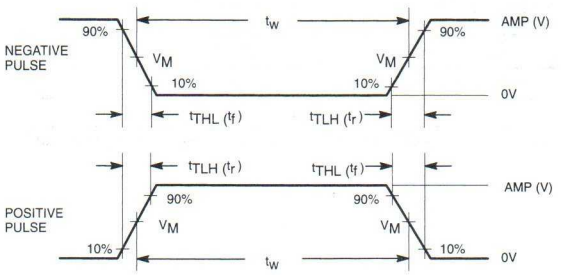


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUITS AND WAVEFORMS



Test Circuit for Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

* *Discontinued part. Please see the Discontinued Products List.*

Buffers

74F1240, ~~74F1241~~*

74F1240 Octal inverter buffer (3-State)

FEATURES

- High impedance NPN base inputs for reduced loading (20µA in High and Low states)
- Low power, light loading
- Functional pin-for-pin equivalent of 74F240 and 74F241
- 1/30th the bus loading of 74F240 and 74F241
- Provides ideal interface and increase fan-out of MOS microprocessors
- Octal bus interface
- 3-State buffer outputs sink 64mA
- 15mA source current

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1240	3.5ns	40mA
74F1241	4.5ns	46mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
20-pin plastic DIP	N74F1240N	SOT146-1
20-pin plastic SOL	N74F1240D	SOT163-1

DESCRIPTION

The 74F1240 and 74F1241 are octal buffers that are ideal for driving bus lines or buffer memory address registers. The outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two Output Enables, $\overline{OE}a$ and $\overline{OE}b$, each controlling four of the 3-State outputs.

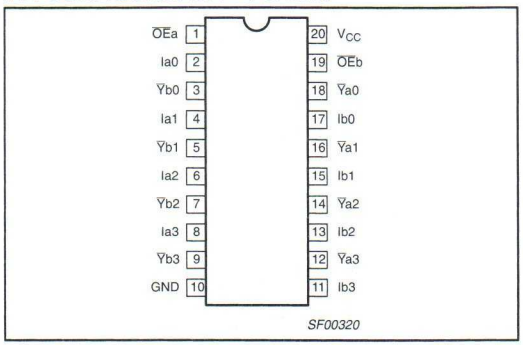
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ian, Ibn	Data inputs	1.0/0.033	20µA/20µA
$\overline{OE}a$, $\overline{OE}b$	Output enable inputs (active Low)	1.0/0.033	20µA/20µA
OEb	Output enable input (active High, 74F1241)	1.0/0.033	20µA/20µA
Yan, Ybn	Data outputs (74F1241)	750/106.7	15mA/64mA
$\overline{Y}an$, $\overline{Y}bn$	Data outputs (74F1240)	750/106.7	15mA/64mA

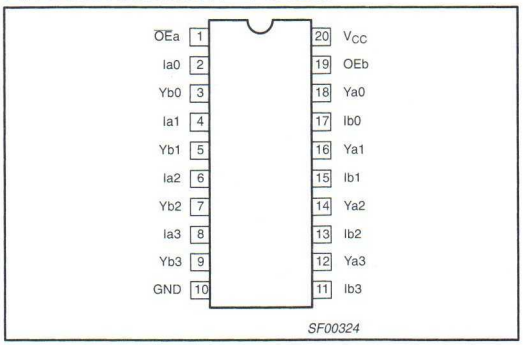
NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

** Discontinued part. Please see the Discontinued Products List.*

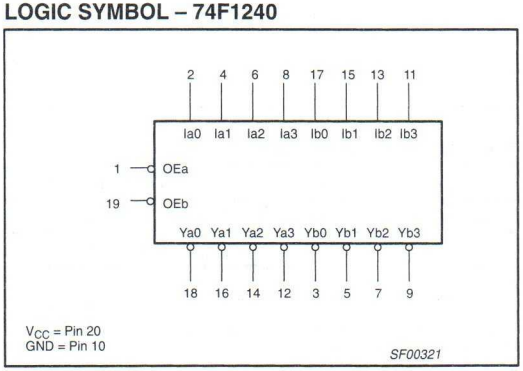
PIN CONFIGURATION – 74F1240



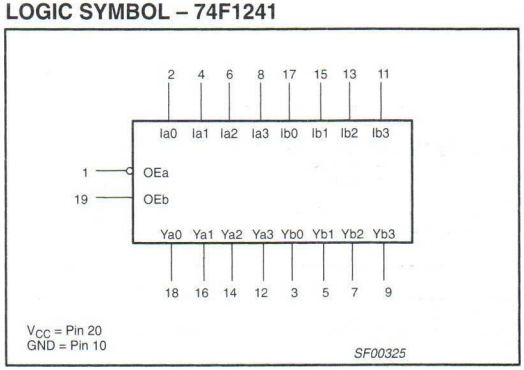
PIN CONFIGURATION – 74F1241



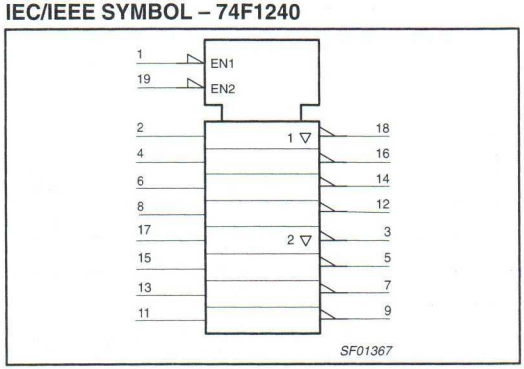
LOGIC SYMBOL – 74F1240



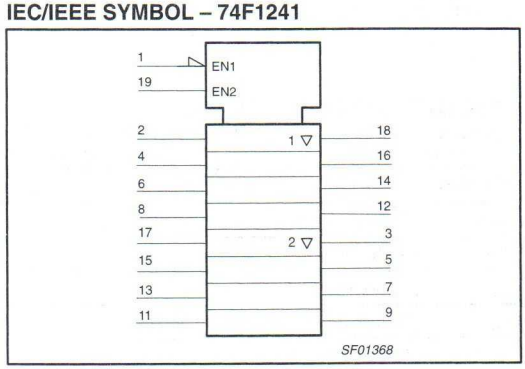
LOGIC SYMBOL – 74F1241



IEC/IEEE SYMBOL – 74F1240

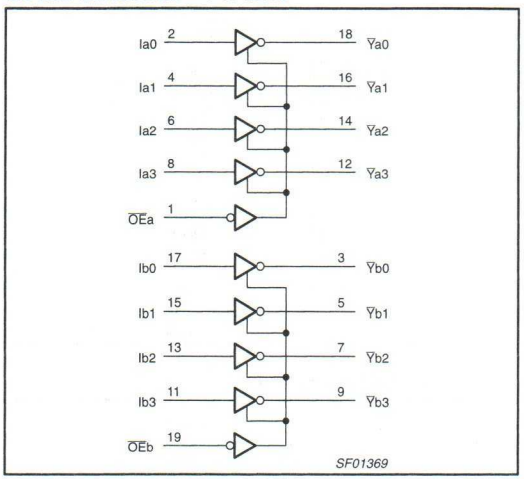


IEC/IEEE SYMBOL – 74F1241

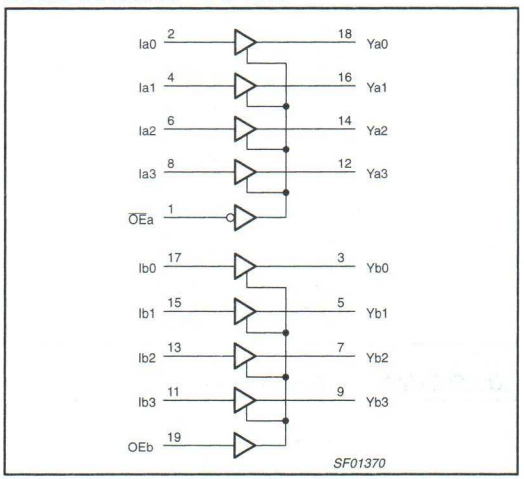


* *Discontinued part. Please see the Discontinued Products List.*

LOGIC DIAGRAM – 74F1240



LOGIC DIAGRAM – 74F1241



FUNCTION TABLE – 74F1240

INPUTS				OUTPUTS	
$\overline{OE}a$	Ia	$\overline{OE}b$	Ib	$\overline{Y}a$	$\overline{Y}b$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

FUNCTION TABLE – 74F1241

INPUTS				OUTPUTS	
$\overline{OE}a$	Ia	OEb	Ib	Ya	Yb
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

* *Discontinued part. Please see the Discontinued Products List.*

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–15	mA
I_{OL}	Low-level output current			64	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							MIN	TYP	MAX	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10% V_{CC}	2.4			V
						±5% V_{CC}	2.7	3.3		V
					I_{OH} = –15mA	±10% V_{CC}	2.0			V
						±5% V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10% V_{CC}		0.38	0.55	V
					I_{OL} = 64mA	±5% V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			–100		–225	mA
I_{CC}	Supply current (total)	74F1240	I_{CCH}	V_{CC} = MAX				22	30	mA
			I_{CCL}					58	75	mA
			I_{CCZ}					44	58	mA
		74F1241	I_{CCH}	V_{CC} = MAX				33	44	mA
			I_{CCL}					62	80	mA
			I_{CCZ}					45	60	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

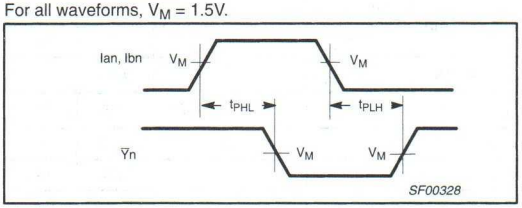
* *Discontinued part. Please see the Discontinued Products List.*

AC ELECTRICAL CHARACTERISTICS

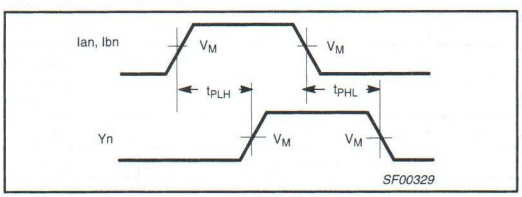
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Ian, Ibn, to $\overline{Y}$n	74F1240	Waveform 1	3.0 1.5	4.5 2.5	6.5 4.5	2.5 1.5	7.5 5.0	ns ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	3.0 4.0	5.5 7.0	7.5 9.0	3.0 4.0	8.0 9.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	6.0 5.5	2.0 2.0	6.5 6.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Ian, Ibn, to Yn	74F1241	Waveform 2	2.5 2.5	4.0 5.0	5.5 6.5	2.5 2.5	6.0 7.0	ns ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	3.0 3.0	5.5 6.5	7.0 8.0	3.0 3.0	7.5 8.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 3 Waveform 4	3.0 3.0	5.5 6.0	7.5 8.0	3.0 3.0	8.5 8.5	ns ns

AC WAVEFORMS

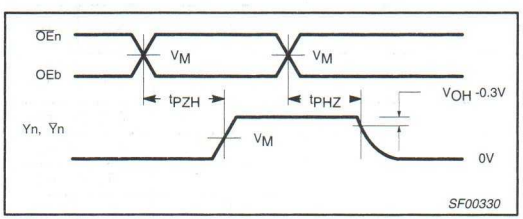
For all waveforms, V_M = 1.5V.



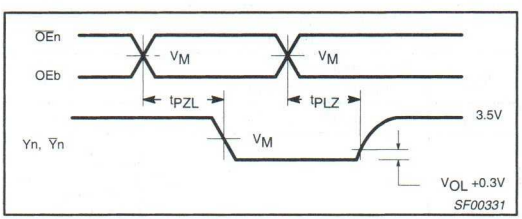
Waveform 1. For Inverting Outputs



Waveform 2. For Non-inverting Outputs



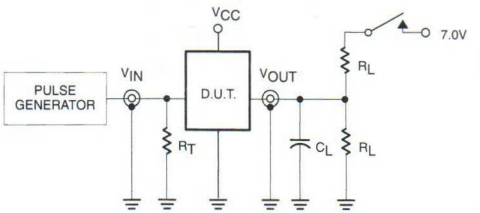
Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



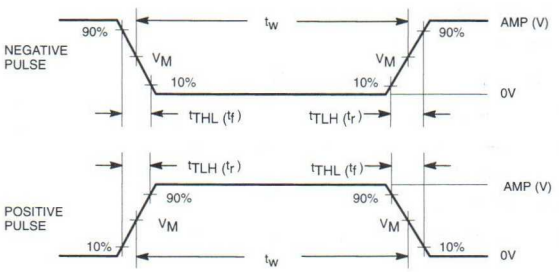
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

* *Discontinued part. Please see the Discontinued Products List.*

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

* *Discontinued part. Please see the Discontinued Products List.*

Octal buffer (3-State) 74F1244

FEATURES

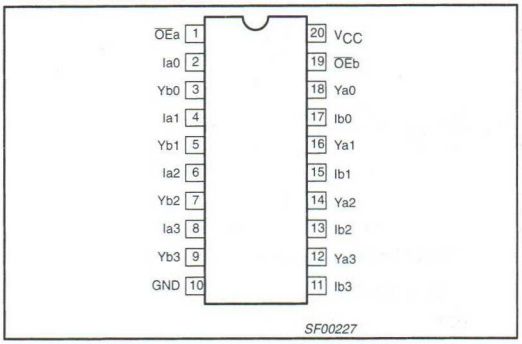
- High impedance NPN base inputs for reduced loading (20µA in High and Low states)
- Low power, light loading
- Functional pin-for-pin equivalent of 74F244
- 1/30th the bus loading of 74F244
- Provides ideal interface and increase fan-out of MOS microprocessors
- Octal bus interface
- 3-State buffer outputs sink 64mA and source 15mA

DESCRIPTION

The 74F1244 is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two Output Enables, $\overline{OE}a$ and $\overline{OE}b$, each controlling four of the 3-State outputs.

The 74F1244 is pin and functionally compatible with the 74F244. The lower power and light bus loading features make it an ideal part to interface directly with MOS microprocessors.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1244	4.5ns	43mA

ORDERING INFORMATION

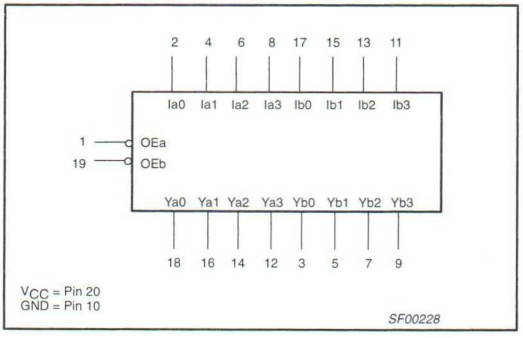
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
20-pin plastic DIP	N74F1244N	SOT146-1
20-pin plastic SOL	N74F1244D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

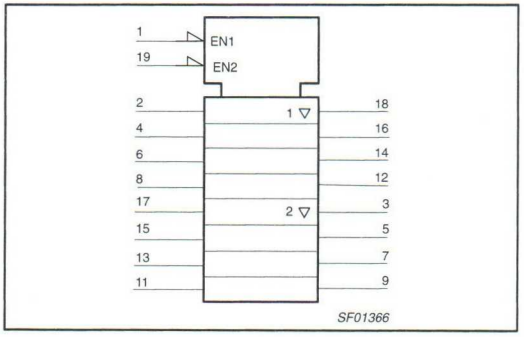
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ian, Ibn	Data inputs	1.0/0.033	20µA/20µA
$\overline{OE}a$, $\overline{OE}b$	Output enable inputs (active Low)	1.0/0.033	20µA/20µA
Yan, Ybn	Data outputs	750/106.7	15mA/64mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

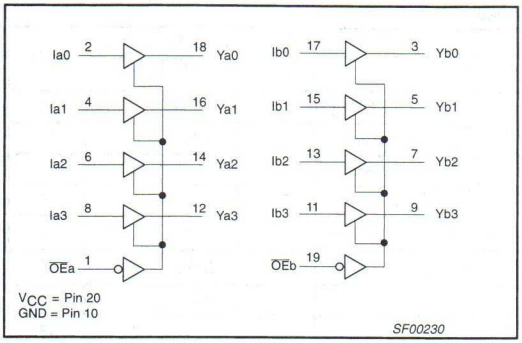
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE}a$	Ia	$\overline{OE}b$	Ib	Ya	Yb
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10% V_{CC}	2.5			V
				±5% V_{CC}	2.7	3.4		V
			I_{OH} = –15mA	±10% V_{CC}	2.0			V
				±5% V_{CC}	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10% V_{CC}		0.38	0.55	V
			I_{OL} = 64mA	±5% V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low-level voltage applied	V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			–100		–225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			30	40	mA
		I_{CCL}				57	75	mA
		I_{CCZ}				43	58	mA

NOTES:

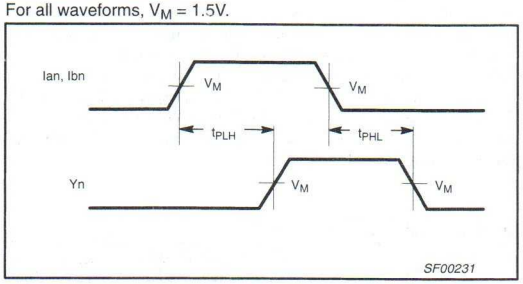
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

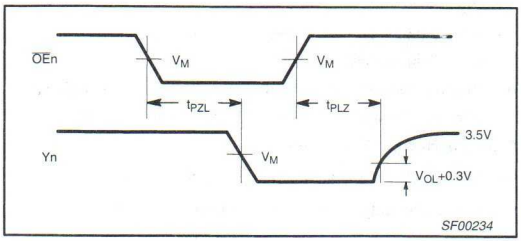
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	Propagation delay	Waveform 1	2.5	4.0	5.5	2.5	6.0	ns
t_{PHL}	In, Ibn to Yn		2.0	5.0	7.0	2.0	7.5	ns
t_{PZH}	Output Enable time	Waveform 2	3.0	6.0	7.5	3.0	8.5	ns
t_{PZL}	to High or Low level	Waveform 3	3.0	6.5	8.0	3.0	8.5	ns
t_{PHZ}	Output Disable time	Waveform 2	2.0	4.0	5.5	2.0	6.0	ns
t_{PLZ}	to High or Low level	Waveform 3	2.0	4.0	5.5	2.0	6.0	ns

AC WAVEFORMS

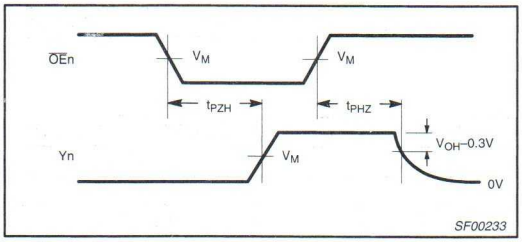
For all waveforms, V_M = 1.5V.



Waveform 1. For Non-Inverting Outputs

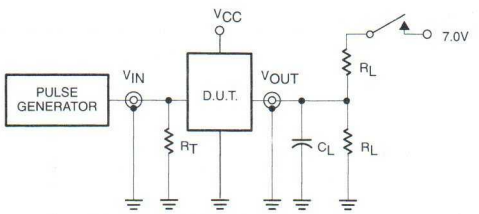


Waveform 3. 3-State Output enable Time to Low Level and Output Disable Time from Low Level

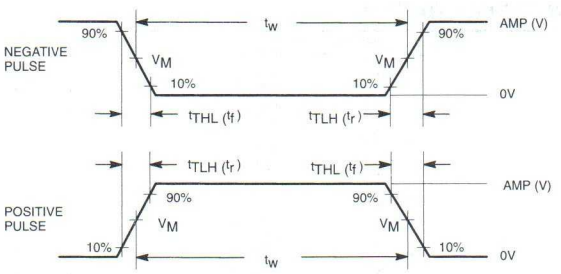


Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

Octal transceiver (3-State) 74F1245

FEATURES

- Same function and pinout as 74F245
- High impedance NPN base inputs for reduced loading (70µA in Low and High states)
- Useful in applications where light loading bus loading or direct interface with output of a MOS microprocessor is desired
- Octal bidirectional bus interface
- Glitch free during 3-State power up and power down
- 3-State buffer outputs sink 64mA and source 15mA

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1245	5.0ns	115mA

DESCRIPTION

The 74F1245 is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both transmit and receive directions. The B port outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features an Output Enable ($\overline{OE}$) input for easy cascading and Transmit/Receive (T/$\overline{R}$) input for direction control. The 3-State outputs, B0–B7, have been designed to prevent output bus loading if the power is removed from the device.

ORDERING INFORMATION

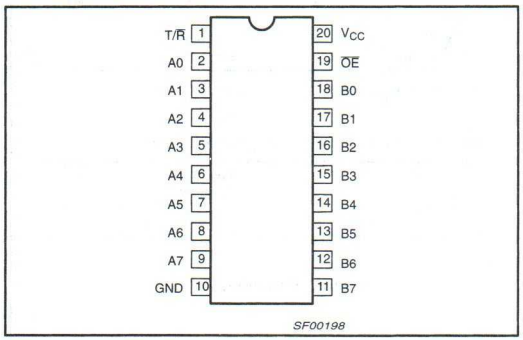
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
20-Pin Plastic DIP	N74F1245N	SOT146-1
20-Pin Plastic SOL	N74F1245D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

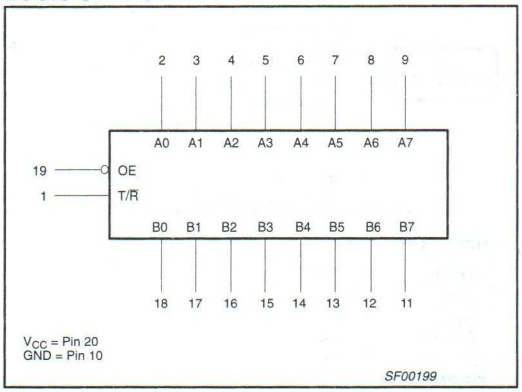
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0–A7, B0–B7	A and B port inputs	3.5/0.117	70µA/70µA
$\overline{OE}$	Output Enable input (active Low)	2.0/0.033	40µA/20µA
T/$\overline{R}$	Transmit/Receive input	2.0/0.033	40µA/20µA
A0–A7	A port outputs	150/40	3.0mA/24mA
B0–B7	B port outputs	750/106.7	15mA/64mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

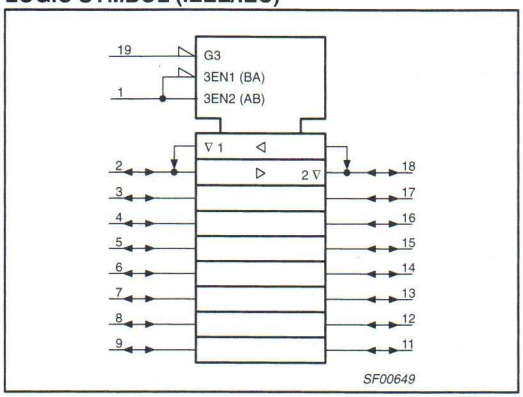
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

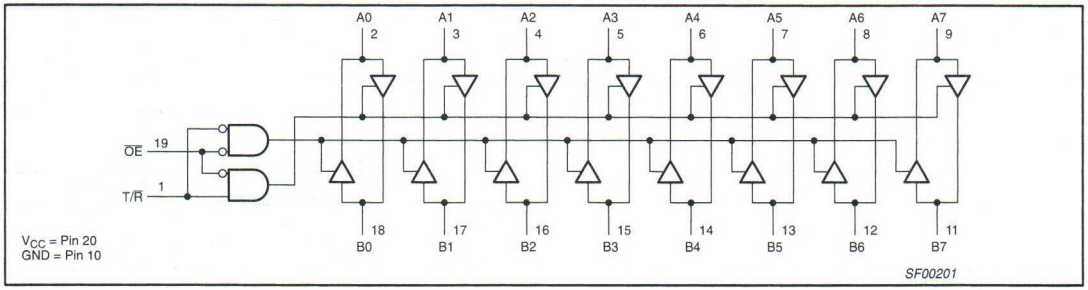


FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	T/$\overline{R}$	An	Bn
L	L	A = B	INPUTS
L	H	INPUTS	B = A
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A0–A7	48	mA
		B0–B7	128	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A0–A7			–3	mA
		B0–B7			–15	mA
I_{OL}	Low-level output current	A0–A7			24	mA
		B0–B7			64	mA
T_{amb}	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	A0–A7, B0–B7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10% V_{CC}	2.4			V
					±5% V_{CC}	2.7	3.3		V
		B0–B7		I_{OH} = –15mA	±10% V_{CC}	2.0			V
					±5% V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A0–A7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10% V_{CC}		0.35	0.50	V
					±5% V_{CC}		0.35	0.50	V
		B0–B7		I_{OL} = 48mA	±10% V_{CC}		0.30	0.55	V
				I_{OL} = 64mA	±5% V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	$\overline{OE}$, T/$\overline{R}$	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A0–A7, B0–B7	V_{CC} = 0.0V, V_I = 5.5V					100	µA
I_{IH}	High-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 2.7V					40	µA
I_{IL}	Low-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied		V_{CC} = MAX, V_O = 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					–70	µA
I_{OS}	Short-circuit output current[3]	A0–A7	V_{CC} = MAX			–60		–150	mA
		B0–B7				–100		–225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				120	155	mA
		I_{CCL}					116	150	mA
		I_{CCZ}					110	165	mA

NOTES:

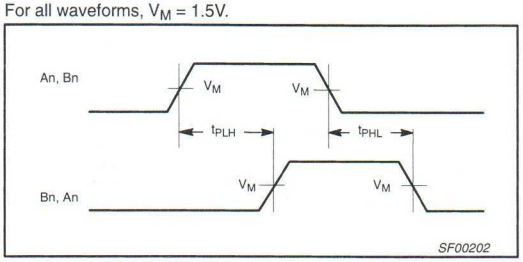
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

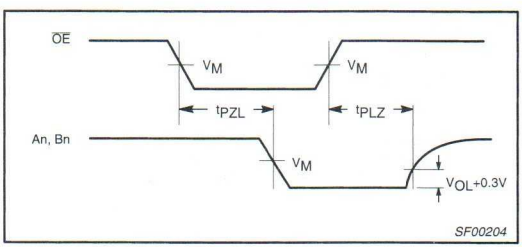
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn, Bn to An	Waveform 1	2.0 2.5	4.0 5.0	6.5 7.5	1.5 2.0	7.0 8.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to An or Bn	Waveform 2 Waveform 3	3.0 4.0	6.0 7.5	8.0 10.0	2.5 3.5	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to An or Bn	Waveform 2 Waveform 3	2.0 4.0	5.0 7.0	8.0 10.0	1.5 4.0	9.0 11.0	ns

AC WAVEFORMS

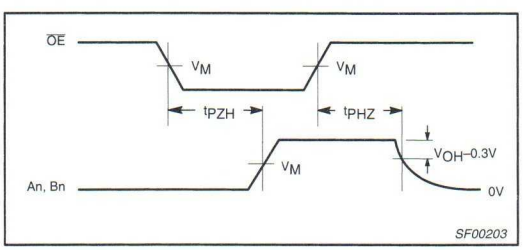
For all waveforms, V_M = 1.5V.



Waveform 1. Propagation Delay for Non-Inverting Output

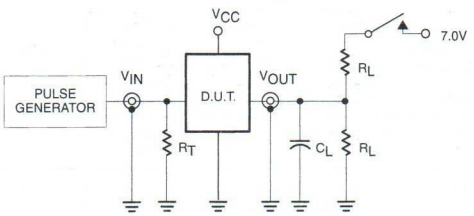


Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level

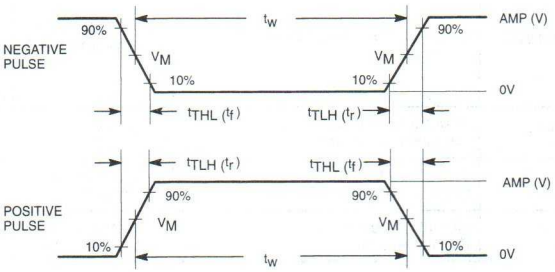
TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open



Input Pulse Definition

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

Latch | 74F1604

FEATURES

- High impedance NPN base inputs for reduced loading (20μA in high and low state)
- Stores 16–bit wide data inputs, multiplexed 8–bit outputs
- Propagation delay 7.0ns typical
- Power supply current 70mA typical

DESCRIPTION

The 74F1604 is a dual octal transparent latch. Organized as 8–bit A and B latches, the latch outputs are connected by pairs to eight 2–input multiplexers. A select (SELECT A/$\overline{B}$) input determines whether the A or B latch contents are multiplexed to the eight outputs. Data from the B inputs are selected when SELECT A/$\overline{B}$ is low; data from the A inputs are selected when SELECT A/$\overline{B}$ is high. Data enters the latch on the falling edge of the latch enable ($\overline{LE}$) input. The latch remains transparent to the data inputs while $\overline{LE}$ is low, and stores the data that is present one setup time before the low–to–high latch enable transition.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1604	7.0ns	70mA

ORDERING INFORMATION

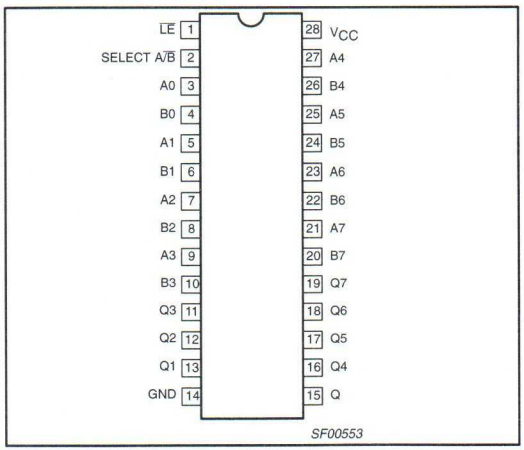
DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
28–pin plastic DIP	N74F1604N	SOT117-2
28–pin plastic SOL	N74F1604D	SOT136-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

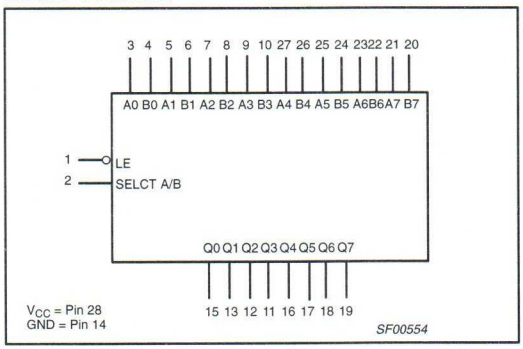
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A7	Data inputs	1.0/0.033	20μA/20μA
B0 – B7	Data inputs	1.0/0.033	20μA/20μA
SELECT A/$\overline{B}$	Select input	1.0/0.033	20μA/20μA
$\overline{LE}$	Latch enable input (active low)	1.0/0.033	20μA/20μA
Q0 – Q7	Data outputs	50/33	1.0mA/20mA

Note to input and output loading and fan out table
One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.

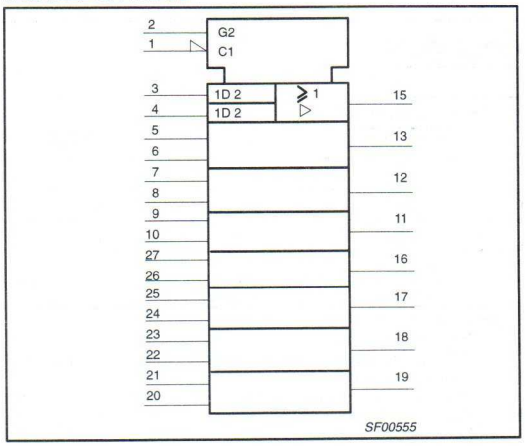
PIN CONFIGURATION



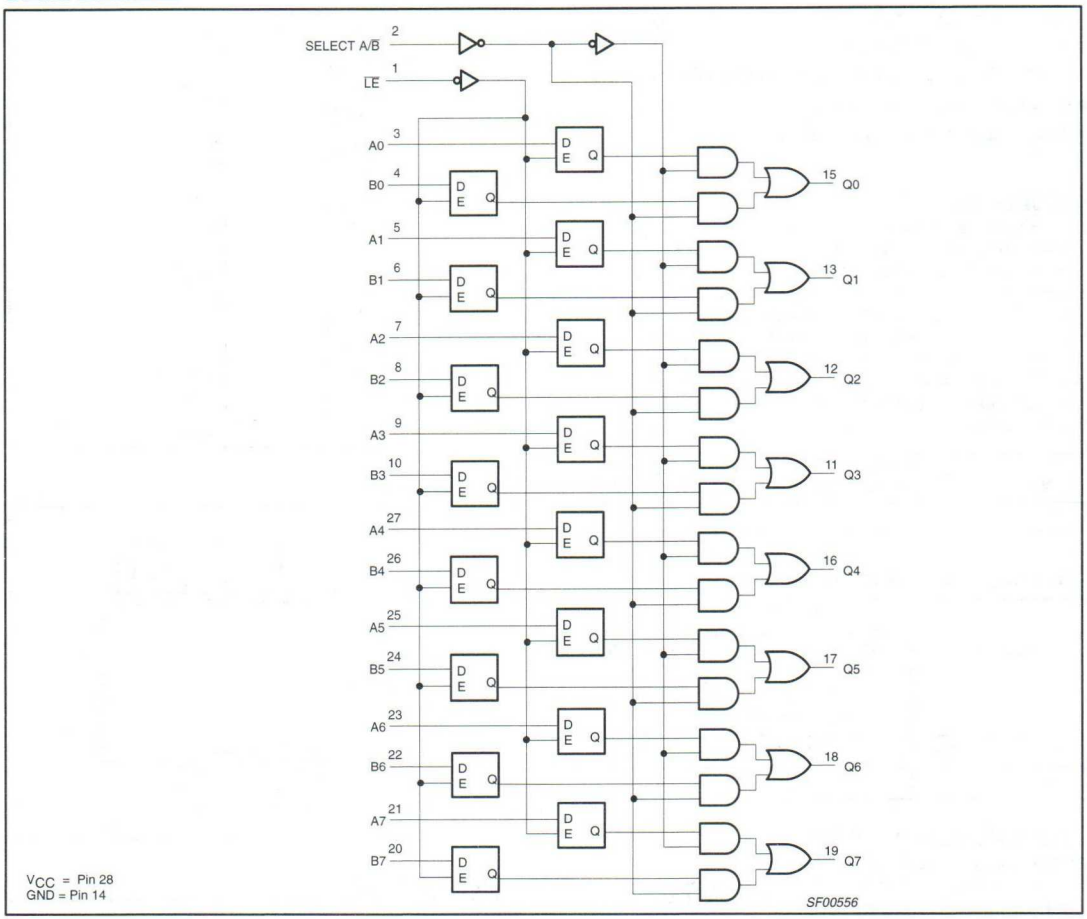
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	OUTPUTS
OPERATING MODE					
A0 – A7	B0 –B7	SELECT A/$\overline{B}$	$\overline{LE}$	Q0 – Q7	
A data	B data	L	L	B data	Enable and read register
A data	B data	H	L	A data	
X	X	X	H	NC	Hold
A data	B data	l	↑	B data	Latch and read register
A data	B data	h	↑	A data	

Notes to function table

H = High–voltage level
h = High–voltage level one setup time before the low–to–high latch enable transition
L = Low–voltage level
l = Low–voltage level one setup time before the low–to–high latch enable transition
NC= No change (If SELECT A/$\overline{B}$ is toggled and the A latched data is different from B latched data then the output will change accordingly.)
X = Don't care
↑ = Low–to–high latch enable transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	40	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–1	mA
I_{OL}	Low–level output current			20	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = –3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{OS}	Short–circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				60	80	mA
		I_{CCL}					75	100	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

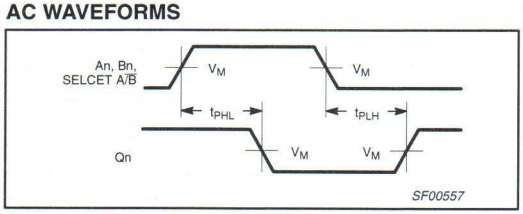
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Qn (non–inverting)	Waveform 2	3.0 3.5	5.5 6.5	8.5 10.0	2.5 3.0	9.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Qn (inverting)	Waveform 1	4.0 2.5	7.0 4.5	10.5 7.5	3.5 2.0	12.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}$ to Qn	Waveform 3	6.5 6.0	9.5 9.0	13.0 12.5	5.5 5.0	15.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay An or Bn to Qn	Waveform 1, 2	4.0 4.0	6.5 7.0	9.5 10.5	3.5 3.5	10.5 12.5	ns

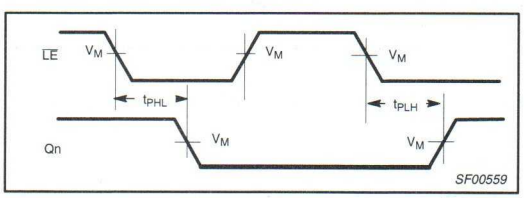
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_D = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_D= 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low An, Bn to $\overline{LE}$	Waveform 4	0.0 1.0			0.0 3.5		ns
t_h (H) t_h (L)	Hold time, high or low An, Bn to $\overline{LE}$	Waveform 4	1.5 3.0			2.0 3.5		ns
t_w (L)	$\overline{LE}$ Pulse width, low	Waveform 4	6.5			7.5		ns

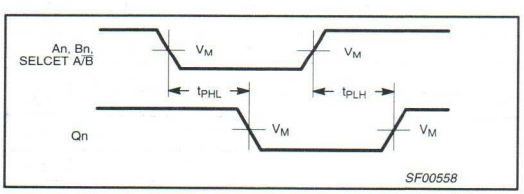
AC WAVEFORMS



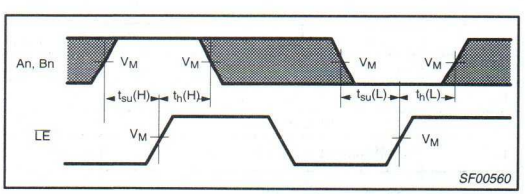
Waveform 1. Propagation delay for SELECT A/$\overline{B}$ to output (A register stored data = low) or An. Bn to output



Waveform 3. Propagation delay for latch enable to output



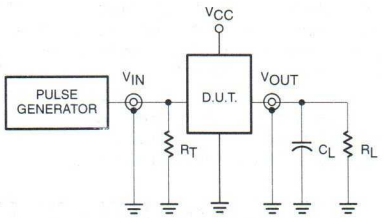
Waveform 2. Propagation delay for SELECT A/$\overline{B}$ to output (A register stored data = low) or An. Bn to output



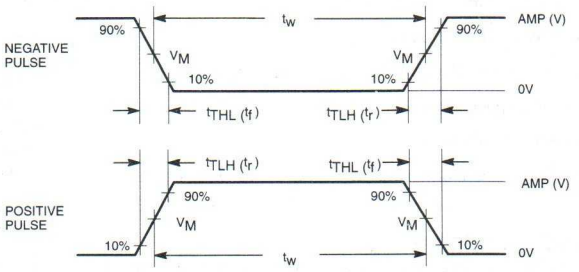
Waveform 4. Setup time and hold times and $\overline{LE}$ pulse width

Note to AC waveforms
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor;
see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Intelligent DRAM controller (IDC) 74F1763

FEATURES

- DRAM signal timing generator
- Automatic refresh circuitry
- Selectable row address hold and $\overline{RAS}$ precharge times
- Facilitates page mode accesses
- Controls 1 MBit DRAMs
- Intelligent burst-mode refresh after page-mode access cycles

PRODUCT DESCRIPTION

The Philips Semiconductors Intelligent Dynamic RAM Controller is a 1 MBit, single-port version of the 74F1764 Dual Port Dynamic RAM Controller. It contains automatic signal timing, address multiplexing and refresh control required for interfacing with dynamic RAMs. Additional features have been added to this device to take advantage of technological advances in Dynamic RAMs. A Page-Mode access pin allows the user to assert $\overline{RAS}$ for the entire access cycle rather than the pre-defined four-clock-cycle pulse width used for normal random access cycles. In addition, the user has the ability to select the $\overline{RAS}$ precharge time and Row-Address Hold time to fit the particular DRAMs being used. $\overline{DTACK}$ has been modified from previous family parts to become a negative true, tri-stated output. The options for latched or unlatched address are contained on a single device by the addition of an Address Latch Enable ($\overline{ALE}$) input. Finally, a burst refresh monitor has been added to ensure complete refreshing after length page-mode access cycles. With a maximum clock frequency of 100 MHz, the F1763 is capable of controlling DRAM arrays with access times down to 40 nsec.

TYPE	f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1763	100 MHz	150 mA

ORDERING INFORMATION

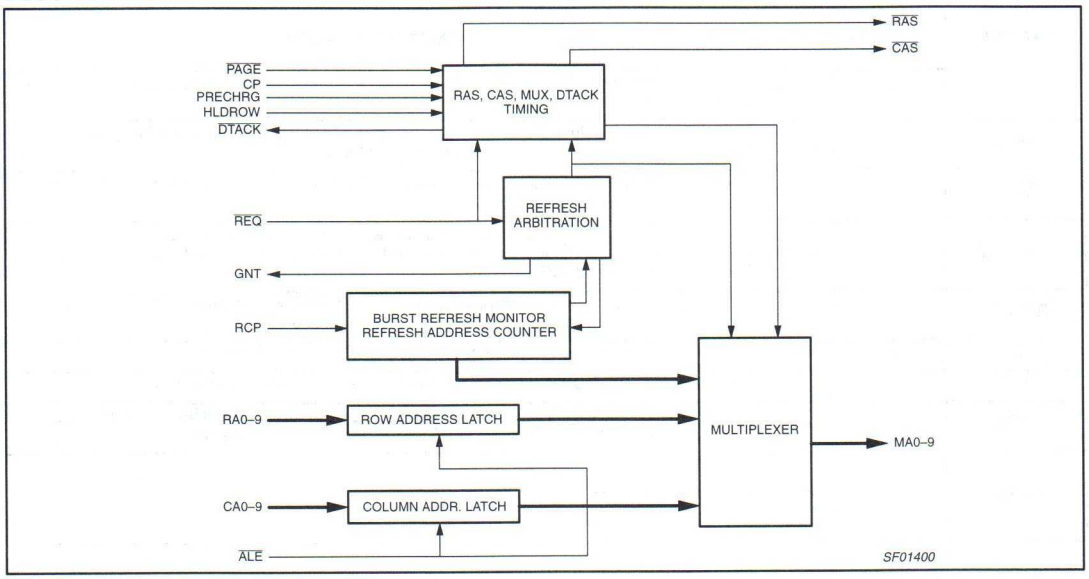
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C TO 70°C	PKG DWG #
48-pin Plastic DIP	N74F1763N	SOT240-1

INPUT AND OUTPUT LOADING FAN-OUT TABLE NO TAG

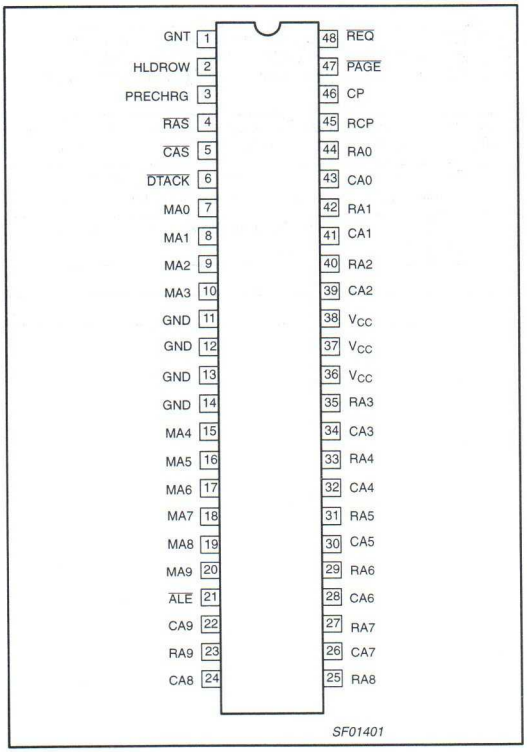
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{REQ}$	DRAM Request Input	1.0/1.0	20 μA/0.6 mA
CP	Clock Input	1.0/1.0	20 μA/0.6 mA
$\overline{PAGE}$	Page Mode Select Input	1.0/1.0	20 μA/0.6 mA
PRECHRG	$\overline{RAS}$ Precharge Select Input	1.0/1.0	20 μA/0.6 mA
HLDROW	Row Hold Select Input	1.0/1.0	20 μA/0.6 mA
$\overline{DTACK}$	Data Transfer Ack. Output	50/80	35 mA/60 mA
GNT	Access Grant Output	50/80	35 mA/60 mA
RCP	Refresh Clock Input	1.0/1.0	20 μA/0.6 mA
RA0–9	Row Address Inputs	1.0/1.0	20 μA/0.6 mA
CA0–9	Column Address Inputs	1.0/1.0	20 μA/0.6 mA
$\overline{ALE}$	Address Latch Enable Input	1.0/1.0	20 μA/0.6 mA
$\overline{RAS}$	Row Address Strobe Output	NA	35 mA/60 mA
$\overline{CAS}$	Column Address Strobe Output	NA	35 mA/60 mA
MA0–9	DRAM Address Outputs	NA	35 mA/60 mA

NOTES:
One (1.0) FAST Unit Load is defined as 20 μA in the HIGH state and 0.6 mA in the LOW state.
FAST Unit Loads do not correspond to DRAM Input Loads. See Functional Description for details.

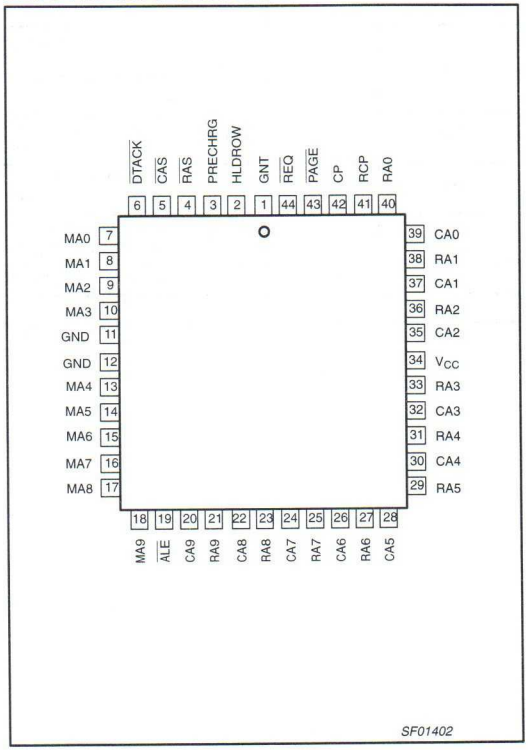
BLOCK DIAGRAM



DIP PIN CONFIGURATION



PLCC PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	PINS DIP	TYPE	NAME AND FUNCTION
$\overline{REQ}$	48	Input	Active Low Memory Access Request input, must be asserted for the entire DRAM access cycle. $\overline{REQ}$ is sampled on the rising edge of the CP clock.
GNT	1	Output	Active High Grant output. When High indicates that a DRAM access (inactive during refresh) cycle has begun. Asserted from the rising edge of the CP clock.
$\overline{PAGE}$	47	Input	Active Low Page-Mode Access input. Forces the IDC to keep $\overline{RAS}$ asserted for as long as the $\overline{PAGE}$ input is Low and $\overline{REQ}$ is asserted Low.
HLDROW	2	Input	Row Address Hold input. If Low will configure the IDC to maintain the row addresses for a full CP clock cycle after $\overline{RAS}$ is asserted. If High will program the IDC to maintain row addresses for a 1/2 CP clock cycle after $\overline{RAS}$ is asserted.
PRECHRG	3	Input	$\overline{RAS}$ Precharge input. A Low will program the IDC to guarantee a minimum of 4 CP clock cycles of precharge. A High will guarantee 3 clock cycles of precharge.
CP	46	Input	Clock input. Used by the Controller for all timing and arbitration functions.
$\overline{RCP}$	45	Input	Refresh Clock input. Divided internally by 64 to produce an internal Refresh Request.
$\overline{DTACK}$	6	Output	Active Low, 3-state Data Transfer Acknowledge output. Enabled by the $\overline{REQ}$ input and asserted four clock cycles after the assertion of $\overline{RAS}$, 3-stated when $\overline{REQ}$ goes High.
RA0–9	44, 42, 40, 35, 33, 31, 29, 27, 25, 23	Inputs	Row Address inputs.
CA0–9	43, 41, 39, 34, 32, 30, 28, 26, 24, 22	Inputs	Column Address inputs. Propagated to the MA0–9 outputs 1 CP clock cycle after $\overline{RAS}$ is asserted, if HLDROW = 0 or 1/2 clock cycle later if HLDROW is 1.
$\overline{RAS}$	4	Output	Active Low Row Address Strobe. Asserted for four clock cycles during each refresh cycle regardless of the $\overline{PAGE}$ input. Also asserted for four clock cycles during processor access if the $\overline{PAGE}$ input is High. If $\overline{PAGE}$ is Low, $\overline{RAS}$ is negated upon negation of $\overline{PAGE}$ or $\overline{REQ}$, whichever occurs first.
$\overline{CAS}$	5	Output	Active Low Column Address Strobe. Always asserted 1.5 CP clock cycles after the assertion of $\overline{RAS}$. Negated upon negation of $\overline{REQ}$. HLDROW input pin does not affect $\overline{RAS}$ to $\overline{CAS}$ timing.
MA0–9	7–10, 15–20	Output	DRAM multiplexed address outputs. Row and column addresses asserted on these pins during an access cycle. Refresh counter addresses presented on these outputs during refresh cycles.
$\overline{ALE}$	21	Input	Active Low Address Latch Enable input. A Low on this pin will cause the address latches to be transparent. A High level will latch the RA0–9 and CA0–9 inputs.
V_{CC}	36–38		+5V ±10% Supply voltage.
GND	11–14		Ground

FUNCTIONAL DESCRIPTION

The 74F1763 1 Megabit Intelligent DRAM Controller (IDC) is a synchronous device with most signal timing being a function of the CP input clock.

Arbitration

Once the DRAM's $\overline{RAS}$ precharge time has been satisfied, the $\overline{REQ}$ input is sampled on each rising edge of the CP clock and an internally generated refresh request is sampled on each falling edge of the same clock. When only one of these requests is sampled as active the appropriate memory cycle will begin immediately. For a memory access cycle this will be indicated by GNT and $\overline{RAS}$ outputs both being asserted and for a refresh cycle by multiplexing refresh address to the MA0–9 outputs and subsequent assertion of $\overline{RAS}$ after 1/2CP clock cycle. If both memory access and refresh requests are active at a given time the request sampled first will begin immediately and the other request (if still asserted) will be serviced upon completion of the current cycle and it's associated $\overline{RAS}$ precharge time.

Memory access

The row (RA0–9) and column (CA0–9) address inputs are latched when $\overline{ALE}$ input is High. When $\overline{ALE}$ is Low the input addresses propagate directly to the outputs. When GNT and $\overline{RAS}$ are asserted, after a $\overline{REQ}$ has been sampled the RA0–9 address inputs will have already propagated to the MA0–9 outputs for the row address. One or one-half CP clock cycles later (depending on the state of the HLDROW input) the column address (CA0–9) inputs are propagated to the MA0–9 outputs. $\overline{CAS}$ is always asserted one and one-half CP clock cycles after $\overline{RAS}$ is asserted. If the $\overline{PAGE}$ input is High, $\overline{RAS}$ will be negated approximately four CP clock cycles after its initial assertion. At this time the $\overline{DTACK}$ output becomes valid indicating the completion of a memory access cycle. The IDC will maintain the state of all its outputs until the $\overline{REQ}$ input is negated (see timing waveforms).

Row address hold times

If the HLDROW input of the IDC is High the row address outputs will remain valid 1/2 CP clock cycle after $\overline{RAS}$ is asserted. If the HLDROW input is Low the row address outputs will remain valid one CP clock cycle after $\overline{RAS}$ is asserted.

$\overline{RAS}$ precharge timing

In order to meet the $\overline{RAS}$ precharge requirement of dynamic RAMs, the controller will hold-off a subsequent $\overline{RAS}$ signal assertion due to a processor access request or a refresh cycle for four or three full CP clock cycles from the previous negation of $\overline{RAS}$, depending on the state of the PRECHRG input. If the PRECHRG input is Low, $\overline{RAS}$ remains High for at least 4 CP clock cycles. If the PRECHRG input is High $\overline{RAS}$ remains High for at least 3 CP clock cycles.

Refresh timing

The refresh address counter wakes-up in an all 1's state and is an up counter. The refresh clock (RCP) is internally divided down by 64 to produce an internal refresh request. This refresh request is recognized either immediately or at the end of a running memory access cycle. Due to the possibility that page mode access cycles may be lengthy, the controller keeps track of how many refresh requests have been missed by logging them internally (up to 128) and servicing any pending refresh requests at the end of the memory access cycle. The controller performs $\overline{RAS}$-only refresh cycles until all pending refresh requests are depleted.

Page-mode access

Fast accesses to consecutive locations of DRAM can be realized by asserting the $\overline{PAGE}$ input as shown in the timing waveforms. In this mode, the controller does not automatically negate $\overline{RAS}$ after four CP clock cycles, but keeps it asserted throughout the access cycle. By using external gates, the $\overline{CAS}$ output can be gated on and off while changing the column address inputs to the controller, which will propagate to the MA_0–MA_9 address outputs and provide a new column address. This is only useful if the $\overline{ALE}$ input is Low, enabling the user to charge addresses. This mode can be used with DRAMs that support page or nibble mode addressing.

Output driving characteristics

Considering the transmission line characteristic of the DRAM arrays, the outputs of the IDC have been designed to provide incident-edge switching (in Dual-Inline-Packaged memory arrays), needed in high performance systems. For more information on the driving characteristics, please refer to Philips Semiconductors application note AN218. The driving characteristics of the 74F1763 are the same as those of the 74F765 shown in the application note.

ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	120	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	–65 to +150	°C

RECOMMENDED OPERATION CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current[1]			–15	mA
I_{OL}	Low-level output current[1]			24	mA
T_A	Operating free-air temperature range	0		70	°C

NOTE:
1. Transient currents will exceed these values in actual operation.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –15 mA	±10% V_{CC}	2.5			V
				±5% V_{CC}	2.7	3.4		V
			I_{OH2}[3] = –35 mA	±5% V_{CC}	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24 mA	±10% V_{CC}		0.35	0.50	V
				±5% V_{CC}		0.35	0.50	V
			I_{OL2}[4] = 60 mA	±5% V_{CC}		0.35	0.80	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					–0.6	mA
I_{OS}	Output current[5]	V_{CC} = MAX, V_O = 2.25V			–100		–225	mA
I_{CC}	Supply current (total)	V_{CC} = MAX					220	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OH2} is transient current necessary to guarantee a Low to High transition in a 70Ω transmission line.
4. I_{OL2} is transient current necessary to guarantee a High to Low transition in a 70Ω transmission line.
5. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

NO	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = 25°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 300pF$ $R_L = 70\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 300pF$ $RL = 70\Omega$		
			MIN	TYP	MAX	MIN	MAX	
1	CP clock period (tcp)		10			10		ns
2	CP clock low time		5			5		ns
3	CP clock high time		5			5		ns
4	RCP clock period		100			100		ns
5	RCP clock low time		10			10		ns
6	RCP clock high time		10			10		ns
7	Setup time $\overline{REQ}(\downarrow)$ to CP(↑)		4	2		4		ns
8	$\overline{REQ}$ High hold time after CP(↑)[1]		0			0		ns
9	$\overline{REQ}$ High pulse width[2]		1/2tcp + 5	1/2tcp + 5	1/2tcp + 5	1/2tcp + 5	1/2tcp + 5	ns
10	Propagation delay CP(↑) to GNT High		8.5	11	13.5	8.5	15.5	ns
11	Propagation delay $\overline{REQ}(\uparrow)$ to GNT Low		8.5	10.5	13	8.5	14	ns
12	$\overline{ALE}$ pulse width Low		4	1		4		ns
13	RA0–9, CA0–9 High or Low setup to $\overline{ALE}(\uparrow)$		2	0		2		ns
14	ALE(↑) to RA0–9, CA0–9 High or Low hold		1	0		1		ns
15	Propagation delay RA0–9, CA0–9 High or Low to MA0–9[3]	$\overline{ALE}$ Low	4	7.5	11	4	14	ns
16	Propagation delay $\overline{ALE}(\downarrow)$ to MA0–9		5.5	8.5	13	5.5	15	ns
17	Propagation delay CP(↑) to $\overline{RAS}(\downarrow)$		8.5	10.5	12.5	8.5	14	ns
18	$\overline{RAS}(\downarrow)$ to MA0–9 (column address) skew	HLDROW = 1	1/2tcp – 2	1/2tcp + 2	1/2tcp + 5.5	1/2tcp – 2.5	1/2tcp + 7	ns
19	$\overline{RAS}(\downarrow)$ to MA0–9 (column address) skew	HLDROW = 0	1tcp – 2	1tcp + 2	1tcp + 5.5	1tcp – 2.5	1tcp + 7	ns
20	$\overline{RAS}(\downarrow)$ to $\overline{RAS}(\uparrow)$ skew	PAGE = 1	4tcp + 1.5	4tcp + 3.5	4tcp + 6	4tcp + 1	4tcp + 6.5	ns
21	Propagation delay CP(↑) to $\overline{RAS}(\uparrow)$		12	14	16.5	12	18.5	ns
22	Propagation delay REQ(↑) to RAS(↑)[4]		14.5	17.5	20	14	24	ns
23	Propagation delay CP(↓) to $\overline{CAS}(\downarrow)$		6	8	10	6	11	ns
24	Propagation delay $\overline{PAGE}(\uparrow)$ to $\overline{RAS}(\uparrow)$[4]		10	12.5	15	10	17	ns
25	$\overline{RAS}(\downarrow)$ to $\overline{CAS}(\downarrow)$ skew		1.5tcp–4.5	1.5tcp–2.5	1.5tcp–0.5	1.5tcp–5.5	1.5tcp	ns
26	Propagation delay $\overline{REQ}(\uparrow)$ to $\overline{CAS}(\uparrow)$		10	12	15	10	17	ns
27	MA0–9 (column address) to $\overline{CAS}(\downarrow)$ skew		1tcp – 8	1tcp – 4	1tcp – 0.5	1tcp – 9	1tcp – 0.5	ns
28	MA0–9 (column address) to $\overline{CAS}(\downarrow)$ skew	HLDROW = 0	1/2tcp – 8	1/2tcp – 4	1/2tcp – 0.5	1/2tcp – 9	1/2tcp – 0.5	ns
29	Set-up time $\overline{PAGE}(\downarrow)$ to CP(↑)		2			2		ns

AC ELECTRICAL CHARACTERISTICS (Continued)

NO	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = 25°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 300pF$ $R_L = 70\Omega$			$T_A = 0°C$ TO $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 300pF$ $RL = 70\Omega$		
			MIN	TYP	MAX	MIN	MAX	
30	Propagation delay $\overline{REQ}$(↓) to $\overline{DTACK}$(↑)		6	8	11.5	6	12	ns
31	Propagation delay CP(↑) to $\overline{DTACK}$(↓)		7.5	9.5	12	7.5	13	ns
32	Propagation delay $\overline{REQ}$(↑) to $\overline{DTACK}$ (3-state)		9	12	13	9	15.5	ns
33	MA0–9 (refresh address) to $\overline{RAS}$(↓) skew		1/2tcp – 5			1/2tcp – 6.5		ns
34	$\overline{RAS}$(↓) to MA0–9 (refresh address) skew		1tcp – 2			1tcp – 2.5		ns
35	RAS(↑) to RAS(↓) skew (precharge)	PRECHRG = 0	4tcp – 6	4tcp – 3.5	4tcp – 1.5	4tcp – 6.5	4tcp – 6.5	ns
36	RAS(↑) to RAS(↓) skew (precharge)	PRECHRG = 1	3tcp – 6	3tcp – 3.5	3tcp – 1.5	3tcp + 1	3tcp – 6.5	ns

NOTES:
1. $\overline{REQ}$ High hold means that, if $\overline{REQ}$ is High at the rising clock edge, it is guaranteed that the $\overline{REQ}$ input was not sampled as Low.
2. A 50% duty cycle clock is recommended. If the duty cycle of the clock is not 50%, $\overline{REQ}$ should be held high for enough time such that a falling CP clock edge samples $\overline{REQ}$ as High. This is to ensure that refresh cycles don't get locked-up.
3. When $\overline{ALE}$ is Low, the address input latches are in the transparent mode and therefore any changes in the address inputs will be propagated to the MA0–9 outputs. Figure 2 illustrates RA0–9 inputs propagating to the MA0–9 outputs, but later in the cycle, if $\overline{ALE}$ is still Low when the CA0–9 inputs are multiplexed to the MA0–9 outputs the CA0–9 inputs will be in the transparent mode.
4. If $\overline{PAGE}$ is High and $\overline{REQ}$ is Low, $\overline{RAS}$ is automatically negated after approximately 4 CP clock cycles. If $\overline{PAGE}$ is Low and $\overline{REQ}$ is also Low, $\overline{RAS}$ will be negated when $\overline{PAGE}$ goes High. $\overline{RAS}$ will always be negated when $\overline{REQ}$ goes High regardless of the state of $\overline{PAGE}$ input.

TIMING DIAGRAMS

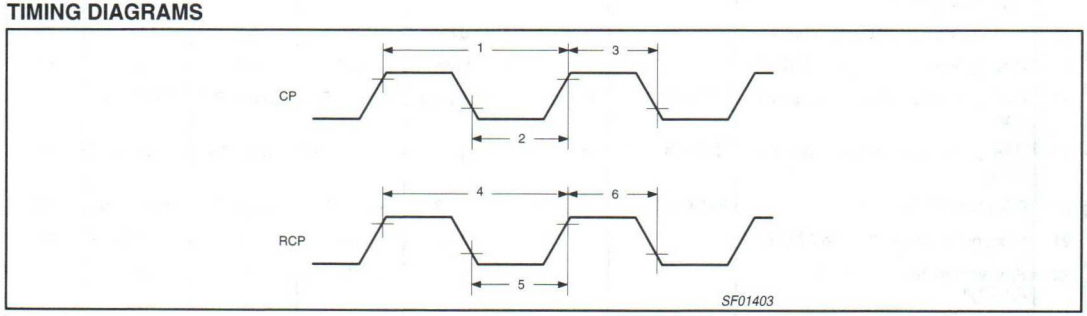
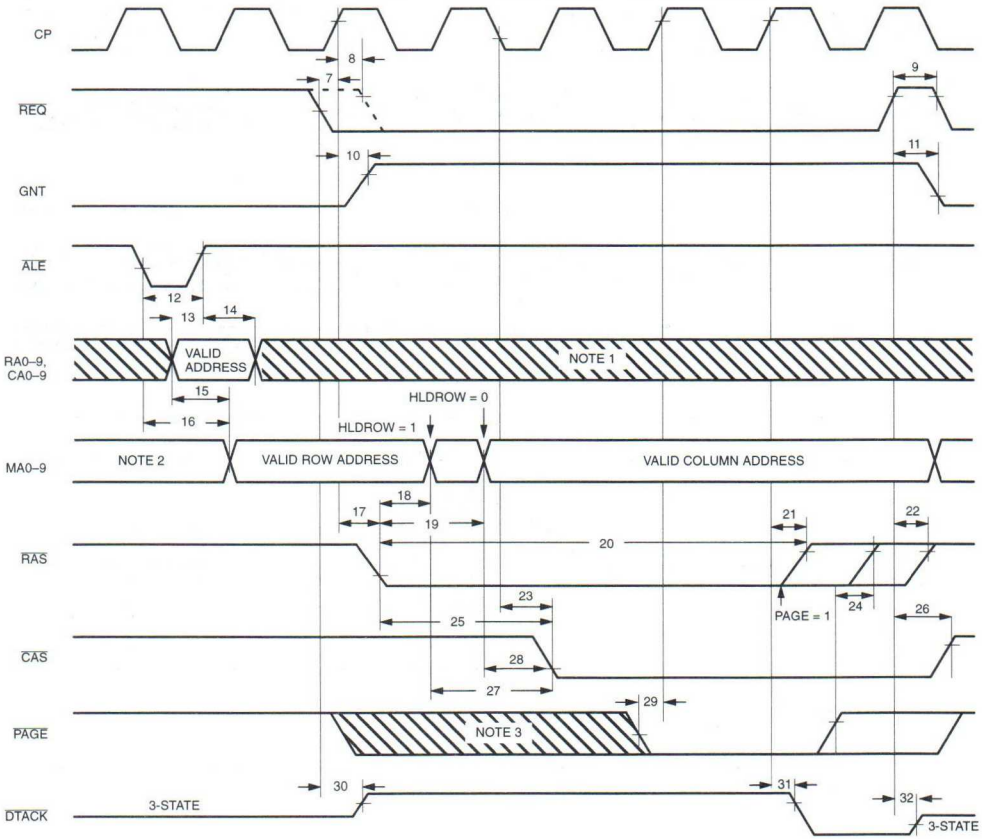


Figure 1. Clock cycle timing

TIMING DIAGRAMS (Continued)

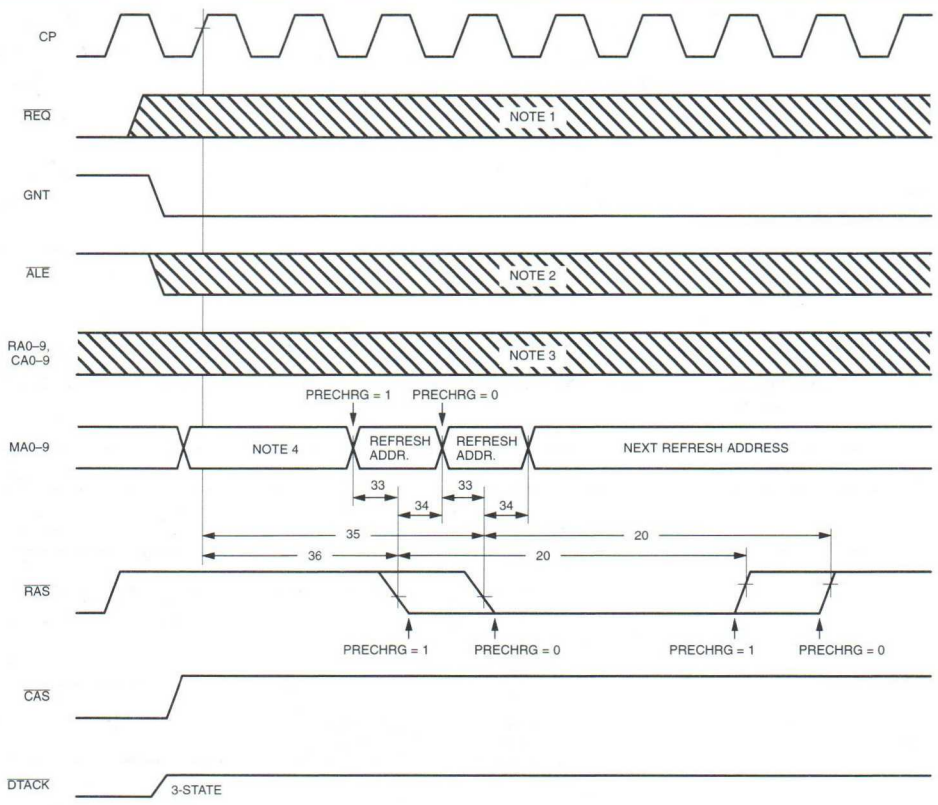


NOTE 1: If the RA0–9 and CA0–9 address inputs are not latched, RA0–9 inputs should remain valid until row address hold time is met and CA0–9 inputs should remain valid until column address hold time is met.
NOTE 2: MA0–9 outputs will contain the present row address on the RA0–RA9 inputs or the last row address latched into the device.
NOTE 3: $\overline{PAGE}$ input may be asserted anytime before this rising clock edge in order to hold $\overline{RAS}$ low.

SF01404

Figure 2. Memory access cycle timing

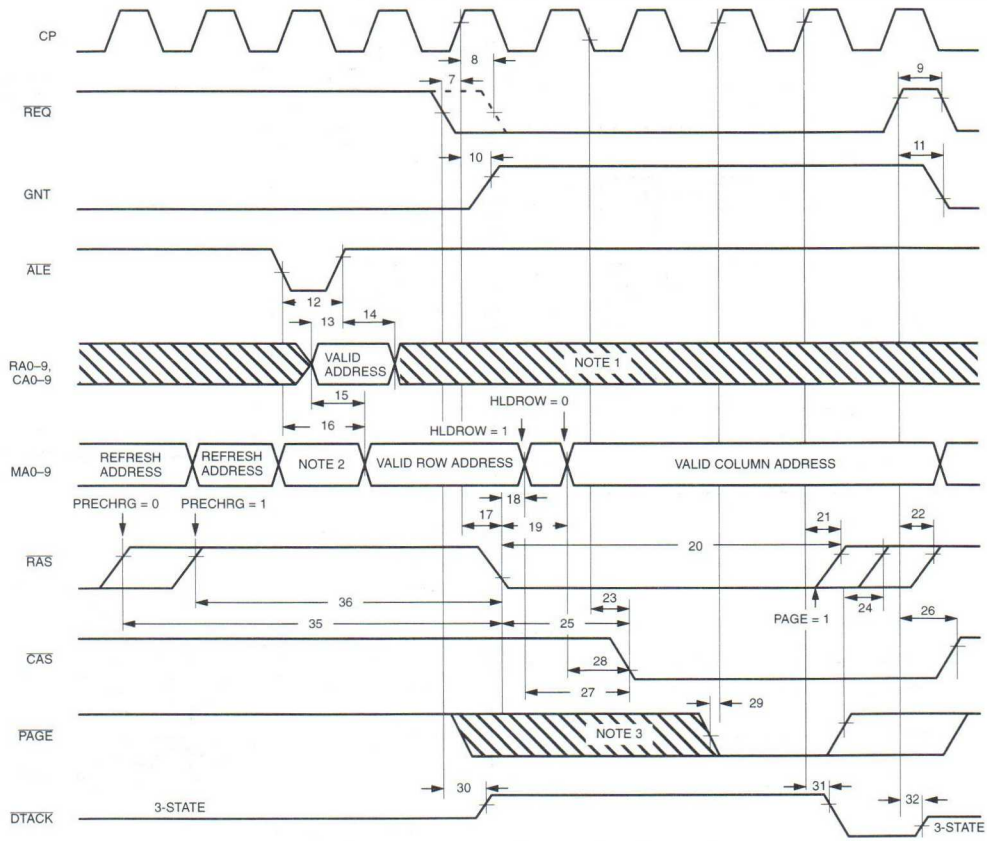
TIMING DIAGRAMS (Continued)



NOTE 1: REQ input is a don't care during a memory refresh cycle. If REQ is asserted during a refresh cycle, it will be recognized at the first rising CP clock edge, following the refresh cycle and its associated RAS precharge time (see Figure 4).
NOTE 2: RA0–9 and CA0–9 address inputs may be latched at anytime during a memory refresh cycle. However, a memory access cycle will not begin until after the completion of the refresh cycle.
NOTE 3: RA0–9 and CA0–9 if in the transparent mode do not propogate to the MA0–9 outputs during a refresh cycle.
NOTE 4: MA0–9 output will contain the present row address on the RA0–RA9 inputs or the last row address latched into the device. *SF01405*

Figure 3. Refresh cycle timing following a memory access cycle

TIMING DIAGRAMS (Continued)



NOTE 1: If the RA0–9 and CA0–9 address inputs are not latched, RA0–9 inputs should remain valid until row address hold time is met and CA0–9 inputs should remain valid until column address hold time is met.
NOTE 2: MA0–9 outputs will contain the present row address on the RA0–RA9 inputs or the last row address latched into the device.
NOTE 3: $\overline{PAGE}$ input may be asserted anytime before this rising clock edge in order to hold $\overline{RAS}$ low.

SF01406

Figure 4. Memory access cycle timing following a refresh cycle

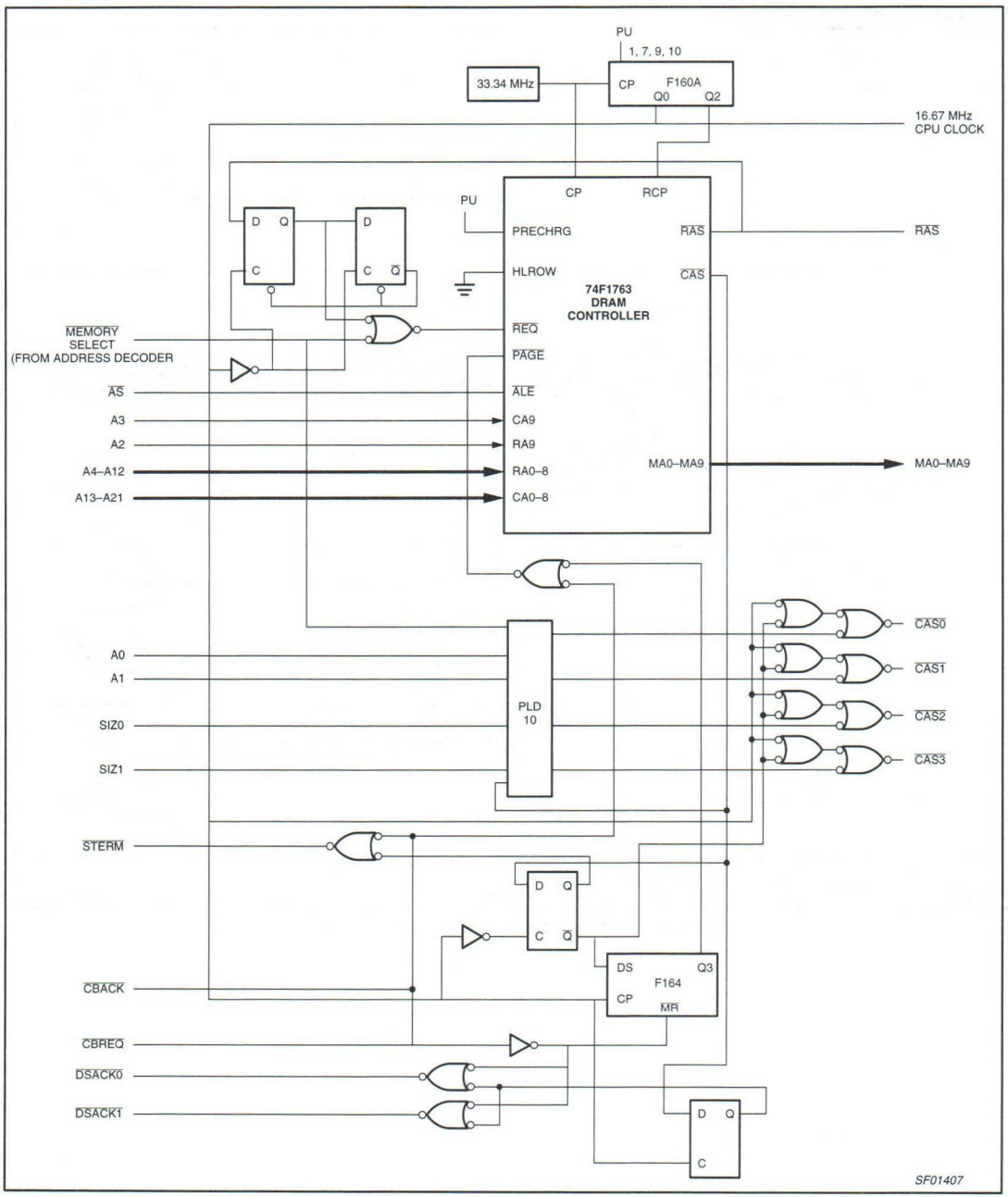
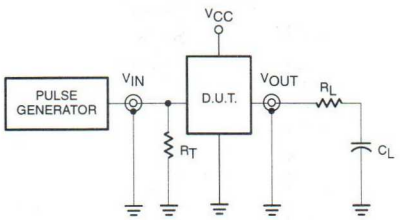
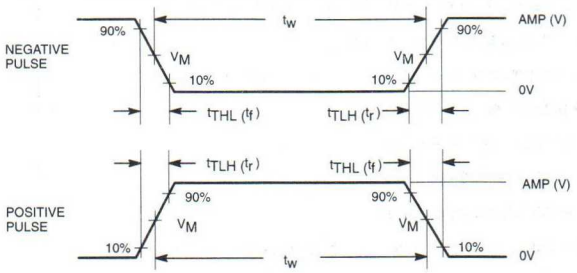


Figure 5. 16.67 MHz 68030 interface with 74F1763 for cache burst mode support using 4Mbytes of 100nsec. nibble-mode DRAMs (Four 32 bit words read to or written from cache in only clock cycles

TEST CIRCUIT AND WAVEFORMS



Test Circuit Simulating RAM Boards



DEFINITIONS:

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep. Rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

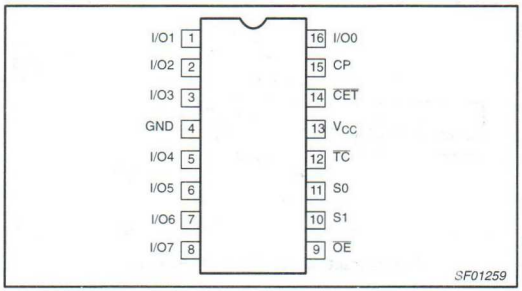
SF01408

8-bit bidirectional binary counter (3-State) 74F1779

FEATURES

- Multiplexed 3-State I/O ports for bus oriented applications
- Built-in look-ahead carry capability
- Center power pins to reduce effects of package inductance
- Count frequency 145MHz typical
- Supply current 90mA typical
- See 74F269 for 24-pin separate I/O port version
- See 74F579 for 20-pin version
- See 74F779 for 16-pin version with abbreviated function table

PIN CONFIGURATION



DESCRIPTION

The 74F1779 is a fully synchronous 8-stage up/down counter with multiplexed 3-State I/O ports for bus-oriented applications. All control functions (hold, count up, count down, synchronous load) are controlled by two mode pins (S0, S1). The device also features carry look-ahead for easy cascading. All state changes are initiated by the rising edge of the clock. When $\overline{CET}$ is High, the data outputs are held in their current state and $\overline{TC}$ is held High. the $\overline{TC}$ output is not recommended for use as a clock or asynchronous reset due to the possibility of decoding spikes.

The 74F1779 differs from 74F779 in that it has an additional hold mode as described in the Function Table.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1779	130MHz	100mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PACKAGE DRAWING NUMBER
16-pin Plastic DIP	N74F1779N	SOT38-4
16-pin Plastic SOL	N74F1779D	SOT162-1

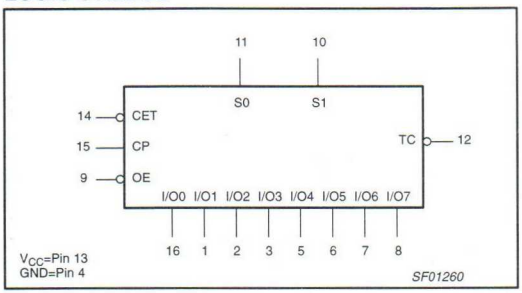
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I/On	Data inputs	3.5/1.0	70μA/0.6mA
	Data outputs	150/40	3.0mA/24mA
S0, S1	Select inputs	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/1.0	20μA/0.6mA
CP	Clock input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{TC}$	Terminal Count output (active Low)	50/33	1.0mA/20mA

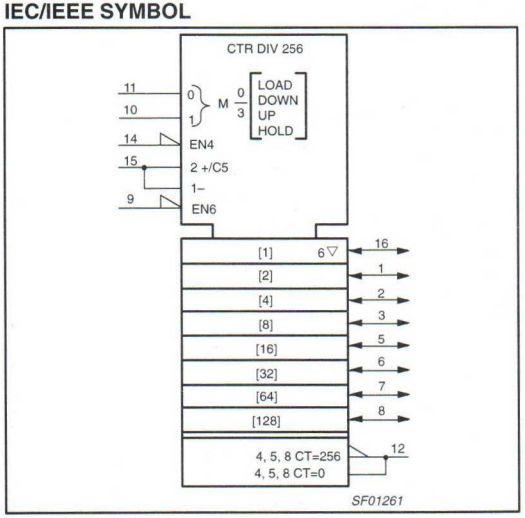
NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

8-bit bidirectional binary counter (3-State) 74F1779

LOGIC SYMBOL



IEC/IEEE SYMBOL

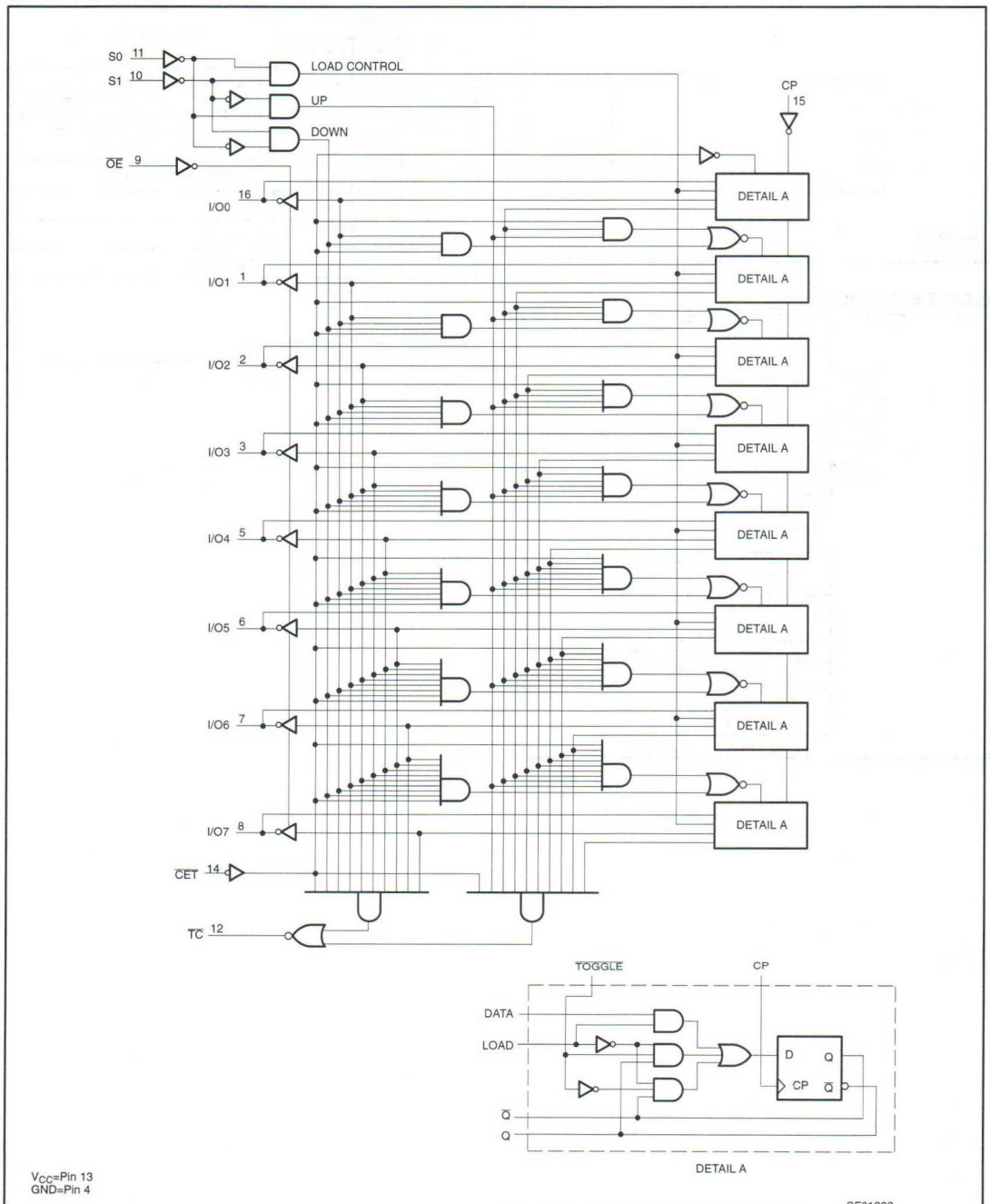


FUNCTION TABLE

INPUTS					OPERATING MODE
S1	S0	$\overline{CET}$	$\overline{OE}$	CP	
X	X	X	H	X	I/O0 to I/O7 in High impedance
X	X	X	L	X	Flip-flop outputs appear on I/O lines
L	L	X	H	↑	Parallel load all flip-flops
(not LL)		H	X	↑	Hold ($\overline{TC}$ held High)
H	H	X	X	↑	Hold
H	L	L	X	↑	Count up
L	H	L	X	↑	Count down

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
(not LL) = S0 and S1 should never be Low voltage level at the same time in the hold mode only.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	$\overline{TC}$	40	mA
		I/On	48	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	$\overline{TC}$			−1	mA
		I/On			−3	mA
I_{OL}	Low-level output current	$\overline{TC}$			20	mA
		I/On			24	mA
T_{amb}	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	$\overline{TC}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/On	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	I/On	V_{CC} = 5.5V, V_I = 5.5V					1	mA
		others	V_{CC} = 5.5V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	except I/On	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					−0.6	mA
$I_{IH}+I_{OZH}$	Off-state output current High-level voltage applied	I/On	V_{CC} = MAX, V_O = 2.7V					70	µA
$I_{IL}+I_{OZL}$	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					−600	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				100	145	mA
		I_{CCL}					100	145	mA
		I_{CCZ}					110	155	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V. T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	115	130		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to I/On	Waveform 1	4.0 5.0	6.5 7.0	10.0 10.5	4.0 5.0	10.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	4.0 4.5	6.5 6.5	9.0 9.0	3.5 4.0	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 2	2.0 2.5	4.0 4.5	6.5 7.0	2.0 2.5	7.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 4 Waveform 5	2.0 4.5	4.0 6.5	6.5 9.0	2.0 4.0	7.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Enable time from High or Low level	Waveform 4 Waveform 5	1.0 1.0	3.0 4.0	6.0 7.0	1.0 1.0	6.5 7.5	ns

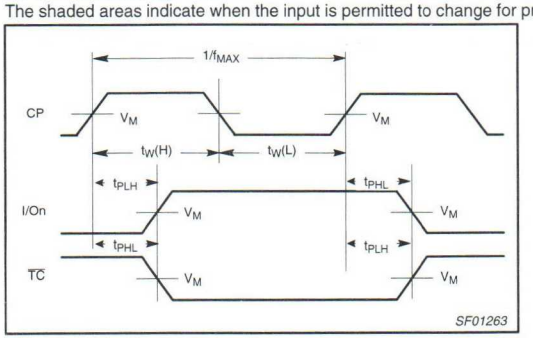
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_n to CP	Waveform 3	4.0 3.5			4.5 3.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CET}$ to CP	Waveform 3	4.5 7.0			5.0 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CET}$ to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low Sn to CP	Waveform 3	7.5 8.5			8.0 9.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Sn to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	3.0 4.5			3.0 5.5		ns

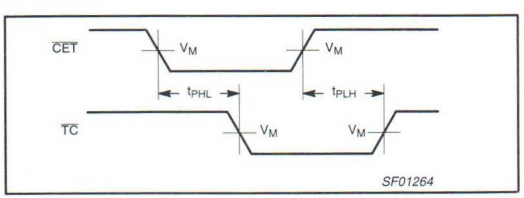
AC WAVEFORMS

For all waveforms, V_M = 1.5V.

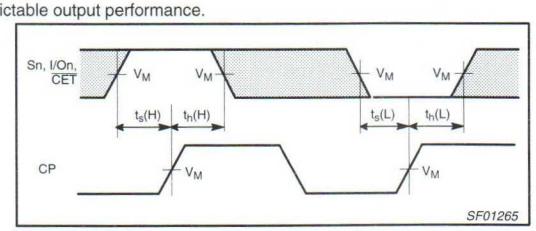
The shaded areas indicate when the input is permitted to change for predictable output performance.



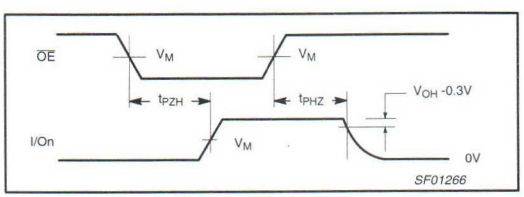
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



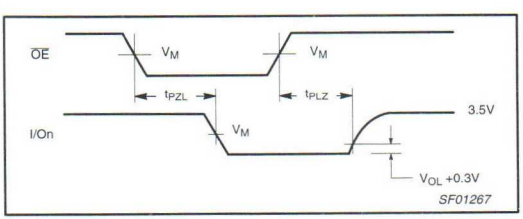
Waveform 2. Propagation Delay, $\overline{CET}$ Input to Terminal Count Output



Waveform 3. Data Setup and Hold Times

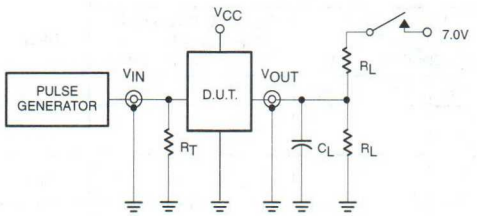


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

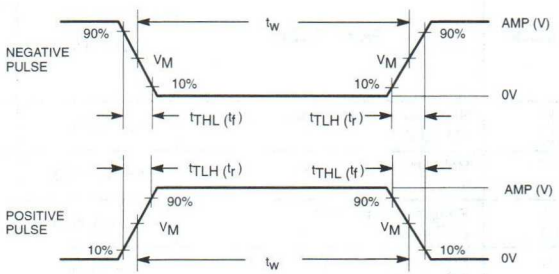


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

Octal buffers | 74F2240, 74F2241

FEATURES

- Octal bus interface
- 30Ω output termination ideal for driving DRAM
- 15mA source current

DESCRIPTION

The 74F2240 and 74F2241 are octal buffers that are ideal for driving dynamic DRAM with impedance matching. The outputs are all capable of sinking 5mA and sourcing up to 15mA. The device features two output enables, each controlling four of the 3-state outputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F2240	4.3ns	37mA
74F2241	4.5ns	30mA

ORDERING INFORMATION

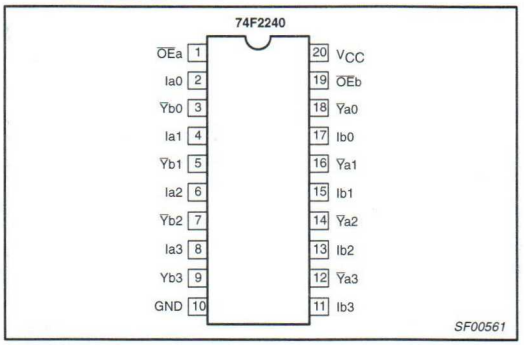
DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
20-pin plastic DIP	N74F2240N, N74F2241N	SOT146-1
20-pin plastic SOL	N74F2240D, N74F2241D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

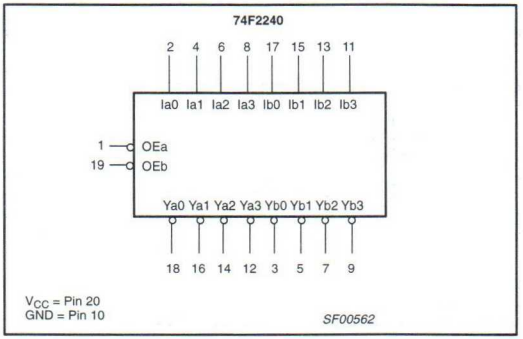
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ian, Ibn	Data inputs	1.0/0.33	20µA/0.2mA
$\overline{OE}$a, $\overline{OE}$b	Output enable inputs (active Low)	1.0/0.33	20µA/0.2mA
OEb	Output enable input (74F2241)	1.0/0.33	20µA/0.2mA
Yan, Ybn	Data outputs (74F2241)	750/8.33	15mA/5mA
$\overline{Y}$an, $\overline{Y}$bn	Data outputs (74F2240)	750/8.33	15mA/5mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

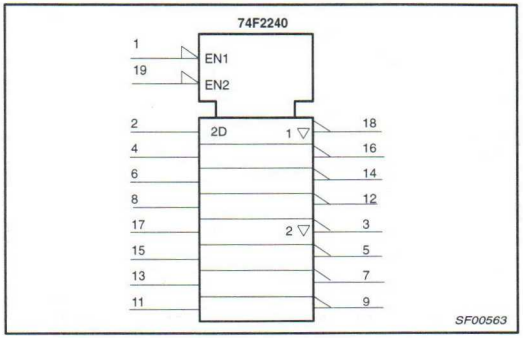
PIN CONFIGURATION



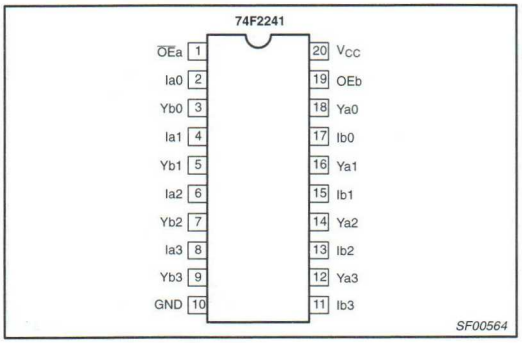
LOGIC SYMBOL



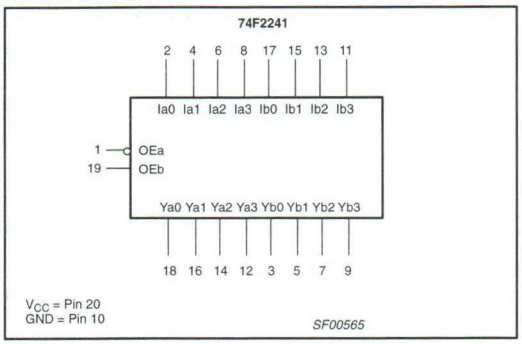
IEC/IEEE SYMBOL



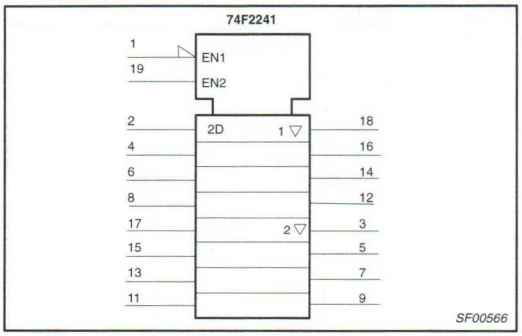
PIN CONFIGURATION



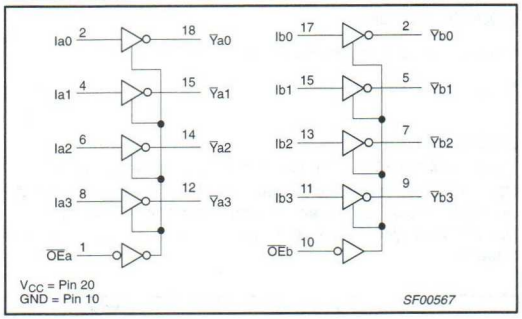
LOGIC SYMBOL



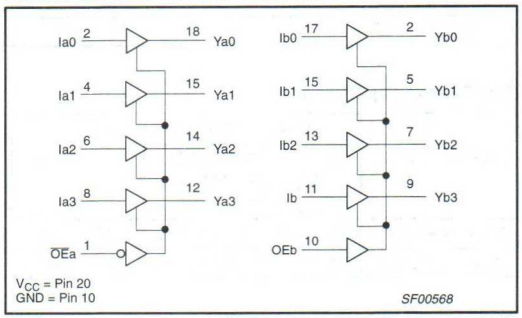
IEC/IEEE SYMBOL



LOGIC DIAGRAM FOR 74F2240



LOGIC DIAGRAM FOR 74F2241



FUNCTION TABLE FOR 74F2240

INPUTS				OUTPUTS	
$\overline{OE}a$	Ia	$\overline{OE}b$	Ib	$\overline{Y}a$	$\overline{Y}b$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

Notes to function table for 74F2240

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

FUNCTION TABLE FOR 74F2241

INPUTS				OUTPUTS	
$\overline{OE}a$	Ia	OEb	Ib	Ya	Yb
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

Notes to function table for 74F2241

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	10	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–15	mA
I_{OL}	Low–level output current			5	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.4		V
					I_{OH} = –15mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL} = MAX	±10%V_{CC}			0.50	V
						±5%V_{CC}		0.42	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				–0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current			V_{CC} = MAX, V_I = 0.5V					–0.2	mA
I_{OZH}	Off–state output current, high–level voltage applied			V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off–state output current, low–level voltage applied			V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short–circuit output current[3]			V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	74F2240	I_{CCH}	V_{CC} = MAX				25	35	mA
			I_{CCL}					53	75	mA
			I_{CCZ}					35	45	mA
		74F2241	I_{CCH}	V_{CC} = MAX				19	30	mA
			I_{CCL}					45	65	mA
			I_{CCZ}					27	40	mA

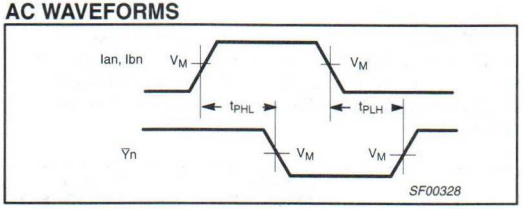
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

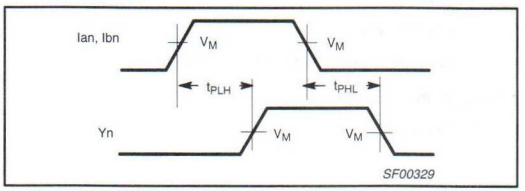
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω MIN	TYP	MAX	LIMITS T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω MIN	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay Ian, Ibn to $\overline{Y}$n	74F2240	Waveform 1	3.0 2.0	5.0 3.5	7.0 5.5	2.5 2.0	8.0 6.0	ns
t_{PZH} t_{PZL}	Output enable time to high or low level		Waveform 3 Waveform 4	3.0 3.5	4.5 5.0	7.0 8.0	2.5 3.0	8.0 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level		Waveform 3 Waveform 4	2.0 1.0	3.5 2.5	6.5 5.5	1.5 1.0	7.0 5.5	ns
t_{PLH} t_{PHL}	Propagation delay Ian, Ibn to Yn	74F2241	Waveform 2	3.0 2.5	4.5 4.5	7.0 6.5	2.5 2.5	8.0 7.5	ns
t_{PZH} t_{PZL}	Output enable time to high or low level		Waveform 3 Waveform 4	3.0 3.5	5.0 5.5	7.0 7.5	2.0 3.0	8.0 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level		Waveform 3 Waveform 4	2.0 1.5	4.0 3.5	6.0 6.0	1.5 1.0	7.0 6.5	ns

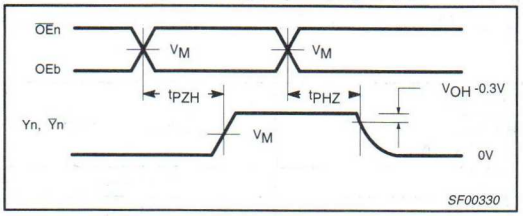
AC WAVEFORMS



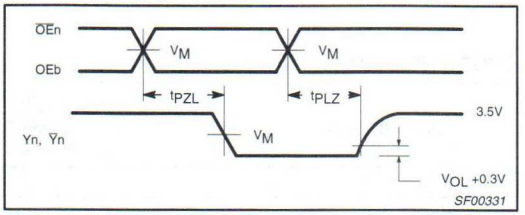
Waveform 1. Propagation delay for inverting outputs



Waveform 2. Propagation delay for non–inverting outputs



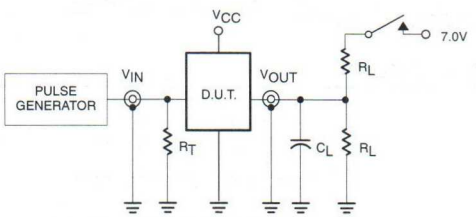
Waveform 3. 3-state output enable time to high level and output disable time from high level



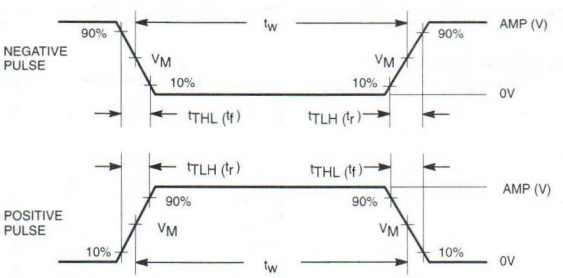
Waveform 4. 3-state output enable time to low level and output disable time from low level

NOTES:
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

Octal buffer with 30Ω equivalent output termination (3-State)

74F2244

FEATURES

- Octal bus interface
- 30Ω output termination ideal for driving DRAM
- 15mA source current
- SSOP Type II Package

DESCRIPTION

The 74F2244 is an octal buffer that is ideal for driving dynamic DRAM with matching impedance. The outputs are all capable of sinking 5mA and sourcing up to 15mA. The device features two output enables, $\overline{OE}a$ and $\overline{OE}b$, each controlling four of the 3–state outputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F2244	4.0ns	30mA

ORDERING INFORMATION

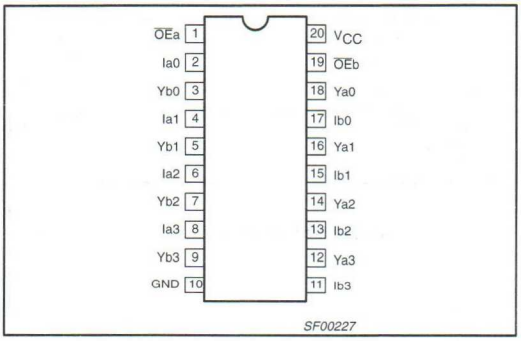
DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
20-pin plastic DIP	N74F2244N	SOT146-1
20-pin plastic SOL	N74F2244D	SOT163-1
20-pin plastic SSOP Type II	N74F2244DB	SOT339-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

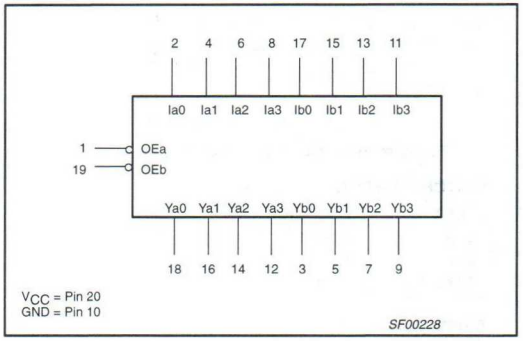
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ian, Ibn	Data inputs	1.0/0.33	20μA/0.2mA
$\overline{OE}a$, $\overline{OE}b$	Output enable inputs (active low)	1.0/0.33	20μA/0.2mA
Yan, Ybn	Data outputs	750/8.33	15mA/5mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.

PIN CONFIGURATION



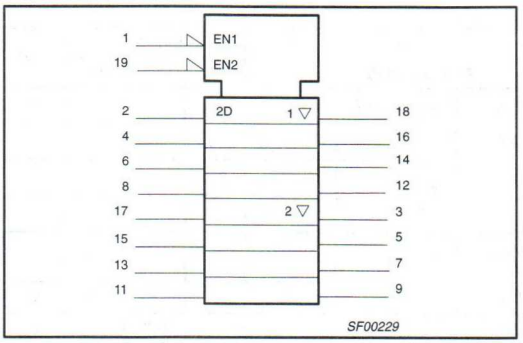
LOGIC SYMBOL



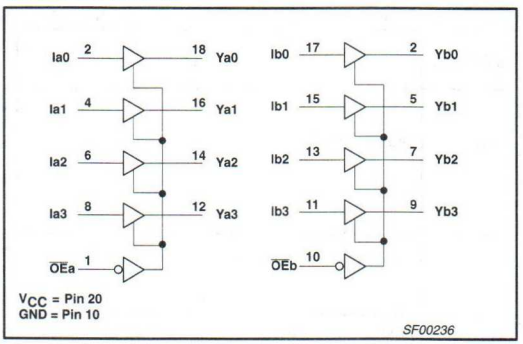
Octal buffer with 30Ω equivalent output termination (3-State)

74F2244

IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE}a$	Ia	$\overline{OE}b$	Ib	Ya	Yb
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	Z	Z

Notes to function table

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	10	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–15	mA
I_{OL}	Low–level output current			5	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10%V_C	2.5			V
				±5%V_{CC}	2.7	3.4		V
			I_{OH} = –15mA	±10%V_C	2.0			V
				±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = MAX	±10%V_C			0.50	V
		V_{IH} = MIN,		±5%V_{CC}		0.42	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				–0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current	V_{CC} = MAX, V_I = 0.5V					–0.2	mA
I_{OZH}	Off–state output current, high–level voltage applied	V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off–state output current, low–level voltage applied	V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short–circuit output current[3]	V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			20	30	mA
		I_{CCL}				45	65	mA
		I_{CCZ}				26	40	mA

NOTES:

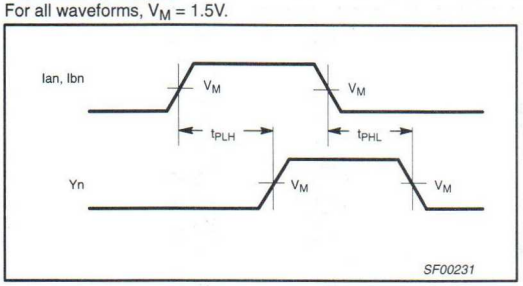
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

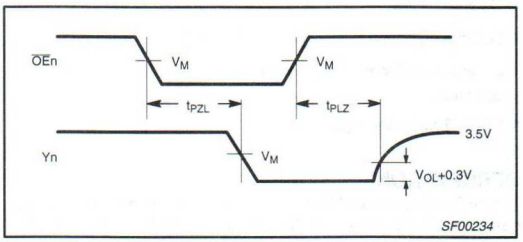
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Ian, Ibn to Yn	Waveform 1	3.0 2.5	4.5 4.5	7.0 7.0	2.5 2.5	8.0 7.5	ns
t_{PZH} t_{PZL}	Output enable time to high or low level	Waveform 2 Waveform 3	2.5 3.0	4.5 5.0	7.5 8.0	2.0 3.0	8.0 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level	Waveform 2 Waveform 3	1.5 1.5	3.5 2.5	6.0 5.5	1.0 1.0	6.0 5.5	ns

AC WAVEFORMS

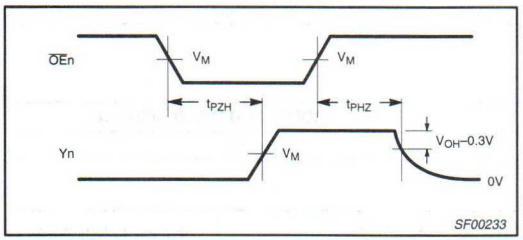
For all waveforms, V_M = 1.5V.



Waveform 1. Propagation delay for data to outputs



Waveform 3. 3-State output enable time to low level and output disable time from low level

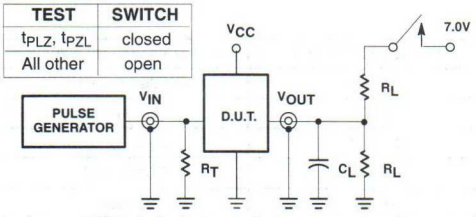


Waveform 2. 3-State output enable time to high level and output disable time from high level

TEST CIRCUIT AND WAVEFORMS

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



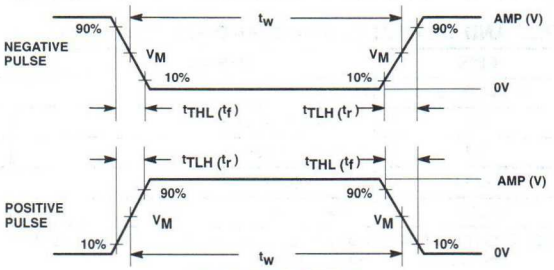
Test circuit for 3-State outputs

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF000235

Octal transceiver with 30Ω equivalent output termination (3-State)

74F2245

FEATURES

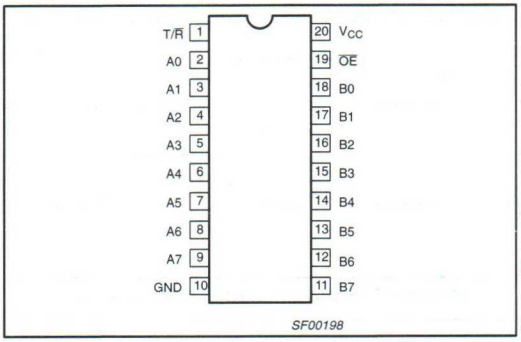
- Octal bidirectional bus interface
- 30 Ohm output termination for driving DRAM
- Outputs are placed in high impedance state during power-off conditions
- SSOP Type II package

DESCRIPTION

The 74F2245 is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both transmit and receive directions. The device features an Output Enable ($\overline{OE}$) input for easy cascading and Transmit/Receive (T/$\overline{R}$) input for direction control. The 3-State outputs, B0-B7, have been designed to prevent output bus loading if the power is removed from the device.

The 30 Ohm series termination on the outputs reduces over/undershoot making them ideal for driving DRAM.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F2245	4.0ns	70mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
20-Pin Plastic DIP	N74F2245N	SOT146-1
20-Pin Plastic SOL	N74F2245D	SOT163-1
20-Pin Plastic SSOP	N74F2245DB	SOT339-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

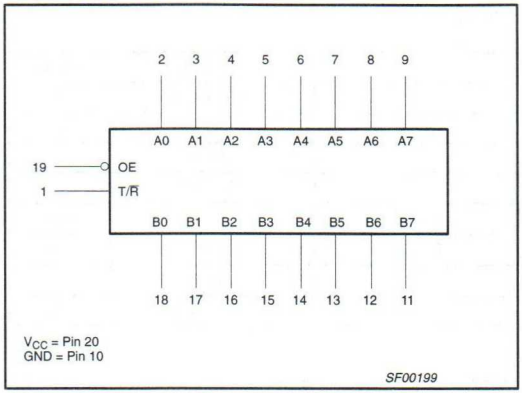
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0-A7, B0-B7	Data inputs	3.5/1.0	70μA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/2.0	20μA/1.2mA
T/$\overline{R}$	Transmit/Receive input	1.0/2.0	20μA/1.2mA
A0-A7	A port outputs	150/8	3.0mA/5mA*
B0-B7	B port outputs	150/8	3.0mA/5mA*

NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.
* 12mA with reduced noise margin

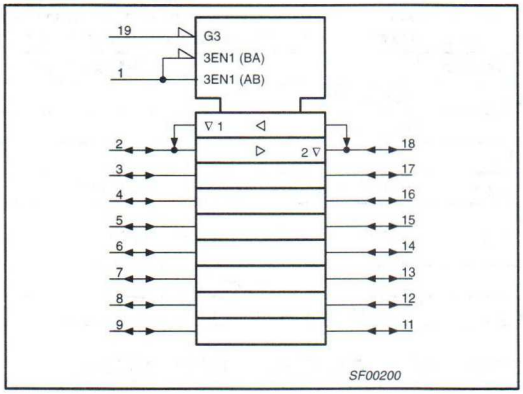
Octal transceiver with 30Ω equivalent output termination (3-State)

74F2245

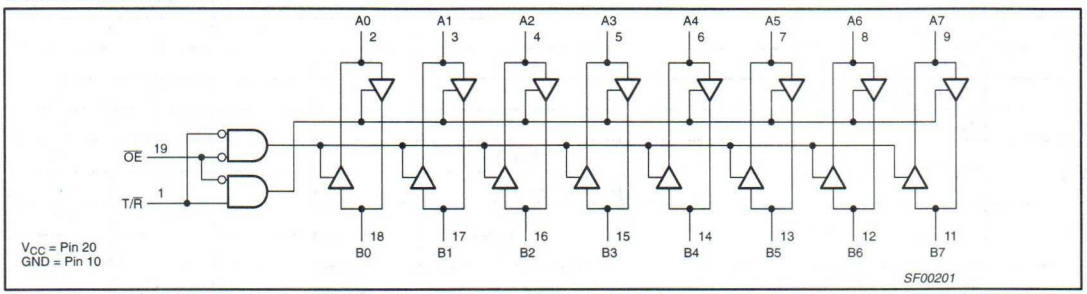
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B data to Bus A
L	H	Bus A data to Bus B
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A0-A7	24	mA
		B0-B7	24	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A0-A7			–3	mA
		B0-B7			–3*	mA
I_{OL}	Low-level output current	A0-A7			5*	mA
		B0-B7			5*	mA
T_{amb}	Operating free-air temperature range		0		+70	°C

* 12 mA with reduced noise margin

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS			UNIT
						MIN	TYP[1]	MAX	
V_{OH}	High-level output voltage	A0-A7, B0-B7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10% V_{CC}	2.4			V
					±5% V_{CC}	2.7	3.4		V
		A0-A7, B0-B7		I_{OH} = –12mA	±10% V_{CC}	2.0			V
					±5% V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A0-A7, B0-B7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 5mA	±10% V_{CC}		0.42	0.50	V
				I_{OL} = 5mA	±5% V_{CC}		0.42	0.50	V
		A0-A7, B0-B7		I_{OL} = 12mA	±10% V_{CC}		0.55	0.67	V
					±5% V_{CC}		0.55	0.67	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	$\overline{OE}$, T/$\overline{R}$	V_{CC} = 5.5V, V_I = 7.0V					100	µA
		A0-A7, B0-B7	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 0.5V					–1.2	mA
I_{IH}+I_{OZH}	Off-state output current High level voltage applied		V_{CC} = MAX, V_O = 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current Low level voltage applied		V_{CC} = MAX, V_O = 0.5V					–600	µA
I_{OS}	Short-circuit output current[3]	A0-A7	V_{CC} = MAX			–60		–150	mA
		B0-B7				–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				60	87	mA
		I_{CCL}					70	100	mA
		I_{CCZ}					75	110	mA

NOTES:

1 For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

2 All typical values are at V_{CC} = 5V, T_{amb} = 25°C.

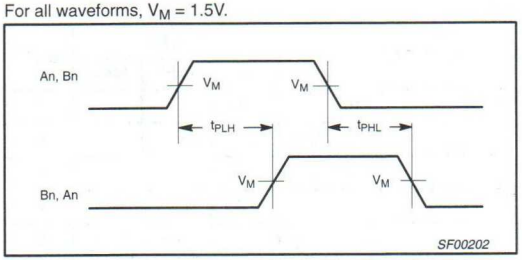
3 Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

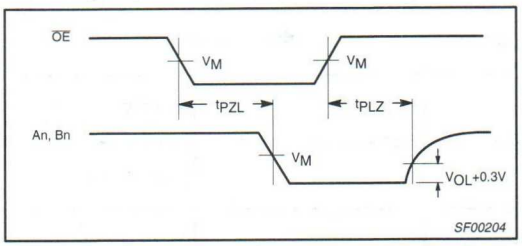
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn, Bn to An	Waveform 1	2.5 2.5	3.5 4.0	7.0 7.0	2.5 2.5	8.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	2.5 3.5	4.5 5.5	8.0 8.5	2.0 3.5	9.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 2 Waveform 3	2.5 1.5	5.0 3.5	7.0 6.5	2.0 1.0	7.5 7.0	ns

AC WAVEFORMS

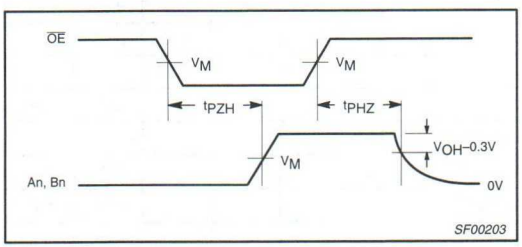
For all waveforms, V_M = 1.5V.



Waveform 1. Propagation Delay for Non-Inverting Output

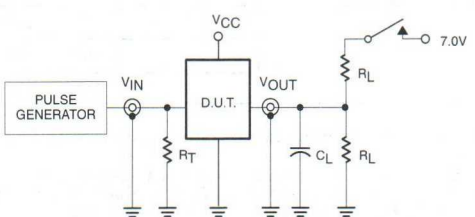


Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

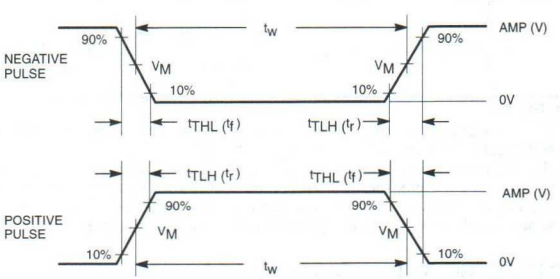


Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

Octal transparent latch with 30Ω equivalent output termination (3-State)

74F2373

FEATURES

- 8-bit transparent latch
- 30 Ohm output termination for driving DRAM
- 3-State outputs glitch free during power-up and power-down
- Common 3-State output register
- Independent register and 3-State buffer operation

DESCRIPTION

The 74F2373 is an octal transparent latch coupled to eight 3-State output devices. The two sections of the device are controlled independently by enable (E) and output enable ($\overline{OE}$) control gates.

The 30 Ohm series termination on the outputs reduces over/undershoot, making them ideal for driving DRAM

The data on the D inputs is transferred to the latch outputs when the enable (E) input is high. The latch remains transparent to the data input while E is high, and stores the data that is present one setup time before the high-to-low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active low output enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is low, latched or transparent data appears at the output.

When $\overline{OE}$ is high, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F2373	4.5ns	35mA

ORDERING INFORMATION

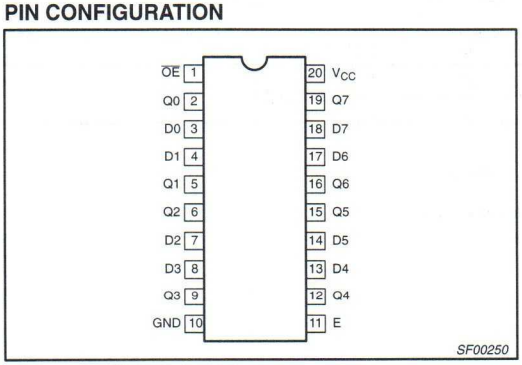
DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
20-pin plastic DIP	N74F2373N	SOT146-1
20-pin plastic SOL	N74F2373D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

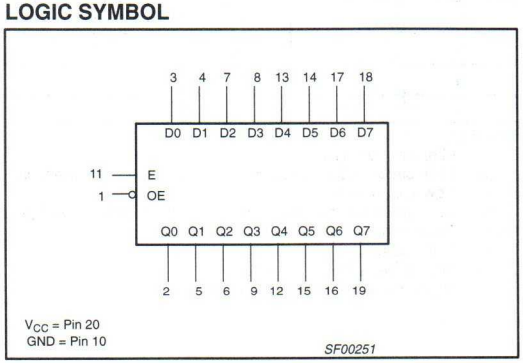
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 - D7	Data inputs	1.0/1.0	20µA/0.6mA
E	Enable input (active high)	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output enable inputs (active low)	1.0/1.0	20µA/0.6mA
Q0 - Q7	3-State outputs	150/40	3.0mA/3.0mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

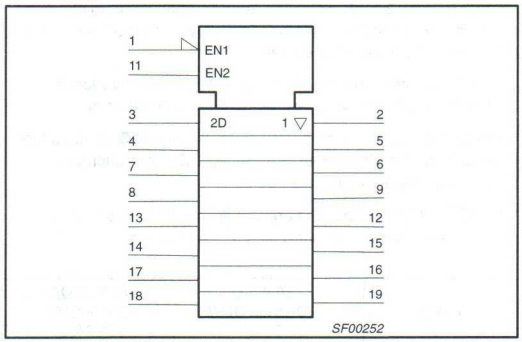
PIN CONFIGURATION



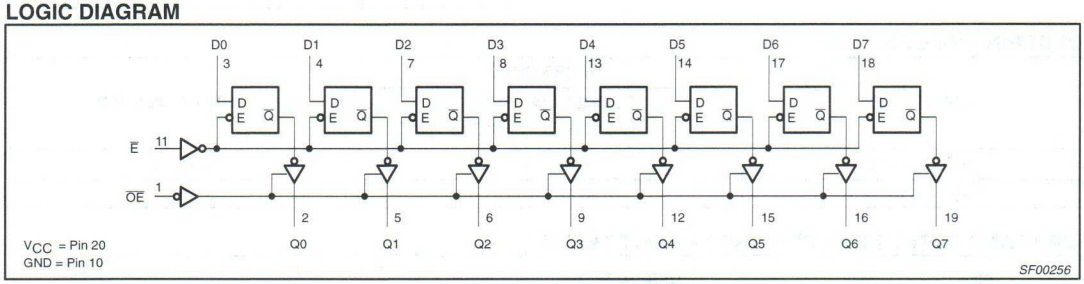
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	Dn		Q0 - Q7	
L	H	L	L	L	Enable and read register
L	H	H	H	H	
L	↓	l	L	L	Latch and read register
L	↓	h	H	H	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	Dn	Dn	Z	

NOTES:

H = High-voltage level
h = High state must be present one setup time before the high-to-low enable transition
L = Low-voltage level
l = Low state must be present one setup time before the high-to-low enable transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-low enable transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	-0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	24	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High-level output current			–3*	mA
I_{OL}	Low-level output current			5*	mA
T_{amb}	Operating free air temperature range	0		+70	°C

* 12mA with reduced noise margin

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}	2.4			V
		V_{IH} = MIN, I_{OH} = –3mA	±5%V_{CC}	2.7	3.4		V
		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}	2.0			V
		V_{IH} = MIN, I_{OH} = –12mA	±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}		0.42	0.50	V
		V_{IH} = MIN, I_{OL} = –5mA	±5%V_{CC}		0.42	0.50	V
		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}		0.67		V
		V_{IH} = MIN, I_{OL} = 12mA	±5%V_{CC}		0.67		V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			35	60	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	Waveform 2	3.0 2.0	5.3 3.7	8.0 6.0	3.0 2.0	9.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay E to Qn	Waveform 1	5.0 3.0	9.0 4.0	12.0 8.0	5.0 3.0	12.5 8.5	ns
t_{PZH} t_{PZL}	Output enable time to high or low level	Waveform 4 Waveform 5	2.0 2.0	5.0 5.6	12.0 8.0	2.0 2.0	12.5 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level	Waveform 4 Waveform 5	2.0 2.0	4.5 3.8	6.5 5.5	2.0 2.0	7.5 6.5	ns

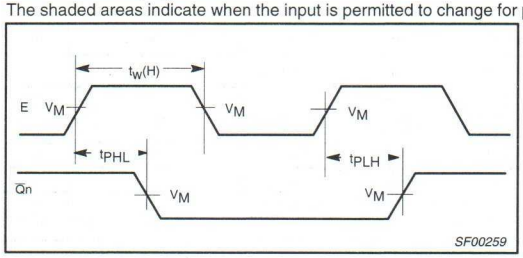
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low level Dn to E	Waveform 3	0 1.0			0 1.0		ns
t_h (H) t_h (L)	Hold time, high or low level Dn to E	Waveform 3	3.0 3.0			3.0 3.0		ns
t_w (H)	E Pulse width, high	Waveform 1	3.5			4.0		ns

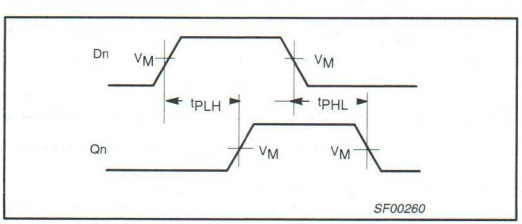
AC WAVEFORMS

For all waveforms, V_M = 1.5V.

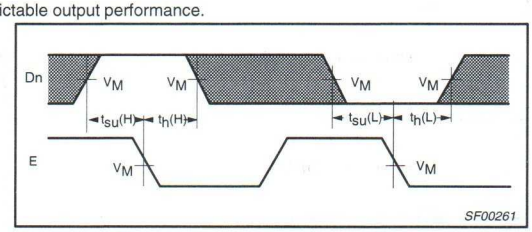
The shaded areas indicate when the input is permitted to change for predictable output performance.



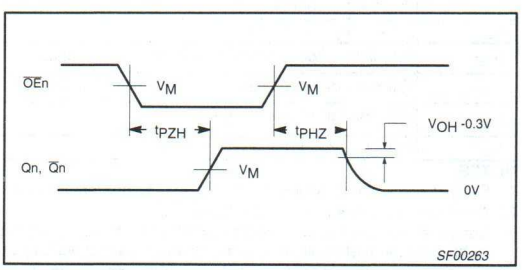
Waveform 1. Propagation delay for enable to output and enable pulse width



Waveform 2. Propagation delay for data to output



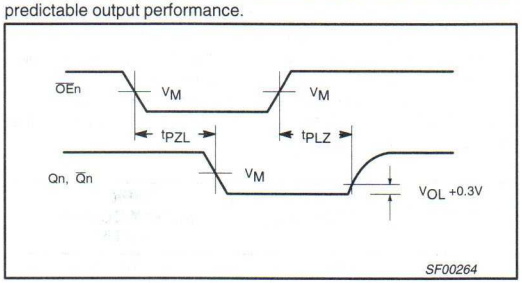
Waveform 3. Data setup time and hold times



Waveform 4. 3-State output enable time to high level and output disable time from high level

AC WAVEFORMS (Continued)

For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

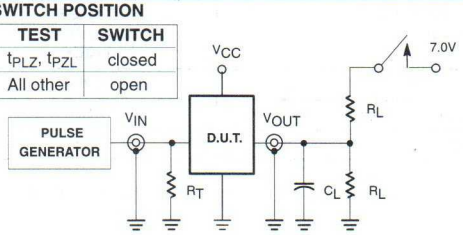


Waveform 5. 3-State output enable time to low level and output disable time from low level

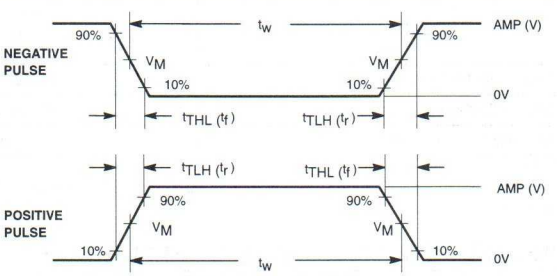
TEST CIRCUIT AND WAVEFORMS

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test circuit for 3-state outputs



Input pulse definition

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00265

Transceivers 74F2952, 74F2953

74F2952 Registered transceiver, non-inverting (3-State)
74F2953 Registered transceiver, inverting (3-State)

FEATURES

- 8-bit registered transceivers
- Two 8-bit, back-to-back registers store data moving in both directions between two bidirectional buses
- Separate Clock, Clock Enable and 3-State Enable provided for each register
- 74F2952 non-inverting
- 74F2953 inverting
- AM2952/2953 functional equivalent
- 'A' outputs sink 24mA and source 3mA
- 'B' outputs sink 64mA and source 15mA
- 300 mil wide 24-pin Slim DIP package

DESCRIPTION

The 74F2952 and 74F2953 are 8-bit registered transceivers. Two 8-bit back-to-back registers store data flowing in both directions between two bi-directional buses. Data applied to the inputs is entered and stored on the rising edge of the Clock (CPXX) provided that the Clock Enable ($\overline{CEXX}$) is Low. The data is then present at the 3-State output buffers, but is only accessible when the Output Enable ($\overline{OEXX}$) is Low. Data flow from 'A' inputs to 'B' outputs is the same as for 'B' inputs to 'A' outputs.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F2952	160MHz	105mA
74F2953	160MHz	105mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PACKAGE DRAWING NUMBER
24-pin Plastic Slim DIP (300mil)	N74F2952N, N74F2953N	SOT222-1
24-pin Plastic SOL[1]	N74F2952D, N74F2953D	SOT137-1
28-pin Plastic Leaded Chip Carrier	N74F2952A, N74F2953A	SOT261-2

NOTE:
1. Thermal mounting techniques are recommended. See *SMD Process Applications* for a discussion of thermal consideration for surface mounted devices.

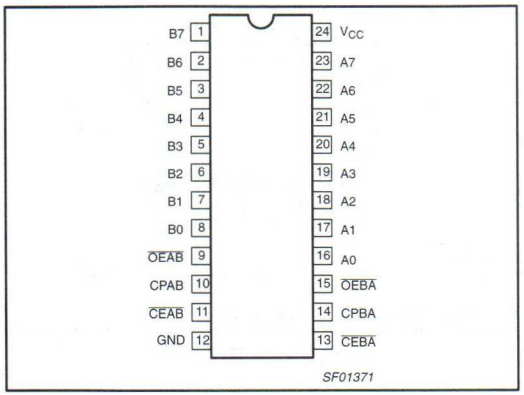
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A7	Port A, 3-State inputs	3.5/1.0	70μA/0.6mA
B0 – B7	Port B, 3-State inputs	3.5/1.0	70μA/0.6mA
CPAB, CPBA	Clock inputs	1.0/1.0	20μA/0.6mA
$\overline{CEAB}$, $\overline{CEBA}$	Clock Enable inputs	1.0/1.0	20μA/0.6mA
$\overline{OEAB}$, $\overline{OEBA}$	Output Enable inputs	1.0/1.0	20μA/0.6mA
A0 – A7	Port A, 3-State outputs	150/40	3.0mA/24mA
B0 – B7	Port B, 3-State outputs	750/106.7	15mA/64mA

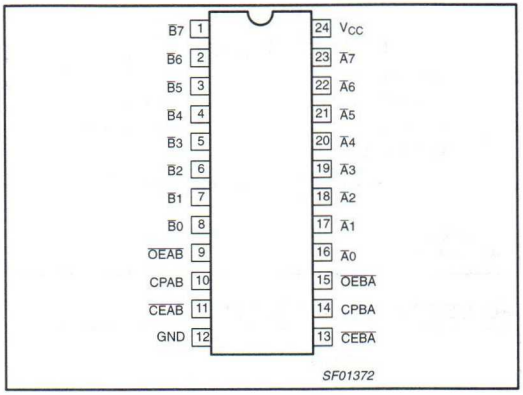
NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATIONS

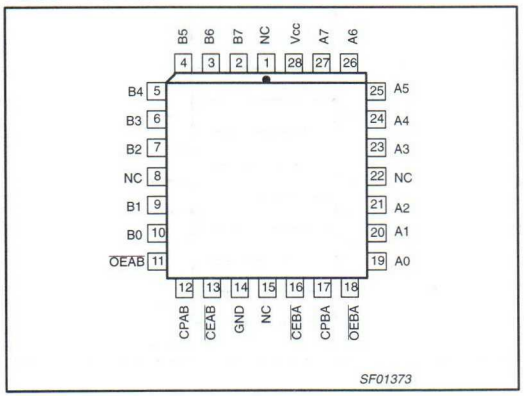
DIP – 74F2952



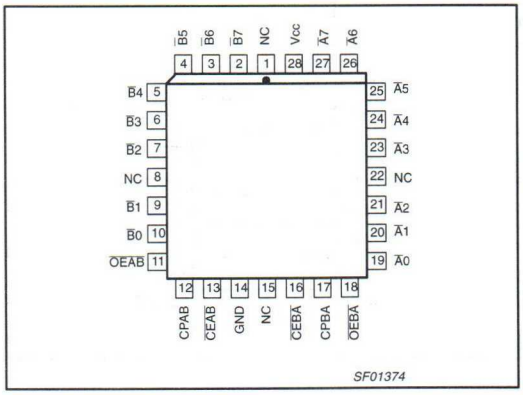
DIP – 74F2953



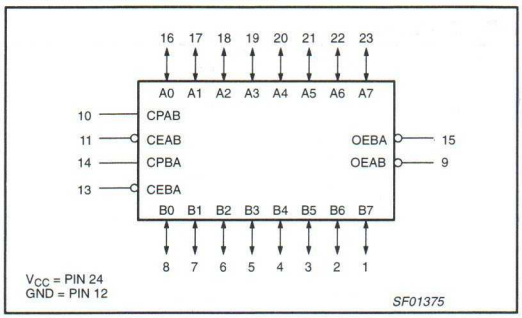
PLCC – 74F2952



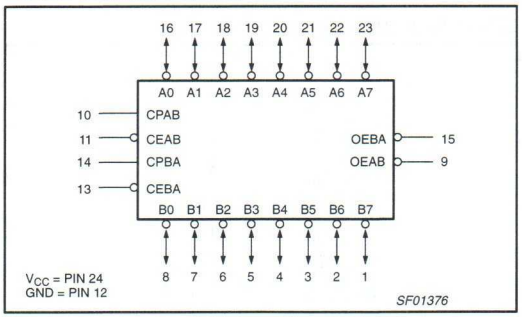
PLCC – 74F2953



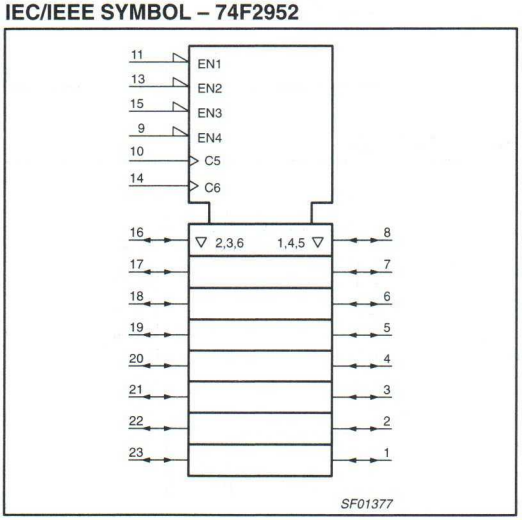
LOGIC SYMBOL – 74F2952



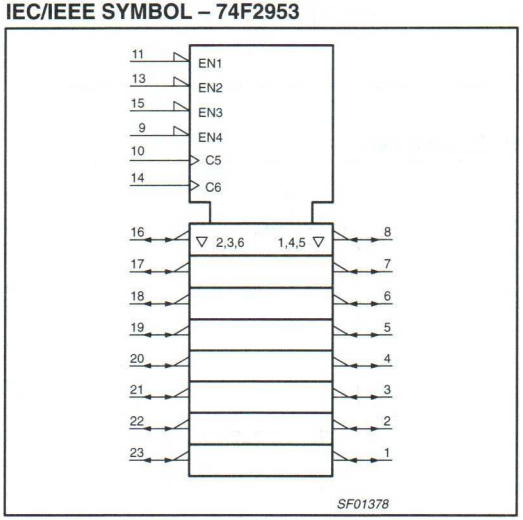
LOGIC SYMBOL – 74F2953



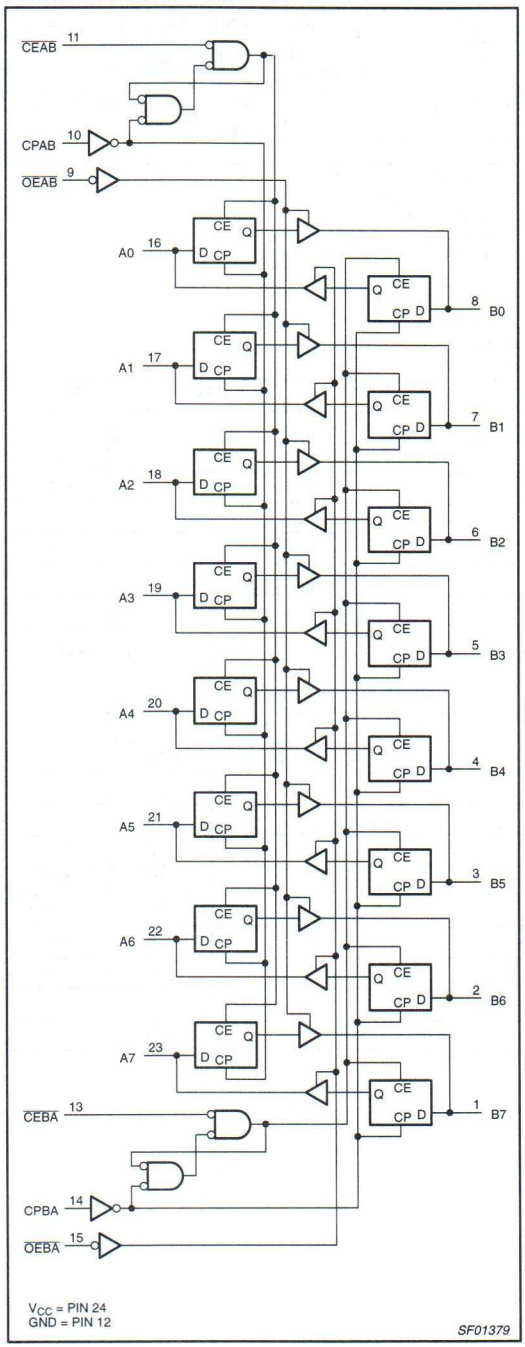
IEC/IEEE SYMBOL – 74F2952



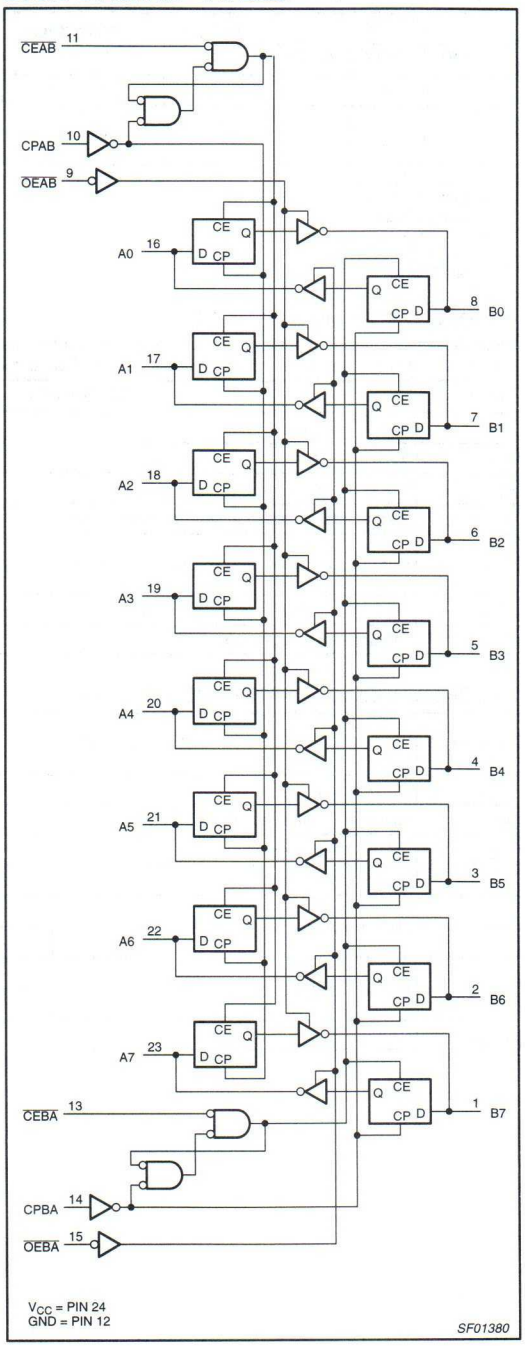
IEC/IEEE SYMBOL – 74F2953



LOGIC DIAGRAM – 74F2952



LOGIC DIAGRAM – 74F2953



FUNCTION TABLE for Register An or Bn

INPUTS			INTERNAL Q	OPERATING MODE
An or Bn	CPXX	$\overline{CEXX}$		
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	

H = High voltage level
L = Low voltage level
↑ = Low-to-High transition
X = Don't Care
XX = AB or BA
NC = No Change

FUNCTION TABLE for Output Enable

INPUTS	INTERNAL Q	An or Bn OUTPUTS		OPERATING MODE
$\overline{OEXX}$		74F2952	74F2953	
H	X	Z	Z	Disable outputs
L	L	L	H	Enable outputs
L	H	H	L	

H = High voltage level
L = Low voltage level
X = Don't Care
XX = AB or BA
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A0 – A7	48	mA
		B0 – B7	128	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A0 – A7			–3	mA
		B0 – B7			–15	mA
I_{OL}	Low-level output current	A0 – A7			24	mA
		B0 – B7			64	mA
T_{amb}	Operating free-air temperature range		0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	A0–A7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10% V_{CC}	2.4			V
					±5% V_{CC}	2.7	3.3		V
		B0–B7		I_{OH} = –15mA	±10% V_{CC}	2.0			V
					±5% V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A0–A7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10% V_{CC}		0.35	0.50	V
					±5% V_{CC}		0.35	0.50	V
		B0–B7		I_{OL} = 48mA	±10% V_{CC}		0.38	0.55	V
				I_{OL} = 64mA	±5% V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	CPAB, CPBA, $\overline{OEAB}$, $\overline{OEBA}$, $\overline{CEAB}$, $\overline{CEBA}$	V_{CC} = 5.5V, V_I = 7.0V					100	µA
		A0–A7, B0–B7	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	CPAB, CPBA, $\overline{OEAB}$, $\overline{OEBA}$, $\overline{CEAB}$, $\overline{CEBA}$	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	CPAB, CPBA, $\overline{OEAB}$, $\overline{OEBA}$, $\overline{CEAB}$, $\overline{CEBA}$	V_{CC} = MAX, V_I = 0.5V					–0.6	mA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied	A0–A7, B0–B7	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied	A0–A7, B0–B7	V_{CC} = MAX, V_O = 0.5V					–600	µA
I_{OS}	Short-circuit output current[3]	A0–A7	V_{CC} = MAX, V_O = 0V			–60		–150	mA
		B0–B7				–100		–225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				90	140	mA
		i_{CCL}					120	175	mA
		I_{CCZ}					105	155	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	145	160		135		MHz
t_{PLH} t_{PHL}	Propagation delay CPBA or CPAB to An or Bn	Waveform 1	3.0 3.5	5.0 6.0	7.5 8.5	2.5 3.5	8.0 9.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn	Waveform 3 Waveform 4	2.0 3.5	4.5 6.0	7.0 9.5	2.0 3.0	8.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn	Waveform 3 Waveform 4	2.0 1.5	4.0 3.5	8.0 6.5	1.5 1.0	9.0 7.0	ns

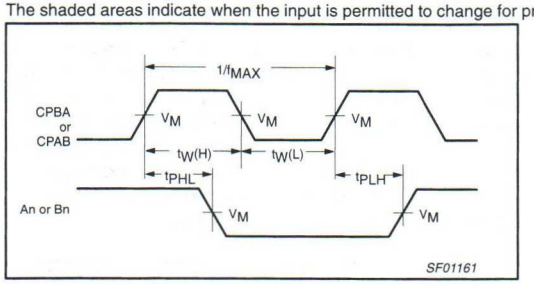
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = +5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5V ± 10%, C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low An or Bn to CPAB or CPBA	74F2952	Waveform 2	4.5 3.5			5.0 4.0		ns
t_s(H) t_s(L)	Setup time, High or Low An or Bn to CPAB or CPBA	74F2953	Waveform 2	4.0 3.5			4.0 4.0		ns
t_h(H) t_h(L)	Hold time, High or Low An or Bn to CPAB or CPBA		Waveform 2	0.0 0.0			0.0 0.0		ns
t_s(H) t_s(L)	Setup time, High or Low $\overline{CEAB}$, $\overline{CEBA}$ to CPAB, CPBA		Waveform 2	0.0 4.0			0.0 4.0		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{CEAB}$, $\overline{CEBA}$ to CPAB, CPBA		Waveform 2	2.5 2.5			2.5 3.0		ns
t_w(H) t_w(L)	CPAB or CPBA pulse width, High or Low		Waveform 1	3.0 3.5			3.0 3.5		ns

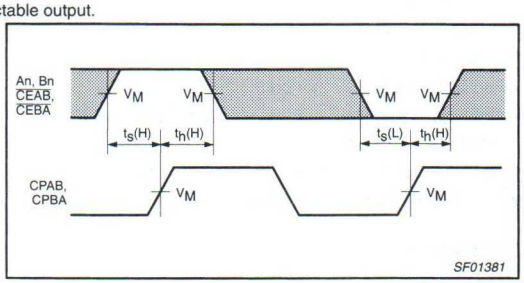
AC WAVEFORMS

For all waveforms, V_M = 1.5V.

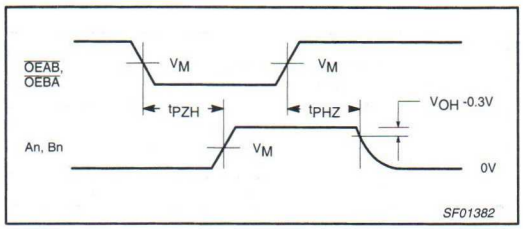
The shaded areas indicate when the input is permitted to change for predictable output.



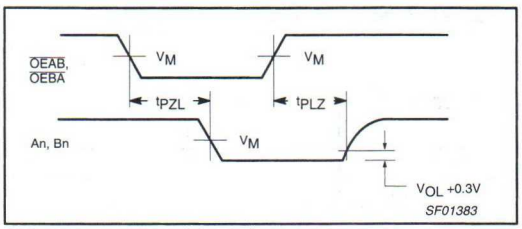
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup and Hold Times

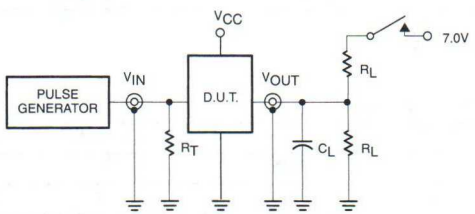


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

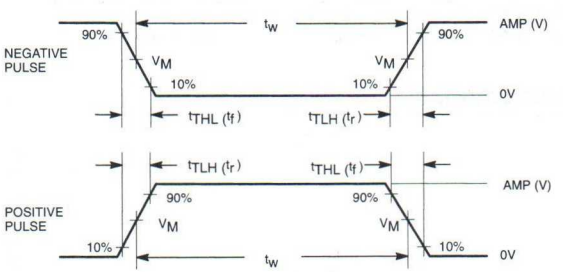


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

Quad 2-input NAND 30Ω driver | 74F3037

FEATURES

- 30Ω line driver
- 67mA output drive capability in the high state
- High speed
- Facilitates incident wave switching
- 3nh lead inductance each on V_{CC} and GND when both side pins are used
- 160mA output drive capability in the low state
- Industrial temperature range available (–40°C to +85°C)

DESCRIPTION

The 74F3037 is a high current line driver composed of four 2–input NAND gates. It has been designed to deal with the transmission line effects of PC boards which appear when fast edge rates are used.

The drive capability of the 74F3037 is 67mA source and 160mA sink with a V_{CC} as low as 4.5V. This guarantees incident wave switching with V_{OH} not less than 2.0V and V_{OL} not more than 0.8mA while driving impedances as low as 30 ohms. This is applicable with any combination of outputs using continuous duty. The propagation delay of the part is minimally affected by reflections when terminated only by the TTL inputs of other devices. Performances may be improved by full or partial line termination.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F3037	2.0ns	16mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
16–pin plastic DIP	N74F3037N	I74F3037N	SOT38-4
16–pin plastic SOL	N74F3037D	I74F3037D	SOT162-1

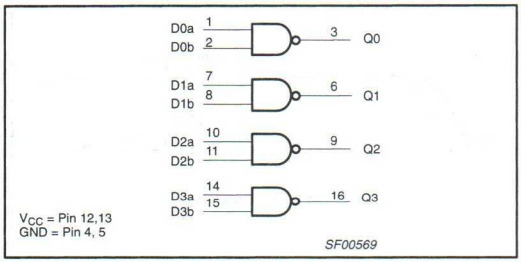
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Q}$n	Data output	3350/266	67mA/160mA

Note to input and output loading and fan out table

One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.

LOGIC DIAGRAM



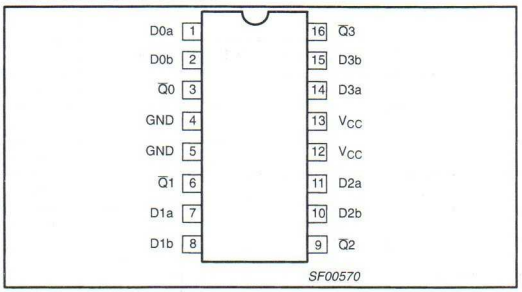
FUNCTION TABLE

INPUTS		OUTPUT
Dna	Dnb	$\overline{Q}$n
L	L	H
L	H	H
H	L	H
H	H	L

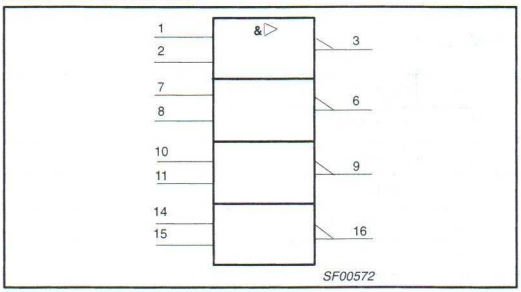
Notes to function table

H = High voltage level
L = Low voltage level

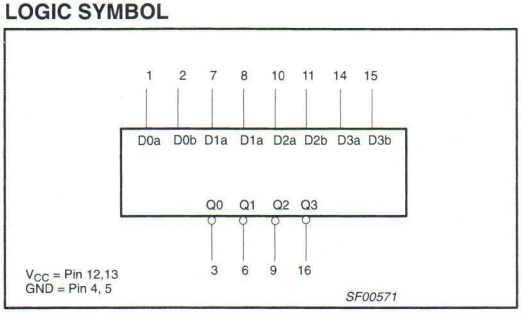
PIN CONFIGURATION



IEC/IEEE SYMBOL



LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		320	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	−40 to +85	°C
T_{stg}	Storage temperature range		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.4			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current				–67	mA
I_{OL}	Low–level output current				160	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High–level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –45mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7			V
				I_{OH1} = –67mA[3]	±10%V_{CC}	2.0			V
V_{OL}	Low–level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10%V_{CC}		0.30	0.50	V
				I_{OL1} = 160mA[4]	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_O	Output current[5]		V_{CC} = MAX, V_O = 2.25V			-100		-200	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				6.0	9.0	mA
		I_{CCL}					30	40	mA

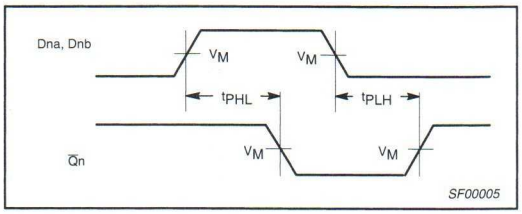
Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. I_{OH1} is the current necessary to guarantee the low to high transition in a 30 ohm transmission line on the incident wave.
4. I_{OL1} is the current necessary to guarantee the high to low transition in a 30 ohm transmission line on the incident wave.
5. I_O is tested under conditions that produce current approximately one half of the true short–circuit current (I_{OS}).

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		T_{amb} =–40°C to +85°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to $\overline{Qn}$	Waveform 1	1.0 1.0	2.0 2.0	5.0 4.5	1.0 1.0	5.5 5.0	1.0 1.0	5.5 5.0	ns

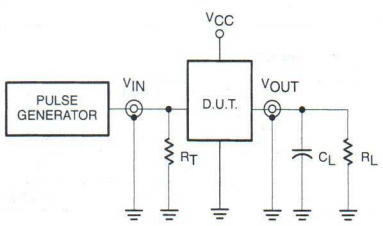
AC WAVEFORMS



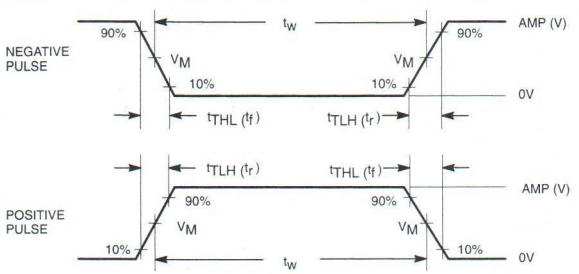
Waveform 1. Propagation delay for inverting outputs

Note to AC waveforms
For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor;
see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Quad 2-input NAND 30Ω line driver (open collector) 74F3038

FEATURES

- 30Ω line driver
- 160mA output drive capability
- High speed
- Facilitates incident wave switching
- 3nh lead inductance each on V_{CC} and GND when both side pins are used

DESCRIPTION

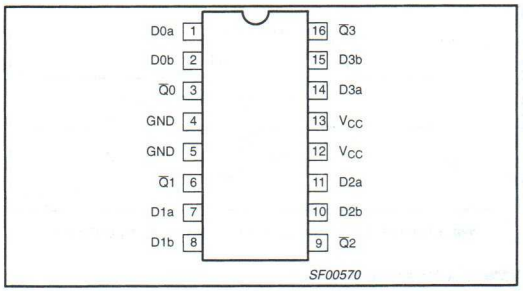
The 74F3038 is a high current Open-Collector Line Driver composed of four 2-input NAND gates. It has been designed to deal with the transmission line effects of PC boards which appear when fast edge rates are used.

The 74F3038 can sink 160mA with a V_{CC} as low as 4.5V. This guarantees incident wave switching with V_{OL} not more than 0.8V while driving impedances as low as 30Ω. This is applicable with any combination of outputs using continuous duty.

The AC specifications for the 74F3038 were determined using the standard FAST load for open-collector parts of 50pF capacitance, a 500Ω pull-up resistor and a 500Ω pull-down resistor. (See Test Circuit).

Reducing the load resistors to 100Ω will decrease the t_{PLH} propagation delay by approximately 50% while increasing t_{PHL} only slightly. The graph of typical propagation delay versus load resistor (see AC Characteristics section for Graph) shows a spline fit curve from four measured data points, R_L = 30Ω, R_L = 100Ω, R_L = 300Ω, and R_L = 500Ω.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F3038	6.0ns	17mA

ORDERING INFORMATION

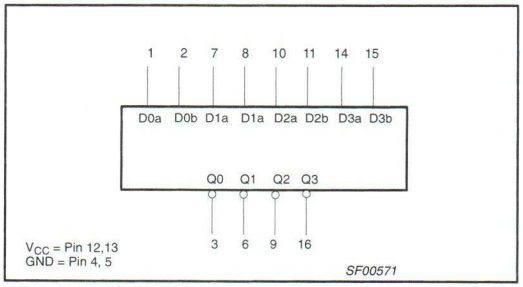
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PACKAGE DRAWING NUMBER
16-pin Plastic DIP	N74F3038N	SOT38-4
16-pin Plastic SOL	N74F3038D	SOT162-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

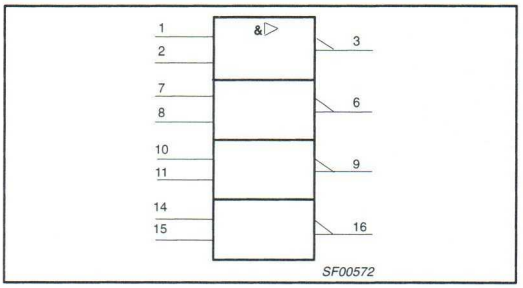
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb	Data inputs	1.0/1.0	20μA/0.6mA
Q̄n	Data outputs	OC/266	OC/160mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state. OC = Open Collector.

LOGIC SYMBOL

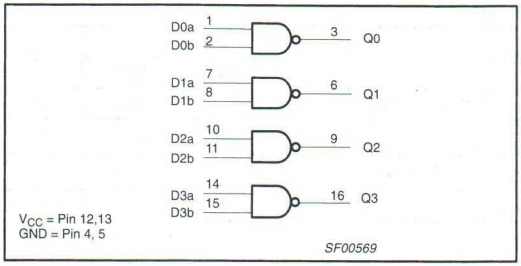


IEC/IEEE SYMBOL



Quad 2-input NAND 30Ω line driver (open collector) 74F3038

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUT
Dna	Dnb	$\overline{Q}n$
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	320	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
V_{OH}	High-level output voltage			4.5	V
I_{OL}	Low-level output current			160	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					MIN	TYP[2]	MAX	
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX					250	µA
V_{OL}	Low-level output current	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10% V_{CC}		0.42	0.55	V
			I_{OL} = 160mA[3]	±5% V_{CC}			0.80	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					–0.6	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		3.5	6.0	mA
		I_{CCL}		V_{IN} = 4.5V		30	40	mA

NOTES:

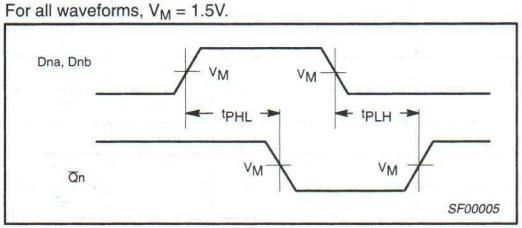
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. I_{OL1} is the current necessary to guarantee the High to Low transition in a 30Ω transmission line on the incident wave.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	Propagation delay	Waveform 1	6.0	8.5	11.5	6.0	12.0	ns
t_{PHL}	Dna, Dnb to $\overline{Q}$n		1.0	2.0	5.0	1.0	5.0	

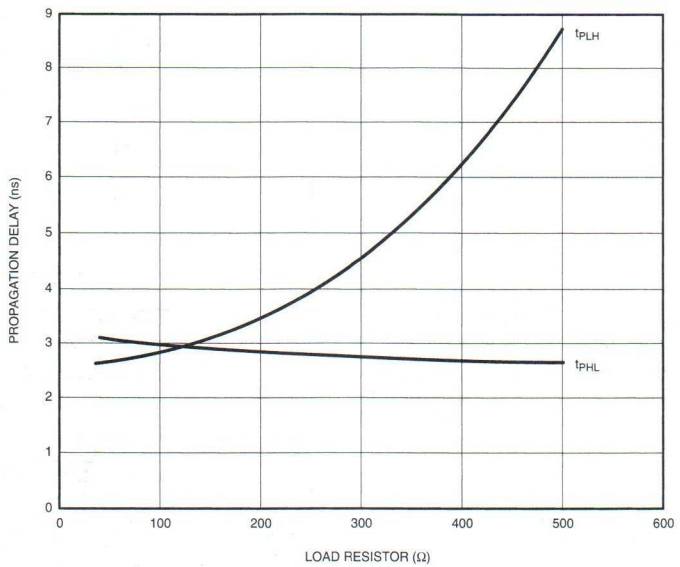
AC WAVEFORMS

For all waveforms, V_M = 1.5V.



Waveform 1. Propagation Delay for Inputs to Output

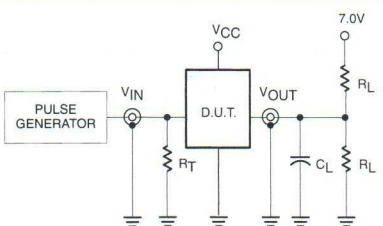
TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS



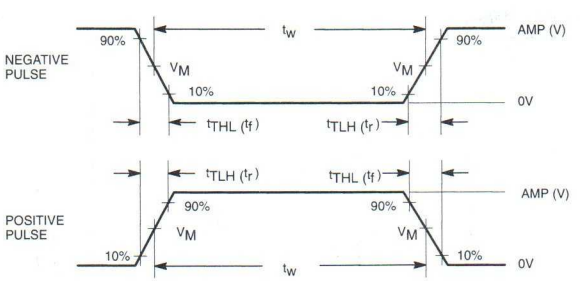
NOTE:
When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}s of the receivers does not exceed the I_{OL} maximum specification.

SF01361

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs



Input Pulse Definition

DEFINITIONS:

R_L = Load resistor;
see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00027

Dual 4-input NAND 30Ω line driver | 74F3040

FEATURES

- 30Ω line driver
- 160mA output drive capability in the Low state
- 67mA output drive capability in the High state
- High speed
- Facilitates incident wave switching
- 3nh lead inductance each on V_{CC} and GND when both side pins are used

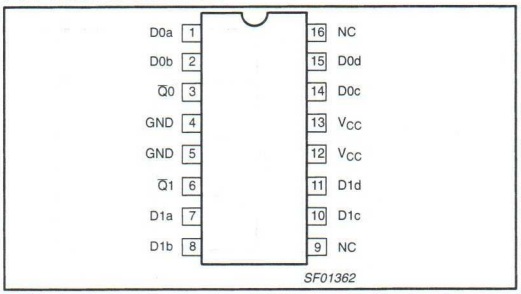
DESCRIPTION

The 74F3040 is a high current Line Driver composed of two 4-input NAND gates. It has been designed to deal with the transmission line effects of PC boards which appear when fast edge rates are used.

The drive capability of the 74F3040 is 67mA source and 160mA sink with a V_{CC} as low as 4.5V. This guarantees incident wave switching with V_{OH} not less than 2.0V and V_{OL} not more than 0.8V while driving impedances as low as 30Ω. This is applicable with any combination of outputs using continuous duty.

The propagation delay of the part is minimally affected by reflections when terminated only by the TTL inputs of other devices. Performance may be improved by full or partial line termination.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F3040	2.0ns	10mA

ORDERING INFORMATION

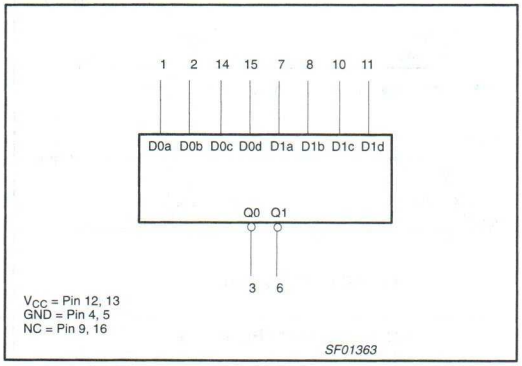
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PACKAGE DRAWING NUMBER
16-pin Plastic DIP	N74F3040N	SOT38-4
16-pin Plastic SOL	N74F3040D	SOT162-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

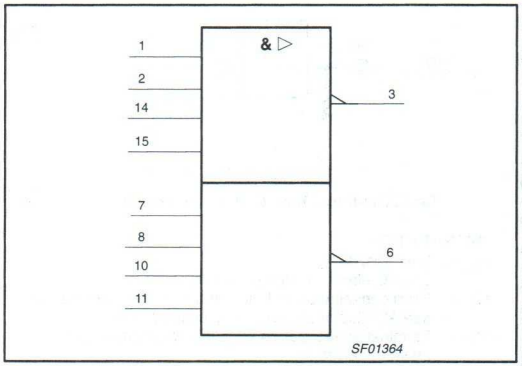
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb, Dnc, Dnd	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Q}$n	Data outputs	3350/266	67mA/160mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

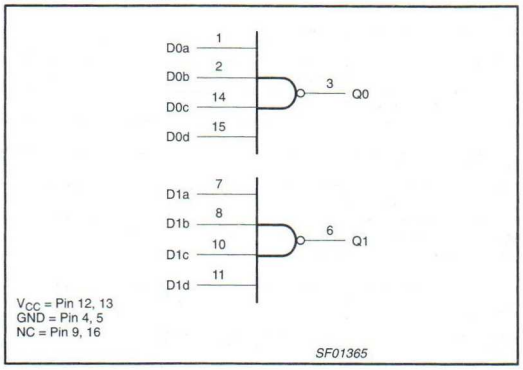
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUT
Dna	Dnb	Dnc	Dnd	$\overline{Q}n$
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	320	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−67	mA
I_{OL}	Low-level output current			160	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –45mA	±10% V_{CC}	2.5			V
				±5% V_{CC}	2.7	3.4		V
			I_{OH1} = –67mA[3]	±10% V_{CC}	2.0			V
V_{OL}	Low-level output current	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10% V_{CC}		0.30	0.50	V
			I_{OL1} = 160mA[4]	±5% V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					–0.6	mA
I_O	Output current[5]	V_{CC} = MAX, V_O = 2.25V			–100		–200	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			3.0	5.0	mA
		I_{CCL}				16	22	mA

NOTES:

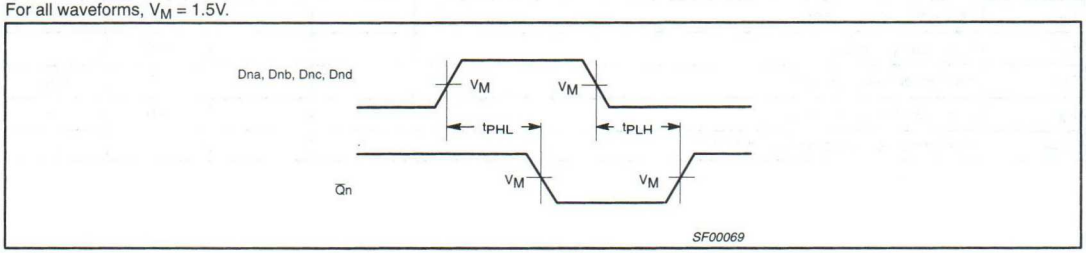
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. I_{OH1} is the current necessary to guarantee the Low-to-High transition in a 30Ω transmission line on the incident wave.
4. I_{OL1} is the current necessary to guarantee the High-to-Low transition in a 30Ω transmission line on the incident wave.
5. I_O is tested under conditions that produce current approximately one half of the true short-circuit output current (I_{OS}).

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb, Dnc, Dnd to $\overline{Q}$n	Waveform 1	1.0 1.0	2.0 2.0	5.0 4.5	1.0 1.0	5.5 5.0	ns

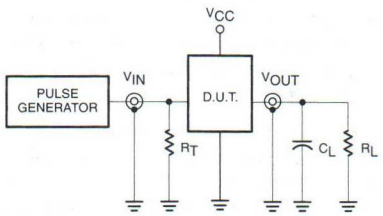
AC WAVEFORMS

For all waveforms, V_M = 1.5V.

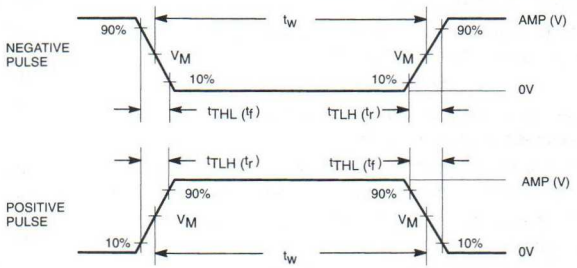


Waveform 1. Propagation Delay for Inputs to Output

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Quad Futurebus backplane transceiver | 74F3893

FEATURES

- Quad backplane transceiver
- Drives heavily loaded backplanes with equivalent load impedances down to 10 ohms
- Futurebus drivers sink 100mA
- Reduced voltage swing (1 volt) produces less noise and reduces power consumption
- High speed operation enhances performance of backplane buses and facilitates incident wave switching
- Compatible with IEEE 896 and IEEE 1194.1 Futurebus Standards
- Built–in precision band–gap (BG) reference provides accurate receiver thresholds and improved noise immunity
- Glitch–free power up/power down operation on all outputs
- Pin and function compatible with NSC DS3893

DESCRIPTION

The 74F3893 is a quad backplane transceivers and is intended to be used in very high speed bus systems.

The 74F3893 interfaces to 'Backplane Transceiver Logic' (BTL). BTL features a reduced (1V to 2V) voltage swing for lower power consumption and a series diode on the drivers to reduce capacitive loading (< 5pF).

Incident wave switching is employed, therefore BTL propagation delays are short. Although the voltage swing is much less for BTL, so is its receiver threshold region, therefore noise margins are excellent.

BTL offers low power consumption, low ground bounce, EMI and crosstalk, low capacitive loading, superior noise margin and low propagation delays. This results in a high bandwidth, reliable backplane.

The 74F3893 has four TTL outputs (Rn) on the receiver side with a common receiver enable input ($\overline{RE}$). It has four data inputs (Dn) which are also TTL. These data inputs are NANDed with the data enable input (DE). The four I/O pins (bus side) are futurebus compatible, sink a minimum of 100mA, and are designed to drive heavily loaded backplanes with load impedances as low as 10 ohms. All outputs are designed to be glitch–free during power up and down.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F3893	3.0ns	55mA

ORDERING INFORMATION

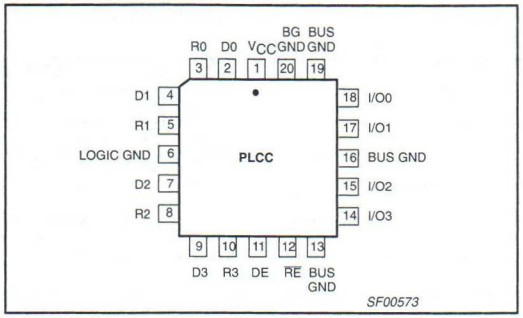
DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
20-pin PLCC	N74F3893A	SOT380-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D3	Data inputs	1.0/0.067	20µA/40µA
DE	Data enable input	1.0/0.33	20µA/200µA
$\overline{RE}$	Receiver enable input	1.0/0.067	20µA/40µA
I/O0 – I/O3	Bus inputs	5.0/0.033	100µA/20µA
I/O0 – I/O3	Bus outputs	OC/166.7	OC/100mA
R0 – R7	Receiver outputs	150/40	3mA/24mA

Notes to input and output loading and fan out table
One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.
OC= Open collector.

PIN CONFIGURATION



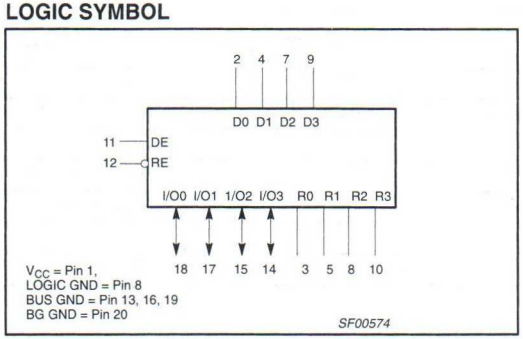
FUNCTION TABLE

INPUTS			INPUT/ OUT-PUT	OUT-PUT	OPERATING
$\overline{DE}$	$\overline{RE}$	Dn	I/On	Rn	MODE
H	L	L	H	L	Transmit to bus
H	L	H	L	H	
H	H	Dn	$\overline{Dn}$	Z	Receiver 3–state,
L	H	X	H	Z	transmit to bus
L	L	X	H	L	Receive, I/On = inputs
L	L	X	L	H	

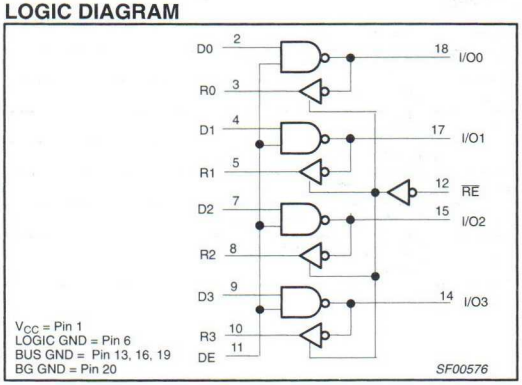
Notes to function table

1. H = High voltage level
2. L = Low voltage level
3. X = Don't care
4. Z = High impedance "off" state

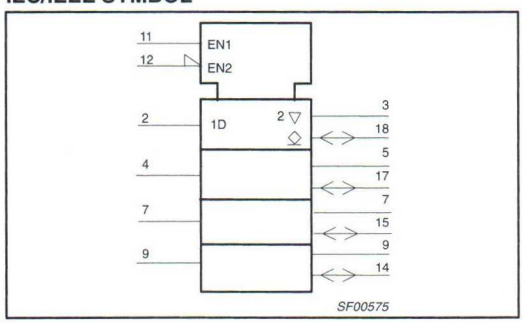
LOGIC SYMBOL



LOGIC DIAGRAM



IEC/IEEE SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−1.5 to +6.5	V
V_{IN}	Input voltage	−1.5 to +6.5	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	−0.5 to 5.5	V
I_{OUT}	Current applied to output in low output state	200	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage	Dn, DE, $\overline{RE}$	2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				−18	mA
V_{TH}	Bus input threshold	I/On only	1.475	1.55	1.625	mA
I_{OH}	High–level output current	Rn only			−3	mA
I_{OL}	Low–level output current				100	mA
T_{amb}	Operating free air temperature range		0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
I_{OH}	High–level output current	I/On	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 1.5V			10	100	µA
V_{OH}	High-level output voltage	Rn	V_{CC} = MAX, V_{IL} = 1.3V, $\overline{RE}$ = 0.8V, I_{OH} = MAX		2.5			V
V_{OHB}	High-level output bus voltage	I/On	V_{CC} = MAX, Dn = DE = 0.8V, V_T = 2.0V, R_T = 10Ω, $\overline{RE}$ = 2.0V		2.5			V
V_{OL}	Low-level output voltage	Rn	V_{CC} = MIN, V_{IN} = 1.8V, $\overline{RE}$ = 0.8V, I_{OL} = 6mA			0.35	0.5	V
V_{OLB}	Low-level output bus voltage	I/On	Dn = DE = V_{IH}, I_{OL} = 100mA		0.75	1.0	1.2	V
			Dn = DE = V_{IH}, I_{OL} = 80mA		0.75	1.0	1.1	V
V_{OCB}	Driver output positive clamp voltage	I/On	V_{CC} = MAX or 0V,	I/On = 1mA	1.9		2.9	V
			Dn = DE = 0.8V, $\overline{RE}$ = 2.0V	I/On = 10mA	2.3		3.2	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V, DE = $\overline{RE}$ = Dn = V_{CC}				100	µA
I_{IH}	High–level input current	Dn, $\overline{RE}$, DE	V_{CC} = MAX, DE = $\overline{RE}$ = Dn =5.5V				20	µA
I_{IHB}	High–level I/O bus current (power off)	I/On	V_{CC} = 0V, Dn = DE = 0.8V, I/On =1.2V, $\overline{RE}$ = 0V				100	µA
I_{IL}	Low–level input current	Dn, $\overline{RE}$	V_{CC} = MAX, V_I = 0.5V, DE = 4.5V				–40	µA
		DE	V_{CC} = MAX, V_I = 0.5V, Dn = 4.5V				–200	µA
I_{ILB}	Low–level I/O bus current (power on)	I/On	V_{CC} = MAX, Dn = DE = 0.8V, I/On =0.75V, $\overline{RE}$ = 0V		–20		20	µA
I_{OZH}	Off–state output current, high–level voltage applied	Rn	V_{CC} = MAX, V_I = 2.7V, $\overline{RE}$ = 2V				20	µA
I_{OZL}	Off–state output current, low–level voltage applied		V_{CC} = MAX, V_I = 0.5V, $\overline{RE}$ = 2V				–20	µA
I_{OS}	Short circuit output current[3]	Rn	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX, ($\overline{RE}$ = V_{IH} or V_{IL})			55	80	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS FOR DRIVER AND DRIVER ENABLE

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_D = 50pF, R_T = 10Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_D= 50pF, R_T = 10Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to I/On	Waveform 1	1.0 1.5	2.0 3.0	5.0 5.5	1.0 1.5	5.5 6.0	ns
t_{PLH} t_{PHL}	Propagation delay DE to I/On	Waveform 1	1.0 1.5	2.0 3.0	4.5 5.5	1.0 1.5	5.5 6.0	ns
t_{TLH} t_{THL}	Dn to I/O transition time 10% to 90%, 90% to 10%	Waveform 1	1.0 1.0		4.0 4.0	1.0 1.0	5.0 5.0	ns
$t_{sk(o)}$	Skew between drivers in same package			1.0				ns

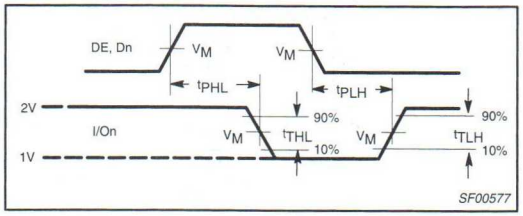
AC ELECTRICAL CHARACTERISTICS FOR RECEIVER

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 1kΩ			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 1kΩ		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay I/On to Rn	Waveform 2	1.0 3.6	2.0 5.5	4.5 7.5	1.0 3.6	5.5 8.5	ns

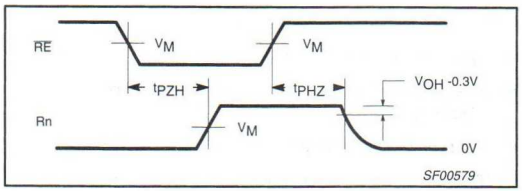
AC ELECTRICAL CHARACTERISTICS FOR RECEIVER ENABLE

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PZH} t_{PZL}	Output enable time to high or low level, $\overline{RE}$ to Rn	Waveform 3, 4	1.5 2.5	3.0 4.0	5.5 7.0	1.5 2.0	6.0 7.5	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level, $\overline{RE}$ to Rn	Waveform 3, 4	1.5 1.5	3.0 3.0	5.5 5.5	1.0 1.0	6.5 6.0	ns

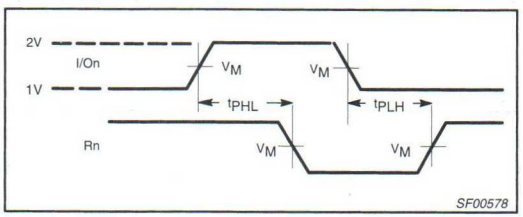
AC WAVEFORMS



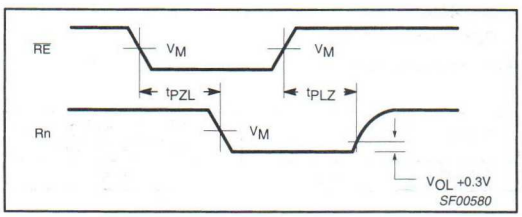
Waveform 1. Propagation delay for driver



Waveform 3. 3–state output enable time to high level and output disable time from high level



Waveform 2. Propagation delay for receiver



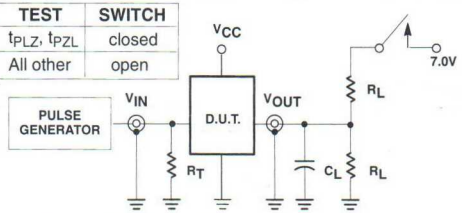
Waveform 4. 3-state output enable time to low level and output disable time from low level

Notes to AC waveforms
1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

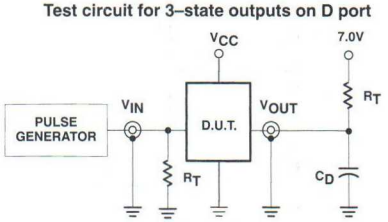
TEST CIRCUITS AND WAVEFORMS

SWITCH POSITION

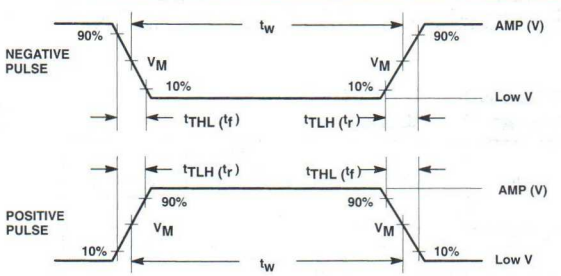
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test circuit for 3–state outputs on D port



Test circuit for outputs on I/O port



Input pulse definition

family	INPUT PULSE REQUIREMENTS						
	amplitude	Low V	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
D port	3.0V	0.0V	1.5V	1MHz	500ns	2.5ns	2.5ns
I/O port	2.0V	1.0V	1.5V	1MHz	500ns	4.0ns	4.0ns

DEFINITIONS:
R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_U = Pull up resistor; see AC Electrical Characteristics for value.
C_D = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SF00581

Synchronizing dual D-type flip-flop/clock driver | 74F5074

FEATURES

- Metastable immune characteristics
- Output skew guaranteed less than 1.5ns
- High source current (I_{OH} = 15mA) ideal for clock driver applications
- Pin out compatible with 74F74
- 74F50728 for synchronizing cascaded D–type flip–flop
- See 74F50729 for synchronizing dual D–type flip–flop with edge–triggered set and reset
- See 74F50109 for synchronizing dual J–$\overline{K}$ positive edge–triggered flip–flop
- Industrial temperature range available (–40°C to +85°C)

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F5074	120MHz	20mA

ORDERING INFORMATION

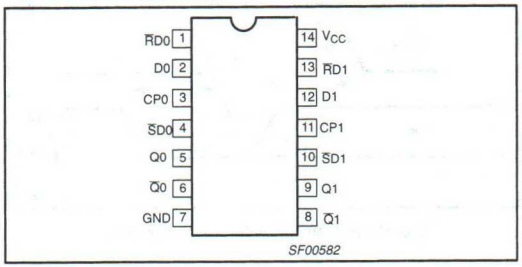
DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
14–pin plastic DIP	N74F5074N	SOT27-1
14–pin plastic SO	N74F5074D	SOT108-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

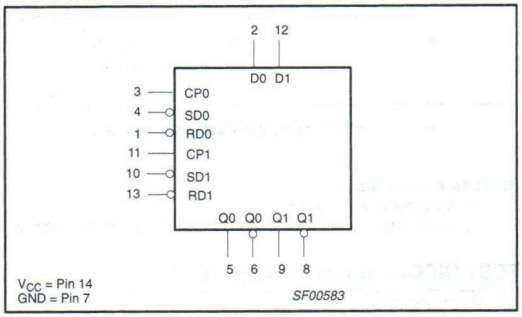
PINS	DESCRIPTION	74F (U.L.) HIGH/ LOW	LOAD VALUE HIGH/ LOW
D0, D1	Data inputs	1.0/0.417	20µA/250µA
CP0, CP1	Clock inputs (active rising edge)	1.0/1.0	20µA/20µA
$\overline{SD}$0, $\overline{SD}$1	Set inputs (active low)	1.0/1.0	20µA/20µA
$\overline{RD}$0, $\overline{RD}$1	Reset inputs (active low)	1.0/1.0	20µA/20µA
Q0, Q1, $\overline{Q}$0, $\overline{Q}$1	Data outputs	750/33	15mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

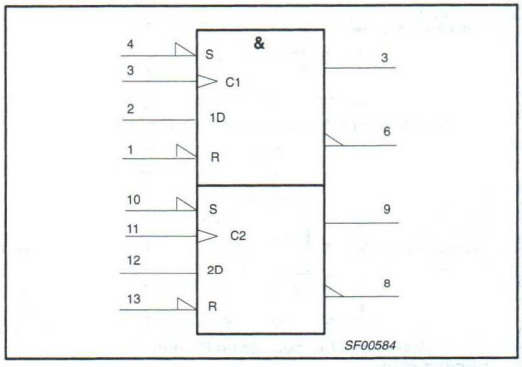
PIN CONFIGURATION



IEC/IEEE SYMBOL

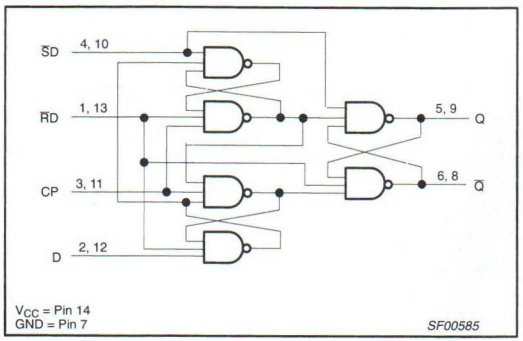


LOGIC SYMBOL



Synchronizing dual D-type flip-flop/clock driver 74F5074

LOGIC DIAGRAM



DESCRIPTION

The 74F5074 is a dual positive edge–triggered D–type featuring individual data, clock, set and reset inputs; also true and complementary outputs.

Set ($\overline{S}$Dn) and reset ($\overline{R}$Dn) are asynchronous active low inputs and operate independently of the clock (CPn) input. Data must be stable just one setup time prior to the low–to–high transition of the clock for guaranteed propagation delays.

Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive–going pulse. Following the hold time interval, data at the Dn input may be changed without affecting the levels of the output.

The 74F5074 is designed so that the outputs can never display a metastable state due to setup and hold time violations. If setup time and hold time are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74F5074 are: $\tau \cong 135$ps and $T_0 \cong 9.8 \times 10^6$ sec where τ represents a function of the rate at which a latch in a metastable state resolves that condition and T_0 represents a function of the measurement of the propensity of a latch to enter a metastable state.

Metastable Immune Characteristics

Philips Semiconductor uses the term 'metastable immune' to describe characteristics of some of the products in its family. Specifically the 74F50XXX family presently consist of 4 products which will not glitch or display an output anomaly under any circumstances including setup and hold time violations. This claim is easily verified on the 74F5074. By running two independent signal generators (see Fig. 1) at nearly the same frequency (in this case 10MHz clock and 10.02 MHz data) the device–under–test can be often be driven into a metastable state. If the Q output is then used to trigger a digital scope set to infinite persistence the $\overline{Q}$ output will build a waveform. An experiment was run by continuously operating the devices in the region where metastability will occur.

When the device–under–test is a 74F74 (which was not designed with metastable immune characteristics) the waveform will appear as in Fig. 2.

Figure 2 shows clearly that the $\overline{Q}$ output can vary in time with respect to the Q trigger point. This also implies that the Q or $\overline{Q}$ output waveshapes may be distorted. This can be verified on an analog scope with a charge plate CRT. Perhaps of even greater interest are the dots running along the 3.5V volt line in the upper right hand quadrant. These show that the $\overline{Q}$ output did not change state even though the Q output glitched to at least 1.5 volts, the trigger point of the scope.

When the device–under–test is a metastable immune part, such as the 74F5074, the waveform will appear as in Fig. 3. The 74F5074 $\overline{Q}$ output will appear as in Fig. 3. The 74F5074 Q output will not vary with respect to the Q trigger point even when the a part is driven into a metastable state. Any tendency towards internal metastability is resolved by Philips Semiconductor patented circuitry. If a metastable event occurs within the flop the only outward manifestation of the event will be an increased clock–to–Q/$\overline{Q}$ propagation delay. This propagation delay is, of course, a function of the metastability characteristics of the part defined by τ and T_0.

The metastability characteristics of the 74F5074 and related part types represent state–of–the–art TTL technology.

After determining the T_0 and t of the flop, calculating the mean time between failures (MTBF) is simple. Suppose a designer wants to use the 74F5074 for synchronizing asynchronous data that is arriving at 10MHz (as measured by a frequency counter), has a clock frequency of 50MHz, and has decided that he would like to sample the output of the 74F5074 10 nanoseconds after the clock edge. He simply plugs his number into the equation below:

$$MTBF = e^{(t'/t)} / T_0 f_C f_I$$

In this formula, f_C is the frequency of the clock, f_I is the average input event frequency, and t' is the time after the clock pulse that the output is sampled (t' < h, h being the normal propagation delay). In this situation the f_I will be twice the data frequency of 20 MHz because input events consist of both of low and high transitions. Multiplying f_I by f_C gives an answer of 10^{15} Hz^2. From Fig. 4 it is clear that the MTBF is greater than 10^{10} seconds. Using the above formula the actual MTBF is 1.51×10^{10} seconds or about 480 years.

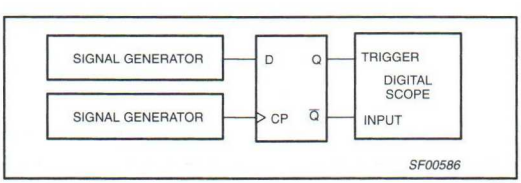


Figure 1. Test Set-up

COMPARISON OF METASTABLE IMMUNE AND NON–IMMUNE CHARACTERISTICS

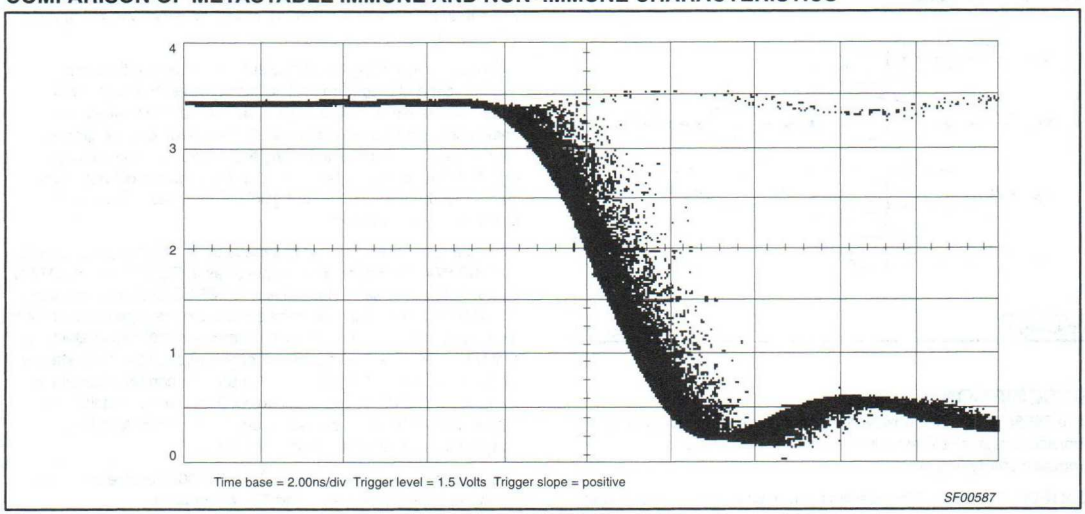


Figure 2. 74F74 $\overline{Q}$ Output triggered by Q output, set-up and hold times violated

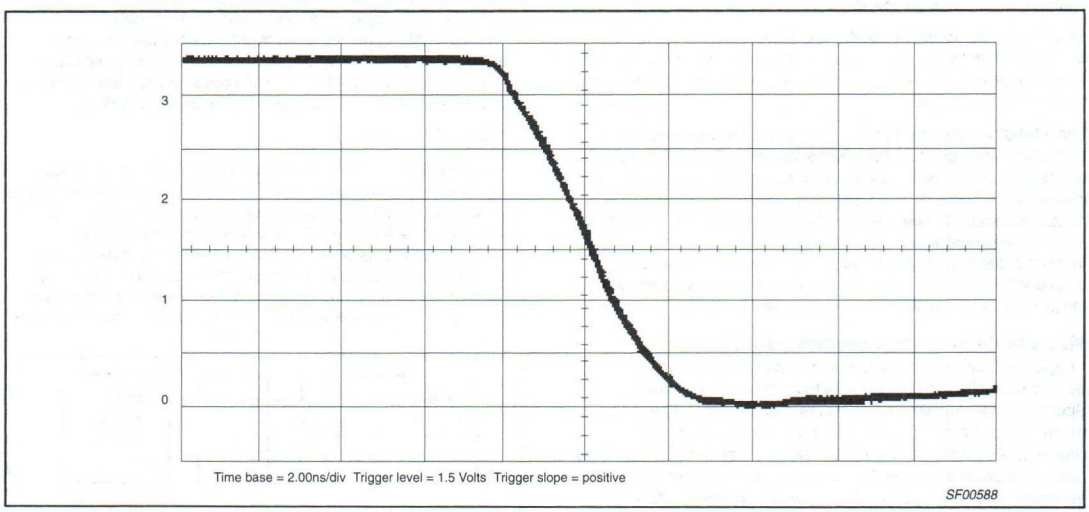
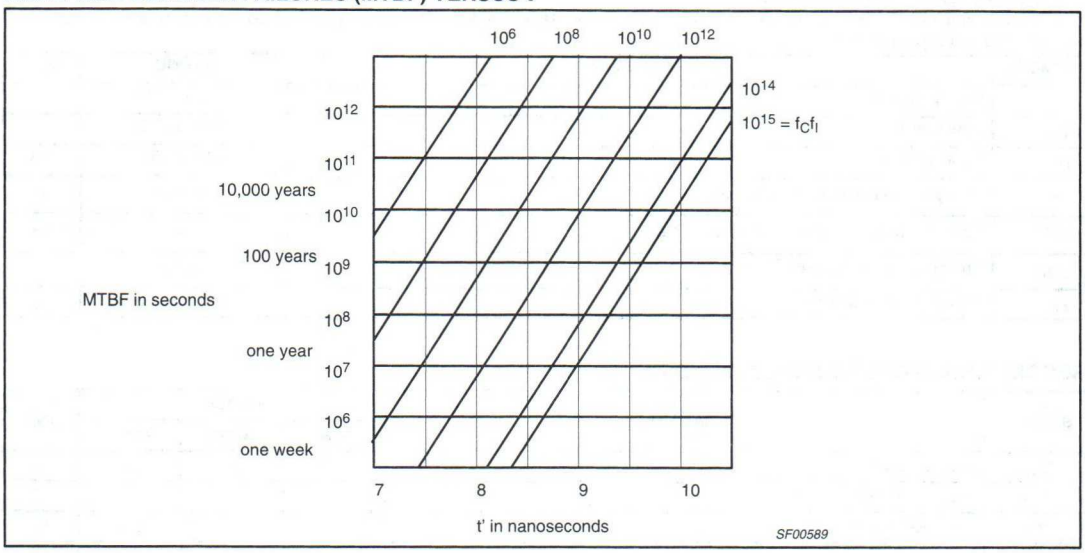


Figure 3. 74F74 $\overline{Q}$ Output triggered by Q output, set-up and hold times violated

MEAN TIME BETWEEN FAILURES (MTBF) VERSUS t'



NOTE: V_{CC} = 5V, T_{amb} = 25°C, τ =135ps, To = 9.8 X 10^6 sec

Figure 4.

TYPICAL VALUES FOR τ AND T_0 AT VARIOUS V_{CC}S AND TEMPERATURES

	T_{amb} = 0°C		T_{amb} = 25°C		T_{amb} = 70°C	
V_{CC}	τ	T_0	τ	T_0	τ	T_0
5.5V	125ps	1.0 X 10^9 sec	138ps	5.4 X 10^6 sec	160ps	1.7 X 10^5 sec
5.0V	115ps	1.3 X 10^{10} sec	135ps	9.8 X 10^6 sec	167ps	3.9 X 10^4 sec
4.5V	115ps	3.4 X 10^{13} sec	132ps	5.1 X 10^8 sec	175ps	7.3 X 10^4 sec

FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$	
L	H	X	X	H	L	Asynchronous set
H	L	X	X	L	H	Asynchronous reset
L	L	X	X	H	H	Undetermined*
H	H	↑	h	H	L	Load "1"
H	H	↑	l	L	H	Load "0"
H	H	↕	X	NC	NC	Hold

NOTES:
H = High voltage level
h = High voltage level one setup time prior to low–to–high clock transition
L = Low voltage level
l = Low voltage level one setup time prior to low–to–high clock transition
NC= No change from the previous setup
X = Don't care
↑ = Low–to–high clock transition
↕ = Not low–to–high clock transition
* = This setup is unstable and will change when either set or reset return to the high level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	40	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				−18	mA
I_{OH}	High–level output current	V_{CC} ± 10%			−12	mA
		V_{CC} ± 5%			−15	mA
I_{OL}	Low–level output current				20	mA
T_{amb}	Operating free air temperature range		0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High–level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OH} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN		±5%V_{CC}	2.7	3.4		V
V_{OL}	Low–level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN		±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current	Dn	V_{CC} = MAX, V_I = 0.5V					-250	µA
		CPn, $\overline{SD}$n, $\overline{RD}$n	V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX				20	30	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs high in turn.

AC ELECTRICAL CHARACTERISTICS

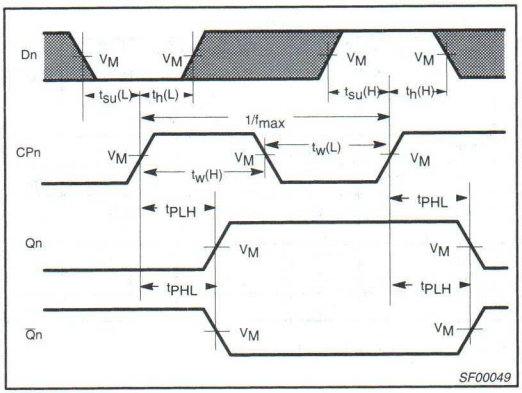
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	105	120		90		ns
t_{PLH} t_{PHL}	Propagation delay CPn to Qn or $\overline{Q}$n	Waveform 1	2.0 2.0	3.9 3.9	6.0 6.0	1.5 2.0	6.5 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}$Dn, $\overline{R}$Dn to Qn or $\overline{Q}$n	Waveform 2	3.0 3.0	4.5 5.0	7.5 7.5	2.5 2.5	8.0 8.0	ns
$t_{sk(o)}$	Output skew[1,2]	Waveform 4			1.5		1.5	ns

NOTES:
1. lt_{PN} actual – t_{PM} actuall for any output compared to any other output where N and M are either LH or HL.
2. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

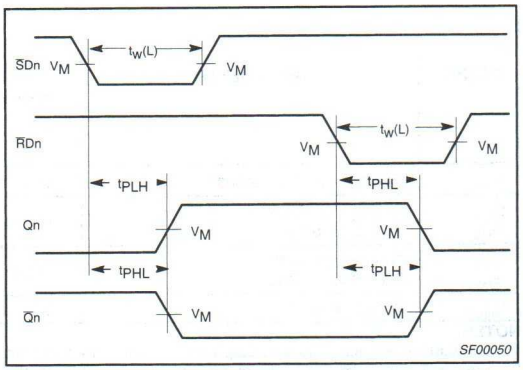
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su}(L)	Setup time, high or low Dn to CPn	Waveform 1	1.5 1.5			2.0 2.0		ns
t_h (H) t_h (L)	Hold time, high or low Dn to CPn	Waveform 1	1.0 1.0			1.5 1.5		ns
t_w (H) t_w (L)	CPn pulse width, high or low	Waveform 1	3.0 4.0			3.0 4.5		ns
t_w (L)	$\overline{S}$Dn or $\overline{R}$Dn pulse width, low	Waveform 2	3.0			4.0		ns
t_{rec}	Recovery time $\overline{S}$Dn or $\overline{R}$Dn to CPn	Waveform 3	3.0			3.5		ns

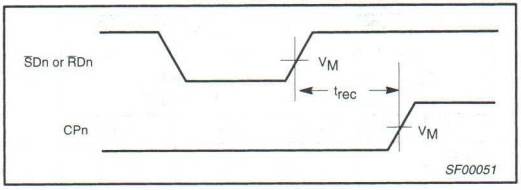
AC WAVEFORMS



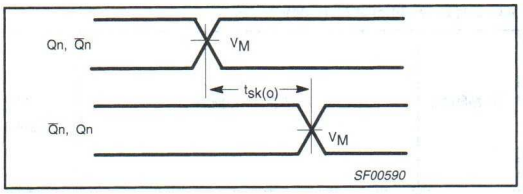
Waveform 1. Propagation delay for data to output, data setup time and hold times, and clock width, and maximum clock frequency



Waveform 2. Propagation delay for set and reset to output, set and reset pulse width



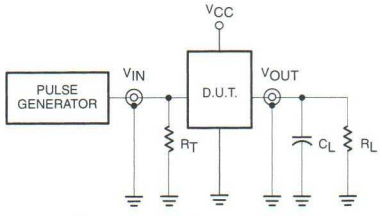
Waveform 3. Recovery time for set or reset to output



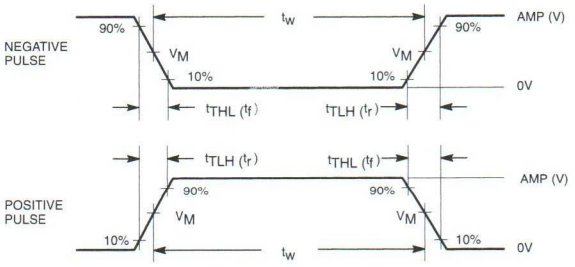
Waveform 4. Output skew

NOTES:
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:
R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Fiber optic LED driver

74F5300

FEATURES

- TTL inputs
- Output enable control
- High current source and sink capability
- Matched propagation delay times (t_{PLH}, t_{PHL})
- Symmetrical rise and fall times
- ESD protection greater than 2000 volts
- Single +5V supply
- Surface mount package

APPLICATIONS

- High speed serial data communication
- Fiber optic data links
- Local area and metropolitan area networks
- Digital Television
- PBX systems

ASSOCIATED PRODUCTS

- NE5210/11/12 transimpedance amplifiers
- NE5214/5217 postamplifiers with link status indicator
- 74F5300 fiber optic LED driver

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F5300	2.5ns	8mA

ORDERING INFORMATION

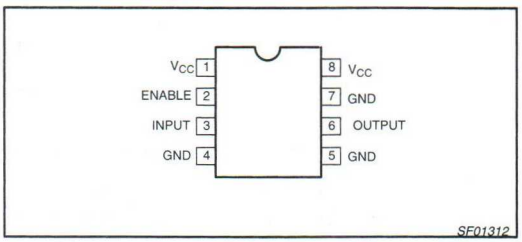
DESCRIPTION	ORDER CODE	DWG. PKG. #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
8–pin plastic DIP	N74F5300N	SOT97-1
8–pin plastic SO	N74F5300D	SOT96-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

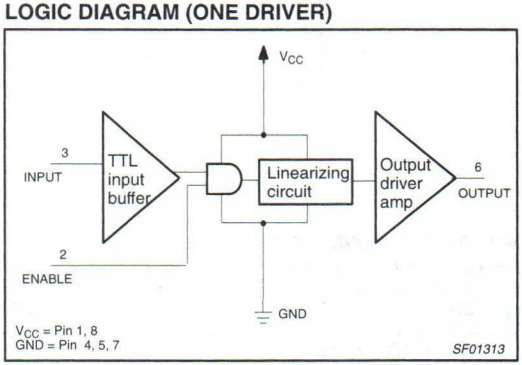
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Input	Data input	1.0/1.0	20µA/0.6mA
Enable	Enable input	1.0/1.0	20µA/0.6mA
Output	Current driver output	8000/266.6	160mA/160m

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

PIN CONFIGURATION



LOGIC DIAGRAM (ONE DRIVER)



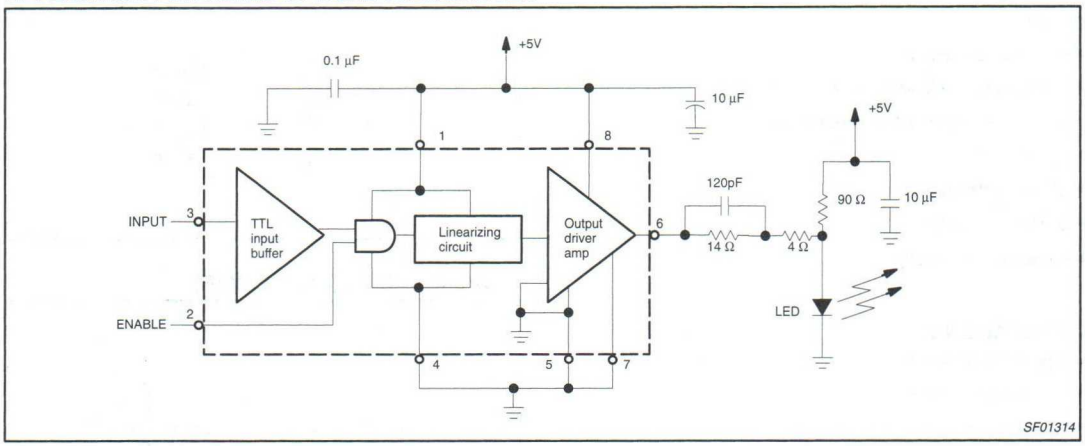
DESCRIPTION

The 74F5300 is a LED driver designed for use in fiber optic links. The 74F5300 is ideally suited for use in high speed optical high transmitter systems.

The TTL input buffer accepts TTL data. A logic high on the enable pin enables the buffer to drive the output driver amplifier. The linearizing circuits ensures a constant propagation delay for t_{PLH} and t_{PHL}, and controls the rise and fall times. The output driver amplifier is capable of sourcing more than 160mA and sinking more than 160mA at low impedances. The high current output driver has been designed to deal with transmission line effects of high speed switching systems with fast rising and falling edges. The performance of the system can be enhanced by matching impedance at the output for proper termination. It exhibits closely matched propagation delays (t_{PLH} and t_{PHL}) and symmetrical rise and fall times. The resulting optical waveform has minimal duty cycle distortion (DCD). When used with the external pre–bias and pre–charging circuits, the response can be tailored to a specific LED to eliminate any overshoot and to minimize the long fall response.

Additionally, this part can be used as the transmitter in a complete fiber optic system when combined with any of the NE5210/5211/5212 preamplifiers and NE5214/5217 postamplifiers for the optical receiver. Please refer to applications note AN1121 in the Philips Semiconductors Fiber Optic Communication Data Book for more specific applications information.

APPLICATION FOR 50Mb/s OPTICAL TRANSMITTER



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	240	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–160	mA
I_{OL}	Low–level output current			160	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –80mA	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.8	3.3	3.9	V
				V_{CC} = 5V	3.0	3.3	3.6	V
			I_{OH} = –160mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10%V_{CC}		0.42	0.55	V
			I_{OL} = 120mA	±10%V_{CC}		0.45	0.60	V
			I_{OL} = 160mA	±10%V_{CC}		0.55	0.80	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			4.0	12	mA
		I_{CCL}	V_{CC} = MAX			10.5	22	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The device is not short circuit protected.

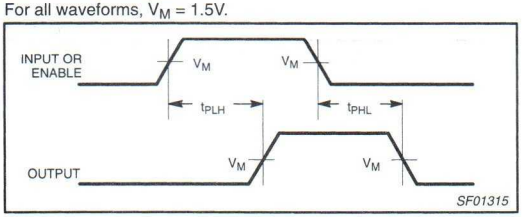
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 100Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 100Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Input or Enable to Output	Waveform 1	1.0 1.0	2.5 2.5	5.0 5.0	1.0 1.0	5.0 5.0	ns
D_{tpw}	Pulse width distortion[1]	Frequency = 10MHz		0.8	1.2		1.8	ns
t_{PS}	Propagation delay skew[2, 4]	Waveform 2		0.7	1.2		1.3	ns
t_{RFS}	Rise and fall time skew[3, 4]			0.6	1.5		1.5	ns
t_{THL} t_{TLH}	Fall time 90% to 10% Rise time 10% to 90%	Test circuits and Waveforms	0.5 1.0	1.4 2.0	3.5 4.0	0.5 1.0	4.0 4.5	ns

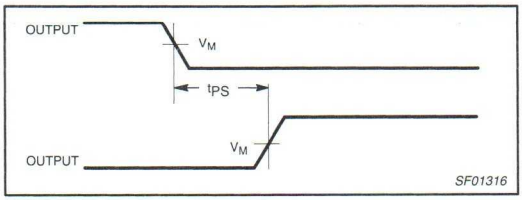
NOTES:
1. D_{tpw} is defined as the difference between input pulse width and output pulse width (0 to 3 volt swing and 50% duty cycle).
2. $| t_{PLH}$ actual – t_{PHL} actual$|$.
3. $| t_{TLH}$ actual – t_{THL} actual$|$.
4. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

AC WAVEFORMS

For all waveforms, V_M = 1.5V.

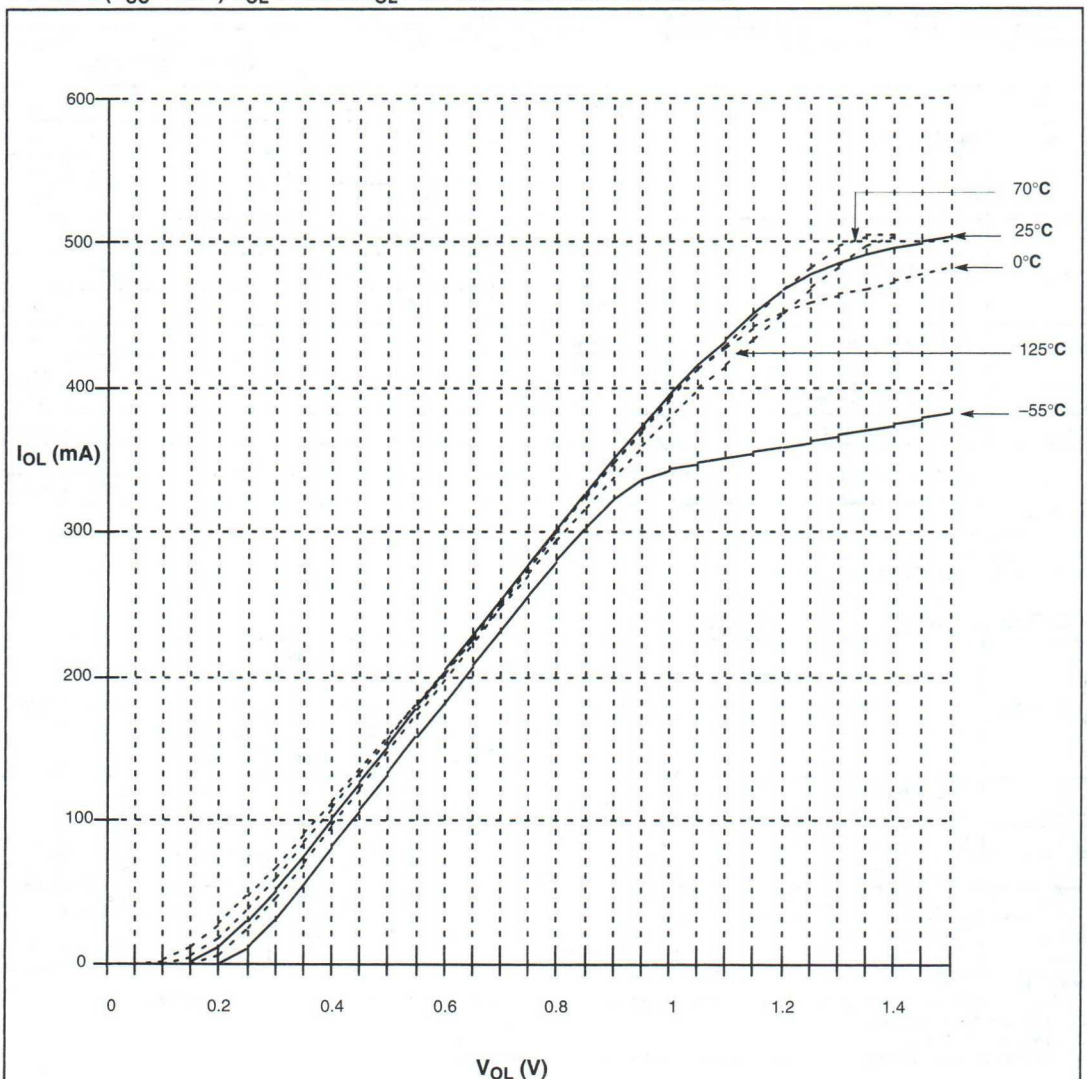


Waveform 1. Propagation delay for input to output

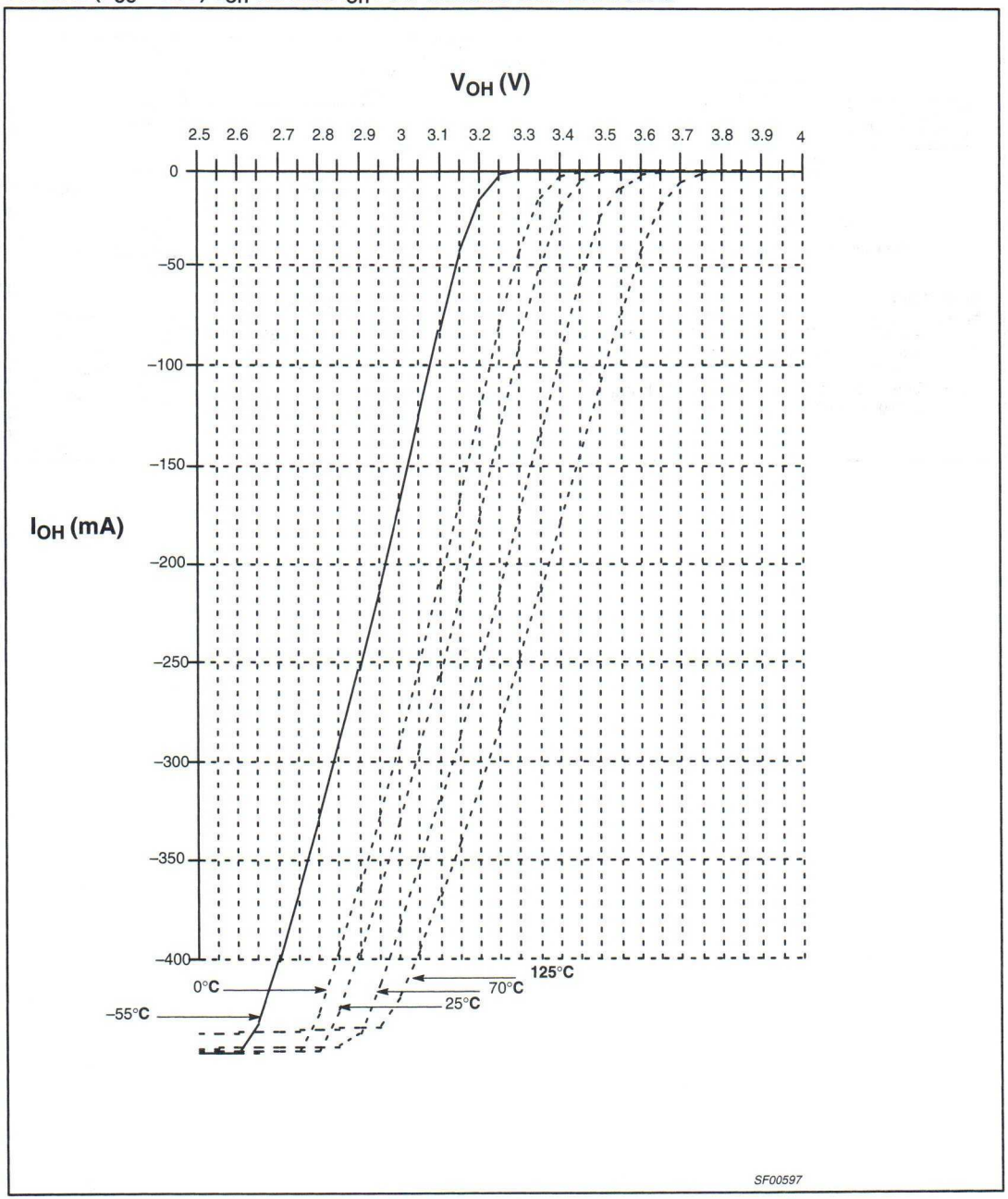


Waveform 2. Propagation delay skew

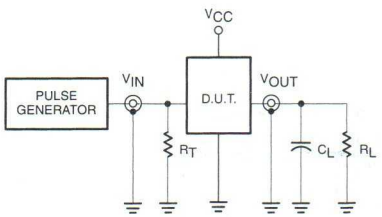
TYPICAL (V_{CC} = 5.0V) V_{OL} VERSUS I_{OL} FOR VARIOUS TEMPERATURES



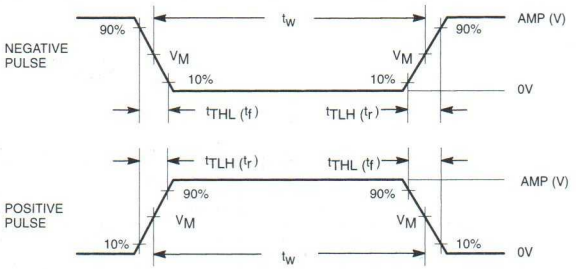
TYPICAL (V_{CC} = 5.0V) V_{OH} VERSUS I_{OH} FOR VARIOUS TEMPERATURES



TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor;
see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS				
	amplitude	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

SF01317

Fiber optic dual LED/clock driver 74F5302

FEATURES

- TTL inputs
- Output enable control
- High current source and sink capability
- Matched propagation delay times (t_{PLH}, t_{PHL})
- Symmetrical rise and fall times
- ESD protection greater than 2000 volts
- Single +5V supply
- Surface mount package

APPLICATIONS

- High speed serial data communication
- Fiber optic data links
- Local area and metropolitan area networks
- Digital Television
- PBX systems

ASSOCIATED PRODUCTS

- NE5210/11/12 transimpedance amplifiers
- NE5214/5217 postamplifiers with link status indicator
- 74F5300 fiber optic LED driver

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F5302	2.5ns	8mA

ORDERING INFORMATION

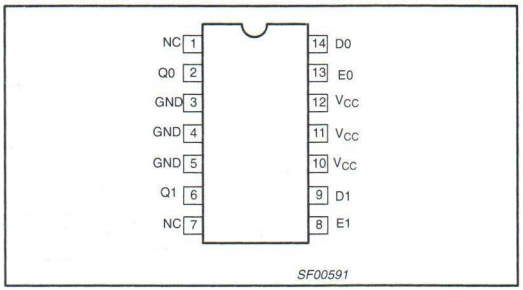
DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
14–pin plastic DIP	N74F5302N	SOT27-1
14–pin plastic SO	N74F5302D	SOT108-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

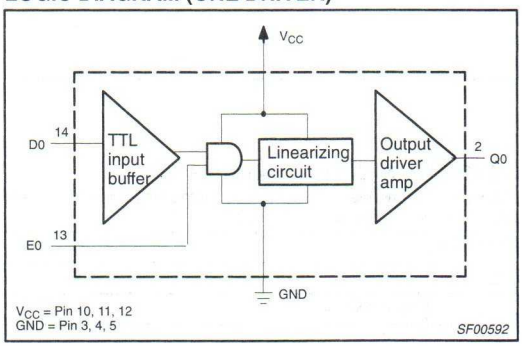
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dn	Data inputs	1.0/1.0	20µA/0.6mA
En	Enable inputs	1.0/1.0	20µA/0.6mA
Qn	Current driver output	8000/266.6	160mA/160mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

PIN CONFIGURATION



LOGIC DIAGRAM (ONE DRIVER)



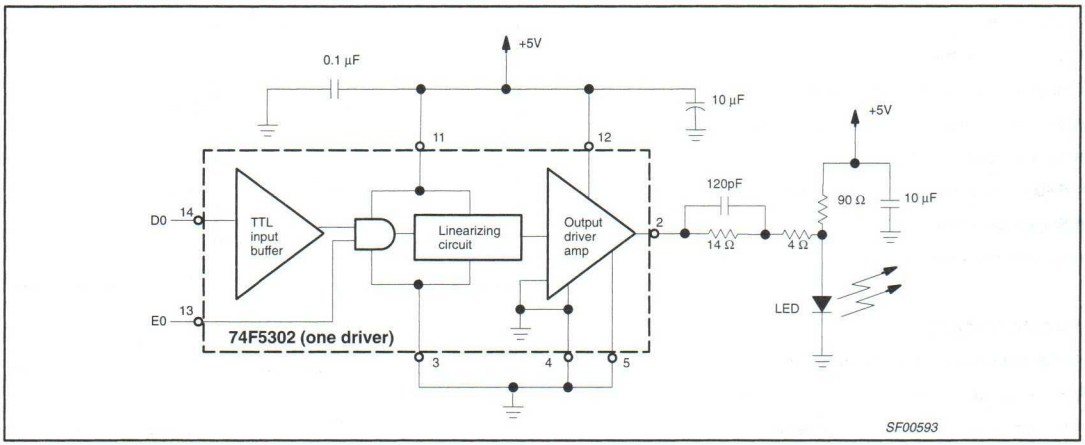
DESCRIPTION

The 74F5302 is a dual LED/clock driver designed for use in fiber optic links. The 74F5302 is ideally suited for use in high speed optical high transmitter systems. It is also ideal for use as a clock driver.

The TTL input buffer accepts TTL data. The linearizing circuits ensures a constant propagation delay for t_{PLH} and t_{PHL}, and controls the rise and fall times. The output driver amplifier is capable of sourcing more than 160mA and sinking more than 160mA at low impedances. The high current output driver has been designed to deal with transmission line effects of high speed switching systems with fast rising and falling edges. The performance of the system can be enhanced by matching impedance at the output for proper termination. It exhibits closely matched propagation delays (t_{PLH} and t_{PHL}) and symmetrical rise and fall times. The resulting optical waveform has minimal duty cycle distortion (DCD). When used with the external pre–bias and pre–charging circuits, the response can be tailored to a specific LED to eliminate any overshoot and to minimize the long fall response.

Additionally, this part can be used as the transmitter in a complete fiber optic system when combined with any of the NE5210/5211/5212 preamplifiers and NE5214/5217 postamplifiers for the optical receiver. Please refer to applications note AN1121 in the Philips Semiconductors Fiber Optic Communication Data Book for more specific applications information.

APPLICATION FOR 50Mb/s OPTICAL TRANSMITTER



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	240	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–160	mA
I_{OL}	Low–level output current			160	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –80mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.8	3.3	3.9	V
					V_{CC} = 5V	3.0	3.3	3.6	V
				I_{OH} = –160mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10%V_{CC}		0.42	0.55	V
				I_{OL} = 120mA	±10%V_{CC}		0.45	0.60	V
				I_{OL} = 160mA	±10%V_{CC}		0.55	0.80	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				5.0	12	mA
		I_{CCL}	V_{CC} = MAX				18	25	mA

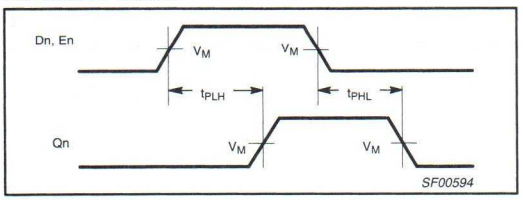
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The device is not short circuit protected.

AC ELECTRICAL CHARACTERISTICS

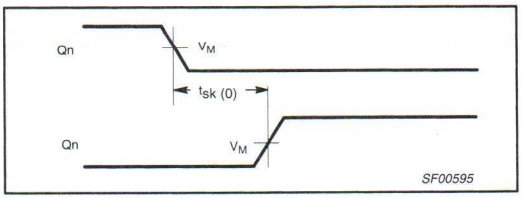
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 100Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 100Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn, En, to Qn	Waveform 1	1.0 1.0	2.0 2.5	4.5 5.0	1.0 1.0	4.5 5.0	ns
D_{tpw}	Pulse width distortion[1]	Frequency = 10MHz		0.8	1.2		1.8	ns
t_{RFS}	Rise and fall time skew[3, 4]			0.3	1.5		2.0	ns
$t_{sk\ (0)}$	Output skew[2, 4]	Waveform 2		0.9	1.3		1.6	ns
t_{THL} t_{TLH}	Fall time 90% to 10% Rise time 10% to 90%	Test circuits and Waveforms	1.0 1.0	1.5 1.8	3.0 3.0	0.5 0.5	4.0 4.5	ns

NOTES:
1. D_{tpw} is defined as the difference between input pulse width and output pulse width (0 to 3 volt swing and 50% duty cycle).
2. $|\ t_{PN}$ actual – t_{PM} actuall for any output compared to any other output where N and M are either LH or HL.
3. $|\ t_{TLH}$ actual – t_{THL} actuall.
4. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

AC WAVEFORMS



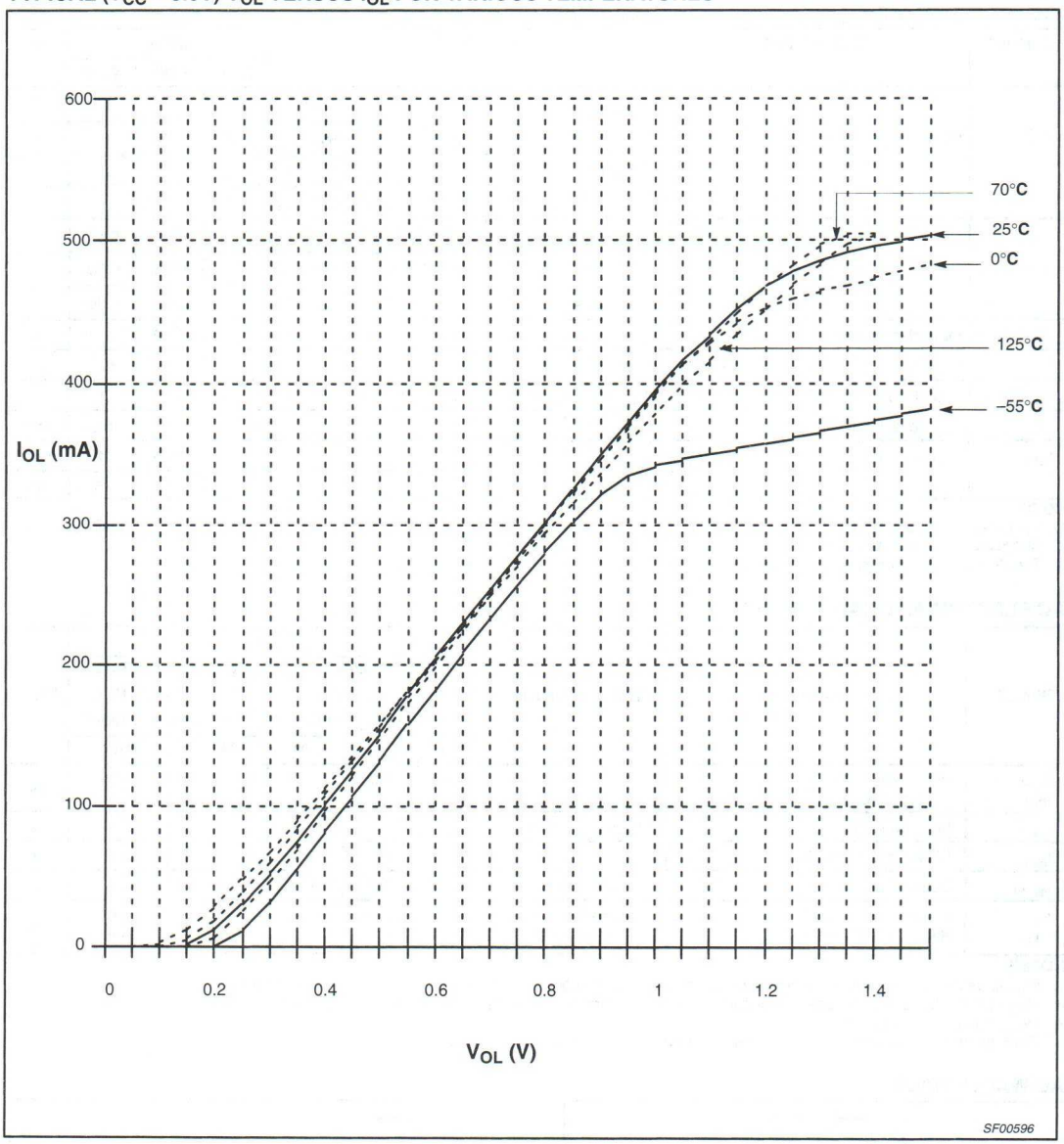
Waveform 1. Propagation delay for input to output



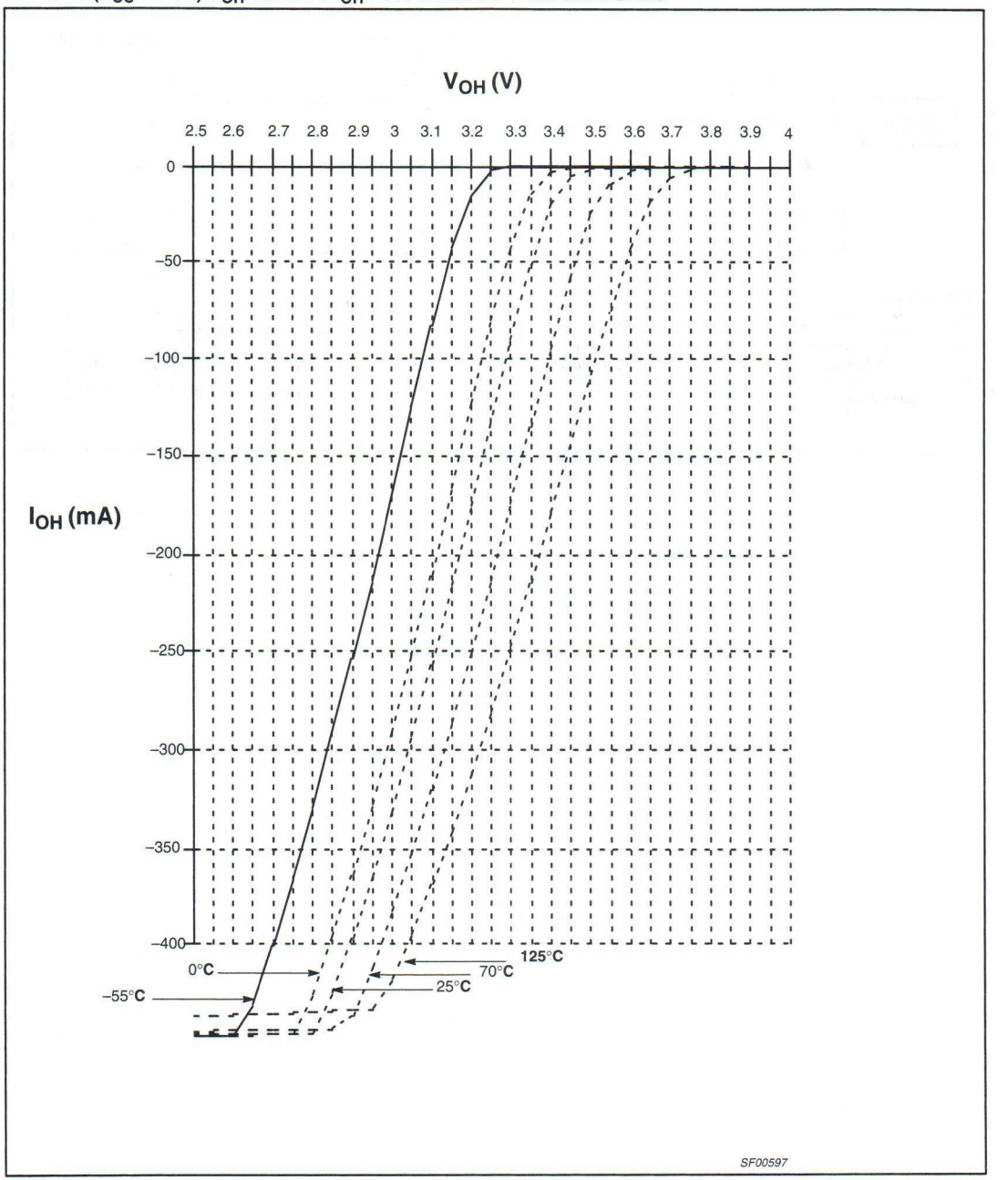
Waveform 2. Output skew

NOTE: For all waveforms, V_M = 1.5V.

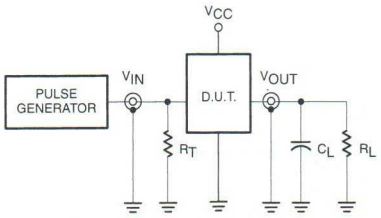
TYPICAL (V_{CC} = 5.0V) V_{OL} VERSUS I_{OL} FOR VARIOUS TEMPERATURES



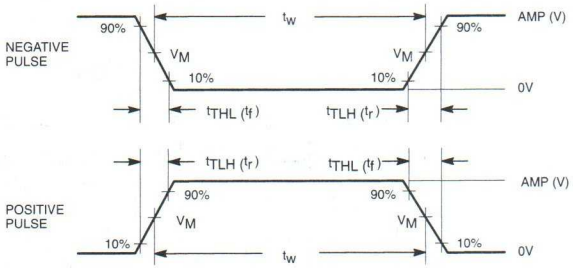
TYPICAL (V_{CC} = 5.0V) V_{OH} VERSUS I_{OH} FOR VARIOUS TEMPERATURES



TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

30Ω line drivers 74F30240*, 74F30244

74F30240 Octal 30Ω line driver with enable, inverting (open collector)
74F30244 Octal 30Ω line driver with enable, non-inverting (open collecor)

FEATURES

- Ideal for driving transmission lines or backplanes. 160mA I_{OL} ideal for applications with impedance as low as 30Ω
- Guaranteed threshold voltages on the incident wave while driving line as low as 30Ω
- High impedance NPN base inputs for reduced loading (20μA in High and Low states)
- Ideal for applications which require high output drive and minimal bus loading
- Octal interface
- 74F30240 inverting
- 74F30244 non-inverting
- Open-Collector outputs sink 160mA
- Multiple side pins are used for V_{CC} and GND to reduce lead inductance (improves speed and noise immunity)
- Available in 24-pin standard slim DIP (300mil) plastic, SOL or CERDIP packages

DESCRIPTION

The 74F30240 and 74F30244 are high current open collector octal buffers composed of eight inverters. The 74F30240 has inverting data paths and the 74F30244 has non-inverting paths. Each device has eight inverters with two Output Enables ($\overline{OE}0$, $\overline{OE}1$), each controlling four outputs. Both drivers are designed to deal with the low-impedance transmission line effects found on printed circuit boards when fast edge rates are used. The 160mA I_{OL} provides ample power to achieve TTL switching voltages on the incident wave.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F30240	9.5ns	62.5mA
74F30244	10.5ns	69mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PACKAGE DRAWING NUMBER
24-pin Plastic Slim DIP (300mil)	N74F30244N	SOT222-1
24–pin Plastic SOL[1]	N74F30244D	SOT137-1

NOTE:
1. Because of the high current sinking capability of these parts, the SOL package should only be used under the following conditions:
   a. 50% duty cycle,
   AND
   b. 3/5 of remaining 50% driving ≤ 100mA (leaving the remaining 2/5 of the drive ≤ 160mA)
   OR
   c. use ≤ 450 linear feet per minute forced air or other thermal mounting techniques.

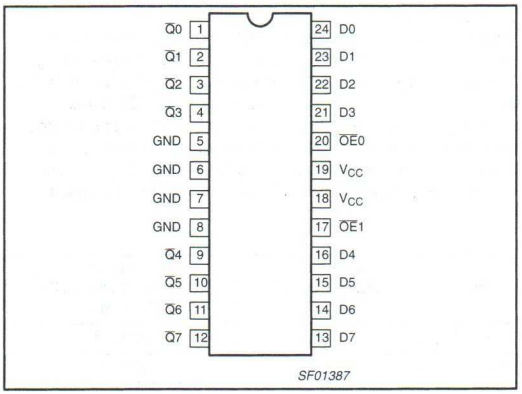
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0–D7	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE}0$–$\overline{OE}1$	Output Enable inputs (Active Low)	1.0/0.033	20μA/20μA
$\overline{Q}0$–$\overline{Q}7$	Data outputs (OC) for 74F30240	OC/266.7	OC/160mA
Q0–Q7	Data outputs (OC) for 74F30244	OC/266.7	OC/160mA

NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state. OC = Open Collector.

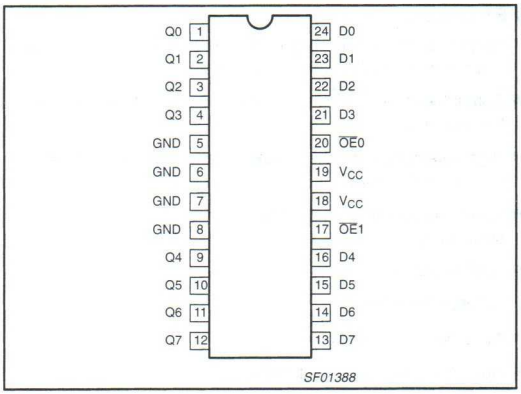
** Discontinued part. Please see the Discontinued Products List.*

PIN CONFIGURATION – 74F30240



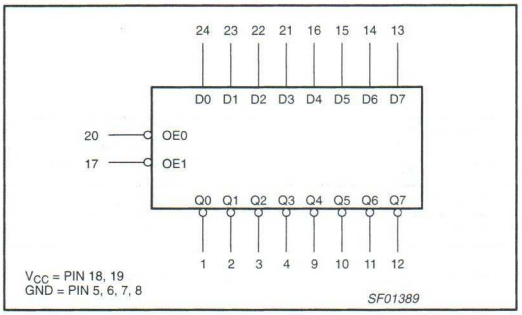
SF01387

PIN CONFIGURATION – 74F30244



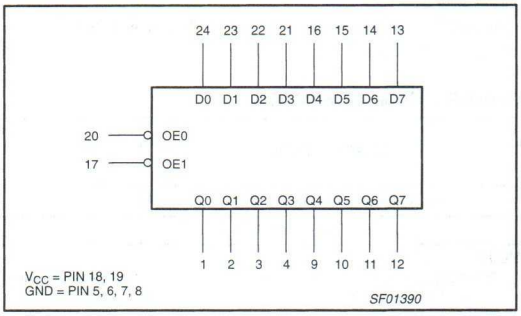
SF01388

LOGIC SYMBOL – 74F30240



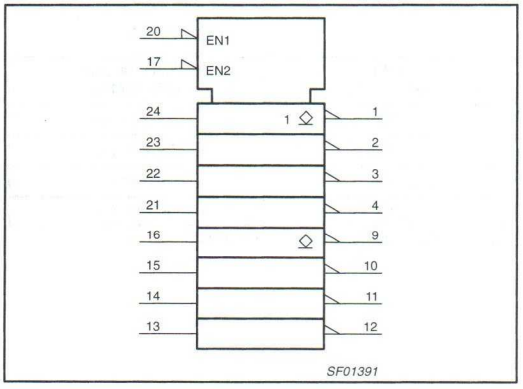
SF01389

LOGIC SYMBOL – 74F30244



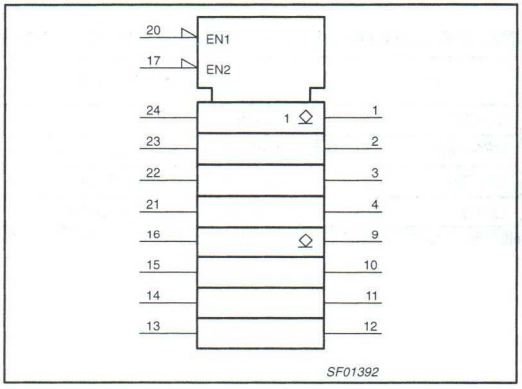
SF01390

IEC/IEEE SYMBOL – 74F30240



SF01391

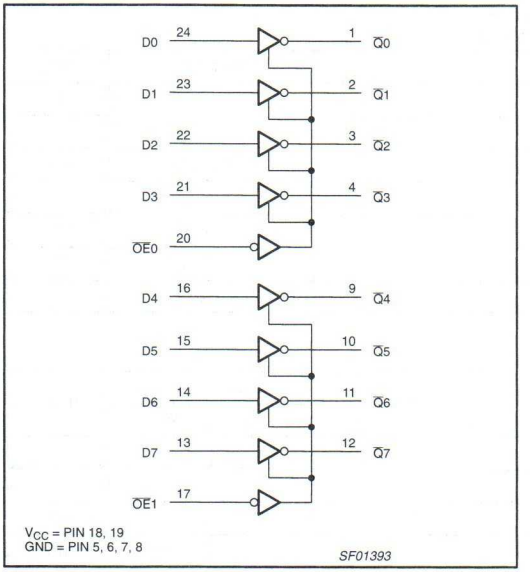
IEC/IEEE SYMBOL – 74F30244



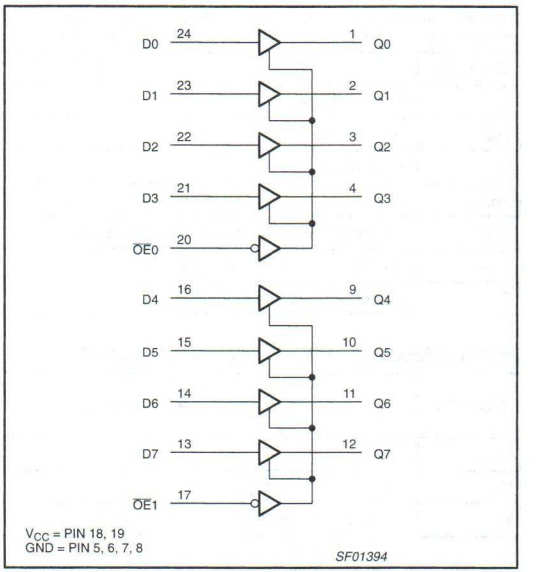
SF01392

* *Discontinued part. Please see the Discontinued Products List.*

LOGIC DIAGRAM – 74F30240



LOGIC DIAGRAM – 74F30244



FUNCTION TABLE

INPUTS		OUTPUTS	
		74F30240	74F30244
$\overline{OE}$n	Dn	$\overline{Q}$n	Qn
L	L	H	L
L	H	L	H
H	X	OFF	OFF

H = High voltage level
L = Low voltage level
X = Don't care
OFF = Pulled up through resistor (Open Collector)

* *Discontinued part. Please see the Discontinued Products List.*

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	320	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
V_{OH}	High-level output voltage			4.5	V
I_{OL}	Low-level output current			160	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							MIN	TYP[2]	MAX	
I_{OH}	High-level output current			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX					250	µA
V_{OL}	Low-level output current			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10% V_{CC}		0.42	0.55	V
					I_{OL} = 160mA[3]	±5% V_{CC}			0.80	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{CC}	Supply current (total)	74F30240	I_{CCH}	V_{CC} = MAX				13	23	mA
			I_{CCL}					70	95	mA
		74F30244	I_{CCH}	V_{CC} = MAX				19	27	mA
			I_{CCL}					70	100	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. I_{OL1} is the current necessary to guarantee the High-to-Low transition in a 30Ω transmission line on the incident wave.

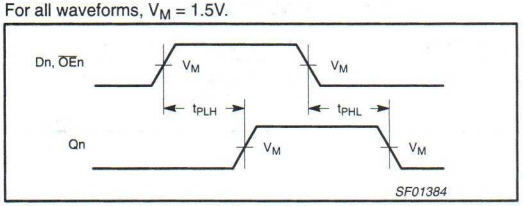
* *Discontinued part. Please see the Discontinued Products List.*

AC ELECTRICAL CHARACTERISTICS

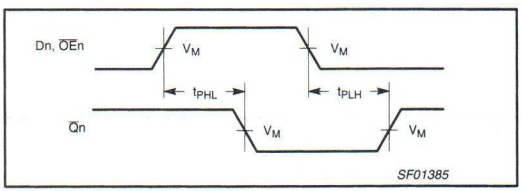
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to $\overline{Q}$n	74f30240	Waveform 2	4.0 1.0	10.0 2.0	14.5 5.0	4.0 1.0	15.0 5.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$n to $\overline{Q}$n		Waveform 1, 2	4.0 3.5	10.0 6.0	14.0 9.0	4.0 3.5	14.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	74f30244	Waveform 1	4.0 3.0	10.5 5.5	14.5 9.0	4.0 3.0	15.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$n to Qn		Waveform 1, 2	4.0 3.5	9.5 6.0	14.0 9.0	4.0 3.5	14.5 10.5	ns

AC WAVEFORMS

For all waveforms, V_M = 1.5V.

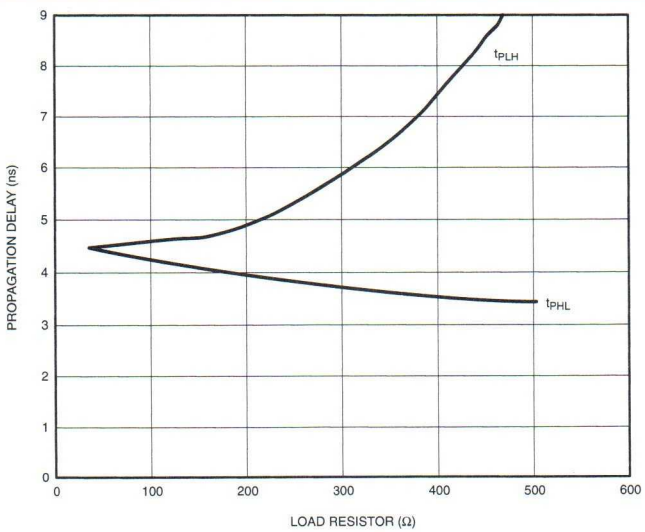


Waveform 1. Propagation Delay for Data to Output



Waveform 2. Propagation Delay for Data to Output

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS

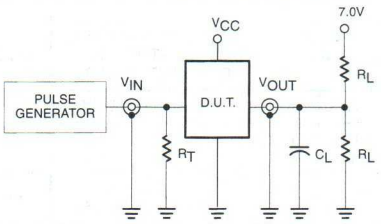


NOTE:
When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}s of the receivers does not exceed the I_{OL} maximum specification.

SF01386

* *Discontinued part. Please see the Discontinued Products List.*

TEST CIRCUIT AND WAVEFORMS



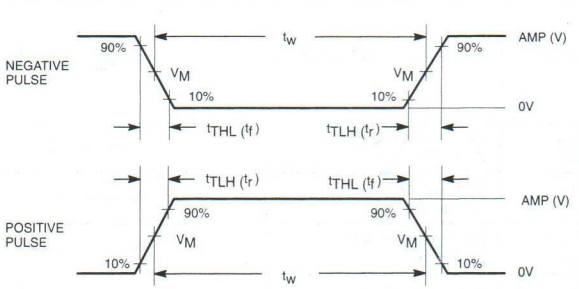
Test Circuit for Open Collector Outputs

DEFINITIONS:

R_L = Load resistor;
see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00027

* *Discontinued part. Please see the Discontinued Products List.*

Synchronizing dual J–$\overline{K}$ positive edge-triggered flip-flop with metastable immune characteristics

74F50109

FEATURE

- Metastable immune characteristics
- Output skew guaranteed less than 1.5ns
- High source current (I_{OH} = 15mA) ideal for clock driver applications
- Pinout compatible with 74F109
- See 74F5074 for synchronizing dual D-type flip-flop
- See 74F50728 for synchronizing cascaded D-type flip-flop
- See 74F50729 for synchronizing dual D-type flip-flop with edge-triggered set and reset

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT(TOTAL)
74F50109	150MHz	22mA

ORDERING INFORMATION

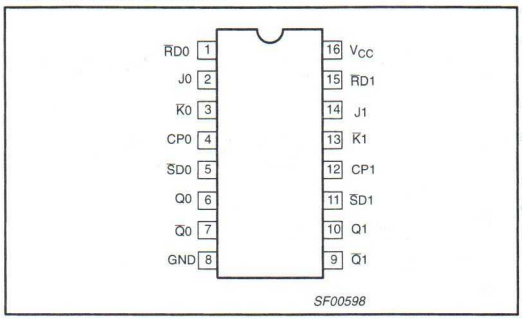
DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
16–pin plastic DIP	N74F50109N	SOT38-4
16–pin plastic SO	N74F50109D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

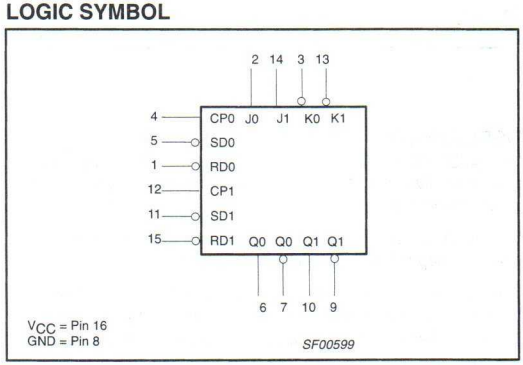
PINS	DESCRIPTION	74F (U.L.) HIGH/ LOW	LOAD VALUE HIGH/LOW
J0, J1	J inputs	1.0/0.417	20µA/250µA
$\overline{K}$0, $\overline{K}$1	K inputs	1.0/0.417	20µA/250µA
CP0, CP1	Clock inputs (active rising edge)	1.0/0.033	20µA/20µA
$\overline{S}$D0, $\overline{S}$D1	Set inputs (active low)	1.0/0.033	20µA/20µA
$\overline{R}$D0, $\overline{R}$D1	Reset inputs (active low)	1.0/0.033	20µA/20µA
Q0, Q1, $\overline{Q}$0, $\overline{Q}$1	Data outputs	750/33	15mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

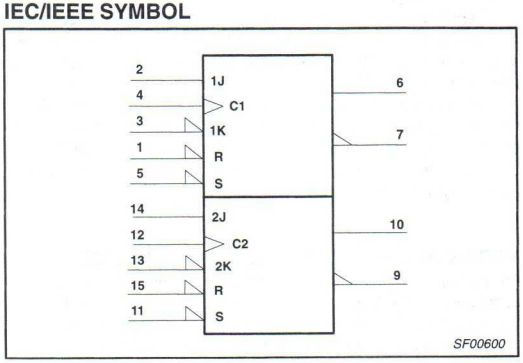
PIN CONFIGURATION



LOGIC SYMBOL



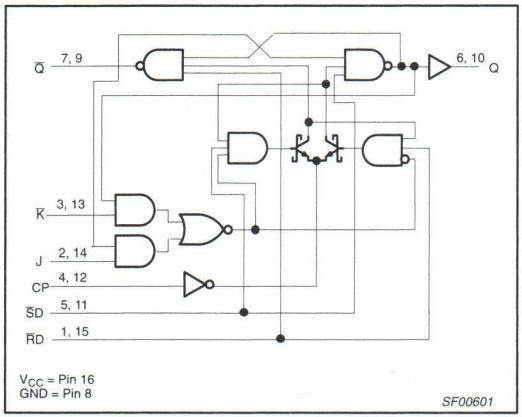
IEC/IEEE SYMBOL



Synchronizing dual J–$\overline{K}$ positive edge-triggered flip-flop with metastable immune characteristics

74F50109

LOGIC DIAGRAM



DESCRIPTION

The 74F50109 is a dual positive edge-triggered JK-type flip-flop featuring individual J, $\overline{K}$, clock, set, and reset inputs; also true and complementary outputs.

Set ($\overline{SD}$) and reset ($\overline{RD}$) are asynchronous active low inputs and operate independently of the clock (CP) input.

The J and $\overline{K}$ are edge–triggered inputs which control the state changes of the flip–flops as described in the function table.
The J and $\overline{K}$ inputs must be stable just one setup time prior to the low–to–high transition of the clock for guaranteed propagation delays. The J$\overline{K}$ design allows operation as a D flip–flop by tying J and $\overline{K}$ inputs together.
The 74F50109 is designed so that the outputs can never display a metastable state due to setup and hold time violations. If setup time and hold time are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74F50109 are: $\tau \cong 135$ps and $\tau \cong 9.8 \times 10^6$ sec where τ represents a function of the rate at which a latch in a metastable state resolves that condition and T_0 represents a function of the measurement of the propensity of a latch to enter a metastable state.

METASTABLE IMMUNE CHARACTERISTICS

Philips Semiconductors uses the term 'metastable immune' to describe characteristics of some of the products in its FAST family. Specifically the 74F50XXX family presently consist of 4 products which displays metastable immune characteristics. This term means that the outputs will not glitch or display an output anomaly under any circumstances including setup and hold time violations.

This claim is easily verified on the 74F5074. By running two independent signal generators (see Fig. 1) at nearly the same frequency (in this case 10MHz clock and 10.02 MHz data) the device–under–test can be often be driven into a metastable state. If the Q output is then used to trigger a digital scope set to infinite persistence the $\overline{Q}$ output will build a waveform.0 An experiment was run by continuously operating the devices in the region where metastability will occur.

When the device–under–test is a 74F74 (which was not designed with metastable immune characteristics) the waveform will appear as in Fig. 2.

Fig. 2 shows clearly that the $\overline{Q}$ output can vary in time with respect to the Q trigger point. This also implies that the Q or $\overline{Q}$ output waveshapes may be distorted. This can be verified on an analog scope with a charge plate CRT. Perhaps of even greater interest are the dots running along the 3.5V volt line in the upper right hand quadrant. These show that the $\overline{Q}$ output did not change state even though the Q output glitched to at least 1.5 volts, the trigger point of the scope.

When the device–under–test is a metastable immune part, such as the 74F5074, the waveform will appear as in Fig. 3. The 74F5074 $\overline{Q}$ output will appear as in Fig. 3. The 74F5074 Q output will not vary with respect to the Q trigger point even when the a part is driven into a metastable state. Any tendency towards internal metastability is resolved by Philips Semiconductors patented circuitry. If a metastable event occurs within the flop the only outward manifestation of the event will be an increased clock–to–Q/$\overline{Q}$ propagation delay. This propagation delay is, of course, a function of the metastability characteristics of the part defined by τ and T_0.

The metastability characteristics of the 74F5074 and related part types represent state–of–the–art TTL technology.

After determining the T_0 and t of the flop, calculating the mean time between failures (MTBF) is simple. Suppose a designer wants to use the 74F50729 for synchronizing asynchronous data that is arriving at 10MHz (as measured by a frequency counter), has a clock frequency of 50MHz, and has decided that he would like to sample the output of the 74F50109 10 nanoseconds after the clock edge. He simply plugs his number into the equation below:

$$MTBF = e^{(t'/t)} / T_0 f_C f_I$$

In this formula, f_C is the frequency of the clock, f_I is the average input event frequency, and t' is the time after the clock pulse that the output is sampled (t' < h, h being the normal propagation delay). In this situation the f_I will be twice the data frequency of 20 MHz because input events consist of both of low and high transitions. Multiplying f_I by f_C gives an answer of 10^{15} Hz^2. From Fig. 4 it is clear that the MTBF is greater than 10^{10} seconds. Using the above formula MTBF is 1.51×10^{10} seconds or about 480 years.

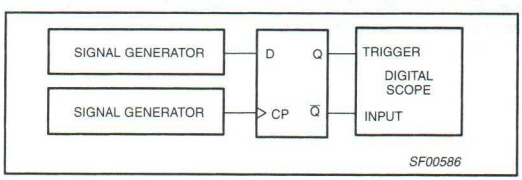


Figure 1. Test setup

COMPARISON OF METASTABLE IMMUNE AND NON–IMMUNE CHARACTERISTICS

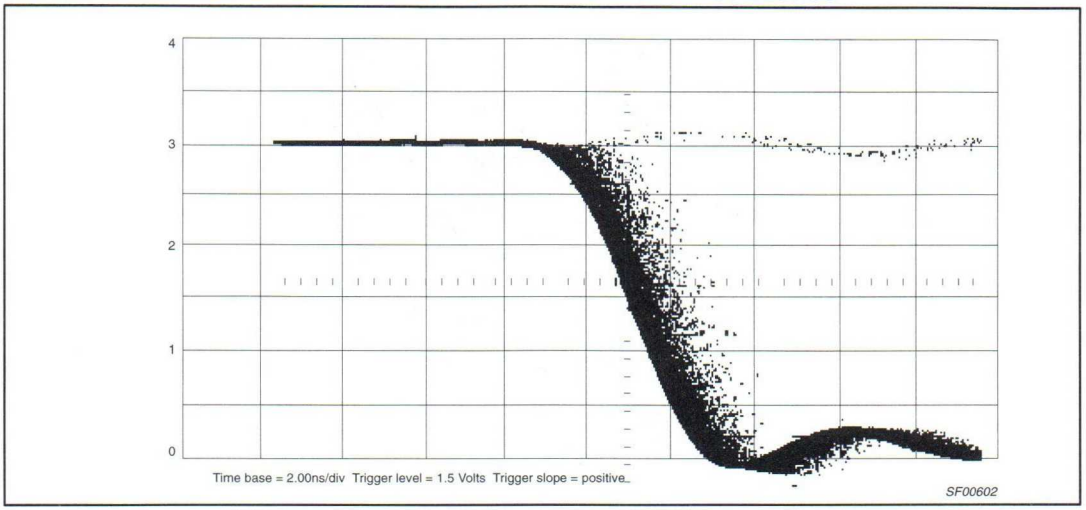


Figure 2. 74F74 $\overline{Q}$ output triggered by Q output, Setup and Hold times violated

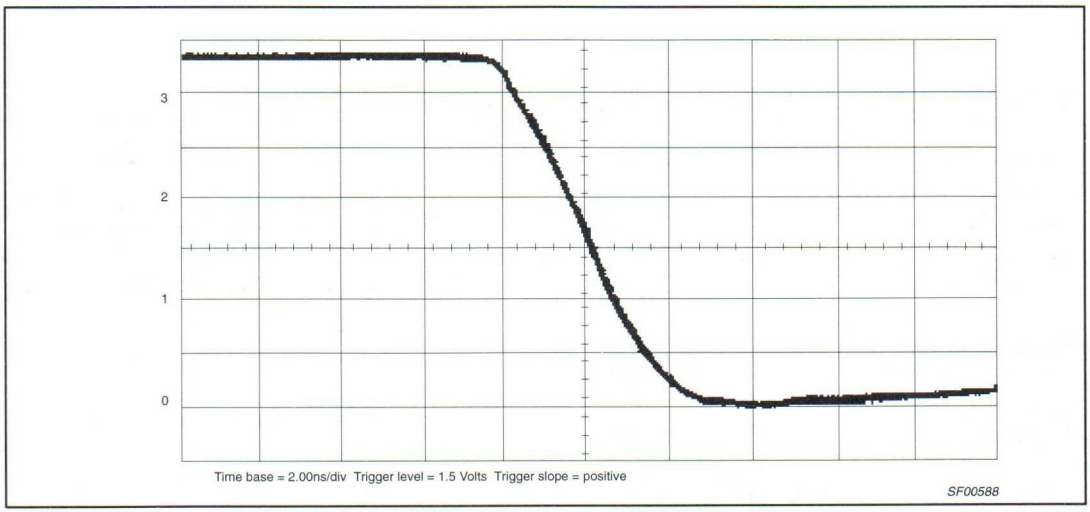
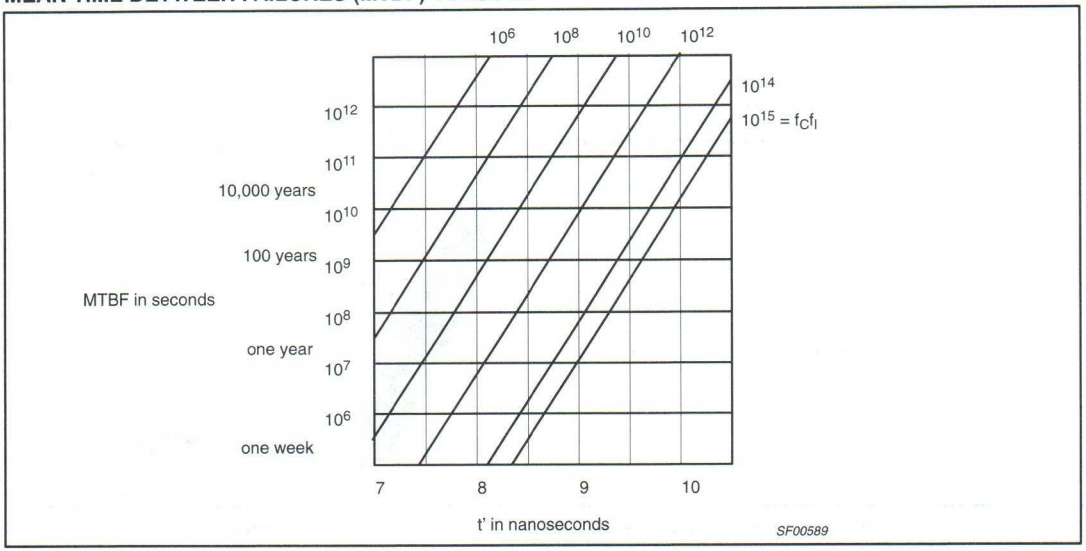


Figure 3. 74F74 $\overline{Q}$ output triggered by Q output, Setup and Hold times violated

MEAN TIME BETWEEN FAILURES (MTBF) VERSUS t'



NOTE: V_{CC} = 5V, T_{amb} = 25°C, τ =135ps, To = 9.8 X 10^8 sec

Figure 4.

TYPICAL VALUES FOR τ AND T_0 AT VARIOUS V_{CC}S AND TEMPERATURES

	T_{amb} = 0°C		T_{amb} = 25°C		T_{amb} = 70°C	
V_{CC}	τ	T_0	τ	T_0	τ	T_0
5.5V	125ps	1.0 X 10^9 sec	138ps	5.4 X 10^6 sec	160ps	1.7 X 10^5 sec
5.0V	115ps	1.3 X 10^{10} sec	135ps	9.8 X 10^6 sec	167ps	3.9 X 10^4 sec
4.5V	115ps	3.4 X 10^{13} sec	132ps	5.1 X 10^8 sec	175ps	7.3 X 10^4 sec

FUNCTION TABLE

INPUTS					OUTPUTS		OPERATING
$\overline{SD}$	$\overline{RD}$	CP	J	$\overline{K}$	Q	$\overline{Q}$	MODE
L	H	X	X	X	H	L	Asynchronous set
H	L	X	X	X	L	H	Asynchronous reset
L	L	X	X	X	H	H	Undetermined*
H	H	↕	X	X	q	$\overline{q}$	Hold
H	H	↑	h	l	$\overline{q}$	q	Toggle
H	H	↑	h	h	H	L	Load "1" (set)
H	H	↑	l	l	L	H	Load "0" (reset)
H	H	↑	l	h	q	$\overline{q}$	Hold 'no change"

NOTES:
H = High–voltage level
h = High–voltage level one setup time prior to low–to–high clock transition
L = Low–voltage level
l = Low–voltage level one setup time prior to low–to–high clock transition
q = Lower case indicate the state of the referenced output prior to the low–to–high clock transition
X = Don't care
↑ = Low–to–high clock transition
↕ = Not low–to–high clock transition
* = Both outputs will be high if both $\overline{SD}$ and $\overline{RD}$ go low simultaneously

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	40	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–1	mA
I_{OL}	Low–level output current			20	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High–level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low–level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN		±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current	Jn, $\overline{K}$n	V_{CC} = MAX, V_I = 0.5V					-250	µA
		CPn, $\overline{S}$Dn, $\overline{R}$Dn	V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX				22	32	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs high in turn.

AC ELECTRICAL CHARACTERISTICS

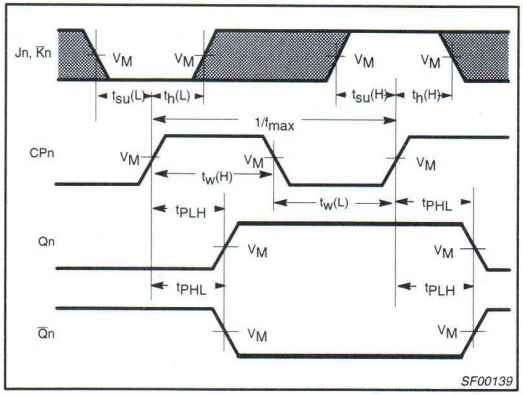
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	130	150		90		ns
t_{PLH} t_{PHL}	Propagation delay CPn to Qn or $\overline{Q}$n	Waveform 1	2.0 2.0	3.8 3.8	6.0 6.0	2.0 2.0	6.5 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}$Dn, $\overline{R}$Dn to Qn or $\overline{Q}$n	Waveform 2	3.5 3.5	5.5 5.5	8.0 8.0	3.0 3.0	8.5 8.5	ns
$t_{sk(o)}$	Output skew[1, 2]	Waveform 4			1.5		1.5	ns

NOTES:
1. $| t_{PN}$ actual – t_{PM} actuall for any output compared to any other output where N and M are either LH or HL.
2. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

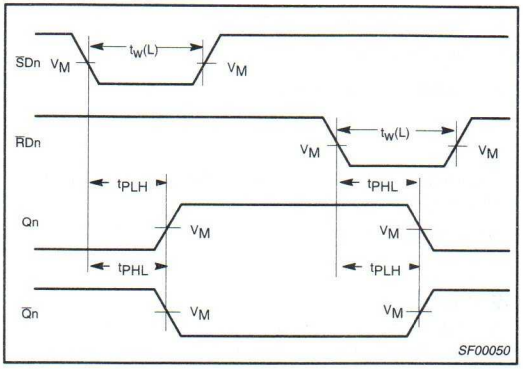
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su}(L)	Setup time, high or low Jn, $\overline{K}$n to CPn	Waveform 1	1.5 1.5			2.0 2.0		ns
t_h (H) t_h (L)	Hold time, high or low Jn, $\overline{K}$n to CPn	Waveform 1	1.0 1.0			1.5 1.5		ns
t_w (H) t_w (L)	CPn pulse width, high or low	Waveform 1	3.0 4.0			3.5 5.0		ns
t_w (L)	$\overline{S}$Dn or $\overline{R}$Dn pulse width, low	Waveform 2	3.5			4.0		ns
t_{rec}	Recovery time $\overline{S}$Dn or $\overline{R}$Dn to CP	Waveform 3	3.0			3.5		ns

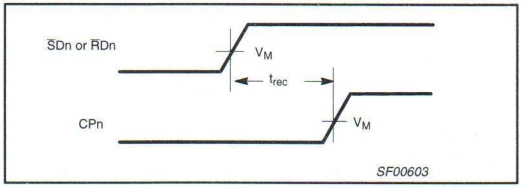
AC WAVEFORMS



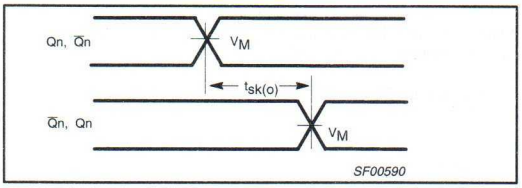
Waveform 1. Propagation delay for data to output, data setup time and hold times, and clock width, and maximum clock frequency



Waveform 2. Propagation delay for set and reset to output, set and reset pulse width



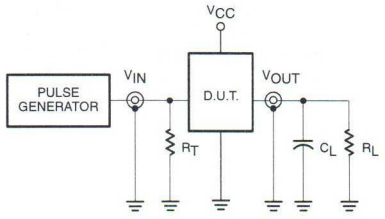
Waveform 3. Recovery time for set or reset to output



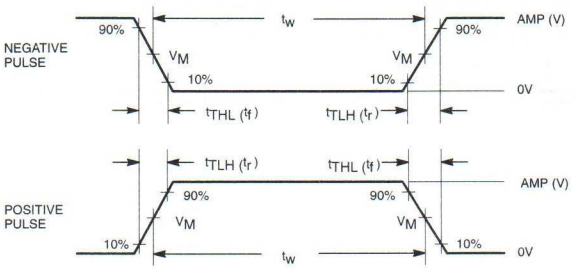
Waveform 4. Output skew

NOTES:
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



DEFINITIONS:
R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

Synchronizing cascaded dual positive edge-triggered D-type flip-flop

74F50728

FEATURES

- Metastable immune characteristics
- Output skew less than 1.5ns
- See 74F5074 for synchronizing dual D-type flip-flop
- See 74F50109 for synchronizing dual J–$\overline{K}$ positive edge-triggered flip-flop
- See 74F50729 for synchronizing dual dual D-type flip-flop with edge-triggered set and reset
- Industrial temperature range available (–40°C to +85°C)

DESCRIPTION

The 74F50728 is a cascaded dual positive edge–triggered D–type featuring individual data, clock, set and reset inputs; also true and complementary outputs.

Set ($\overline{S}$Dn) and reset ($\overline{R}$Dn) are asynchronous active low inputs and operate independently of the clock (CPn) input. They set and reset both flip–flops of a cascaded pair simultaneously. Data must be stable just one setup time prior to the low–to–high transition of the clock for guaranteed propagation delays.

Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive–going pulse. Following the hold time interval, data at the Dn input may be changed without affecting the levels of the output. Data entering the 74F50728 requires two clock cycles to arrive at the outputs.

The 74F50728 is designed so that the outputs can never display a metastable state due to setup and hold time violations. If setup time and hold time are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74F50728 are: $\tau \cong 135$ps and $T_0 \cong 9.8 \times 10^6$ sec where τ represents a function of the rate at which a latch in a metastable state resolves that condition and T_0 represents a function of the measurement of the propensity of a latch to enter a metastable state.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F50728	145 MHz	23mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
14–pin plastic DIP	N74F50728N	I74F50728N	SOT27-1
14–pin plastic SO	N74F50728D	I74F50728D	SOT108-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

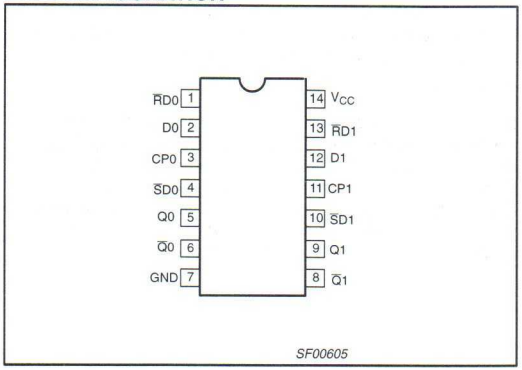
PINS	DESCRIPTION	74F (U.L.) HIGH/ LOW	LOAD VALUE HIGH/ LOW
D0, D1	Data inputs	1.0/0.417	20µA/250µA
CP0, CP1	Clock inputs (active rising edge)	1.0/1.0	20µA/20µA
$\overline{S}$D0, $\overline{S}$D1	Set inputs (active low)	1.0/1.0	20µA/20µA
$\overline{R}$D0, $\overline{R}$D1	Reset inputs (active low)	1.0/1.0	20µA/20µA
Q0, Q1, $\overline{Q}$0, $\overline{Q}$1	Data outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

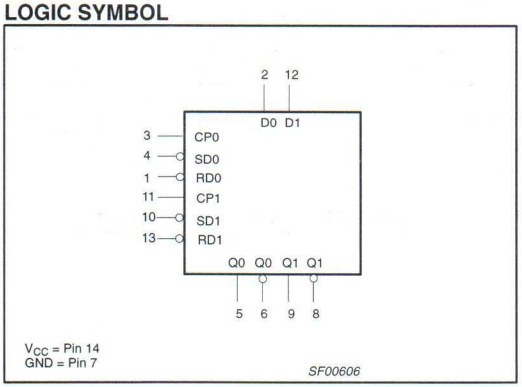
Synchronizing cascaded dual positive edge-triggered D-type flip-flop

74F50728

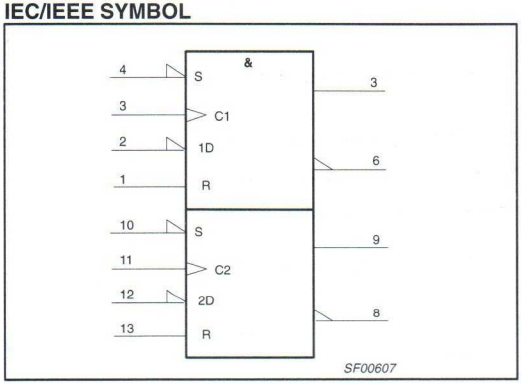
PIN CONFIGURATION



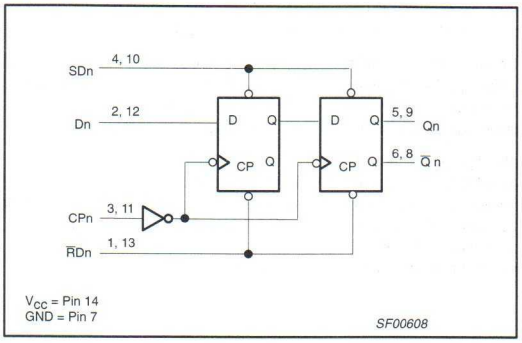
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



NOTE: Data entering the flip–flop requires two clock cycles to arrive at the output.

SYNCHRONIZING SOLUTIONS

Synchronizing incoming signals to a system clock has proven to be costly, either in terms of time delays or hardware. The reason for this is that in order to synchronize the signals a flip–flop must be used to "capture" the incoming signal. While this is perhaps the only way to synchronize a signal, to this point, there have been problems with this method. Whenever the flop's setup or hold times are violated the flop can enter a metastable state causing the outputs in turn to glitch, oscillate, enter an intermediate state or change state in some abnormal fashion. Any of these conditions could be responsible for causing a system crash. To minimize this risk, flip–flops are often cascaded so that the input signal is captured on the first clock pulse and released on the second clock pulse (see Fig.1). This gives the first flop about one clock period minus the flop delay and minus the second flop's clock–to–Q setup time to resolve any metastable condition. This method greatly reduces the probability of the outputs of the synchronizing device displaying an abnormal state but the trade-off is that one clock cycle is lost to synchronize the incoming data and two separate flip–flops are required to produce the cascaded flop circuit. In order to assist the designer of synchronizing circuits Philips Semiconductors is offering the 74F50728.

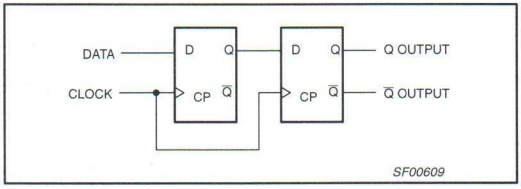


Figure 1.

The 50728 consists of two pair of cascaded D–type flip–flops with metastable immune features and is pin compatible with the 74F74. Because the flops are cascaded on a single part the metastability

characteristics are greatly improved over using two separate flops that are cascaded. The pin compatibility with the 74F74 allows for plug–in retrofitting of previously designed systems.

Because the probability of failure of the 74F50728 is so remote, the metastability characteristics of the part were empirically determined based on the characteristics of its sister part, the 74F5074. The table below shows the 74F5074 metastability characteristics.

Having determined the T_0 and τ of the flop, calculating the mean time between failures (MTBF) for the 74F50728 is simple. It is, however, somewhat different than calculating MTBF for a typical part because data requires two clock pulses to transit from the input to the output. Also, in this case a failure is considered of the output beyond the normal propagation delay.

Suppose a designer wants to use the flop for synchronizing asynchronous data that is arriving at 10MHz (as measured by a frequency counter), and is using a clock frequency of 50MHz. He simply plugs his number into the equation below:

$$MTBF = e^{(t'/t)}/T_o f_C f_I$$

In this formula, f_C is the frequency of the clock, f_I is the average input event frequency, and t' is the period of the clock input (20 nanoseconds). In this situation the f_I will be twice the data frequency of 20 MHz because input events consist of both of low and high data transitions. From Fig. 2 it is clear that the MTBF is greater than 10^{41} seconds. Using the above formula the actual MTBF is 2.23 X 10^{42} seconds or about 7 X 10^{34} years.

TYPICAL VALUES FOR τ AND T_0 AT VARIOUS V_{CC}S AND TEMPERATURES

	T_{amb} = 0°C		T_{amb} = 25°C		T_{amb} = 70°C	
	τ	T_0	τ	T_0	τ	T_0
V_{CC} = 5.5V	125ps	1.0 X 10^9 sec	138ps	5.4 X 10^6 sec	160ps	1.7 X 10^5 sec
V_{CC} = 5.0V	115ps	1.3 X 10^{10} sec	135ps	9.8 X 10^6 sec	167ps	3.9 X 10^4 sec
V_{CC} = 4.5V	115ps	3.4 X 10^{13} sec	132ps	5.1 X 10^8 sec	175ps	7.3 X 10^4 sec

MEAN TIME BETWEEN FAILURES VERSUS DATA FREQUENCY AT VARIOUS CLOCK FREQUENCY

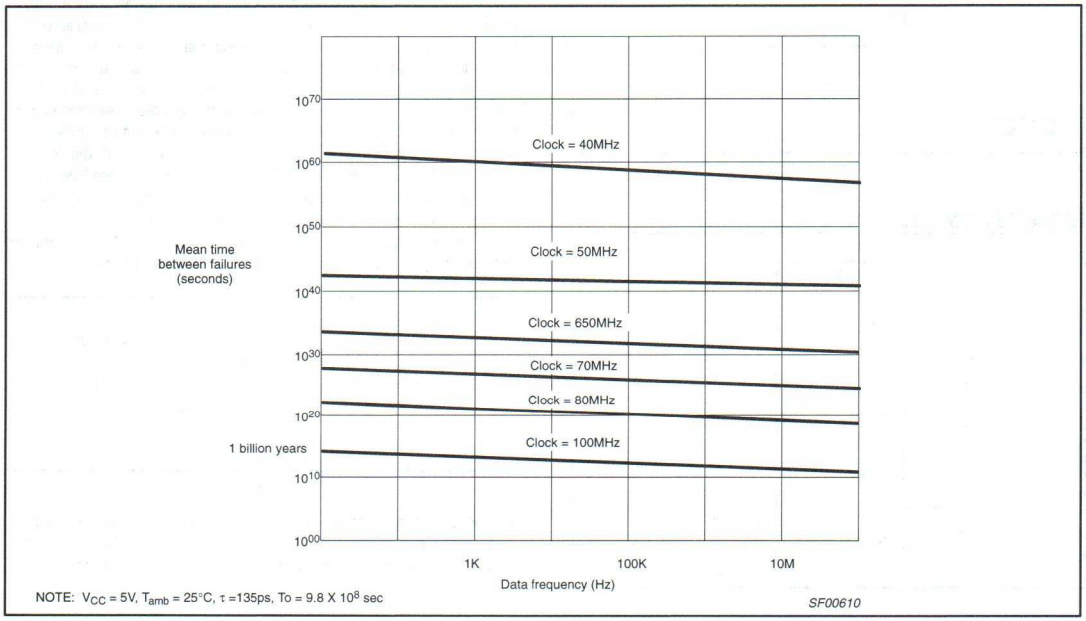


Figure 2.

FUNCTION TABLE

INPUTS				INTERNAL REGISTER	OUTPUTS		OPERATING MODE
$\overline{S}$Dn	$\overline{R}$Dn	CPn	Dn	Q	Qn	$\overline{Q}$n	
L	H	X	X	H	H	L	Asynchronous set
H	L	X	X	L	L	H	Asynchronous reset
L	L	X	X	X	H	H	Undetermined*
H	H	↑	h	h	H	L	Load "1"
H	H	↑	l	l	L	H	Load "0"
H	H	L	X	NC	NC	NC	Hold

NOTES:

H = High voltage level
h = High voltage level one setup time prior to low–to–high clock transition
L = Low voltage level
l = Low voltage level one setup time prior to low–to–high clock transition
NC= No change from the previous setup
X = Don't care
* = This setup is unstable and will change when either set of reset return to the high–level
↑ = Low–to–high clock transition.
** = Data entering the flip–flop requires two clock cycles to arrive at the output (see logic diagram)

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.4			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current				–3	mA
I_{OL}	Low–level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = MIN	I_{OH} = MAX	±10%V_{CC}	2.5			V
			V_{IL} = MAX,		±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN		±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current	Dn	V_{CC} = MAX, V_I = 0.5V					-250	µA
		CPn, $\overline{SD}$n, $\overline{RD}$n						–20	µA
I_{OS}	Short–circuit output current[3]		V_{CC} = MAX, V_O = 2.25V			-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX				23	34	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs high in turn.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS: T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			LIMITS: T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		LIMITS: T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	100	145		85		70		ns
t_{PLH} t_{PHL}	Propagation delay CPn to Qn or $\overline{Q}$n	Waveform 1	2.0 2.0	3.8 3.8	6.0 6.0	1.5 2.0	6.5 6.5	1.5 2.0	7.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SD}$n $\overline{RD}$n to Qn or $\overline{Q}$n	Waveform 2	3.5 3.5	5.0 5.0	8.0 8.0	3.0 3.0	9.0 8.5	3.0 3.0	10.5 10.0	ns
$t_{sk(o)}$	Output skew[1, 2]	Waveform 4			1.5		1.5		1.5	ns

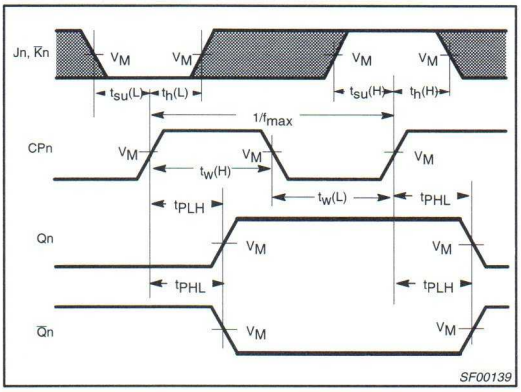
NOTES TO AC ELECTRICAL CHARACTERISTICS

1. $|t_{PLH}$ actual $-t_{PHL}$ actual $|$ for any one output compare to any other output where N and M are either LH or HL.
2. Skew lines are valid only under same conditions (temperature, V_{CC}, loading, etc.,).

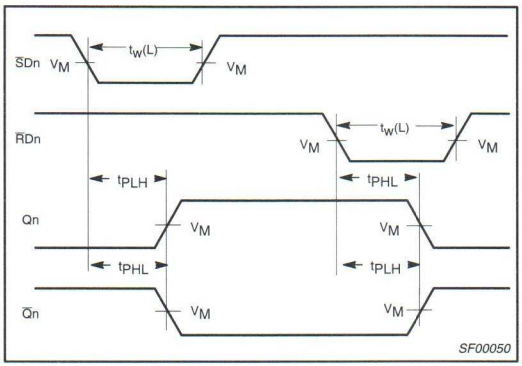
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = −40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{su} (H) t_{su}(L)	Setup time, high or low Dn to CPn	Waveform 1	1.5 1.5			2.0 2.0		2.0 2.0		ns
t_h (H) t_h (L)	Hold time, high or low Dn to CPn	Waveform 1	0.0 0.0			1.5 1.5		1.5 1.5		ns
t_w (H) t_w (L)	CPn pulse width, high or low	Waveform 2	3.0 4.0			3.5 5.0		4.0 5.5		ns
t_w (L)	$\overline{SD}$n, $\overline{RD}$n pulse width, low	Waveform 2	4.5			4.0		4.5		ns
t_{rec}	Recovery time $\overline{SD}$n, $\overline{RD}$n to CPn	Waveform 3	3.5			3.5		3.5		ns

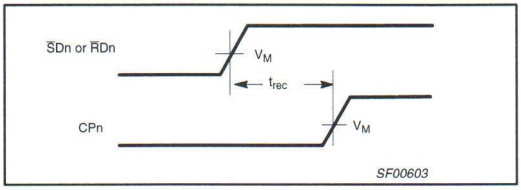
AC WAVEFORMS



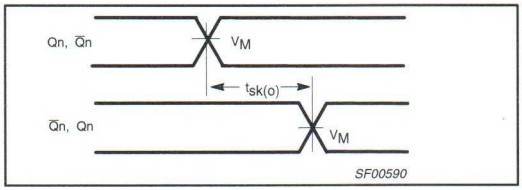
Waveform 1. Propagation delay for data to output, data setup time and hold times, and clock width, and maximum clock frequency



Waveform 2. Propagation delay for set and reset to output, set and reset pulse width



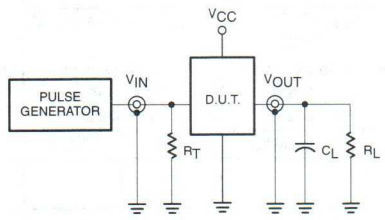
Waveform 3. Recovery time for set or reset to output



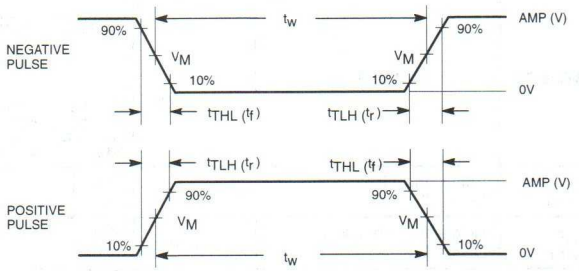
Waveform 4. Output skew

NOTES:
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

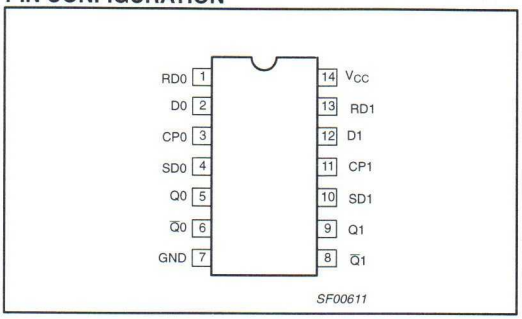
Synchronizing dual D-type flip-flop with edge-triggered set and reset and metastable immune characteristics

74F50729

FEATURES

- Metastable immune characteristics
- Output skew less than 1.5ns
- High source current (I_{OH} = 15mA) ideal for clock driver applications
- See 74F5074 for synchronizing dual D–type flip–flop
- See 74F50109 for synchronizing dual J–$\overline{K}$ positive edge–triggered flip–flop
- See 74F50728 for synchronizing cascaded dual D–type flip–flop
- Industrial temperature range available (–40°C to +85°C)

PIN CONFIGURATION



DESCRIPTION

The 74F50729 is a dual positive edge–triggered D–type featuring individual data, clock, set and reset inputs; also true and complementary outputs.

The 74F50729 is designed so that the outputs can never display a metastable state due to setup and hold time violations. If setup time and hold time are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74F50729 are: $\tau \cong 135$ps and $\tau \cong 9.8 \times 10^6$ sec where τ represents a function of the rate at which a latch in a metastable state resolves that condition and T_o represents a function of the measurement of the propensity of a latch to enter a metastable state.

Set (SDn) and reset (RDn) are asynchronous positive–edge triggered inputs and operate independently of the clock (CPn) input. Data must be stable just one setup time prior to the low–to–high transition of the clock for guaranteed propagation delays.

Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive–going pulse. Following the hold time interval, data at the Dn input may be changed without affecting the levels of the output.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F50729	120 MHz	19mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
14–pin plastic DIP	N74F50729N	I74F50729N	SOT27-1
14–pin plastic SO	N74F50729D	I74F50729D	SOT108-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

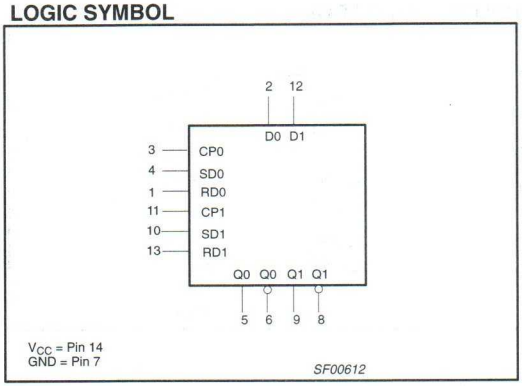
PINS	DESCRIPTION	74F (U.L.) HIGH/ LOW	LOAD VALUE HIGH/ LOW
D0, D1	Data inputs	1.0/0.417	20µA/250µA
CP0, CP1	Clock inputs (active rising edge)	1.0/1.0	20µA/20µA
SD0, SD1	Set inputs (active rising edge)	1.0/1.0	20µA/20µA
RD0, RD1	Reset inputs (active rising edge)	1.0/1.0	20µA/20µA
Q0, Q1, $\overline{Q}$0, $\overline{Q}$1	Data outputs	750/33	15mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

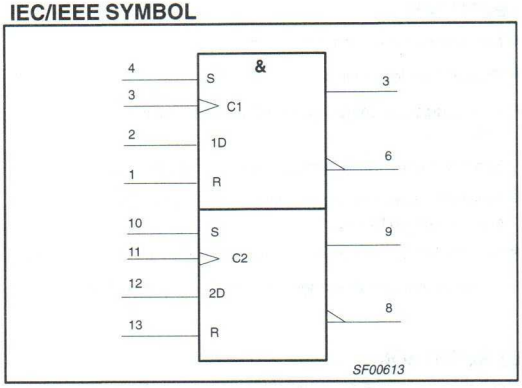
Synchronizing dual D-type flip-flop with edge-triggered set and reset and metastable immune characteristics

74F50729

LOGIC SYMBOL



IEC/IEEE SYMBOL



METASTABLE IMMUNE CHARACTERISTICS

Philips Semiconductors uses the term 'metastable immune' to describe characteristics of some of the products in its family. Specifically the 74F50XXX family presently consist of 4 products which will not glitch or display metastable immune characteristics. This term means that the outputs will not glitch or display an output anomaly under any circumstances including setup and hold time violations. This claim is easily verified on the 74F5074. By running two independent signal generators (see Fig. 1) at nearly the same frequency (in this case 10MHz clock and 10.02 MHz data) the device–under–test can be often be driven into metastable state. If the Q output is then used to trigger a digital scope set to infinite persistence the $\overline{Q}$ output will build a waveform. An experiment was run by continuously operating the devices in the region where metastability will occur.

When the device–under–test is a 74F74 (which was not designed with metastable immune characteristics) the waveform will appear as in Fig. 2.

Figure 2 shows clearly that the $\overline{Q}$ output can vary in time with respect to the Q trigger point. This also implies that the Q or $\overline{Q}$ output waveshapes may be distorted. This can be verified on an analog scope with a charge plate CRT. Perhaps of even greater interest are the dots running along the 3.5V volt line in the upper right hand quadrant. These show that the $\overline{Q}$ output did not change state even though the Q output glitched to at least 1.5 volt, the trigger point of the scope.

When the device–under–test is a metastable immune part, such as the 74F5074, the waveform will appear as in Fig. 3. The 74F5074 $\overline{Q}$ output will appear as in Fig. 3. The 74F5074 Q output will not vary with respect to the Q trigger point even when the a part is driven into a metastable state. Any tendency towards internal metastability is resolved by Philips Semiconductors patented circuitry. If a metastable event occurs within the flop the only outward manifestation of the event will be an increased clock–to–Q/$\overline{Q}$ propagation delay. This propagation delay is, of course, a function of the metastability characteristics of the part defined by τ and T_0.

The metastability characteristics of the 74F5074 and related part types represent state–of–the–art TTL technology.

After determining the T_0 and t of the flop, calculating the mean time between failures (MTBF) is simple. Suppose a designer wants to use the 74F50729 for synchronizing asynchronous data that is arriving at 10MHz (as measured by a frequency counter), has a clock frequency of 50MHz, and has decided that he would like to sample the output of the 74F50729 10 nanoseconds after the clock edge. He simply plugs his number into the equation below:

$$MTBF = e^{(t'/t)} / T_o f_C f_I$$

In this formula, f_C is the frequency of the clock, f_I is the average input event frequency, and t' is the time after the clock pulse that the output is sampled (t' < h, h being the normal propagation delay). In this situation the f_I will be twice the data frequency of 20 MHz because input events consist of both of low and high transitions. Multiplying f_I by f_C gives an answer of 10^{15} Hz^2. From Fig. 3. it is clear that the MTBF is greater than 10^{10} seconds. Using the above formula the actual MTBF is 1.51 X 10^{10} seconds or about 480 years.

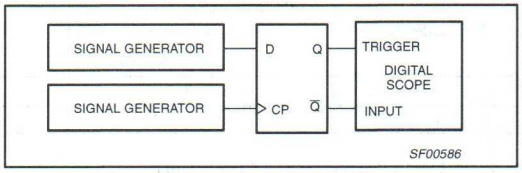


Figure 1. Test Setup

COMPARISON OF METASTABLE IMMUNE AND NON–IMMUNE CHARACTERISTICS

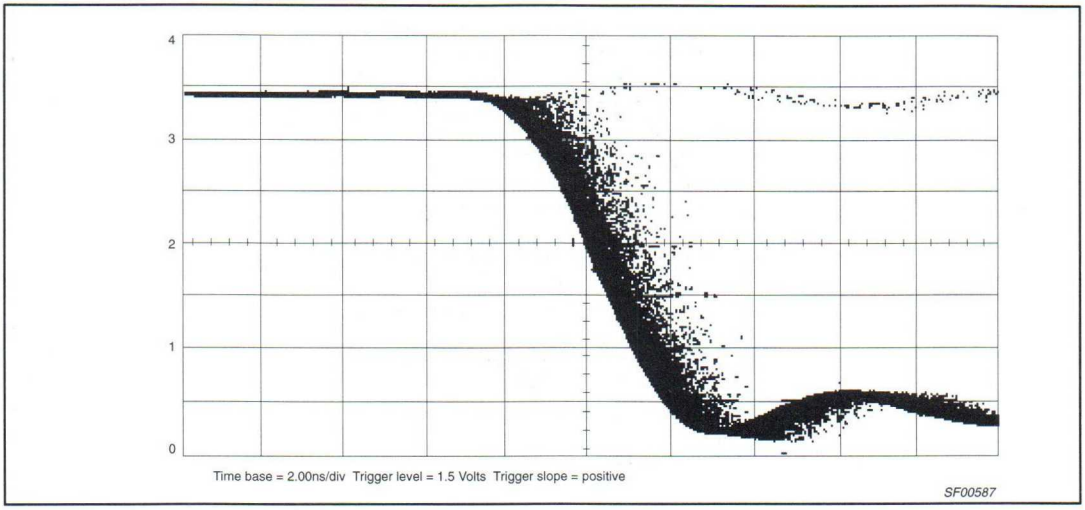


Figure 2. 74F74 $\overline{Q}$ output triggered by Q output, setup and hold times violated

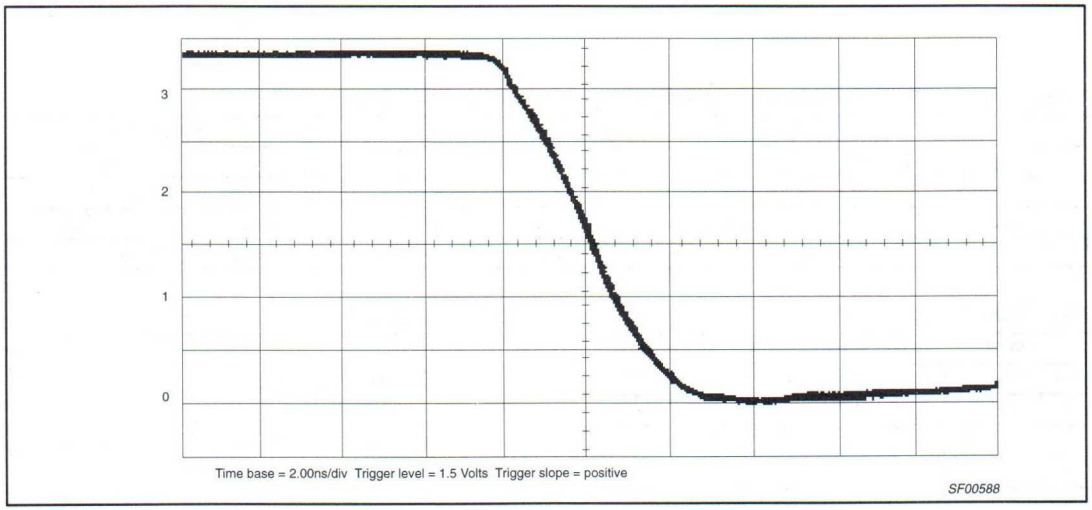
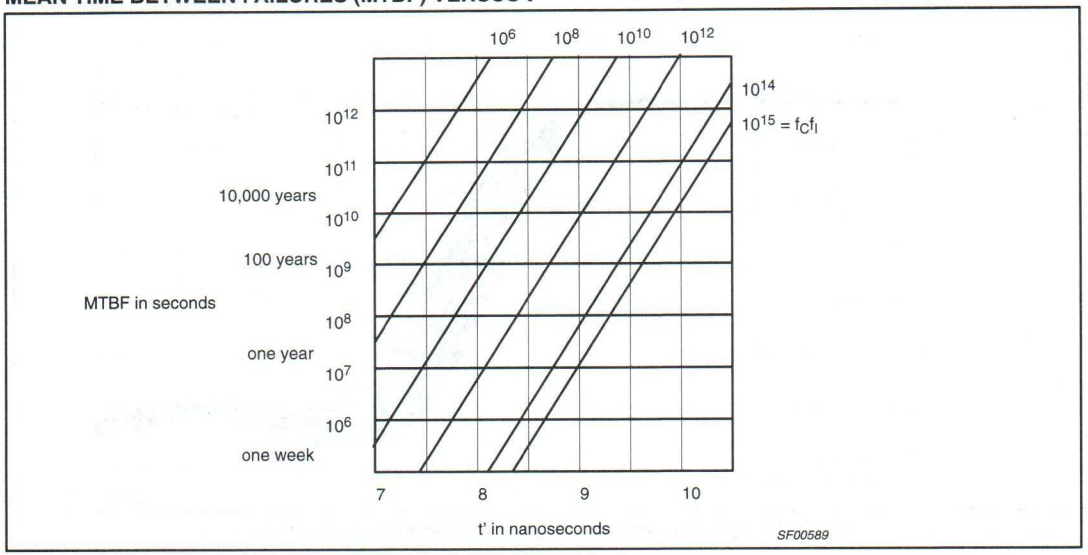


Figure 3. 74F74 $\overline{Q}$ output triggered by Q output, setup and hold times violated

MEAN TIME BETWEEN FAILURES (MTBF) VERSUS t'



NOTE: V_{CC} = 5V, T_{amb} = 25°C, τ =135ps, To = 9.8 X 10^6 sec

Figure 4.

TYPICAL VALUES FOR τ AND T_0 AT VARIOUS V_{CC}S AND TEMPERATURES

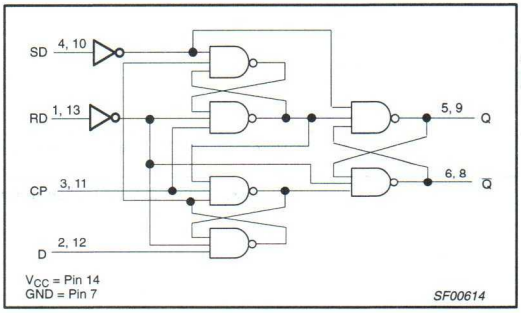
	T_{amb} = 0°C		T_{amb} = 25°C		T_{amb} = 70°C	
V_{CC}	τ	T_0	τ	T_0	τ	T_0
5.5V	125ps	1.0 X 10^9 sec	138ps	5.4 X 10^6 sec	160ps	1.7 X 10^5 sec
5.0V	115ps	1.3 X 10^{10} sec	135ps	9.8 X 10^6 sec	167ps	3.9 X 10^4 sec
4.5V	115ps	3.4 X 10^{13} sec	132ps	5.1 X 10^8 sec	175ps	7.3 X 10^4 sec

FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$	MODE
↑	↥	X	X	H	L	Asynchronous set
↥	↑	X	X	L	H	Asynchronous reset
↥	↥	↑	h	H	L	Load "1"
↥	↥	↑	l	L	H	Load "0"
↥	↥	↥	X	NC	NC	Hold

NOTES:
1. H = High–voltage level
2. h = High–voltage level one setup time prior to low–to–high clock transition
3. L = Low–voltage level
4. l = Low–voltage level one setup time prior to low–to–high clock transition
5. NC= No change from the previous setup
6. X = Don't care
7. ↑ = Low–to–high clock transition
8. ↥ = Not low–to–high clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IH}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current	$V_{CC} \pm 10\%$			–12	mA
		$V_{CC} \pm 5\%$			–15	mA
I_{OL}	Low–level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS MIN	LIMITS TY.[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = MIN V_{IL} = MAX,	I_{OH} = MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = –15mA	±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current	Dn	V_{CC} = MAX, V_I = 0.5V					-250	µA
		CPn, SDn, RDn						–20	µA
I_{OS}	Short–circuit output current[3]		V_{CC} = MAX, V_O = 2.25V			-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX				19	27	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs high in turn.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_{amb} = +25°C; V_{CC} = +5.0V; C_L = 50pF; R_L = 500Ω			LIMITS T_{amb} = 0°C to +70°C; V_{CC} = +5.0V ± 10%; C_L = 50pF; R_L = 500Ω		LIMITS T_{amb} = –40°C to +85°C; V_{CC} = +5.0V ± 10%; C_L = 50pF; R_L = 500Ω		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	105	120		85		75		ns
t_{PLH} t_{PHL}	Propagation delay CPn to Qn or $\overline{Q}$n	Waveform 1	2.0 2.0	3.9 3.9	6.0 6.0	1.5 2.0	6.5 6.5	1.5 2.0	7.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay SDn RDn to Qn or $\overline{Q}$n	Waveform 2	2.0 3.0	4.0 5.0	6.5 7.5	1.5 2.0	7.5 8.0	1.5 2.0	7.5 8.0	ns
$t_{ok(o)}$	Output skew[1, 2]	Waveform 4			1.5		1.5		1.5	ns

NOTES:

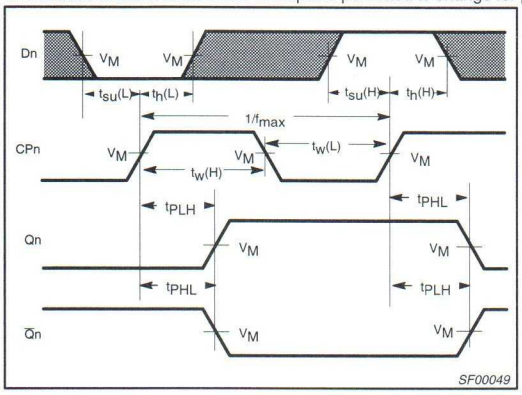
1. I t_{PLH} actual –t_{PHL} actual I for any one output compared to any other output where N and M are either LH or HL.
2. Skew lines are valid only under same conditions (temperature, V_{CC}, loading, etc.,).

AC SETUP REQUIREMENTS

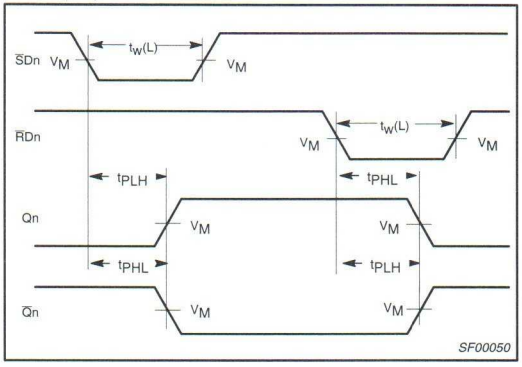
SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{su} (H) t_{su}(L)	Setup time, high or low Dn to CPn	Waveform 1	1.5 1.5			2.0 2.0		2.0 2.0		ns
t_h (H) t_h (L)	Hold time, high or low Dn to CPn	Waveform 1	1.0 1.0			1.5 1.5		1.5 1.5		ns
t_w (H) t_w (L)	CPn pulse width, high or low	Waveform 2	3.0 4.0			3.5 6.0		3.5 6.0		ns
t_w (L)	SDn, RDn pulse width, low	Waveform 3	3.5			4.0		4.0		ns
t_{rec}	Recovery time SDn, RDn to CPn	Waveform 3	6.0			6.5		6.5		ns
t_{rec}	Recovery time SDn to RDn or RDn to SDn	Waveform 3	6.0			1.0		1.0		ns

AC WAVEFORMS

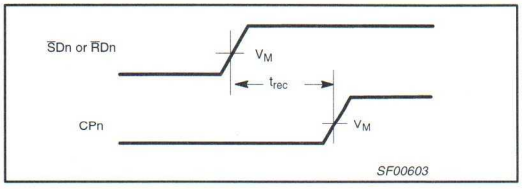
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



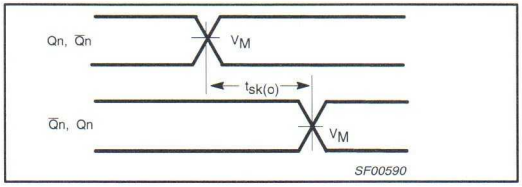
Waveform 1. Propagation delay for data to output, data setup time and hold times, and clock width, and maximum clock frequency



Waveform 2. Propagation delay for set and reset to output, set and reset pulse width

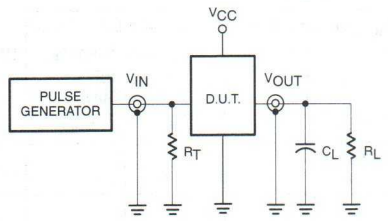


Waveform 3. Recovery time for set or reset to output

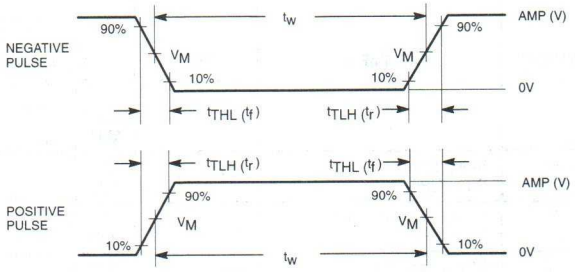


Waveform 4. Output skew

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

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Section 3
Application Notes

FAST TTL Logic Series

CONTENTS

AN202	Testing and specifying FAST logic	863
AN203	Test fixtures for high speed logic	868
AN212	Package lead inductance considerations in high-speed applications	877
AN214	74F extended octal-plus family applications	883
AN215	74FXXXX "Light Load" input products	895
AN216	Arbitration in shared resource systems	901
AN217	Metastability tests for the 74F786 – 4-input asynchronous bus arbiter	906
AN219	A metastability primer	911
AN220	Synchronizing and clock driving solutions – using the 74F50XXX family	914
AN242	Skew definitions	917
AN2021	Thermal considerations for FAST logic products	918

Testing and specifying FAST logic

AN202

INTRODUCTION

FAST™ is a second generation Schottky logic family that utilizes advanced oxide-isolation techniques to increase the speed and decrease the power dissipation beyond the levels achievable with conventional junction isolated families. The improved performance of the family is exhibited in two ways — first, the speed and power characteristics of the devices are improved, and second, the conditions under which speed and power are specified are much tighter. For instance, LS and S TTL families offer AC limits only at a nominal +5.00V V_{CC} supply voltage and at room temperature, 25°C. By contrast, FAST guarantees improved AC performance and specifies that performance over a supply variation of +5.00V ±10% and at temperatures from 0°C to 70°C. Thus the designer no longer needs to derate his propagation delays from the data sheet limits to compensate for speed degradation over the temperature range.

With every advance of this magnitude, there arise new considerations that must be kept in mind both by the system designer and the user setting up test procedures. FAST is no exception, and it is these considerations that will be addressed in this application note. This paper represents an attempt to describe the way the FAST logic parts are specified, why they are specified in the way they are, and how the parts may be tested in the qualification lab and at incoming inspection to verify their performance.

THE FAST DATA SHEET PHILOSOPHY

Philips Semiconductors FAST data sheets have been configured with an eye to quick usability ... they are self contained and should require no reference to other sections for information. The typical propagation delays listed at the top of the page are the average between t_{PLH} and t_{PHL} for the most significant data path through the part. In the case of clocked products, this is sometimes the maximum frequency of operation, but in any event, this number is a 5.00V – 25°C typical specification. The I_{CC} typical current is shown in that same specification block is the average current (in the case of a gate, this will be the average of the I_{CCH} and I_{CCL} currents) at room temperature and V_{CC} = 5.00V. It represents the total current through the package, not the **current through individual functions**.

Other considerations are the Fanout and Loading tables. Some manufacturers relate these numbers in therms of 7400 gate loads ... Philips Semiconductors feels that FAST is unlikely to be mixed with other logic families and so gives the loading factors in terms of FAST unit loads. A FAST unit load is defined to be 0.6mA in the Low state and 20μA in the High state. Thus in the case of the 74F00 gate, the inputs are specified as 1 Ful (FAST unit load) each ... the outputs need a little explanation. The standard FAST output is specified with an I_{OL} sink current of 20mA and an I_{OH} of +1.0mA. Thus the fanout of this gate in the Low state is 20mA/0.6mA or 33 FAST unit loads. In the High state the fanout is 1mA/20μA or 50 FAST unit loads. In each case, the Fanout and Loading Table on the Philips data sheets states the High/Low fanout numbers ... thus the 74F00 output fanout is specified as 50/33 Ful.

ABSOLUTE MAXIMUM RATINGS

The Absolute Maximum Ratings table carries the maximum limits to which the part can be subjected without damaging it ... there is no implication that the part will function at these extreme conditions. Thus, specifications such as the most negative voltage that may be applied to the outputs only guarantees that if less than –0.5V is applied to the output pin, after that voltage is removed the part will still be functional and its useful life will not have been shortened — it is difficult to imagine the meaning of the term "functionality" WHILE that voltage is applied to the output.

Input voltage and output voltage specification in this table reflect the device breakdown voltages in the positive direction (+7.0V) and the effect of the clamping diodes in the negative direction (–0.5V).

RECOMMENDED OPERATING CONDITIONS

The Recommended Operating Conditions table has a dual purpose. In one sense, it sets some environmental conditions (operating free-air temperature), and in another, it sets the conditions under which the limits set forth in the DC Electrical Characteristics table and AC Electrical Characteristics table will be met. Another way of looking at this table is to think of it, not as a set of limits guaranteed by Philips Semiconductors, but as the conditions Philips Semiconductors uses to test the parts and guarantee that they will then meet the limits set forth in the DC and AC Electrical Characteristics tables.

Some care must be used in interpreting the numbers in this table. Philips Semiconductors feels strongly that the specifications set forth in a data sheet should reflect as accurately as possible the operation of the part in an actual system. In particular, the input threshold values of V_{IH} and V_{IL} can be tested by the user with parametric test equipment ... if V_{IH} and V_{IL} are applied to the inputs, the outputs will be at the voltages guaranteed by the DC Electrical Characteristics table providing that there is adequate grounding and the input voltages are free from noise, otherwise a guardbanded V_{IH} and V_{IL} should be used, i.e., 2.5V instead of 2.0V and 0.5V instead of 0.8V. There is a tendency on the part of some users to use V_{IH} and V_{IL} as conditions applied to the inputs to test the part for functionality in a "truth-table exerciser" mode. This frequently causes problems because of the noise present at the test head of automated test equipment. Parametric tests, such as those used for the output levels under the V_{IH} and V_{IL} conditions are done fairly slowly, on the order of milliseconds, and any noise present at the inputs has settled out before the outputs are measured. (This is not the case with clocked or enabled parts and poor or moderate fixturing may induce oscillations or severe ground bounce if noise is present.) But in functionality testing, the outputs are examined much faster, before the noise on the inputs is settled out and the part has assumed its final and correct output state. Since these are unloaded outputs, having faster edge rates, this causes more noise, If the outputs are loaded, the 50pF per output pin can cause substantial ground bounce. Thus V_{IH} and V_{IL} should never be used in testing the functionality of any TTL part including FAST. For these types of tests input voltages of +4.5V and 0.0V should be used for the High and Low states respectively.

In no way does this imply that the devices are noise sensitive in the final system. The use of "hard" Highs and Lows during functional testing is done primarily to (1) reduce the effects of the large amounts of noise typically present at the test heads of automated test equipment with cables that may at times reach several feet and (2) deal with testing parts exhibiting fast edge rates and 50pF per output pin. The situation in a system on a PC board is less severe than in a noisy production environment.

FAST is a trademark of Fairchild Camera and Instrument Corporation.

Testing and specifying FAST logic

AN202

DC ELECTRICAL CHARACTERISTICS

This table reflects the DC limits used by Philips Semiconductors during its testing operations and conducted under the conditions set forth under the Recommended Operating Conditions table. V_{OH}, for example, is guaranteed to be no less than 2.7V when tested with V_{CC} = +4.75V, V_{IH} = 2.0V, V_{IL} = 0.8V, across the temperature range from 0° to 70°C, and with an output current of I_{OH} = −1.0mA. In this table, one sees the heritage of the original junction isolated Schottky family ... V_{OL} = 0.5V at I_{OL} = 20mA. This gives the user a guaranteed worst-case Low state noise immunity of 0.3V. In the High state the noise immunity is 0.7V worst case. Although at first glance it would seem one-sided to have greater noise immunity in the High state than in the Low, this is a useful state of affairs. Because the impedance of an output in the High state is generally much higher than in the Low state, more noise immunity in the High state is needed. This is because the noise source couples noise onto the output connection of the device — that output tries to pull the noise source down by sinking the energy to ground or to V_{CC} depending on the state. The ability of the output to do that is determined by its output impedance. The lower half of the output stage is a very low-impedance transistor which can effectively pull the noise source down. Because of the higher impedance of the upper stage of the output, it is not as effective in shunting the noise energy to V_{CC}, so that an extra 0.4V of noise immunity in the High state compensates for the higher impedance. The result is a nice balance of sink and drive current capabilities with the optimum amount of noise immunity in both states.

I_I, the maximum input current at maximum input voltage, is a measure of the input leakage current at the guaranteed minimum input breakdown voltage of 7.0V. Although some users consider this to be a test of the input breakdown itself, that voltage is typically over 15V. At room temperature, this leakage current should be less than 10μA. (This is not the case with NPN input designated parts.)

Short-Circuit Output Current is a parameter that has appeared on digital data sheets since the inception of integrated circuit logic devices, but the meaning and implications of that **specification** have totally changed. Originally, I_{OS} was an attempt to reassure the user that if a stray oscilloscope probe accidentally shorted an output to ground the device would not be damaged. In this manner, an extremely long time was associated with the I_{OS} test. However, thermally induced malfunctions could occur after several seconds of sustained test. Over a period of time, I_{OS} became a measure of the ability of an output to charge line capacitance. Assume a device is driving a long line and is in the Low state. When the output is switched High, the rise time of the output waveform is limited by the rate at which the line capacitance can be charged to its new state of V_{OH}. At the instant that the output switches, the line capacitance looks like a short to ground. I_{OS} is the current demanded by the capacitive load as the voltage begins to rise and the demand decreases. The full value of I_{OS} need only be supplied for a few hundred microseconds at most, even with 1.0μF of line capacitance tied to the output, a load that is unrealistically high by several orders of magnitude.

The effective of a large I_{OS} surge through the relatively small transistors that make up the upper part of the output stage is not serious, AS LONG AS THAT CURRENT IS LIMITED TO A SHORT DURATION. If the hard short is allowed to remain, the full I_{OS} current will flow through that output state and may cause functional failure or damage to the structure. A test induced failure may occur if the I_{OS} test time is excessive. As long as the I_{OS} condition is very brief, typically 50ms or less with automated test equipment, the local heating does not reach the point where damage or functional failures might occur. As we have already seen, this is considerably longer than the time of the effective current surge that must be supplied by the device in the case of charging line capacitance. The Philips Semiconductors data sheet limits for I_{OS} reflect the conditions that the part will see in the system — full I_{OS} spikes for extremely short periods of time. Problems could occur if slow test equipment or test methods ground an output for too long a time causing functional failure or damage.

AC TESTING

FAST data sheets carry several types of AC information. The AC Characteristics table contains the guaranteed limits when tested under the conditions set forth under the AC Test Circuits and Waveforms. In some cases, the test conditions are further defined by the AC Setup Conditions — this is generally the case with counters and flip-flops where setup and hold times are involved. All of the AC Characteristics are guaranteed with 50pF load capacitances and with the fewest number possible of outputs switching, depending upon the functionality of the device. One of the sets of limits is specified at 25°C and +5.00V V_{CC} — these relate closely to the standard Schottky specification which are under similar conditions but use only 15pF load capacitances. While these numbers are convenient for comparing the two families, keep in mind that using full 50pF loads with the Schottky devices would add several nanoseconds to their propagation delays. These numbers are ideal for checking out test jigs and correlating data since they do not involve temperature or supply voltage spreads. For system design, full specifications are included that include temperature and supply voltage variations — in one case the military ranges and in the other, the commercial ranges.

AC TEST JIGS AND SETUPS

Each FAST data sheet spells out the test circuit used to check AC performance, the waveforms, measurement points, rep rate, test loads, etc., but these are only the quantifiable variables involved in this testing. There is another more complex side to the issue — test jigs and equipment setups.

To get an appreciation for the problems involved in testing FAST, consider these facts. The output rise and fall times on FAST outputs are very sharp. Translating these edge rates into the effective sine wave equivalents generates frequencies on the order of several hundred MHz. At these frequencies, attention to RF phenomena is required.

Because of these RF frequencies, it is necessary to have an AC test jig that has minimal modifying effect on the input and output waveforms. To do this, the jig must be constructed properly. The following items are key in dealing with AC jig construction.

BYPASSING CAPACITORS

Philips Semiconductors uses high quality capacitors that have good RF qualities to decouple the power supply lines on the test jig, right at the V_{CC} pin to the ground plane. Four capacitors with absolute minimum lead length are used. Microwave chip capacitors are recommended. (Note: In some sensitive test environments it is advisable to decouple the V_{CC}, as well as bypass. This is done by passing the V_{CC} through a wire wrapped around a ferrite core 6-8 times. The inductor created helps decouple the noise from V_{CC} and reduces dramatically the tendency for feedback oscillations through the V_{CC} and ground current loop. This is a key problem on clocked parts since the ground bounce created by the fast edge rates and high currents will effect V_{CC} and ground substantially and thereby effect internal thresholds.) These are one each, 10μF dipped tantalum, 0.1μF dipped tantalum or chip, 0.001μF chip and 100pF chip.

GROUNDING

One of the biggest contributors to waveform degradation is improper grounding. In reference to the test jig, the grounding is best done with one or more large ground planes that are directly connected to the ground pin of the test socket. The Philips Semiconductors AC Test Jigs, both DIP and SO styles, are constructed as a four layer PC board with the 2 internal layers as ground planes. Ground planes are also interdigitated between all signal lines to decrease crosstalk. There are holes drilled in these and they are plated through to connect with the internal 2 layers and the top and bottom layers. See Figure 3 to see the interdigitated ground planes on the PCB layout of the SO jig. This grounding scheme has been used with great success in 10k and 100k ECL fixturing. The board is laid out so that the characteristic impedance of the signal lines is 50Ω. This is done by using industry standard stripline techniques. The ground plane also passes down through the center of the part on the bottom side of the board and the ground pin is soldered to it using copper wire to connect the pin and the ground plane. On the top side of the board, the V_{CC} plane goes through the center of the part too, and connects to the V_{CC} pin in like manner as the ground pin. See Figure 1. As the V_{CC} is brought on board, the V_{CC} wire is wrapped around a $^1/_2$ inch ferrite core, 6-8 times, then makes connection with the V_{CC} plane on the top side.

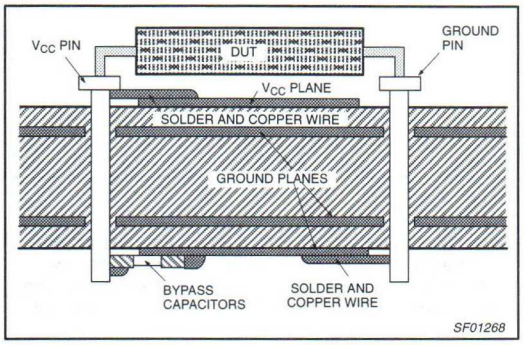


Figure 1.

INTERCONNECTS

The next concern is getting the input signal to the part and the output signal to the measurement system. As stated before, the Philips Semiconductors jig is laid out for a 50Ω characteristic impedance. We recommend that the user maintain a 50Ω environment for the input signal as close as possible to the input pin and then terminate in 50Ω. On our jig, we terminate with a 50Ω chip resistor. The signal is brought on board through an SMB connector to the 50Ω trace on the top side of the board. The signal is terminated by the chip resistor, R3, see Figure 2a and 2b. the signal proceeds to the DUT pin, a distance of about 0.5 inches, through Jumper 1 (in the Input Only position), and the rest of the trace. The same pin on the opposite side of the board has a 450Ω chip resistor soldered to it. The other side of this resistor, R1, is soldered to a 50Ω trace on the bottom side of the board that runs to an SMB connector on the edge of the jig. This connects to the 50Ω input of the Sampling Oscilloscope. This 450Ω resistor in series with the 50Ω input of the scope creates a 10X divided 500Ω probe for the scope and provides impedance matching for the scope. See Figure 2b. This circuit also doubles as the resistive portion of the FAST AC Output Load and thereby allows the output to be sensed in the same fashion. When the input is not used for a signal or generator input, the line may be switched to one of three voltage sources, $V_S1 - V_S3$, by use of a DIP switch on each pin. It may also be left open and the 50Ω pull-down resistor that is used for an input terminator pulls the line to ground and can be used as a hard low level. See Figure 2b. This scheme eliminates excessive cabling to each input to provide static input levels and thereby reduces parasitic inductances and cross-talk. It also eliminates the need for bulky and sometimes unreliable high impedance probes by using the 50Ω input of the Sampling Scope. With the designed-in flexibility of Jumper 1 and Jumper 2, and the selectable nature of V_{CC} and Ground pin designations, one can configure this board for any V_{CC} and Ground pin designations, select which pins are outputs or inputs and even provide the proper pull-up for 3-State outputs. This makes the board entirely universal for designated V_{CC}/Ground configurations. To explain this, the output of the device is connected to its capacitive load by Jumper 1 in the Output Only position. This means that no pin can be both output and input at the same time, but can be either. Jumper 2 allows an output to be connected to the 3-State pull-up resistor, R2, and have that connected to the needed 7V. See Figure 2a and 2b. The scope is connected in the same way as the input, with the 450Ω resistor and the 50Ω of the scope comprising the 500Ω needed for the FAST load. One other consideration exists. In small part quantity testing, the elimination of a socket is very desirable, using inserted pins that are flush with the jig. In larger quantity testing, sockets may be needed, however. If this is the case, some degradation in the performance will occur due to the increased lead inductance for each pin, which is observable, and the addition of group delay through the socket may alter or affect the readings obtained.

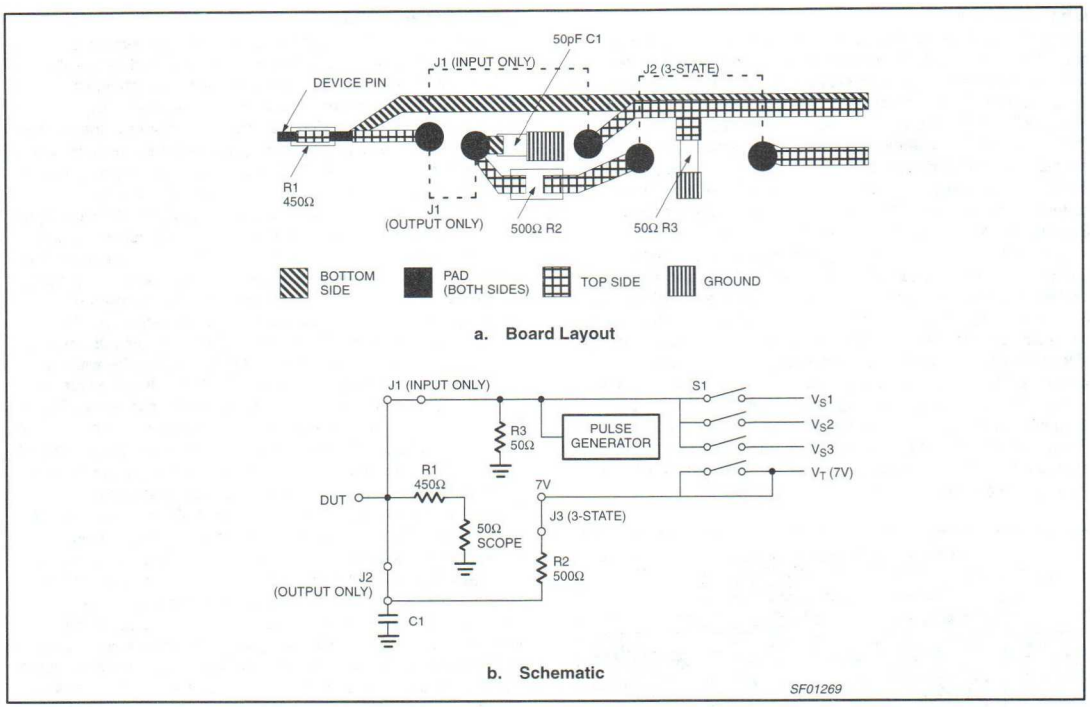


Figure 2. FAST AC Test Fixture

HIGH-FREQUENCY DESIGN

The exact jig delay time is determined by the size of the universal jig that is being used. It is important to know that the frequency response of the jig must be High to prevent any delay factor from varying with the edge rates. The frequency response of the jig indicates how constant the impedance remains over frequency. The characteristics impedance of a transmission line is expressed as:

$$Z_O = \frac{V}{I} = \sqrt{\frac{L_O}{C_O}}$$

Where L_O is the inductance per unit length, C_O is the capacitance per unit length, Z_O is in Ohms, L_O in Henrys, and C_O in Farads. Propagation velocity and its inverse, delay per unit length d, are also expressed in L_O and C_O ...

$$V = \frac{1}{\sqrt{L_O C_O}} \qquad \delta = \sqrt{L_O C_O}$$

where δ is expressed in nanoseconds, L_O is in microhenrys per unit length, and C_O in microfarads per unit length. From this, it is clear that if the Z_O changes over frequency, then the delay per unit length will vary as well. Therefore, it is imperative to know how the jig responds over frequency and that all measurement line lengths are identical.

Frequency response also depends on the phase as well as the magnitude of the impedance. If the phase changes so does the delay, since delay is the derivative of phase change with frequency. An S-parameter analysis is needed in evaluating jig performance.

UNIVERSAL JIG CONSTRUCTION

Jig universality is with respect to chip pin count and V_{CC} and ground pin placements and as such, separate universal test jigs are built for 14, 16, 20, 24, and 28 pin parts.

An S-parameter analysis was performed in a network analyzer to optimize the jig layout. This assured that the jig had a flat frequency response over the spectrum of interest for FAST products. Figure 2b shows the schematic of the fixture and Figure 2a shows a drawing of the board layout, component placement and signal paths. The equipment used to analyze the jigs and loads was: HP8505A Network Analyzer, HP8503A S-Parameter Test Set and HP8501A Storage Normalizer. In some measurements the equipment was driven by an HP9845B desk-top computer.

Jigs produced in this way should have minimal lead length to reduce the characteristic inductance. This in turn minimizes reflections with their accompanying waveform distortions. and measurement inaccuracies.

AC TEST LOADS FOR THE PHILIPS SEMICONDUCTORS JIG

As stated previously, the Network Analyzer was also used to design and optimize AC test loads to be used with the universal jig. FAST product loads require 50pF load capacitance and 500Ω resistance to ground.

Philips Semiconductors meets the 50pF requirement through the use of a 45pF load, 4pF jig capacitance, and 3pF probe capacitance. The result, 52pF, is slightly more stringent than required.

A few words about load capacitors are in order. All capacitors have an associated inductance. Due to this inductance, a capacitor will form a series resonant circuit at some frequency. For single 50pF capacitors, this typically occurs between 200 and 600MHz depending on the type of capacitor. Above this resonant frequency, the capacitor has inductive characteristics and does not present a capacitive load. this is very important with FAST because harmonics due to the sharp edge transition rates occur at 600MHz and above.

The Philips Semiconductors FAST loads solve this problem by reducing the load capacitor lead inductance by paralleling three 15pF chip capacitors. The resulting load is 45pF. At the same time, since smaller value caps are used to build up the capacitive load, the associated series resonant point is above 1.2GHz.

The load resistors are 1/8W selected 510Ω ± 10Ω chip resistors.

The entire load assembly is constructed on the jig PCB along with the input termination, and the jumpers which select an input or output path. The load circuit is detailed on the FAST data sheets for 3-State parts.

CORRELATION

While numerous ATE systems are available and are very efficient, it is imperative that the ATE correlate to a user's bench setup. Since the Philips Semiconductors FAST parts are all characterized on the setup described in this note, it is just as important that the user's bench jigs meet the same performance criteria. Without similar jigs, it will be very difficult to correlate AC data.

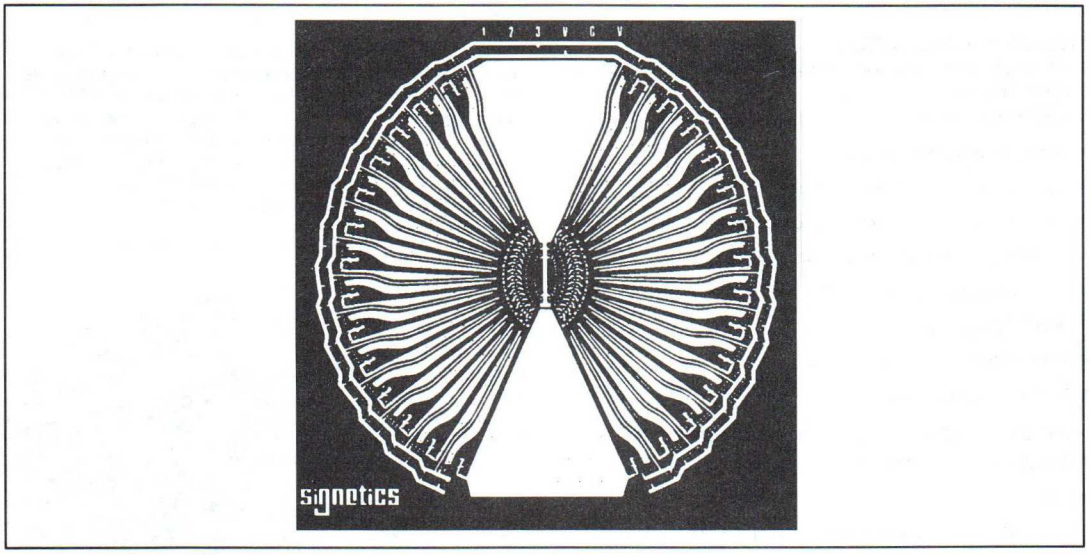


Figure 3.

Test fixtures for high speed logic

AN203

INTRODUCTION

The Philips Semiconductors Logic Product Group (LPG) operates a Characterization Laboratory in Albuquerque, New Mexico. This Lab maintains the capability of testing the 11 logic product families the Group supports. These include: BiCMOS ABT, ABTH, LVT, ALVT, FAST-74FXXX, ALS-74ALSXXX, High-Speed CMOS-74HCXXX, High-Speed CMOS/TTL-74HCTXXX, Advanced CMOS/TTL.

Due to the great diversity of product families and the different testing requirements and complexity of the product types of each family, Philips Semiconductors LPG Characterization has designed and built a bench test AC fixture that is specifically designed to address to only the High-speed logic families. It has the advantages of being very versatile, has high bandwidth capability (≥750MHz), is 50Ω system compatible, and is manually programmable for the input static voltages. This provides the ability to have one fixture that addresses many product types across families. The extent of this versatility is explained in the following Application Note. The families that this fixture is intended to support are: FAST, ALS, ABT, LVT, ALVT (Note: This fixture is compatible with any 500Ω pull-down load.).

THEORY OF OPERATION

There are several key points in testing the faster edge-rate logic families. They are:

- Very good bypassing and decoupling (they are different).
- Large ground and V_{CC} planes
- Low-impedance signal lines (i.e., 50Ω)
- Signal lines that are uniform in impedance over frequency
- Signal lines must have high bandwidth (>500MHz)
- Low-inductance paths for the DUT leads, including V_{CC} and GND
- Output AC load close to the DUT
- Measurement point close to the DUT
- Avoidance of ground loops (especially on inputs at DC levels)

Also of concern to the test engineer and the manager are:

- Versatility and/or ease of use (there are tradeoffs)
- Cost
- The number of fixtures needed to support products

Each of these concerns have merit and must be understood by the user of these logic families if valid and correlatable results are to be found.

V_{CC} and GND

The secret in V_{CC} and GND use in fixturing is to do the things that reduce the noise that can: 1) get to your part, and 2) come from your part. This is done by reducing the noise of the V_{CC} as it arrives to the fixture, by judicious application of frequency dependant bypassing at the DUT V_{CC} pin to GND and reducing inductance from the V_{CC} and GND pins of the DUT to the point where good contact of the bypassing and V_{CC} and GND planes occur. All of these are techniques used in good RF and microwave board design. By reducing parasitic inductances and cleaning up any sources of noise, good signal integrity is better maintained.

These points are evident in the fixture Philips Semiconductors has designed. Part of the noise reduction of the power supply as it arrives is done by bypassing the power supply at its terminals. The power is then brought to the fixture via banana cables, (as short as possible), to jacks on the chassis of the fixture. An 18 gauge wire, attached to the jack, is wrapped through an inch ferric core 8-12 times for decoupling of any spikes. (Details of the cores used are included in the parts list.) This acts as a Low-pass filter. The wire is then soldered to the bottom of the PC board onto the large V_{CC} plane that narrows to the V_{CC} bus running between the pins of the DUT. See Figures 1, 2, and 3 for detail.

Triangle-shaped, the V_{CC} plane provides a Low inductive path for the V_{CC} to the DUT pin. See Figures 2 and 3 for the board layouts. The V_{CC} bus from this plane travels down between the DUT pins to that connection. This is so connection to the V_{CC} bus is easy and very short. The DUT may have V_{CC} located on any pin with this configuration. The pin is connected to the V_{CC} bus by soldering small copper braid or similar Low-inductance wire capable of carrying the current for the device, see Figure 4.

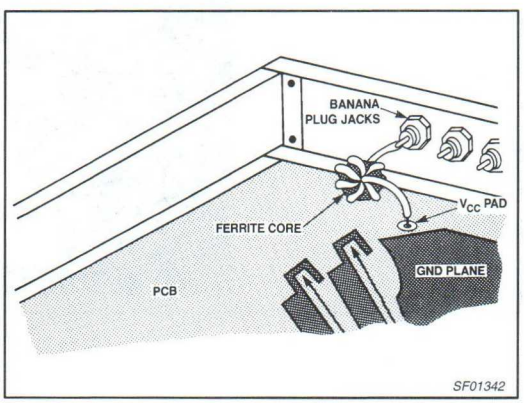


Figure 1. Underside View of PCB Fixture Ferrite Core Placement

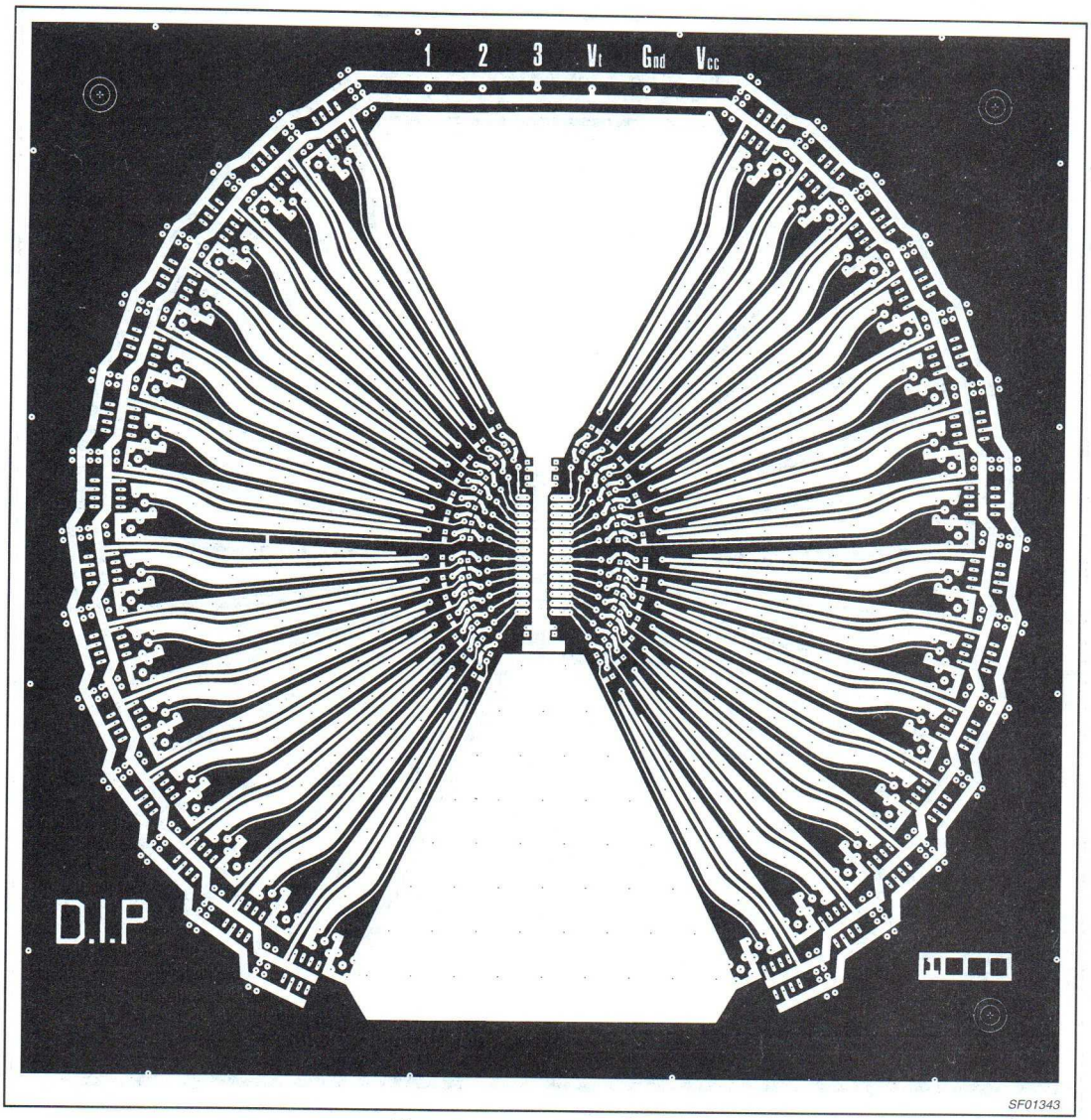


Figure 2. Board Layout — Top Side

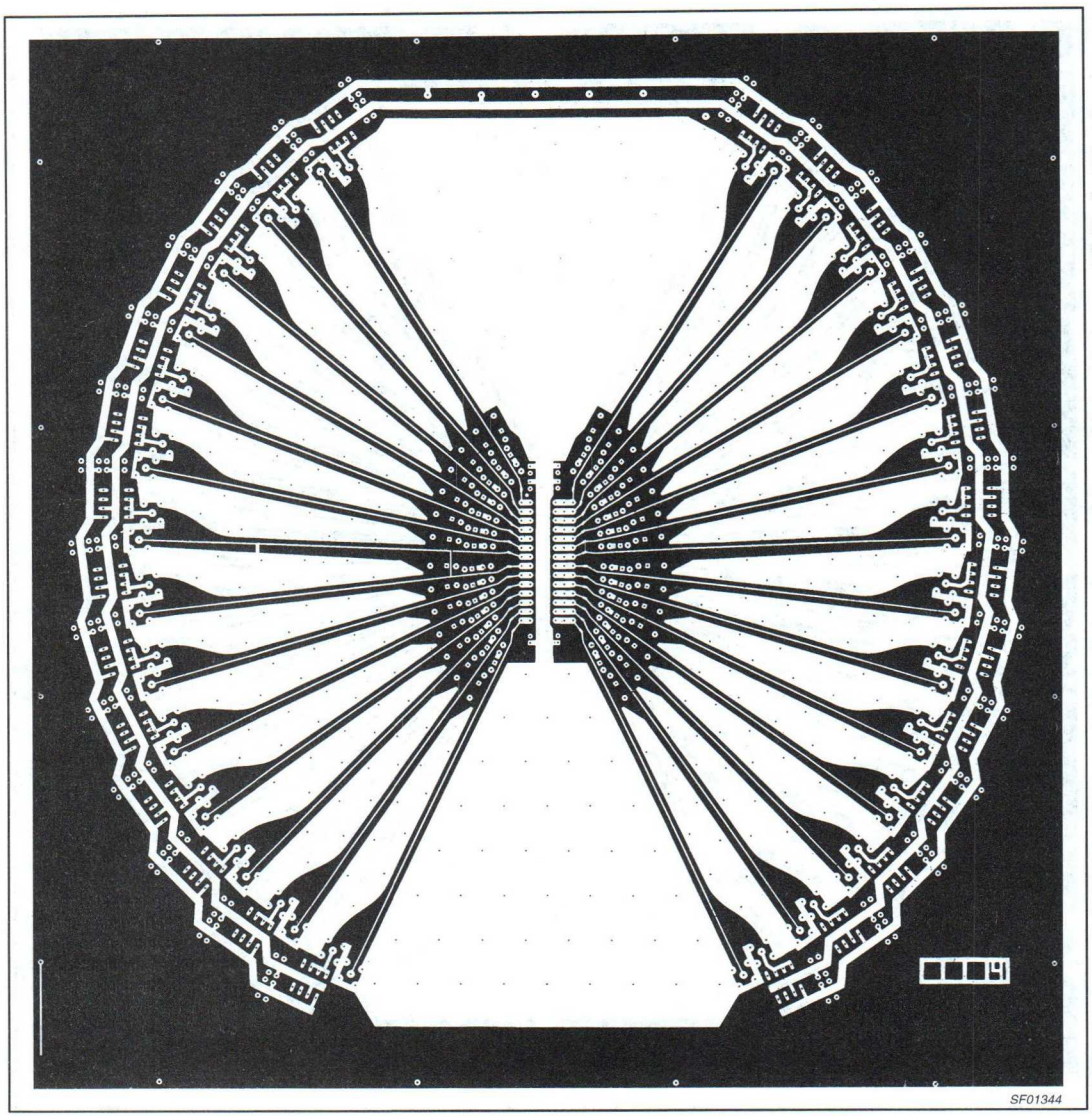


Figure 3. Board Layout — Bottom Side

On the opposite side of the top layer of the board is a triangle-shaped ground plane. Ground planes are also located on the bottom layer of the board in the same places as the V_{CC} and ground planes of the top layer. Since this fixture is laid out for 50Ω stripline, layers 2 and 3 are almost total ground plane, with holes in them for feed-throughs and components. Also found between the signal lines, on the top and bottom layers, are ground plane "fingers" that are connected to all 4 layers by plated-through holes. This provides good separation of the signal lines resulting in lower cross-talk.

The bottom layer ground plane consists of two triangle-shaped planes connected by a bus strip that runs between the DUT pins. This was done for 3 reasons: First, this allows connection of any ground pin of the DUT to the ground, regardless of location; like the V_{CC} connection on the top layer. Second, it allows the connection of the bypass capacitors from the V_{CC} pin to the ground with the shortest possible lead length. Characterization uses typically 2 or 3 ceramic chip capacitors and 1 or 2 dipped tantalum capacitors (35V) to bypass the V_{CC} pin. It is important to keep the dipped tantalum capacitor's leads as short as possible to reduce series inductance.

The recommended values of capacitors are: 100pF, 0.01μF, 0.1μF. and 10μF. We have found at times, the need to adjust these values depending upon the product type and its performance. Some noise sensitive circuits need more bypassing in the lower and extreme higher values of capacitance. And third, the connection of the two planes eliminates possible ground loops and the feed-throughs create a ground mesh and give an excellent ground plane for the circuit. Figure 4 illustrates the bypass connections.

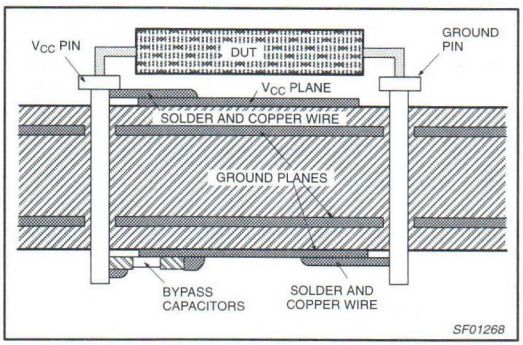


Figure 4. Decoupling Connections

BYPASS AND DECOUPLING

It is important to understand the difference between decoupling, as with the ferrite core, and bypassing, as with capacitors. Decoupling occurs as High-frequency signals are removed by saturation of the ferrite core. This prevents "noise" that may be on the V_{CC} power supply from getting on the V_{CC} plane. The action of the bypassing capacitors is to: 1) "pass" any non-DC signals that occur on the V_{CC} (due to the part's operation) to ground, and 2) be able to provide the "instantaneous" current demands of the part as it switches.

The various values of capacitors are intended to provide a Low-impedance path at all operating frequencies. Since real-world capacitors have resonance points at a given frequency, depending upon their value and type of capacitor (and actually turn inductive above the resonance point), using different values that have different resonance points allows an across-frequency Low-impedance path for V_{CC} noise.

An important point in the use of bypass capacitors is the minimization of lead length. Lead length represents inductance; inductance in series with the capacitance. If it is too much, it can cause resonance and oscillation problems with the part and/or power supplies and nullify the benefit of the capacitors. It also plays a major part in inhibiting the effect of the "instantaneous" current response needed by the part from the bypass capacitors. It actually can cause the ground of the device to track the change in current to the degree of the lead inductance. The lower the inductance, the lower the "ground bounce" effect. Hence, short or no lead lengths on capacitors are needed to help prevent the effects of ground bounce.

SIGNAL LINES

A signal line is defined as a line that carries the input stimulus, either DC or AC, or output response, to or from the device. Since these signals are measured and determine the data which characterizes the part, it is critical that they are of the highest integrity and represent, as far as physically possible, the action of the part; not the nuances of the fixture. To achieve this, the line must not be able to change the signal over the measurable frequencies of the device, nor affect the delay of the part.

The fixture as designed, has 50Ω signal lines determined by a stripline layout method. The 50Ω value was selected for several reasons:

1. The 50Ω value matches impedance with the pulse generators that are used as input stimulus.
2. The output loads specified for this fixture are either a 500Ω pull-down or a 50Ω pull-down (ECL), in parallel with a capacitive load. This allows the 50Ω signal line to be terminated into this load for either a 10:1 or a 1:1 match.
3. A Low-impedance line will have better characteristics with regards to cross-talk and resisting external noise.

There are two types of signal lines on this fixture: input and output; both of which are 50Ω transmission lines. The input line is on the top side of the board and is always terminated in 50Ω. It is connected to the DUT via a 0.3″ jumper, Jumper #1 for input. When this jumper is installed, the DUT pin is available only as an input. To allow this line to be used as an output, a 0.1″ jumper, Jumper #1 for output, is used instead of the 0.3″ jumper. This connects the DUT pin to the AC load when the DUP pin is an output. See Figure 6.

The output signal line can be dedicated two different ways. The first method, used for ECL, is to leave shorted the 50Ω trace and have it run directly into the SMB connector into the 50Ω sampling system. The second method is to cut the trace at the DUT pin and solder the 450Ω chip resistor, R1, across the cut. This, combined with the 50Ω scope, then appears to the part as either a 500Ω probe for the input signal or the 500Ω output AC load for the output signal.

The signal lines are equal length and therefore do not introduce any extraneous delay from pin to pin. We also characterized the impedance of the lines over frequency to ensure minimal distortion over the frequency range and any effective change in propagation delay caused by the relationship of inductance and group delay, see Application Note AN202. Figure 5 illustrates the frequency response of the signal lines in impedance.

This is considered to be high bandwidth and encompasses the frequency range exhibited by ALS, ACL, ECL, and FAST logic families.

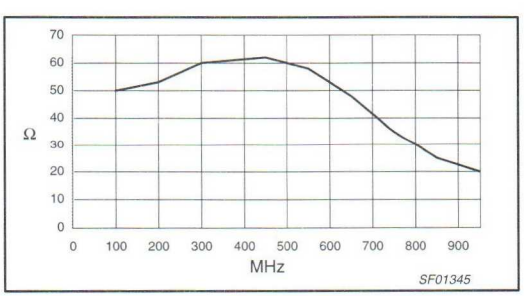


Figure 5. Signal Line Frequency Response

LOADING

The explanation of the two types of AC loads that may be used will be covered in two parts. First the ALS, ACL, and FAST implementation will be discussed, then the ECL implementation.

ALS and FAST Implementation

The FAST and ALS product families AC load is specified as a 50pF capacitor and a 500Ω resistor in parallel. This load has the advantage of being adaptable to both a High-impedance (A.T. E.) or a Low-impedance (bench) measurement environment. The Philips Semiconductors fixture uses a Low-impedance environment primarily for two reasons. The first reason is that experience of the last 5 years has told us that High-impedance present a reliability concern and can introduce hard to detect errors into the waveform.

The second reason being that most suppliers of these technologies provide data based upon the Low-impedance approach and most large users of these products do so as well. This also allows the fixture to be used for ECL testing since that product uses a totally 50Ω environment. Figure 6 illustrates how this test fixture implements the 50pF/500Ω load schematically.

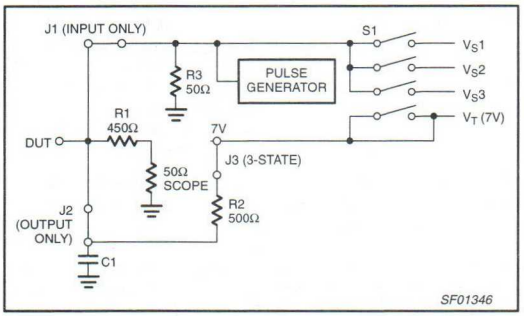


Figure 6. PCB Fixture Schematic

The fixture was laid out to present the load as close as possible to the device, and yet allow for flexibility in deciding if a certain pin is an output or an input. This distance is critical due to its inductive effect upon ground bounce phenomena. It is acknowledged here that a fixture dedicated to a single device type without jumpers, and therefore placing the load virtually on the pin of the device, would show the ground bounce phenomena for simultaneous switching to be less than that of this fixture. However, this fixture can be so dedicated by not using the pads as provided, but rather by using the ground bus, like the bypass capacitors used. The flexibility of this fixture substantially reduces the cost of fixturing for these families. Studies on simultaneous switching with this fixture have shown dramatically favorable results to previous fixtures. Those studies continue. For work other than that of simultaneous switching, there will be no appreciable difference with a dedicated fixture.

As illustrated in Figure 7, the load is shared with the 50Ω input of the measurement system; a 50Ω sampling oscilloscope. The 450Ω resistor: R1, is soldered to the socket pin of the device and is in series with the 50Ω input of the scope. Figure 7 illustrates this on the board layout of one input/output pin. This allows virtually a probe tip on the device pin. The load capacitor: C1, is a 33pF ceramic chip capacitor. This is added to the measured value of 17pF of board capacitance, achieving the 50pF value specified for the load. The distance from the pin to the capacitor is 0.5 inches and is adequate for the testing of these product families.

For testing 3-State parameters, the 500Ω resistor: R2, is connected to it's pull-up supply. V_t via a 0.3″ jumper: Jumper #2. The V_t supply is bussed to each pin and may or may not be connected with that jumper. See Figures 6 and 7.

Input Stimulus and Measurement

When the input is not used for a signal input, the line may be switched to one of three voltage sources: V_{S-1} through V_{S-3}, by the use of a DIP switch on each pin. It may also be left open and then the 50Ω pull-down resistor: R1, pulls the line to ground and can be used as a hard low level. See Figure 6. These voltage levels are brought in from external supplies through banana connectors like V_{CC}. This scheme eliminates excessive cabling to each input to provide the static input levels and thereby reduces parasitic inductances and cross-talk. Each of the 3 busses and the V_t bus all have places for bypass capacitors in the event of noise on the static levels. Figure 8 illustrates the DIP switch and SMB connectors and how they control the input stimulus and output measurement.

As stated previously, the measurements are made with 50Ω sampling systems. The connections to these systems are made via SMB connectors. This was chosen since it is compatible with SMC; it is push-on, it is small for easy configuration, and it is capable of high bandwidth operation. Figure 8 illustrates where the connections are made, where the pulse generators connect to the input and an SMB connector. Since the 450Ω resistor: R1, is soldered directly to the pin of the device, the actual probe tip is at that point. See Figure 7. This has the advantage of eliminating any distance from the device to the probe tip, thus guaranteeing accurate results.

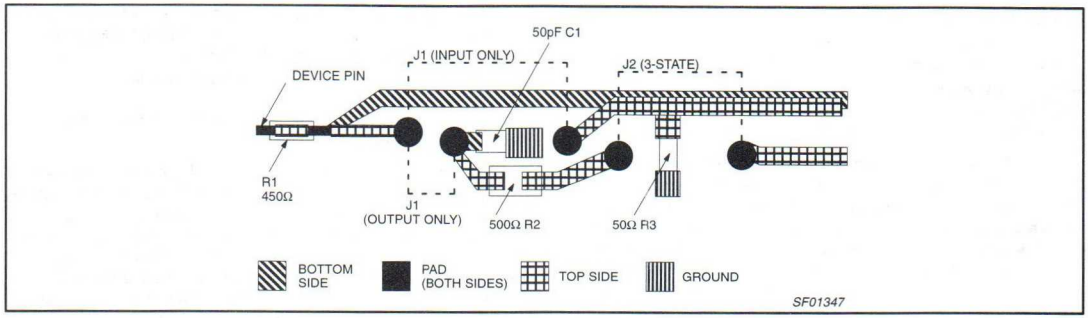


Figure 7. Fixture — Board

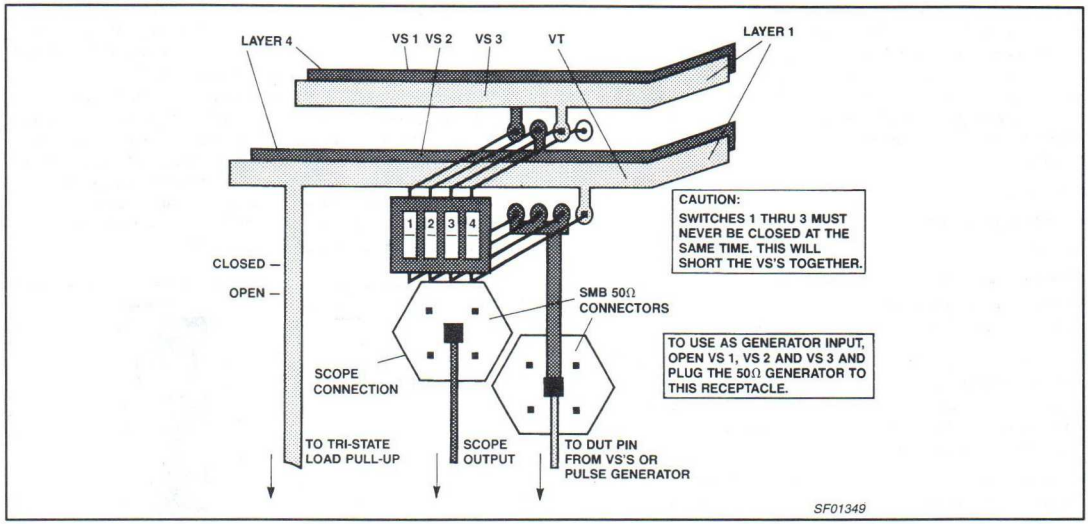


Figure 8. DIP Switch Connection for V_{S-1}, V_{S-2}, V_{S-3}, and V_T and the SMB Connectors for Input Signals and Output Measurement

Versatility and Cost

At some point, there is a choice between the most technically attractive options and the cost of options. This fixture has been primarily designed to optimize the cost effectiveness of test fixturing yet yielding a technically sound tool. To do this, a compromise has been made between the ease of use and the versatility.

In the construction of the fixture, a choice is made as to where the V_{CC} and GND pins are to be located. This then dedicates this particular fixture to part types with this V_{CC} and GND configurations. This is also done with a dedicated fixture. However, on a dedicated fixture, the pins are individually constructed to be either an input or an output, and in so doing, the fixture is usable for 1-to-4 devices. The Philips Semiconductors fixture, once dedicated to a particular V_{CC} and GND configuration, is built up to have both input and output components on all signal pins. The selection of which pin is an output or an input is made by inserting the appropriate jumper, See Figures 5 and 6. The same applies in doing 3-State testing. The tradeoff here is that it would probably take less time to setup the dedicated fixture than the Philips Semiconductors fixture. To help compensate for that tradeoff, we have the three Vs supplies that may be switched into any pin to provide input static levels and eliminate the need to bus input High or Low levels by external cabling. For the user that means the only connections being made to the fixture are:

- The V_{CC} (banana jack)
- The (GND) (banana jack): this is the common ground of all input supplies.
- The V_{S-1}, V_{S-2}, and V_{S-3} supplies (banana jack): these may be any voltage and are switchable. Philips Semiconductors connects programmable supplies to these connectors.
- The V_T supply (banana jack): this is the 3-State pull-up voltage and is permanently connected to the bus to each pin. It is selectable by Jumper #2, see Figures 6 and 7. For FAST and ALS products this is 7V. For ACL products this is $V_{CC\times2}$ and it is not used for ECL applications.
- Input Stimulus (inside SMB connector: this is found on every input/output pin. More than one pin may be used in this manner.

  CAUTION: When using this connector as an input stimulus, make sure V_{S-1}–V_{S-3} are disconnected. This will short the power supplies to the generator if they are not disconnected.
- Output Measurement or Scope Connection (outside SMB connector: this is also found on every input/output pin. More than one pin may be used in this manner. Remember, if this pin is not connected to a scope and is an output, a 50Ω resistor must be connected here to ground to complete the 50Ω resistive load. Philips Semiconductors has constructed 50Ω load by soldering a high-quality (High-frequency) 50Ω resistor inside a female SMB cable connector. See Figure 9.

  CAUTION: V_S 1.2 and 3 are all on the same DIP switch. Since they connect to the same bus per pin, **ONLY ONE SUPPLY MAY BE CONNECTED AT ONE TIME**, Otherwise, this will result in a short between power supplies connected.

With these 6 connections, the fixture is capable of testing the product lines as mentioned.

The cost of this fixture ranges from 550 per fixture, dedicated to a 20-pin device in quantities of 1-10, to as low as 385 per fixture of the same type in quantities over 100. This is not substantially higher than the cost of a dedicated fixture; which is estimated at 200- 500. The factor to consider would be the quantity of fixtures for the number of products to be tested. To have a dedicated fixture for every 2-3 product types versus a "universal" test fixture for 20-30 product types is worth considering from a cost standpoint.

Included in Appendix 1 is the parts list for this fixture and the supplies used by Philips Semiconductors. This in no way constitutes Philips Semiconductors endorsements of these suppliers and the customer may select their own supplier if they so desire. This fixture is offered to the public to duplicate and use within their own environments. Philips Semiconductors will not provide any materials but will allow the manufacturers of the board and materials to build and/or supply for any requesting party. Pricing and availability are left to the vendors and Philips Semiconductors has no control over those issues. The intent is to provide something for users of High-speed logic that has been proven and tested in a true High-speed use, and provide a characterization of these products prior to their introduction to the market place.

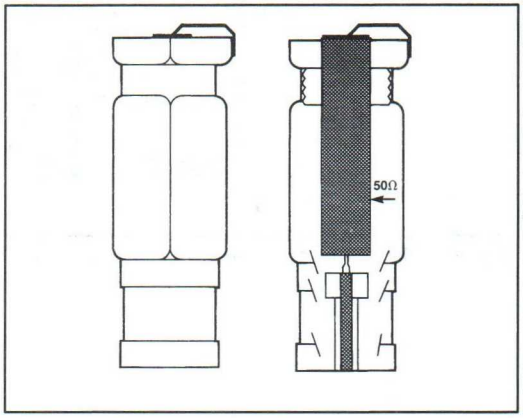


Figure 9. 50Ω Load Resistors Using Output Pin SMB Cable Connectors

APPENDIX 1 — COMPONENT AND VENDOR LIST

The following prices are quoted for a 30 piece build of a 24 pin test fixture and are not binding in any way.

COMPONENT AND VENDOR LIST

ITEM		PART TYPE		REQUIREMENT	SUPPLIER
Printed circuit motherboard	SO and SOL	#SD8512.28		1 part per configuration	
	DIP	#SD8512.31			
SO and SOL sockets (SOIC through hole socket)		14 pin	001-014	1 part per board	Surface Mount Devices, Inc. PO Box 16818 Stamford, CT 06903 (203) 322-8290
		16 pin	001-016		
		16L pin	001-116		
		20 pin	001-120		
		24 pin	001-124		
		28 pin	001-128		
Socket terminal pins	For DIP boards	LSG-1AG14-1		Number of pins equal to the part pin count times by (7) seven. 24 × 7 = 160 × .20=	
	For SO and SOL boards			Number of pins equal to the part pin count times by (5) five. 24 × 5 = 120 × .20=	
Shorting blocks (jumper)		0.3 inch	8136-475G1	1 part per pin cost per part × 24 =	Augat
		0.2 inch	8136-651P2		
Chip resistor		50 Ω 1%	CRCW 1210	1 part per pin cost per part × 24 =	Dale Electronics, Inc. 2300 Riverside Blvd. Norfolk, NE, 68701 (402) 371-0080
		450 Ω 1%	CRCW 1206		
		500 Ω 1%	CRCW 1206		
Chip capacitor (ceramic)		33 pF	500R15N330JP	1 part per pin	Johanson Dielectric
		15 pF	500R15N150JP4	1 part per board cost per part × 1 =	
		0.015µF	500S41W103P4		
		0.1µF	500S41W104P4		
Dip Tantalum capacitor		10 µF	106k025NLF	1 part per board cost per part × 1 =	Mallory
		47 µF	476k020WLG		
Ferrite core			T80-1	1 part per board cost per part × 1 =	Amidon Associates 12033 Otsego Street North Hollywood, CA 91607 (818) 760-4429
Mounting screw		4-40 × 1/4 Philips pan head machine screw		16 parts per board cost per part × 16 =	Bonneville Industry Supply Co. 40 So. 1500 W., Orem, UT (801) 225-7770
Banana plug jack		H.H. Smith type, White	1509-101 (order code: 28F1178)	6/board-color your choice cost per part × 6 =	Newark Electronics
		H.H. Smith type, Red	1509-102 (order code: 35F870)		
		H.H. Smith type, black	1509-103 (order code: 35F869)		
		H.H. Smith type, green	1509-104 (order code: 28F1179)		
		H.H. Smith type, blue	1509-105 (order code: 28F1180)		
		H.H. Smith type, yellow	1509-107 (order code: 28F1182)		

COMPONENT AND VENDOR LIST (continued)

ITEM	PART TYPE		REQUIREMENT	SUPPLIER
Switch	4-bit side actuated piano-dip	76PSB04	1 part per pin cost per part × 1 =	Grayhill Co.
Connectors	Snap on SMD	51-051-0000-220, straight jack receptacle	2 parts per pin cost per part × 48 =	Sealectro
Mounting frame	Philips Semiconductors number CB-10		1 per test fixture	Electronic Chassis Corp. 468 North 1200 West Lindon, Utah 84062 (801) 785-9113
Hookup wire	No. 18/20 gauge Teflon coated		24 inches per test fixture	

The following components may be needed in use of the test fixtures but are not part of the test fixtures

61-001-0000-89	50Ω terminator plug
51-007-0000	Straight Cable Clamp Type
51-083-0000-222	"T" adaptor J-J-J
51-085-0000	"T" adaptor J-P-J
51-072-0000	Adaptor J-J
51-073-0000	Adaptor P-P
51-001-0020	Shorting plug
61-002-0000-89	50Ω terminator jack

Supplier:

APPENDIX II — CONSTRUCTION HINTS

A suggested order of assembly is as follows:

1. Cut traces for 450 ohm resistor. (Not needed for ECL).
2. Install SMB connectors. Note: Elevate base from board 0.05".
3. Install DIP switches. Note: Numbers on switches may not correlate to Vs supply numbers.
4. Install Augat socket pin.
5. Install load/termination resistors and capacitors.
6. Strap V_{CC} and GND pins to appropriate bus strips.
7. Install bypass capacitors.
8. Clean flux off of board and components.
9. Check for lead to frame shorts on PLCC board. (Not discussed in App note).
10. Install banana jacks on frame.
11. Attach board to frame with 1/4 Philips pan head machine screws.
12. Wrap wire 8-12 times around ferrite core. Leave enough wire to connect to frame and board. See Figure 1.
13. Connect V_{CC}, GND, and voltage supplies from banana jacks to board.
14. Remove all remaining flux. Keep "flus-off" from banana jacks.

Hints on construction:

- A 0.05" shim that fits under the SMB connector base helps elevate it during construction.
- Mount the SMB connector with flat side out rather than point side out. See Figure 8.
- Solder Augat socket pins in with a part inserted to hold the pins steady.
- "Piano DIP" switches have the numbers reversed from the board notation. Taping a new number on the board designations will help match the switches.
- Hints for solder chip components: apply a small amount of solder on one side of the pads on the board.
- Keep DIP switches and SMB connectors spaced as far away from each other as the holes permit, i.e., push the SMBs in and the DIP switches out.

Package lead inductance considerations in high-speed applications

AN212

Authors: Stephen C. Hinkle, Jeffrey A. West

INTRODUCTION

A circuits become faster, more concern needs to be focused on packaging and interconnects in order to fully utilize device performance. One area of concern is with the package leads between the chip and the board environment. The current flowing into or out of an integrated circuit is conducted through a lead frame trace and bonding wire connecting the integrated circuit to outside circuitry. these leads are circuit elements, inductors, and have a definite effect on the circuit performance because they generate noise in high-speed applications.

Inductance is the measure of change in the magnetic field surrounding a conductor resulting form the variation of the current flowing through the conductor. The change in current through the inductor induces a counter electromotive force, EMF, which opposes that change in current.

An example is a buffer driver discharging a 50pF load. At a switching rate of about 3V in 2ns, the current generated by discharging that capacitor at that rate is:

$$I = C\frac{dV}{dt} \simeq 50pF \cdot \frac{3v}{2ns} = 75mA.$$

All this current flows through the ground lead of the package. Changing the current through this lead generates a ground lead voltage or ground bounce. A typical lead inductance has been measured to be about 10nH. Switching 75mA through a ground lead with an inductive value of 10nH causes a ground bounce of about:

$$V = L\frac{dI}{dt} \simeq 10nH \cdot \frac{75mA}{1ns} = 750mV.$$

Figure 1 illustrates the current surge and ground bounce during switching. This was modeled using the equations:

$$V(t) = \frac{3V}{1 + E^{(t-t_O)/K}}$$

$$I_C(t) = C\frac{dV(t)}{dt}$$

$$V_L(t) = L\frac{dI_C(t)}{dt} = LC\frac{D^2V(t)}{dt^2}$$

If more than one output is switched at a time, this ground bounce can get very large. Changing the ground reference on the chip can have significant effects on circuit performance. A V_{CC} bounce can also be calculated when the 50pF load capacitors are being charged and can also have serious effects on circuit performance.

Some of the problems caused by package lead inductance are:

1. Adding delay through buffer parts
2. Changing the state of flip-flop parts
3. Output glitching on unswitched outputs
4. Circuit oscillations.

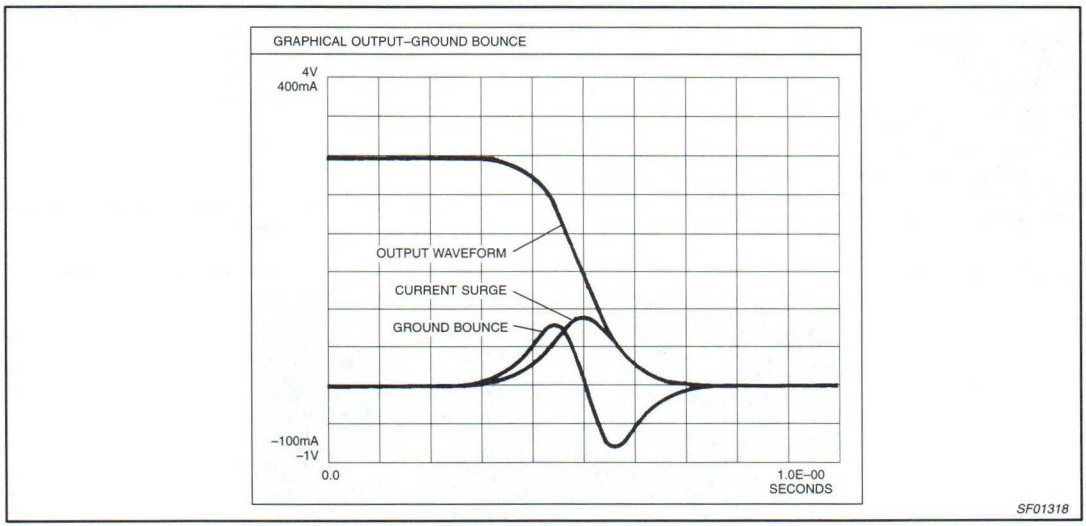


Figure 1.

Package lead inductance considerations in high-speed applications

AN212

GENERAL PROBLEMS ASSOCIATED WITH GROUND BOUNCE IN HIGH-SPEED CIRCUITS

Adding Delay Through Buffer Parts

Delay through a buffer part is not only a function of the gate itself but is also a function of how many gates in the package are switching at once. Switching more than one output at a time adds to the current being forced through the ground lead of the package. the ground potential seen by the chip rises because of the lead inductance. This rise in ground potential raises the threshold of the gate and tends to turn the gate back OFF slowing the discharge rate of the load capacitor. The gate does not finish switching until the ground bounce settles out.

Figure 2 shows an example of a buffer connected to a test load. Probing on the ground pad, V_G, shows the effect ground lead inductance has on the ground pad potential.

Figures 3 and 4 show the ground and V_{CC} bounce during switching on a 74F240 Buffer. The effect of ground bounce on this part is to slow the propagation delays from 3ns with only one output switching to 5ns with all 8 outputs switching at once. AC specifications are usually generated with only one gate switching at a time. For example, the 74F240 t_{PHL} limits are 2.0ns minimum, 3.5ns typical and 4.7ns maximum. Therefore, when using AC specifications based on single gate switching, a derating factor for multiple switching should be used. A derating factor of 250 to 300ps per output switching has been suggested as a reasonable number and some customers are using this i their internal specifications.

Integrated Circuits Containing Flip-Flops

Integrated circuits containing flip-flops might be seriously affected by inductive ground bounce because of the possibility of the flip-flops changing states. To explore this effect, the 74F374, and Octal D-type Flip-Flop, was analyzed by comparing test results from the conventional corner mount V_{CC} and ground package to that of a side mount V_{CC} and ground version. A test setup as used where alternate 1's and 0's were clocked into seven of the eight flip-flops to obtain simultaneous output switching and worst case ground bounce. The eighth flip-flop input was held at a DC bias of 2.0V. This should result in its output being held at a constant 1 level.

Figure 5 shows the corner mount results. The ground bounce is sufficient to couple the output of the eighth flip-flop (Q7) to less than 2.0V during the transition of the other seven outputs represented by Q6. The output then charges to a marginal V_{OH} level.

Figure 6 shows the results from the side mount version. Output glitching during the transition of the other seven outputs is still present, but due to the approximately 50% reduction in lead inductance over the corner mount version, the output is allowed to charge back to its original V_{OH} level.

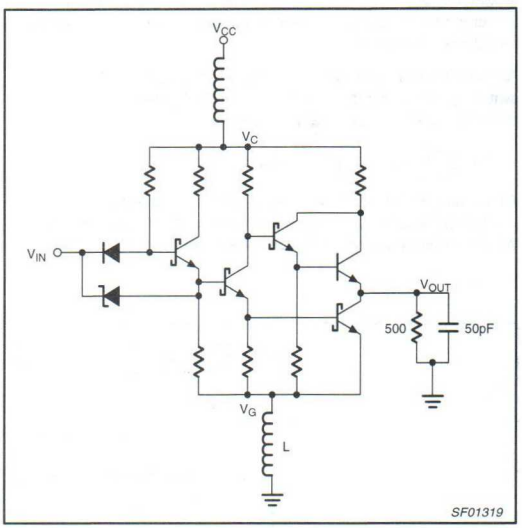


Figure 2.

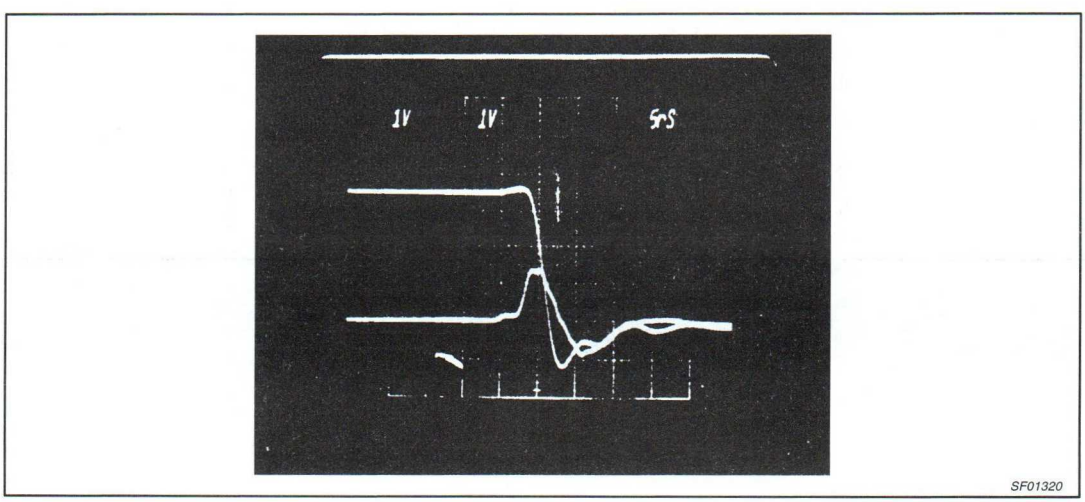
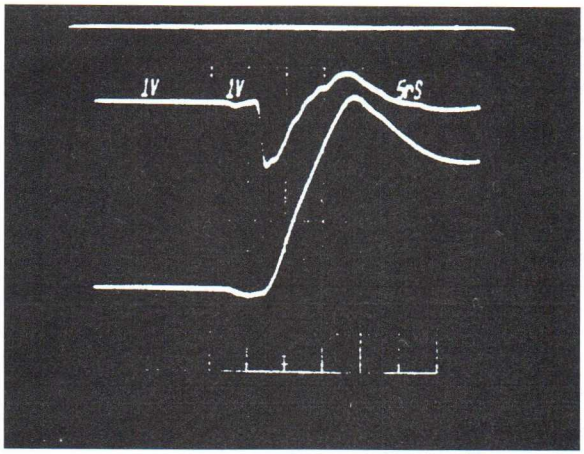


Figure 3.

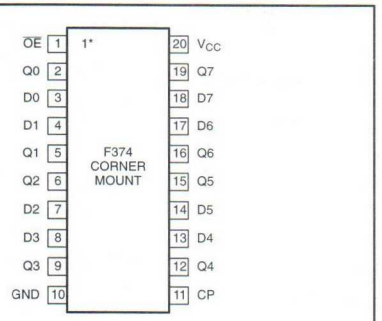
Package lead inductance considerations in high-speed applications

AN212

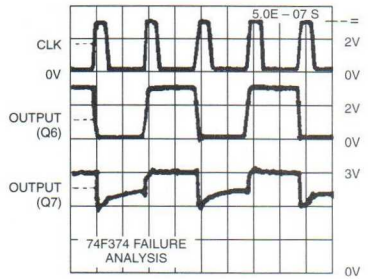


SF01321

Figure 4.

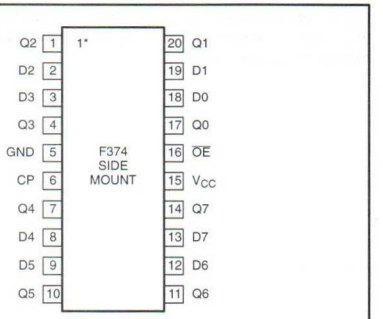


74F374 Failure Analysis

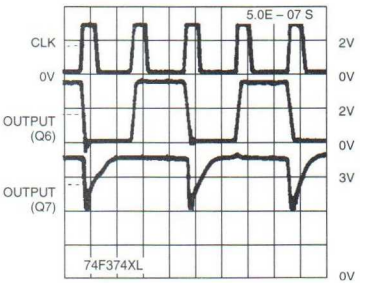


SF01322

Figure 5.



74F374XL



SF01323

Figure 6.

Output Glitching During Multiple Switching

In some cases, the effects of ground bounce can be minimized if properly taken into consideration during the design and layout of the integrated circuit. Note in Figure 7, the glitch that was present on the output of the 74F11, a triple 3-input AND gate, during an early transition of the other two outputs. A newer version of the 74F11 is shown in Figure 8. Note that the glitch has been greatly minimized.

Circuit Oscillations

A fourth area of concern is the possibility of circuit oscillations during slow input transitions through threshold. This would be of importance if the delay through the part is on the order of the natural period of the ground inductance and the load capacitance.

During testing, a particular problem has been seen when the inputs are driven by a power supply by way of a cable. Because there is a delay through the cable, it takes time for the power supply to sense a change in the impedance at the input near threshold. This delay sets up oscillations between the power supply and the input of the part when the input is held near threshold.

Inductance Measurements and Verification

To verify that lead inductance caused these problems, the lead inductance was measured and circuit simulations done to show circuit behavior. Measurement of lead inductance was accomplished using an HP S-parameter test set. These measured values of lead inductance were used in a circuit simulation program. The results of the simulation show voltage and current wave forms similar to the measured waveforms.

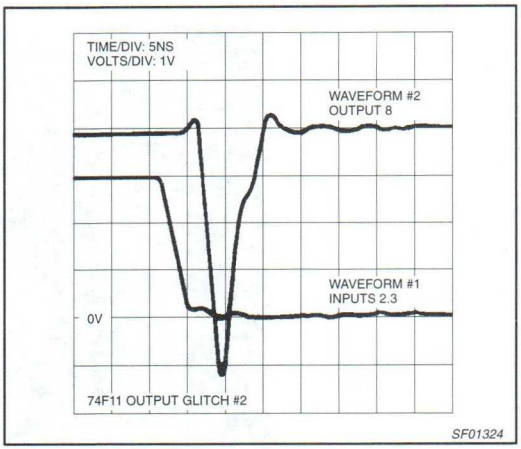


Figure 7.

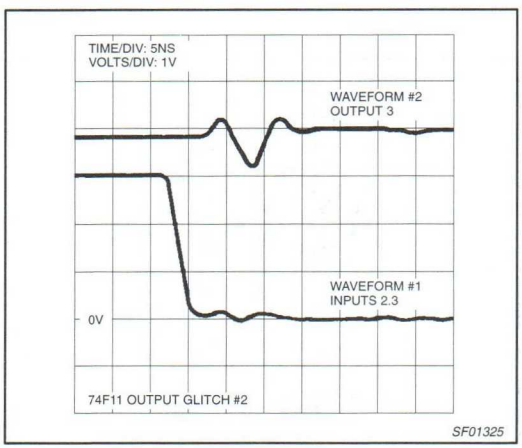


Figure 8.

Package lead inductance considerations in high-speed applications

AN212

Derivation of the S-parameter Method

The general form for voltage and current along a transmission line is:

$$\bar{V}(z) = V^+ e^{-\gamma z} + V^- e^{\gamma z}$$
$$I(z) = I^+ e^{-\gamma z} - I^- e^{\gamma z}$$

Where V^+, V^-, I^+, I^- are constants, usually complex, determined by the boundary conditions, z is the distance from the load and gamma (γ) is a complex term involving a real or loss term and an imaginary or phase shift term.

$$\gamma = \alpha + j\beta$$

$$\gamma \simeq 1/2(R\sqrt{C/L} + G\sqrt{L/C}) + j\omega\sqrt{LC}.$$

Considering the lossless case where R = 0 and G = 0, $\gamma = j\beta$ and only results in a phase shift. The equations for voltage and current then become:

$$\bar{V}(z) = V^+ e^{-j\beta z} + V^- e^{j\beta z}$$

$$\bar{I}(z) = I^+ e^{-j\beta z} - I^- e^{j\beta z}$$

To find Z_1 set z = O. (See Figure 9).

$$\bar{Z}_1 = \bar{V}_1/\bar{I}_1 = (V^+ + V^-)/(I^+ - I^-)$$

since, $I^+ = V^+/Z_0$ and,

$I^- = V^-/Z_0$,
$Z_1 = (V^+ + V^-)/(V^-/Z_0 - V^+/Z_0)$, or,

$$\bar{Z}_1 = Z_0 \frac{1 + V^-/V^+}{1 - V^-/V^+}$$

V^-/V^+ is called the reflection coefficient and is usually complex,

$$\Gamma = V^-/V^+.$$

The impedance at the load then becomes:

$$\bar{Z}_1 = Z_0 \frac{1 + \Gamma}{1 - \Gamma}$$

On the S-parameter test set, the magnitude of the reflection coefficient, $|\Gamma|$, is measured in dB at a particular angle,

$$\Gamma_{real} = 10^{(|\Gamma\,dB|/20)} \angle \theta.$$

For an inductor,

$$\bar{Z}_1 = Z_0 \frac{1 + \Gamma}{1 - \Gamma} = R + j\omega L$$

usually $R \simeq 0$ and L can be solved for directly.

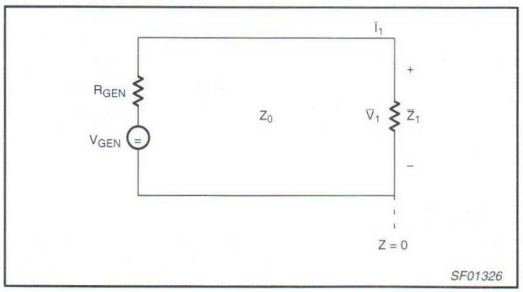


Figure 9.

Example

A 16-pin package measuring from pin 8 to 16 has a reflection coefficient $\Gamma_{dB} = -0.5 \angle 162°$, Z_0 of the system is 50Ω and the measurement frequency is 50MHz.

$$\Gamma_{dB} = -0.5 \angle 162°$$

$$\Gamma_{real} = 0.944 \angle 162° = -0.898 + j0.292$$

$$\bar{Z}_1 = Z_0 \frac{1 + \Gamma}{1 - \Gamma} = 50 * \frac{0.102 + j0.292}{1.898 - j0.292}$$

$$= 50 * \frac{0.309 \angle 70.7°}{1.920 \angle -8.74°}$$

$$= 8.05 \angle 79°$$

$$\bar{Z}_1 = 1.475 + j7.914$$

$$L = 7.914/(2\pi * 50MHz) = \underline{25.19nH}$$

Alternately, using the approximation R = 0, so $|Z_1| = \omega L$:

$$L = \frac{8.05}{2\pi * 50MHz} = \underline{25.62nH}$$

Three packages were used to measure lead inductance, a 16-pin CERDIP, a 24-pin CERDIP and a 24-pin skinny CERDIP. V_{CC} and ground were double bonded to an 80×80 mil blank die. Table 1 shows the results of the measurements.

These values are the total inductance V_{CC} to ground. Each lead inductance would be about one half these numbers.

Table 1.

PACKAGE	REFLECTION COEFFICIENT	INDUCTANCE
16-pin (300mil-wide)		
8 to 16	−0.50 ∠ 162°C	25.62nH
4 to 12	−0.32 ∠ 172°C	11.51nH
24-pin (600mil-wide)		
12 to 24	−0.56 ∠ 157°C	32.78nH
6 to 18	−0.29 ∠ 157°C	18.33nH
24-pin (300mil-wide)		
12 to 24	−0.47 ∠ 160°C	28.39nH
6 to 18	−0.34 ∠ 170°C	14.27nH

Package lead inductance considerations in high-speed applications

AN212

Simulation of Measured Values

Both ground and V_{CC} bounce for the 74F240 were simulated using the inductive values measured. The results were similar to the measured data of the 74F240. Figures 3 and 4. The simulation of the 74F240 is shown in Figure 10. this shows the pad V_{CC}, the pad ground (V_G) and the inputs (V_{IN}) and output (V_{OUT}) when all 8 buffers are switched simultaneously.

SUMMARY

A major contributor to noise in High-speed circuits is package lead inductance. Integrated circuits are packaged with lead frame traces and bonding wire. These leads act as inductors. Voltage generated across these leads follow the law:

$$V = L\frac{di}{dt}$$

This represents noise to an integrated circuit chip and can cause performance degradation. The faster the switching rates become,, the more lead inductance can affect circuit performance.

As circuits become faster, more care should be taken in packaging and chip layout. In some cases like the 74F11, a better layout can help remove potential problems but in most cases like the 74F240, the noise is strictly a function of the package. Care should be taken in integrated circuit packages to minimize lead lengths. Side mount V_{CC} and ground pins, smaller packages such as the surface mounted SO, and High levels of board integration are fa few possibilities which would help minimize lead lengths.

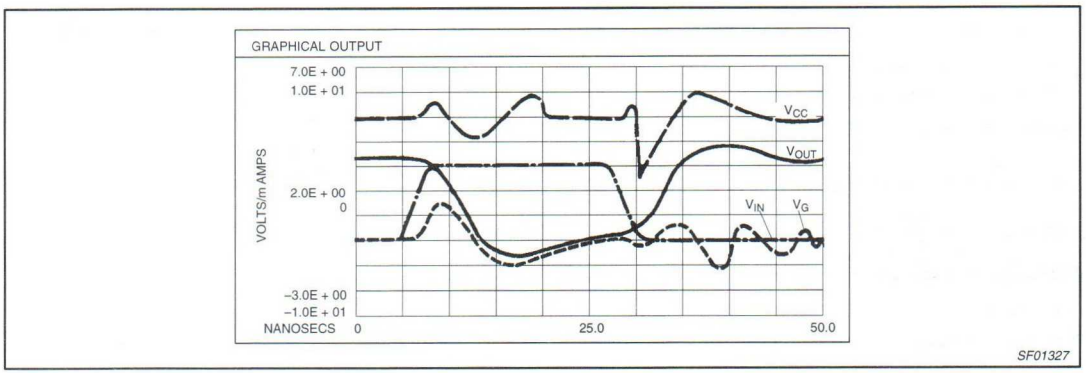


Figure 10.

74F extended octal-plus family applications AN214

74F Extended Octal-Plus Family Features

- 8-, 9-, and 10-bit "Light-Load" bus products
  - Buffers/Drivers
    With and without latches or registers
    With and without 8-bit parity checker/generator
  - Transceivers
    With and without dual registers
    With and without 8-bit parity checker/generator
- Patented "Light-Load" inputs:
  - Input Current = ±20µA per input
  - Transceiver I/O pins = ±70µA
- High performance output drive currents:
  - I_{OL} = 64mA/48mA @ ±5%/10% V_{CC}
  - I_{OH} = –15mA/–3mA @ ±5%/10% V_{CC}
- "Flow-through" or "broadside" I/O pin configuration
- Ideal for MOS CPU, peripherals and semi-custom bus interface
- 24-pin, 300mil-wide, plastic slim-DIPs
- High performance buffers — $t_{P(max)}$ = 7.5ns
- High performance latches/registers — f_T = 100MHz

Introduction

The 74F Extended Octal-Plus Family incorporates all of the latest Philips Semiconductors octal, 9-bit and 10-bit buffer, transceiver, latch and register functions. all devices in this family utilize the Philips Semiconductors patented "Light-Load" NPN, ±20µA input current structure and have "flow-through" or "broadside" input/output pin configurations where the inputs and outputs are lined-up on opposite sides of a standard 24-pin Slim-DIP package. The "light-load" inputs, "broadside" design and high functional density/performance of the family make this product line ideal for buffering the limited drive capabilities of standard, custom and semicustom MOS VLSI devices to the rigorous environments of today's leading edge high performance logic designs. The family also is an excellent choice for all general interface applications.

"Flow-Through" Design

The "flow-through" or "broadside" chip layout/package design is illustrated in Figure 1 showing the block diagrams and pin configurations of the 74F828 10-bit Inverting buffer. Note that all of these "broadside" designs allow logic signals to flow into one side and out of the other without crossing or folding back on signal paths such as the 74F240 Octal Buffers (Figure 2). If you compare the physical layout requirements of the path of PC board bus lines for the 74F828 to that of the 74F240's "zig-zag" path, you will see the significant advantages of the 74F Extended Octal-Plus Family's "flow-through" design in simplifying the design and layout of large, high density, bus-oriented PC boards.

The 24-pin, 300mil-wide, Slip-DIP Solution

With the advent of advanced Schottky TTL technology came the ability to significantly increase the functional density of standard logic building blocks. However, not until the development of the 24-pin, 300mil-wide, Slim-DIP package was it possible to take full advantage of these new chip densities. The entire family provides significant advantages in package count, pin count and packing density when compared to older technologies. Further density enhancements can be achieved by using Philips surface mounted packages.

By combining high functional density into a 24-pin 300mil-wide Slim-DIP package, the Philips Semiconductors 74F Extended Octal-Plus Family allows the reduction of PC board parts count and cost while optimizing layout with "broadside" chip designs, reducing total system power dissipation and increasing system reliability.

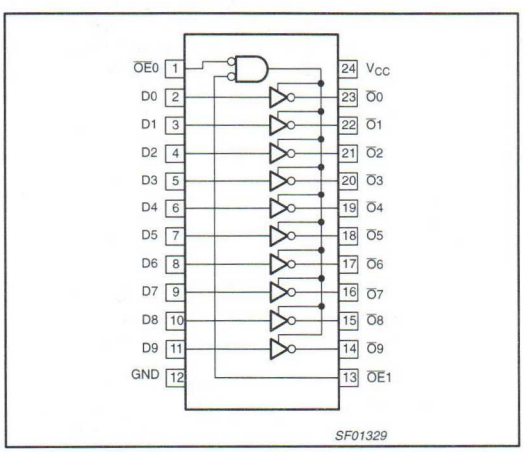


Figure 1. 74F828 Broadside Pin Configuration

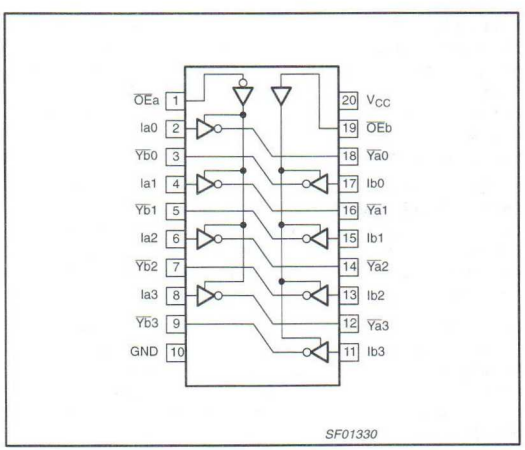


Figure 2. 74F240 'Zig-Zag" Pin Configuration

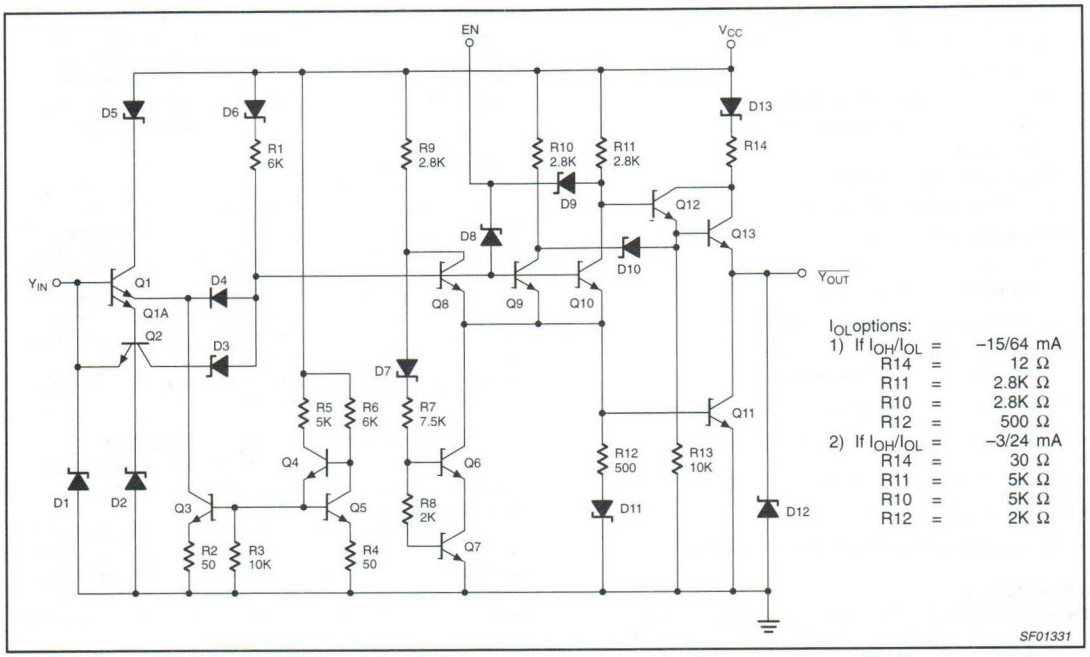


Figure 3. 74F455 Buffer/Drive Cell Circuit Diagram

The 8-, 9-, and 10-bit Series 24-pin Solution

Whether your system requires an 8–, 9-, or 10-bit bus interface, the Extended Octal-Plus Family has standardized solutions in 24-pin/Slim-DIP/Broadside input/output packages with corner power supply pins (12 & 24) and standard designations for common control functions located at or near the package corners. Octals offer more mode control inputs than do the 9- or 10-bit products. Virtually all family devices with 3-State outputs are guaranteed to source/sink −15/64mA @ V_{OH}/V_{OL} = 2.0/0.55V (except for the 74F841–846 Latched Drivers, which are spec'ed at −15mA/48mA). The A_N port outputs of several of the family's transceivers are guaranteed to supply −3mA/48mA).

The Octal Parity Bus Series offers several notable exceptions to the above standard pinouts. This series has three parts with two center-package ground pins to minimize ground-bounce noise. All outputs (except the A_N port of the 74F657 Parity Bus Transceiver spec'ed at −3mA/24mA) are guaranteed to source/sink more than −15mA/64mA.

Current PC board, multi-layer technology make is possible to take into consideration the physical location of input/output pins, transmission line characteristics and supply power distribution. Lining up all inputs and output on opposite sides of the package allows the address, data and control bus signal to flow in a direct physical path from the µP CPU through the bus interface chips and onto the appropriate bus. This "broadside" bus design approach produces very clean PC board layouts and may, in fact eliminate and entire PC board interconnection layer. Standardization of power supply, mode control and input/output pins, whether 8-, 9-, or 10-bit bus functions, permits simplified, structured PC board layout.

Input Structures

Referring to Figure 3, the 74F455 Inverting Buffer/Driver Cell Circuit Diagram is an example of the family's input and output circuitry. The patented Philips Semiconductors "Light-Load" NPN input structure (Q1/23/4/5, R1/2/3/4/5/6 and D4) and turn-OFF speed-up circuit (Q2 and D2/3) are used throughout the 74F Extended Octal-Plus Family. the "Light-Load" NPN input is actually a high speed, differential amplifier with the reference side, the anode of D4, clamped at two diode voltage drops above ground (BE junctions of Q8/9/10 and Q 11 of ~1.4V at 25°C). When the V_{IH} rises above this clamp voltage, the BE junction of Q1 is forward based allowing beta amplified, CE current to flow into the <1.0mA constant current source, Q3 (driven by Q4/5 and R2/3/4/5/6). The beta of Q1 is guaranteed, by design, to be >50, thereby guaranteeing that the input base bias current will be <20µA. The emitter of Q1 rises to $1V_{BE}$ (~300mV) below the V_{IH}, reverse biasing D4 and permitting C8/9/10 base bias current to flow through R1.

The patented turn-OFF circuit consisting of Q2 and D2/3 produces a dynamic speed to help turn Q8/9/10 OFF quickly. During the time that the Q1 is turned-ON (input = V_{IH} >2.0V), the revers-biased Schottky diode, D2, acting as a capacitor, will be charged to the voltage at the emitter of Q1A or $1V_{BE}$ voltage drop below the input (>2.0 – $1V_{BE}$). When the input is switched to <V_{IL} (or <0.8V), the D2 stored charge discharges through the BE of Q2. Q2 CE current through D3 rapidly turns Q8/9/10 OFF.

These circuit innovations produce high performance, very low input bias current (±20µA) gate inputs. This input leakage represents a 30X reduction over the standard 74F family's 600µA input current with virtually no loss in speed. The 74F Extended Octal-Plus

Transceivers have an input loading current of ±70μA, which is the combination of the "Light-Load" NPN input structure's ±20μA and the 3-State Hi-Z output's ±50μA leakage current.

The low "Light-Load" input current and high speed performance makes this family ideal for interfacing to low drive capability, slower MOS CPU, peripherals and semi-custom chips used in most of today's state-of-the-art logic designs. Besides very low input current requirements, this "Light-Load" input has another significant advantage over "traditional" input structures: Very low input capacitance (smaller stored charge) due to very small device geometries. Therefore, when Extended Octal-Plus devices are connected to a bus, they present less AC bus loading and do not significantly lower the characteristic impedance of the bus to the extent "traditional" input structures do. Thus, the amount of the AC current a bus driver has to produce to change the state of the bus is lowered and in many cases can make a difference between incident wave switching of the bus versus losing time waiting for a reflected wave.

The Philips Semiconductors 74F "Light-Load" input structure is discussed in more detail in *Application Note AN215*.

Output Drive Capabilities

Virtually all devices in the EXtended Octal-Plus Family are guaranteed to source/sink more than –15mA/64mA @ $V_{OH}V_{OL}$ = 2.0/0.55V. One exception is the 74F841-thru-846 Series of Bus Interface Latches which are specified at –15/48mA. Several of the family's transceiver products have lower A_N output drive capabilities to reduce package power dissipation. Refer to Tables 1 and 3.

For example, the 74F657 Parity Bus Transceiver has two output ports with different capacities: The A_N port is guaranteed to source/sink –3mA/24mA (I_{OH}/I_{OL} = 2.4/0.50V), and the B_N port has an output drive capability of –15mA/64mA at 2.0V/0.55V. The 74F657's A_N port is designed to interface the chip side of the PC board to the backplane bus, while the B_N port is capable of driving a transmission line or bus backplane line.

Referring to Figure 3, all of the Family's 3-State, totem-pole output structures have a schottky blocking diode, D13, in their pull-up output structures. These diodes block leakage current from flowing into the outputs when V_{CC} is either open or shorted to ground.

This gives a very important advantage of being able to power down a PCB (or several PCBs) without disabling the bus and even without producing any glitching on the bus due to an undesired change in the output state of the device being powered down.

The output short-circuit (I_{OS}) limiting resistor (R14), the anode-to-cathode resistance/voltage drop of D13 and the collector-to-emitter/base-to-emitter resistance/voltage drop of Q13 limit the amount of current that can be sourced from a HIGH level output at a specified V_{OH}. For most of the parts in the family, R14 is equal to 12Ω. the A_N port of several of the transceivers utilize an R14 of 30Ω producing I_{OH} (@ V_{OH} = 20V) of –6mA versus –15mA from the B_N ports 12Ω R14.

The output HIGH level sourcing current, I_{OH}, at a specified output voltage, V_{OH}, can be calculated by subtracting the voltage drops of D13, the pull-up darlington transistor, Q12/13, and the desired V_{OH} level from V_{CC} and dividing by the value of R14 plus the anode-to-cathode resistance of D13 and the collector-to-emitter/ base-to-emitter resistance.

Assumptions:
$V_{D13} \cong 0.5V$ @ $R_{ON} = 3\Omega$ @ 25°C),
$V_{Q12/13} \cong 1.2V$ @ $R_{ON} = 8\Omega$ @ 25°C)
$I_{OH} = 1[V_{CC}–(V_{D13} + V_{Q12/Q13} + V_{OH})]/(R14 + R_{D13} + R_{Q13})$.
$I_{OH}(R14 = 12\Omega) = –[4.5V–(0.5V + 1.2V + 2.0V)]/23\Omega = –35mA$
$I_{OH}(R14 = 30\Omega) = –[4.5V–(0.5V + 1.2V + 2.0V)]/41\Omega = –20mA$
$I_{OS} = I_{OH}$ @ V_{OH} = 0.0V and V_{CC} = 5.5V
$I_{OS}(R14 = 12\Omega) = –[5.5V–(0.5V + 1.2V)]/23\Omega = –165mA$
$I_{OS}(R14 = 30\Omega) = –[5.5V–(0.5V + 1.2V)]/41\Omega = –93mA$

Obviously, we have been very conservative in the I_{OH} specification to guardband against all conditions of temperature and input/output/supply voltage levels. The R_{ON} resistances of the output pullup transistors and blocking diode are large enough to prevent I_{OS} from exceeding –225mA for R14 = 12Ω and –150mA for R14 = 30Ω. (Refer to Table 1.)

Table 1. Family Output Drive Capabilities Using the 74F657 Parity Bus Transceiver

DC ELECTRICAL CHARACTERISTICS
Over recommended operating conditions, V_{IL} = MAX and V_{IH} = MIN)

SYMBOL	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	All outputs	I_{OH} = –3mA ±10% V_{CC}	2.4			V
			I_{OH} = –3mA ±5% V_{CC}	2.7	3.4		V
		B_N port, PARITY, $\overline{ERROR}$	I_{OH} = –15mA ±10% V_{CC}	2.0			V
			I_{OH} = –15mA ±5% V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A_N port	I_{OL} = 24mA ±10% V_{CC}		0.35	0.50	V
			I_{OL} = 24mA ±5% V_{CC}		0.35	0.50	V
		B_N port, PARITY, $\overline{ERROR}$	I_{OL} = 48mA ±10% V_{CC}		0.40	0.55	V
			I_{OL} = 48mA ±5% V_{CC}		0.40	0.55	V
I_{OS}	A_N output High level short circuit current (R14 = 30Ω)		V_{CC} = MAX			–150	mA
	B_N output High level short circuit current (R14 = 12Ω)		V_{CC} = MAX			–225	mA

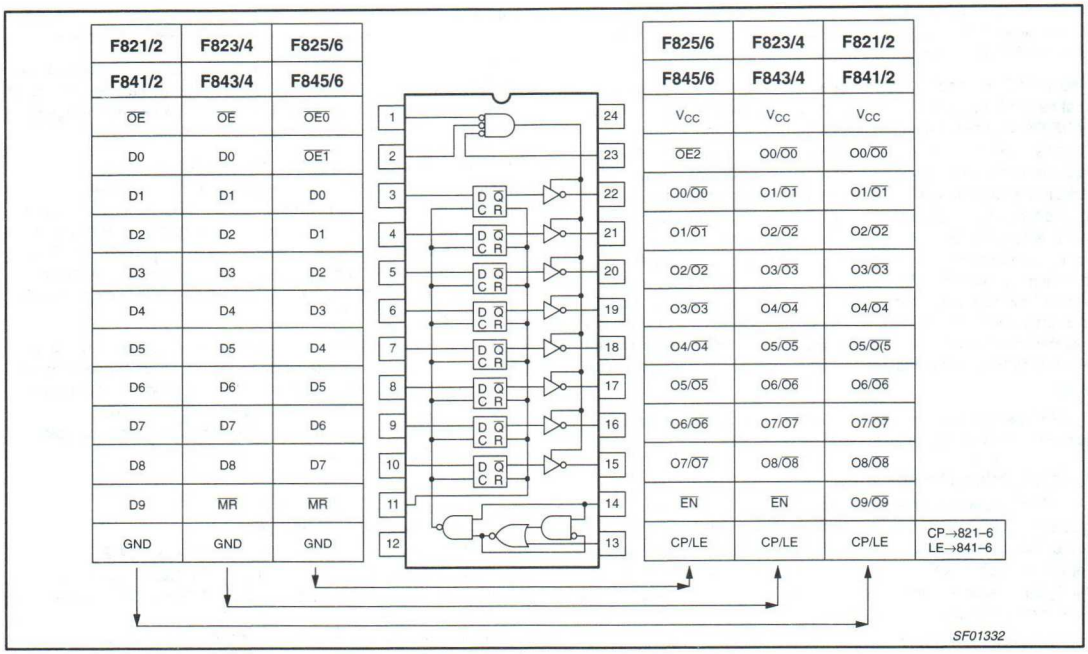


Figure 4. 74F82X and 74F84X Registered/Latched Buffer Pin Configurations

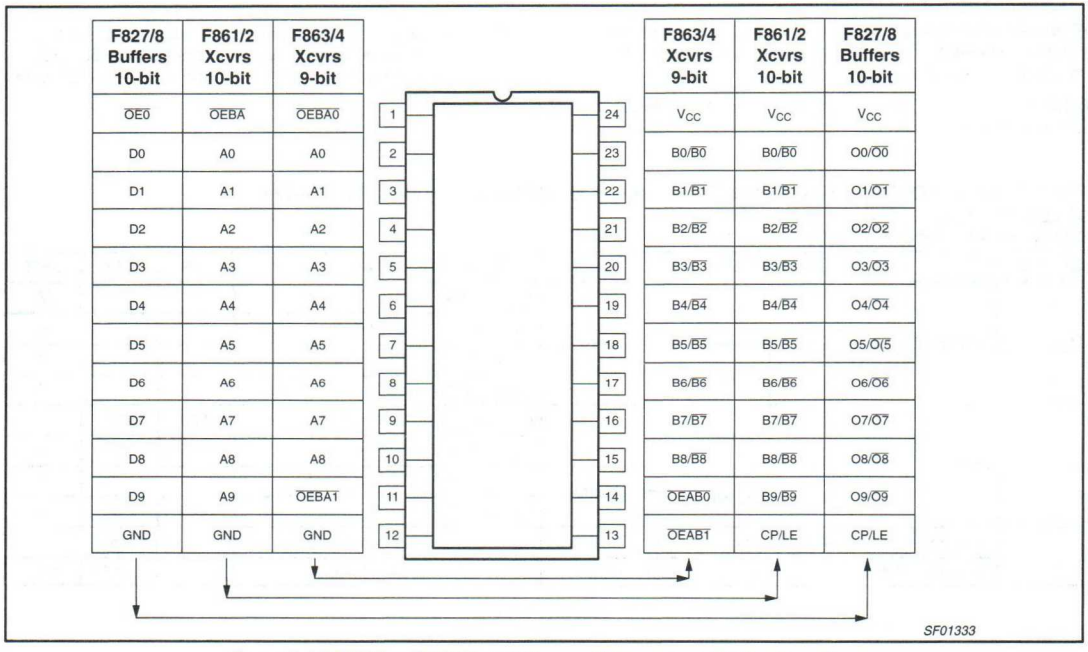


Figure 5. 74F827/8 and 74F861–4 Buffers and Transceivers Pin Configurations

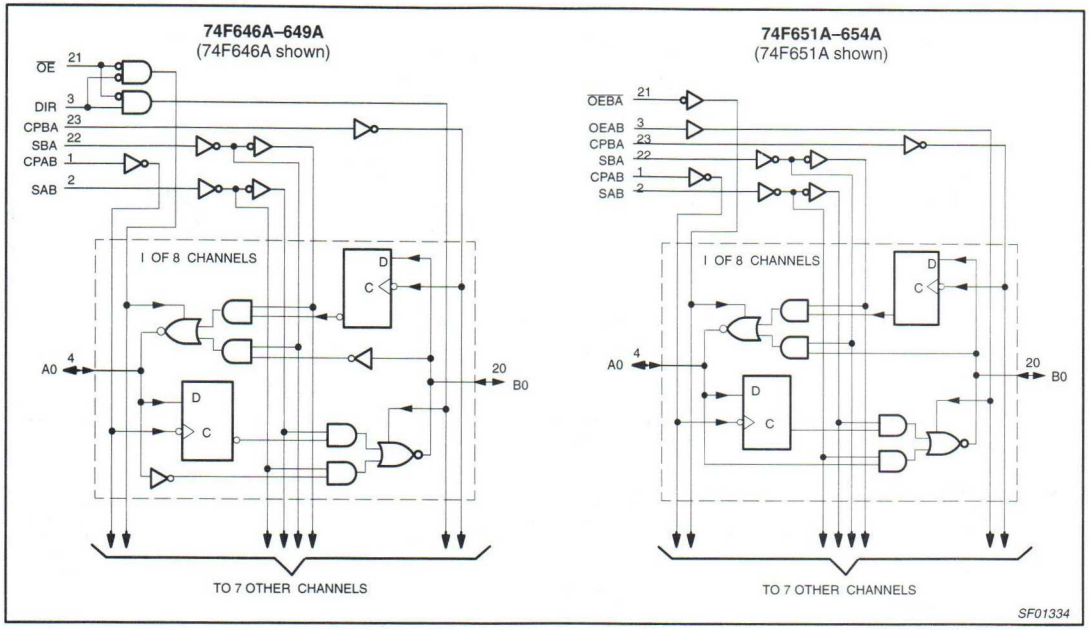
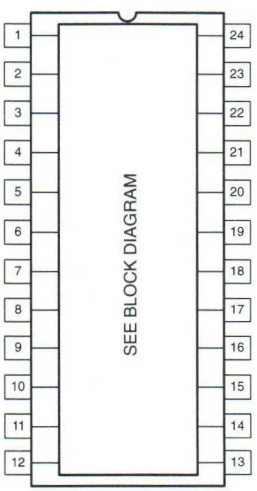


Figure 6. 74F646A–649A and 74F651A–654A Registered Transceivers Simplified Logic Block Diagrams

F646A/7A 3-St/OC	F648A/9A 3-St/OC	F651A/3A 3-St/OC	F652A/4A 3-St/OC
CPAB	CPAB	$\overline{OEBA}$	$\overline{OEBA0}$
SAB	SAB	SAB	SAB
DIR	DIR	OEAB	OEAB
A0	$\overline{A0}$	$\overline{A0}$	A0
A1	$\overline{A1}$	$\overline{A1}$	A1
A2	$\overline{A2}$	$\overline{A2}$	A2
A3	$\overline{A3}$	$\overline{A3}$	A3
A4	$\overline{A4}$	$\overline{A4}$	A4
A5	$\overline{A5}$	$\overline{A5}$	A5
A6	$\overline{A6}$	$\overline{A6}$	A6
A7	$\overline{A7}$	$\overline{A7}$	A7
GND	GND	GND	GND



F652A/4A 3-St/OC	F651A/3A 3-St/OC	F648A/9A 3-St/OC	F646A/7A 3-St/OC
V_{CC}	V_{CC}	V_{CC}	V_{CC}
CPBA	CPBA	CPBA	CPBA
SBA	SBA	SBA	SBA
$\overline{OEBA}$	$\overline{OEBA}$	$\overline{OE}$	$\overline{OE}$
B0	$\overline{B0}$	$\overline{B0}$	B0
B1	$\overline{B1}$	$\overline{B1}$	B1
B2	$\overline{B2}$	$\overline{B2}$	B2
B3	$\overline{B3}$	$\overline{B3}$	B3
B4	$\overline{B4}$	$\overline{B4}$	B4
B5	$\overline{B5}$	$\overline{B5}$	B5
B6	$\overline{B6}$	$\overline{B6}$	B6
B7	$\overline{B7}$	$\overline{B7}$	B7

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Figure 7. 74F646A–649A and 74F651A–654A Dual Registered Transceivers Pin configurations

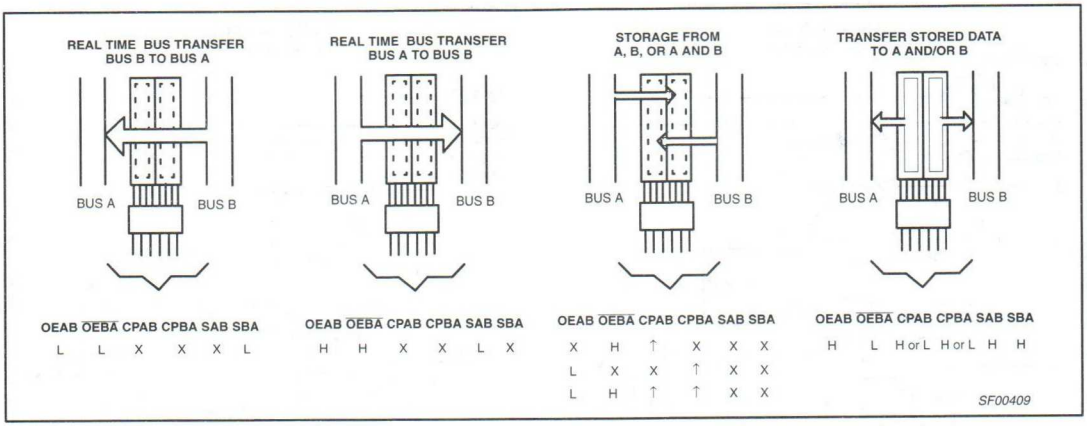


Figure 8. 74F651A–654A Registered Transceivers Storage Options (74F646A–649A not shown)

Table 2. Parity Bus Family versus the Competition

PART NUMBER	DESCRIPTION	TOTAL # OF PINS	t_{PDmax}* IN to OUT	t_{PDmax}* IN to PARITY	I_{CCmax}**	POWER PINS	BROADSIDE DESIGN
74F455/F456 vs. 74F240/F244 + 74F280	Octal Parity Buffer	24	7.5ns	16.0ns	110mA	Center	Yes
		38	7.5ns	14.5ns	125mA	Corner	No
74F655A/F656A vs. 74F240/F244 + 74F280	Octal Parity Buffer	24	7.5ns	16.0ns	110mA	Corner	Yes
		38	7.5ns	14.5ns	125mA	Corner	No
74F657 vs. 74F240/F245 + 74F280 + 1 AND gate	Octal Parity Transceiver	24	7.5ns	16.0ns	110mA	Center	Yes
		38	8.0ns	14.5ns	125mA	Corner	No

NOTES:

* Propagation delays of DATA IN-to-DATA OUT and IN-to-PARITY OUT, T_{amb} = 0°C to 70°C, V_{CC} = +5.0V ±10%, Output Load = C_L = 50pF, and R_L = 500Ω.

** Worst case power, T_{amb} = 0°C to 70°C, V_{CC} = +5.0V ±10%, Output Load = C_L = 50pF, and R_L = 500Ω.

74F821–74F863 Series

The 74F821 through 74F863 Series of Octal 9-bit and 10-bit Buffers, Latch Buffers, Register Buffers and Transceivers are standardized around the AMD 298XX series with one significant difference—the Philips Semiconductors "Light-Load" NPN input offers a 50:1 reduction in input loading (1000μA vs. 20μA). This series illustrates the standardized on 24-pin/300mil-wide Slim-DIP packages, "broadside" input/output pinouts and control function pins. All 74F8XX 3-State outputs are guaranteed to source/sink –15mA/64mA, except for the 74F84X Latched Buffers, which are specified at –15mA/48mA.

The logic diagram and pin configurations of the 74F828 Non-Inverting 10-bit Buffer (Figure 1) and the 74F821–826 and 74F841–846 Registered/Latched Buffers (Figure 4) are excellent illustrations of the standardized pin configuration illustrating "broadside" chip design.

Figure 5 shows the pinouts of the 74F827/828 buffers and 74F861–864 Transceivers. There currently are no 9-bit buffer offerings in this series.

Registered Transceiver Series

the 74F646A–649A and 74F651A–654A Octal Dual-Registered Transceivers offer a "Light-Load" combination of a 74F245 type transceiver with two 74F373/374 type octal registers within a 24-pin Slim-DIP broadside input/output package. This series offers a significant 6:1 package count reduction advantage over older technologies.

Figure 6 shows the 74F646A and 74F651A Transceivers Simplified Block Diagrams, and this series' pin configurations are depicted in Figure 7. Figure 8 graphically illustrates four optional storage and transfer modes of the 74F651A Octal, Non-Inverting, 3-State, Dual-Registered Transceiver. The 74F654A will be used to explain the operation of the entire series. The 74F646A/648A (3-State, INV/NINV) and the 74F647/649 (O.C., INV/NINV) Octal Dual-Registered Transceivers offer optional signal direction control logic and output enable to the 74F651A–654A series.

This series allows you to store or real-time transfer data in either direction through the transceiver function. Data at the A_N port can be stored in either the A_N port register or the B_N register and, then, can

be transferred either from the A_N port register to the B_N port outputs or from the B_N port register to the A_N port outputs.

The same capabilities are available to data presented to the B–port. When a port's output buffers are enabled ($\overline{OE}$ = LOW and DIR = LOW for A_N outputs enabled or HIGH for B_N outputs enabled), the SXX select inputs (SAB and SBA) control the two EX-OR gates allowing the output port data to come either directly from the other port (real-time transfer) or from the other port's input storage register.

The CPABN and CPBA inputs are the LOW-to-HIGH edge-triggered clock inputs for the A_N port register and B_N port register. Data presented to either port's inputs can be clocked into its input register on a LOW-to-HIGH CPXX input regardless of the logic levels on any of the other mode control inputs.

The 74F651A–654A's OEAB and $\overline{OEBA}$ output enable inputs may be tied together to enable the B outputs when HIGH or A_N outputs when held LOW or can be used separately to independently control the two output ports. Tying the 74F651A–654A's OEAB and $\overline{OEBA}$ together is logically equivalent to the DIR input of the 74F646A–649A.

Parity Bus Series Advantages

The increased functional density of the Parity Bus Series produces a 2:1 package reduction (plus 1 AND gate) and, therefore, 38:24 pin reduction. Power dissipation savings of 82.5mW for the 74F455/456/655A/656A Drivers and 137.5mW for the 74F657 are also achieved through shared internal logic. Table 2 shows the package/pin advantage as well as the worst case propagation delays and I_{CC} of the Family versus their competition.

Figure 9 is a summary of the pin configurations of the entire Parity Bus Drivers and Transceiver Series.

The 74F455/456/655A/656A Octal Parity Bus Drivers and the 74F657 Octal Parity Bus Transceiver Series combines the popular Philips Semiconductors 74F24X buffer/transceiver functions with the 74F280B 9-bit Parity Generator/Checker, "Broadside" input/output pin configurations, "Light-Load" inputs and an increased guaranteed sink/source capabilities of –15mA/64mA for low impedance bus environments. The 74F445/446 Drivers with their multiple center-package ground supply pins are logically identical to the 74F655A/656A Drivers, except for the latter's single corner-package supply pins and an additional $\overline{Output\ Enable}$ input. The 74F657 Parity Bus Transceiver allows the parity to be generated and checked in both directions in a single package replacing one 74F245 Transceiver, 20-pin DIP and two 74F280, 16-pin DIPs plus a couple of gates.

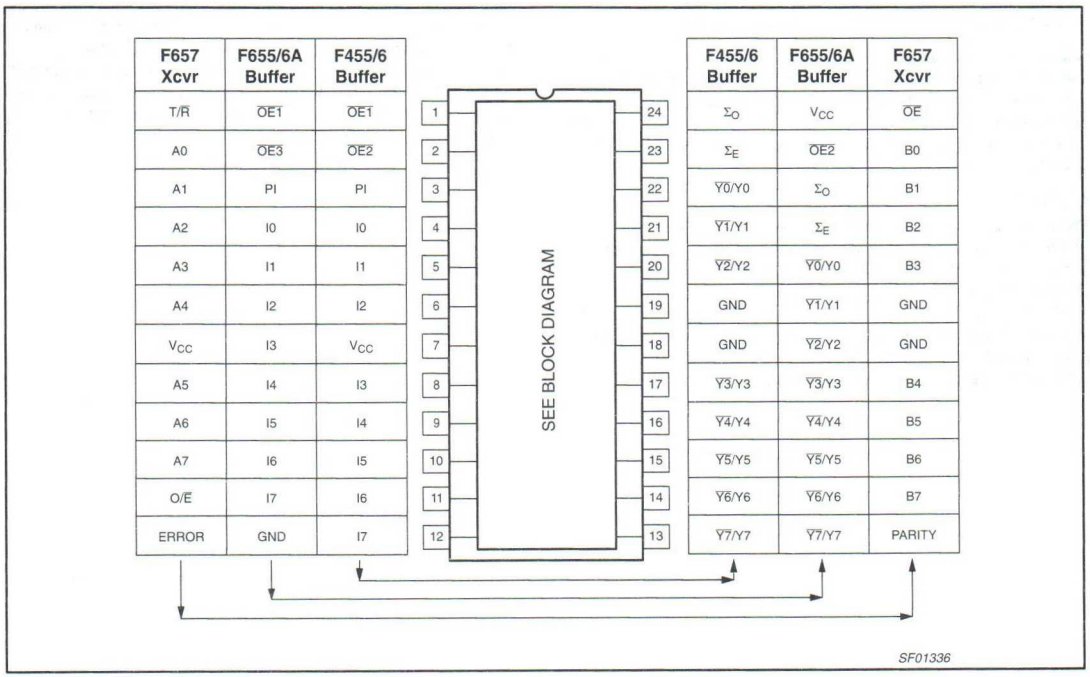


Figure 9. 74F Octal Parity Drivers/Transceiver Pin Configurations

74F657 Operation

The 74F657 Parity Bus Transceiver, as shown in its simplified logic diagram, Figure 10, is a combination of a 74F245 Octal Transceiver and a 74F280B 9-bit Parity Generator/Checker plus one AND gate. Figure 11 expands the logic block diagram of the Family's Parity Tree Logic (inside the dashed line of Figure 10).

During TRANSMIT mode (A_N = Hi-Z), the PARITY and $\overline{ERROR}$ outputs are generated from the A_N input/output port. In the RECEIVE mode, the B_N port is the input from the system or mother board bus (B-port outputs = Hi-Z).

For best speed performance, PARITY should always be generated from the A_N port for the B_N port (TRANSMIT mode), and parity $\overline{ERROR}$ should always be checked for data coming in on the B-port (RECEIVE mode). EVEN or ODD parity generation and checking is determined by the EVEN/$\overline{ODD}$ input (EVEN = HIGH, and ODD = LOW).

In the TRANSMIT mode (T/$\overline{R}$ = HIGH), transmitted data travels from the A-port to the B-port in less than 8.0ns generating a PARITY bit output in less than 16.0ns. Whereas, in the RECEIVE mode (T/$\overline{R}$ = LOW), received data traverses from the B-port to the A-port path in, again, less than 8.0ns, but then the $\overline{ERROR}$ checking output, being generated from the output data presented to the A-port and the PARITY input, takes an additional 16.5ns or less to stabilize. Therefore, the total RECEIVEd-data-to-$\overline{ERROR}$ checking output propagation time is the sum of the B_N-to-A_N delay (8ns) and the A_N/PARITY-to-$\overline{ERROR}$ output delay (16.5ns) or 22.5ns.

However, in many cases, the propagation delay that has to be taken into consideration does not have to include parity calculation time and could be equal to that of just the transceiver part (8ns). This is due to the fact that it may not be too late to interrupt whatever needs to be interrupted in case of a parity error after the data has already gone by (i.e., via late bus error).

Parity Tree Analysis

The basic 3-input Comparator Cell, inside the dashed line in Figure 11, is used throughout the Parity Bus Series. If there are an even number of HIGH inputs (0 or 2) the output of the 3-Input Comparator Cell will be HIGH, while an odd number (1 or 3) will produce an output LOW. The 74F657's Parity Tree Logic, combines four of the 3-Input Comparators with a 2-input comparator, a 2-input AND gate and output buffers for PARITY and $\overline{ERROR}$ to produce the complete parity generator/checker logic.

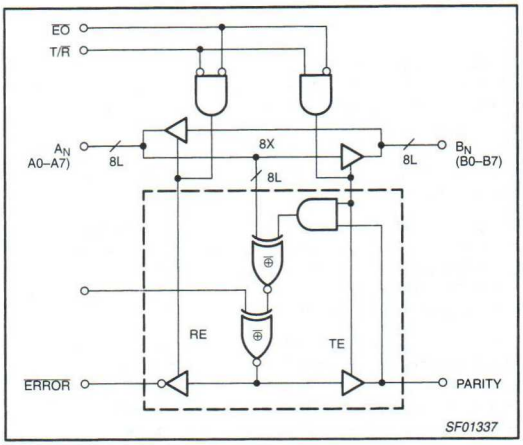


Figure 10. 74F657 Simplified Block Diagram

The 74F588 IEEE-488 Octal Transceiver

The 74F588 is a non-inverting IEEE-488 standard transceiver contains eight bidirectional 3-State buffers. The B_N port outputs can source/sink –15mA/64mA (guaranteed) and have series termination resistors as specified in the IEEE-488 specification. The A_N port, which interfaces to the PC board or system logic bus, is guaranteed to source/sink –3mA/24mA. The 74F588 pinout is identical to that of the 74F545 Octal Transceiver with the IEEE-488 termination resistors in series with the B_N port.

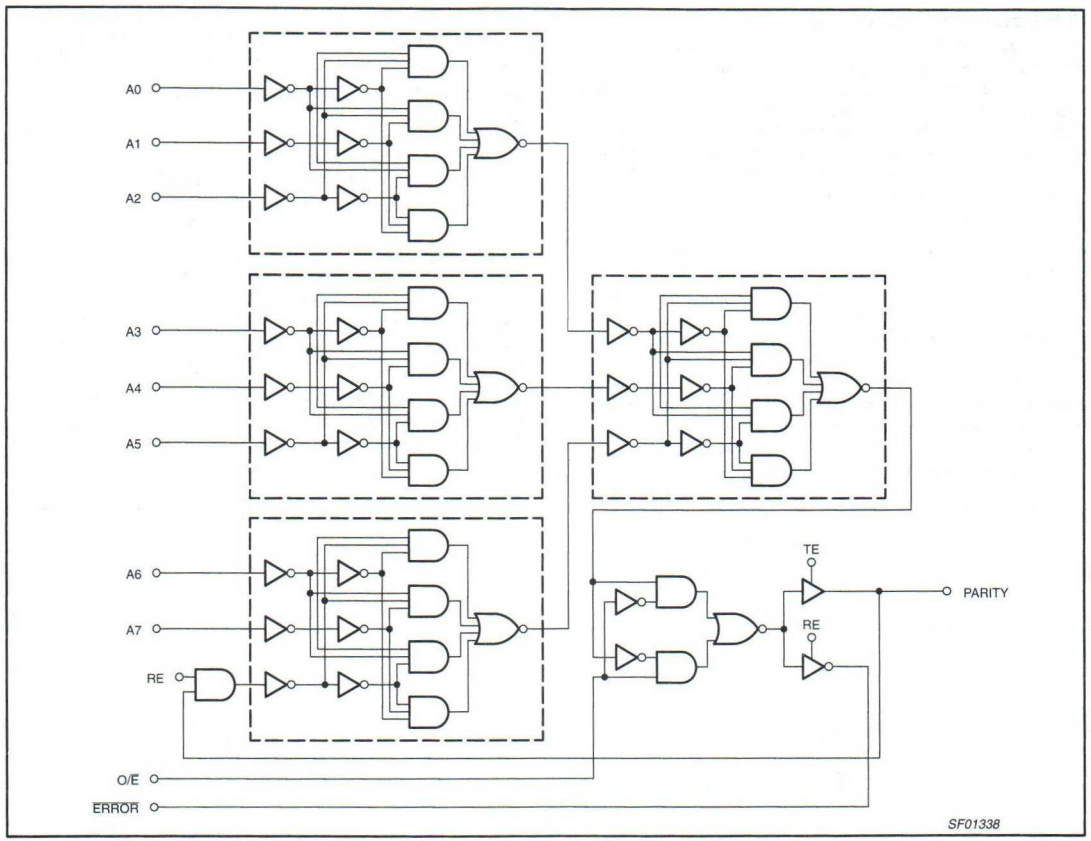


Figure 11. 74F657 Parity Tree Logic Diagram

Metastability in Latches and Registers

Interfacing a basically asynchronous real-world with synchronous logic systems can and does cause many circuit designer headaches. The problem: latches and registers which are **normally** considered to have only two stable states (High and Low) actually have a third—The METASTABLE State. This third operating point occurs when the corss-coupled latch is exactly balanced. This state is only stable when there is no noise on the chip which would tend to destabilize the perfect energy balance between the bi-stable states of the latch. Refer to Figure 12.

Metastability can occur when input data violate the setup time or hold time specifications at the clocking or strobing edge of the synchronizing clock input. With no system noise, the latch cannot decide "yes or no", so it is possible for the latch to "go metastable" or "maybe". With noise on the chip, random energy will "nudge" the latch toward one of its "bi-stable" states—HIGH or LOW. This metastable state time can range from nanoseconds to milliseconds. With today's very high performance logic families, the metastable condition can last for, perhaps, 1000 times the latch's normal propagation delay time. A metastable latch has an unpredictable delay time during which the output is between logic levels. This metastable state can easily last more than 50ns with today's high performance logic families and WILL cause systems to "crash" if great care is not taken with asynchronous, real-world interfacing.

The D-type latch shown in Figure 12 has DATA applied to NAND gate 1 and $\overline{\text{DATA}}$ applied to NAND gate 2. When the LE (Latch Enable) input is LOW, gates 1 and 2 outputs are HIGH and the G3/4 R-S latch is latched and stable. When LE is HIGH, the latch appears to be transparent to the DATA input—Q equals DATA. On the HIGH-to-LOW transition of LE, the DATA logic level that meets the latch's setup and hold time is stored in the latch.

If DATA changes during the setup time to hold time period, it is possible for both outputs of gates 1 and 2 to be in the input thresholds region of gates 3 and 4, respectively. Under these conditions, the latch (gates 3 and 4) could be perfectly balanced in the METASTABLE state. Eventually, chip and system noise will cause the latch to be forced into a HIGH/LOW stable state.

The Extended Octal-Puls Family, while not entirely immune, has been made metastable resistant by using design techniques which force the latch toward a stable state much more quickly than older bus interface families.

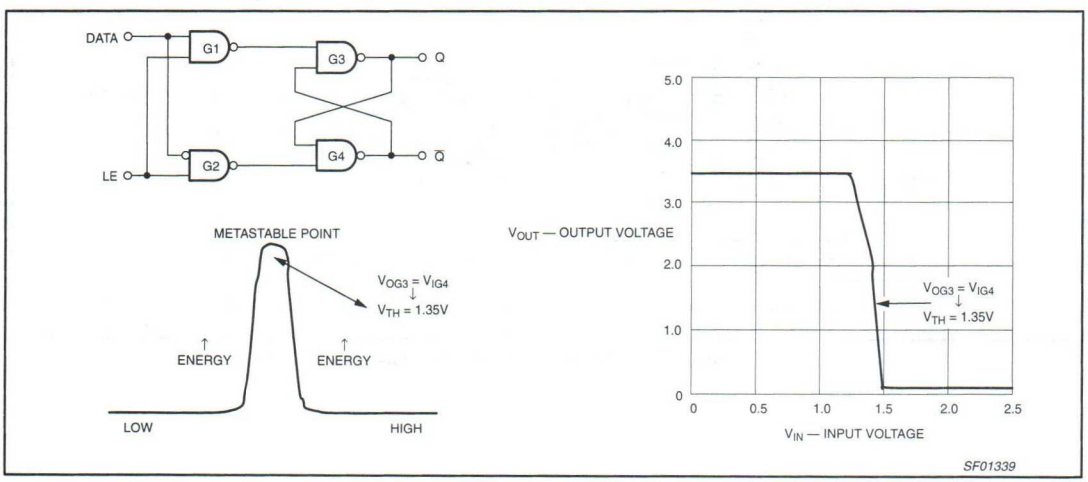


Figure 12. Metastability in Latches and Registers

Dual-Registered Transceiver Applications

Figure 13 illustrates how the 74F646A-649A and 74F651A-654A can be used to either synchronize data transfer between two systems, or pipeline data. Data is stored in a register, then, while retrieving more data, the first data is read. When the second is available, it can either be stored or read directly. Two slower systems can be multiplexed into a high speed system in the same way.

Parity Bus Transceiver Applications

Figure 14 illustrates the functional density advantages of the Parity Bus Series using the 74F657 in a typical microprocessor/data bus transceiver application. Note the 74F245 + 74F280B version would still require a 2-input AND gate and 3-State buffers for the PARITY and $\overline{\text{ERROR}}$ outputs. And, of course, it would require an order of magnitude higher input current than a single 74F657 would, and would also introduce much higher capacitive loading (for both the bus and the microcontroller).

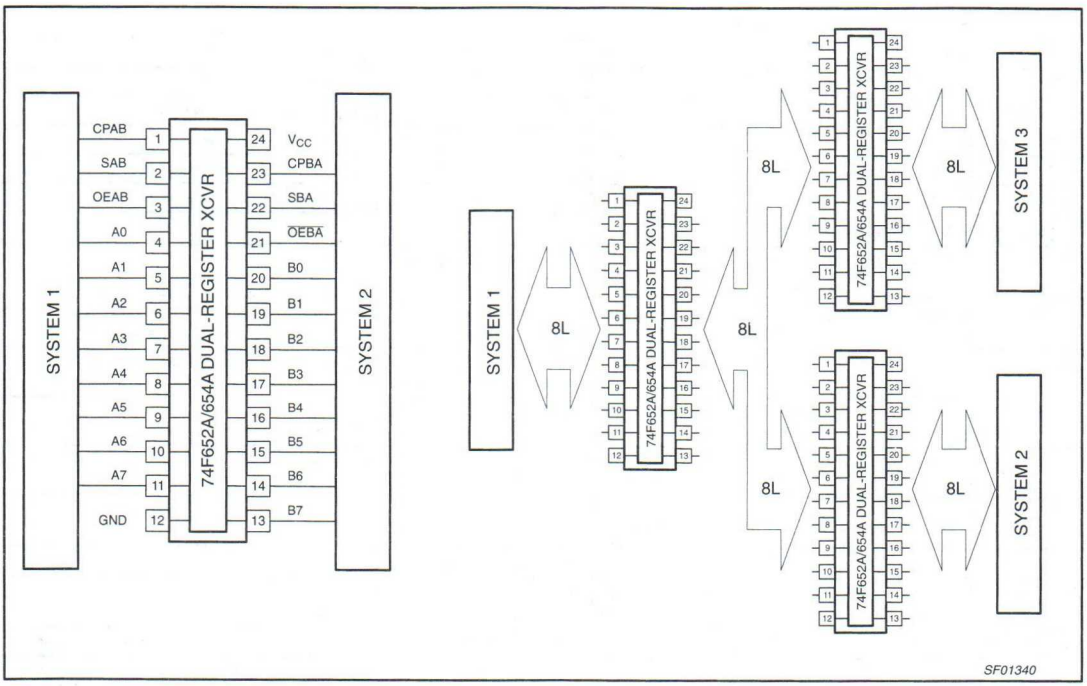


Figure 13. 74F Extended Octal-Plus Dual-Registered Transceiver Applications

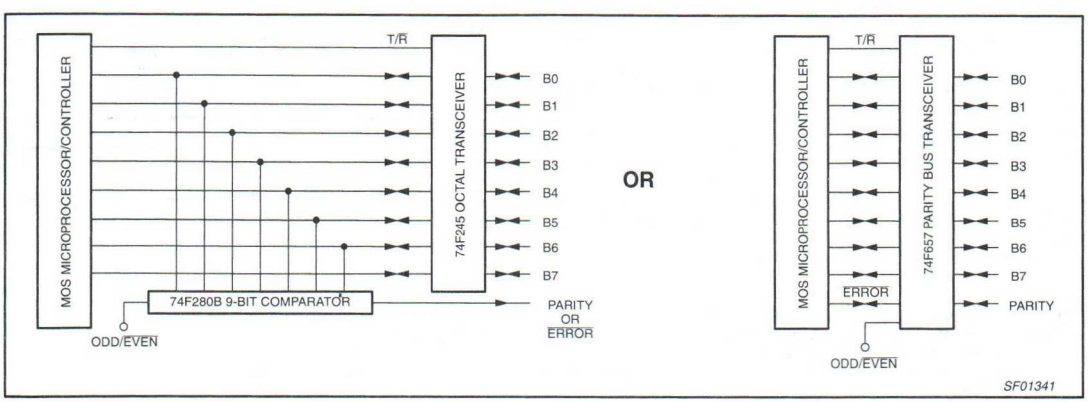


Figure 14. 74F657 Parity Bus Transceiver Applications

Table 3. The Extended Octal-Plus Family Capabilities Summary

Part Number	# Bits	Polarity	Output	Broad-side	I_{OH}/I_{OL} MIN	Storage	Speed	Parity	Comments
"Light-Load" buffer and Line Driver Functions									
74F455/456	8-bit	INV/NINV	3-St	Yes	–15/64mA	None	7.5ns	Yes	Multiple/Ctr Pkg. GND Pins, Σ_E, Σ_O = –15/64mA
74F540/541	8-bit	INV/NINV	3-St	Yes	–15/64mA	None	7.5ns	No	Broadside pinout of 74F240
74F655A/656A	8-bit	INV/NINV	3-St	Yes	–15/64mA	None	7.5ns	Yes	Σ_E, Σ_O = –15/64mA
74F827/828	10-bit	NINV/INV	3-St	Yes	–15/64mA	None	9.0ns	No	
"Light-Load" Register and Latch Functions									
74F821/822	10-bit	NINV/INV	3-St	Yes	–15/64mA	Reg	100MHz	No	Data, $\overline{MR}$, OE, & Clock EN Inputs
74F823/824	9-bit	NINV/INV	3-St	Yes	–15/64mA	Reg	100MHz	No	Data, $\overline{MR}$, OE, & Clock EN Inputs
74F825/826	8-bit	NINV/INV	3-St	Yes	–15/64mA	Reg	100MHz	No	Data, $\overline{MR}$, OE, & Clock EN Inputs
74F841/842	10-bit	NINV/INV	3-St	Yes	–15/48mA	Latch	100MHz	No	Data, $\overline{MR}$, OE, & LE Enable Inputs
74F843/844	9-bit	NINV/INV	3-St	Yes	–15/48mA	Latch	100MHz	No	Data, $\overline{MR}$, OE, & LE Enable Inputs
74F845/846	8-bit	NINV/INV	3-St	Yes	–15/48mA	Latch	100MHz	No	Data, $\overline{MR}$, OE, & LE Enable Inputs
"Light-Load" Transceiver Functions									
74F545	8-bit	NINV	A_N 3-St B_N 3-St	Yes Yes	–3/24mA –15/64mA	None None	7.0ns 7.0ns	No No	
74F550/551	8-bit	NINV/INV	B_N 3-St A_N 3-St	Yes Yes	–15/64mA –3/24mA	B_N-Reg A_N-Reg	10.5ns 10.5ns	No No	$A_N \rightarrow B_N$, ERROR, status registers, 50MHz $B_N \rightarrow A_N$, Multiple/Center Pkg. GND pins **
74F552	8-bit	NINV	B_N 3-St A_N 3-St	Yes Yes	–15/64mA –3/24mA	B_N-Reg A_N-Reg	10.5ns 10.5ns	Yes Yes	$A_N \rightarrow B_N$, PARITY, $\overline{ERROR}$, status registers $B_N \rightarrow A_N$, Multiple/Center Pkg. GND pins **
74F588	8-bit	NINV	A_N = 3-St B_N 3-St	Yes Yes	–3/24mA –15/64mA	None None	7.5ns 7.5ns	No No	 IEEE-488/GPIB w/line term. resistors
74F620/623	8-bit	INV/NINV	B_N 3-St A_N 3-St	Yes Yes	–15/64mA –3/24mA	None None	7.5ns 7.5ns	No No	$A_N \rightarrow B_N$ $B_N \rightarrow A_N$
74F621/622	8-bit	NINV/INV	B_N OC A_N OC	Yes Yes	OC/64mA OC/24mA	None None	13.0ns 12.5ns	No No	$A_N \rightarrow B_N$ $B_N \rightarrow A_N$
74F640	8-bit	INV	A/B 3-St	Yes	–15/64mA	None	7.5ns	No	$A_N \leftrightarrow B_N$
74F641/642	8-bit	NINV/INV	B_N OC A_N OC	Yes Yes	OC/64mA OC/20mA	None None	13.0ns 12.0ns	No No	$A_N \rightarrow B_N$ $B_N \rightarrow A_N$
74F646A/648A	8-bit	NINV/INV	A/B 3-St	Yes	–15/48mA	2 Reg	11.0ns	No	$A_N \leftrightarrow B_N$, registers for A_N & B_N ports, 80MHz (min.)
74F647/649	8-bit	NINV/INV	AB OC	Yes	OC/64mA	2 Reg	19.5ns	No	$A_N \leftrightarrow B_N$, registers for A_N & B_N ports, 40MHz (min.)
74F651A/652A	8-bit	INV/NINV	A/B 3-St	Yes	–15/48mA	2 Reg	11.5ns	No	$A_N \leftrightarrow B_N$, registers for A_N & B_N ports, 80MHz (min.)
74F653/654	8-bit	NINV/INV	B_N 3-St A_N OC	Yes Yes	–15/64mA OC/64mA	B_N-Reg A_N-Reg	11.0ns 20.0ns	No No	$A_N \rightarrow B_N$, B_N port = 85MHz (min.) $B_N \rightarrow A_N$, A_N port = 45MHz (min.)
74F657	8-bit	NINV	B_N 3-St A_N 3-St	Yes Yes	–15/64mA –3/24mA	None None	8.0ns 8.0ns	Yes No	$A_N \rightarrow B_N$, PARITY, $\overline{ERROR}$ = –15/64mA $B_N \rightarrow A_N$, Multiple/Center Pkg. GND pins
74F861/862	10-bit	NINV/INV	A/B 3-St	Yes	–15/64mA	None	10.0ns	No	$A_N \leftrightarrow B_N$
74F863/864	9-bit	NINV/INV	A/B 3-St	Yes	–15/64mA	None	10.0ns	No	$A_N \leftrightarrow B_N$
74F1245	8-bit	NINV	B_N 3-St A_N 3-St	Yes Yes	–15/64mA –3/24mA	None None	8.0ns 8.0ns	No No	$A_N \rightarrow B_N$, "Light-Load" pin-for-pin 'F245 replacement $B_N \rightarrow A_N$
74F2951/2952	8-bit	INV/NINV	A/B 3-St	Yes	–15/64mA	2 Reg	12.5ns	No	$A_N \leftrightarrow B_N$, registers for A_N & B_N ports, 80MHz (min.) **

NOTES:
All parameters are worst-case, unless otherwise specified.
3-St = 3-State
OC = Open Collector
Reg = LOW-to-HIGH edge clocked D-type register
Latch = HIGH logic level on the Latch Enable logic, data passes directly through D-type latch,
HIGH-to-LOW logic level transition of the Latch Enable, data is stored in the D-type latch.
** = These devices utilize standard FAST input structures producing input currents of +20µA and –0.6mA.
$\overline{MR}$ = Master Reset
OE = Output Enable

74FXXXX "Light Load" input products AN215

Major "Light Load" Input Features

- Patented "Light Load" NPN input structure
  - Normal Input pins = ±20μA per input
  - Transceiver I/O pins = ±70μA per I/O pin
  - Primarily capacitive loading = <10pF
- Ideal for MOS CPU, peripherals, and semi-custom bus interfaces
- Patented turn-OFF speed-up circuit
- No significant speed disadvantage – standard 74F speeds
- PC board transmission line drive capability: –15/64mA I_{OH}/I_{OL}
- "Broadside" design in 20-, 24-, and 28-pin slim-DIP packages
- "Light Load" family includes:
  - 19 Buffers and line driver parts
  - 19 Shift register, register and latch parts
  - 19 Transceivers (no storage)
  - 8 Dual registered transceivers
  - 7 Arithmetic functions

Introduction

The Philips Semiconductors 74F "Light Load" product line is a high performance, TTL bus compatible series of very low input bias current (±20μA), buffer/driver, transceiver, register, multiplexer and arithmetic MSI functions. The patented "Light Load", ±20μA NPN input structure, shown in Figure 1, combined with a unique input speed-up circuit (also patented) makes this product line ideal for interfacing with all MOS devices, without any speed degradation. When compared to the I_{IL} of standard FAST inputs of 600μA (larger for some other logic families) this "Light Load" input shows a 30:1 reduction in I_{IL} loading (600μA/20μA).

These devices were specifically designed to meet the requirements of buffering low output drive MOS VLSI/LSI devices from the rigorous loading environment PC board/motherboard buses and system backplanes. The "Light Load" inputs and improved speed performance make this product line ideal for interfacing to low output drive capability, slower MOS CPU, peripherals and semi-custom chips used in most state-of-the-art logic designs today. Using these "Light Load" input bus products, MOS chip outputs will only have to drive the small amount of distributed PC trace capacitance and inductance loading. The MOS device output drive capability is not wasted on drivers/transceivers with large DC input current drive requirements.

See Table 1 for a complete listing of the part numbers and functions of the "Light Load" product line.

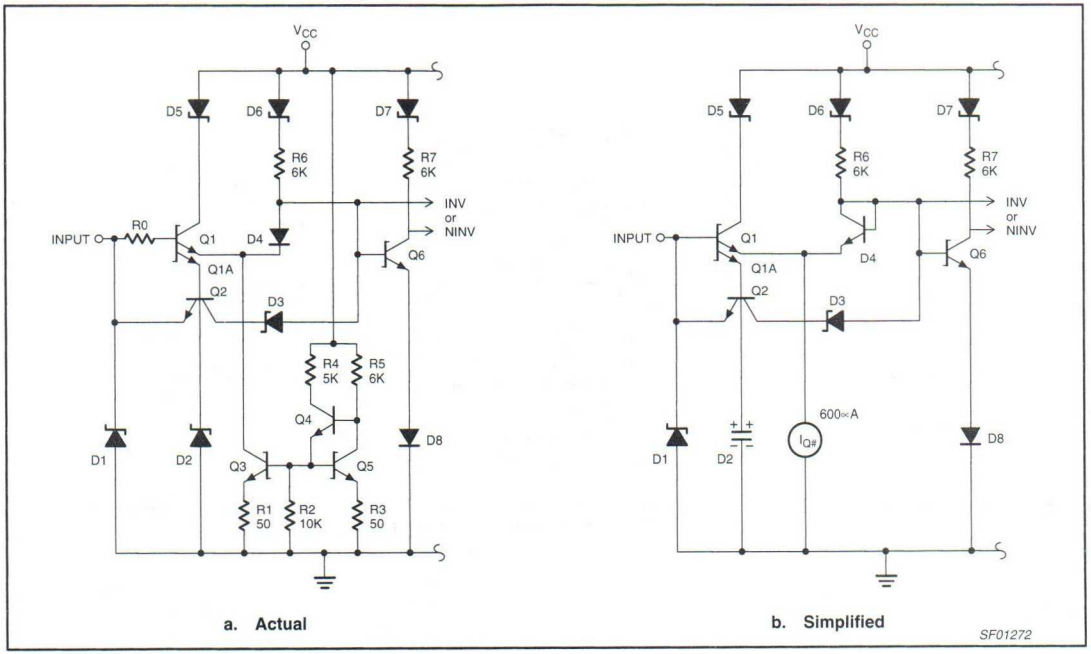


Figure 1. The "Light Load" and Speed-Up Circuit Input Structure (Actual & Simplified)

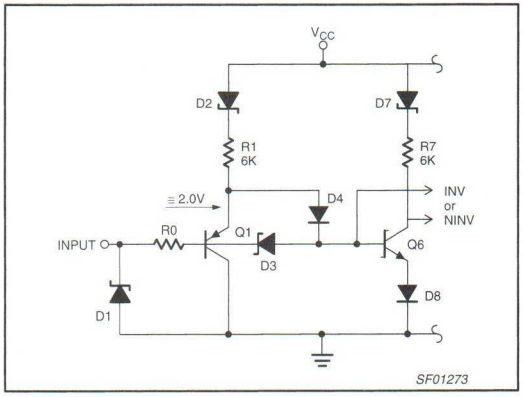


Figure 2. Future "Light Load" PNP Input

"Flow-Through" Design

Figure 3 illustrates the pin configurations of the 74F84X Latched Buffer series. Notice that all of the "Light Load" input data bus products use a "Flow-Through" design which allows logic signals to flow into one side and out of the other without crossing or folding back on signal paths such as the 74F24X octal series. Comparing the physical PC board signal bus path layout required for the 74F845 Octal Registered Buffer to that of the zig-zag signal path of the 74F240 Octal Inverting Buffer, you will see the significant advantages of this product line's "Flow-Through" design in simplifying the design and layout of large, bus-oriented PC boards.

The "Light Load" input product line combines "Flow-Through" design, high speed performance and high functional density into 20-, 24-, and 28-pin, 300-mil Slip-DIP packages significantly reducing system propagation delays, parts count, power dissipation, PC board area/complexity and, therefore, total cost while enhancing total system reliability.

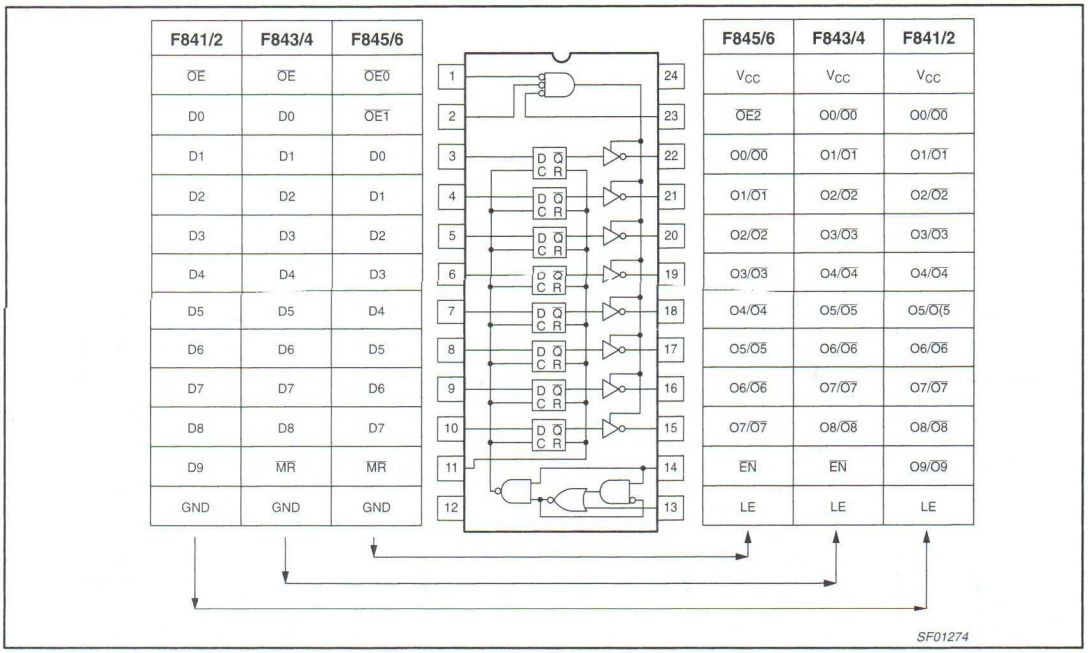


Figure 3. 74F84X Latched Buffer Pin Configurations

74FXXXX "Light Load" input products AN215

Input Structure – Differential Amplifier

Figure 1 shows the circuit diagram of the patented "Light Load" NPN input (Q1/3, R6, & D4) and the Turn-OFF Speed-Up circuit (Q2, D2, & D3). This input structure is actually a linear differential amplifier consisting of Q1, D4 and a constant current sink made up of Q3/4/5 and R1/2/3. The input bias current of this amplifier is less than ±20μA for V_I between 0.0V and 5.5V. The Turn-OFF Speed-Up circuit (D2/Q2/D3) quickly discharges Q6's base-collector stored-charge to ground. the following analysis assumes room temperature and 5.0V_{CC} operation.

The Q1's base is the input side of the differential amplifier and D4's anode is the reference side. When the input is HIGH (2.0V), Q1 is turned-ON and I_{CE} plus I_{BE} current flows into Q3's constant current sink network of ~600μA. Since D4's anode is clamped at 1.3V to 1.4V by the V_{BE} of Q6 plus D8's voltage drop, and since Q1's emitter voltage is pulling the cathode of D4 up to greater than ~1.4V (the 2.0V_{IH} minus Q1's 0.6V_{BE}), R6's (6K) current cannot flow through D4 and forward biases Q6's base-emitter.

Since Q6 is a Schottky clamped transistor, it has a V_{CEsat} ~0.5V. When Q6 is turned-ON by R6, the voltage at its collector drops to ~0.9V from ground (adding in D8 voltage drop), which turns-OFF the output totem-pole pull-down driver transistors and turns-ON the pull-up. This topic will be discussed in more detail in the next section (refer to Figure 4).

Input Structure – Constant Current Sink

The constant current sink produced by Q3/4/5 and R1/2/3/4/5 sinks a relatively constant 600μA to ground. this "current mirror" circuit drives the base-to-ground voltage of Q3 and Q5 to Q5 V_{BE} plus the voltage drop across R3. Since Q3 and Q5 are identical, the voltage drops across R1 will equal that of R3. Therefore, the current through R1 equals the current through R3 times the ratio of R3:R1.

The base bias currents for Q3 and Q5 is supplied by Q4. Because of the relatively high βs of Q3 and Q5 (>50), their base currents of ~10μA do not significantly effect the currents through R3 and R1 (β or BETA = transistor current gain). At 25°C and V_{CC} = 5.0V, R3's current is approximately equal to:

$$I_{R3} = [V_{CC} - (V_{BE-Q4} + V_{BE-Q5})]/(R3 + R5)$$

$$I_{R3} = (5.0V - 1.2V)/(50\Omega + 6000\Omega) \cong 600\mu A$$

Therefore:

$$I_{CE-Q3} \cong I_{R1} = I_{R5} \times (R3/R1) \cong 600\mu A$$

With Q1's β also greater than 50, the HIGH logic level input bias current is less than 20μA:

$$I_{OH} = I_{CE-Q3}/BETA_{Q1} \cong 600\mu A/>50) < 12\mu A$$

The "Light Load" PNP Input

We will soon be introducing a new product line of "Light Load" PNP devices. One of the first products will be the 74F821 through 74F826 Registered Buffers, which will have the same pin configurations and options as the 74F841 through 74F846 Latched Buffers (see Figure 3). The 74F82X series will provide a positive-going edge triggered clock input to its 8-, 9-, and 10-bit register storage parts versus the 74F84X series' HIGH level Latch Enabled latches.

With Philips Semiconductors latest oxide-isolated process, a new, high performance "Light Load" PNP input structure will soon be available. This new PNP input, shown in Figure 2, provides a high impedance AND input structure versus the NPN input OR input and reduces the chip power dissipation by eliminating the requirement for a constant current source for each input.

The PNP input is still a differential amplifier with the cathode of D3 referenced to 2 V_{BE} voltage drops from ground. When the input is HIGH ($V_{IH} \geq 2V$), no Q1 emitter-base current can flow because the anode of D3 is clamped to the 2 V_{BE}. As D4 forward biased with the current from R1, the output driver transistor (Q60 turns ON. When the input is LOW ($V_{IL} \leq 0.8V$), Q1's emitter-base junction is forward biased, which turns ON the β amplified emitter-collector current of Q1. When Q1 is ON, the anode of D4 is clamped OFF by the input V_{IL} voltage plus Q1's emitter-base drop (V_{IL} + $Q1_{VBE} \leq 0.8V + 0.6V = 1.4V$). Therefore, the input threshold at the base of Q1 is ≅ 1.4V (2 V_{BE}) at 25°C.

With the β of Q1 typically greater than 100, the V_{IL} input bias current is guaranteed to be less than 20μA. With the input HIGH, the input leakage is also guaranteed to be less than 20μA. The β amplification of Q1 is basically the only difference between this PNP input's 20μA I_{IL} and the standard diode input's I_{IL} of 600μA.

When the base of Q1 is switched LOW, the Schottky diode D3 provides a turn-OFF speed-up path to ground, which quickly discharges the base of the driver transistor (Q6).

Output Structures

A characteristic example of the output structures found throughout the 74FXXXX Light Load product line is the 74F657 Parity Bus Transceiver, which has two basic output designs. Figure 4 illustrates the74F657's output structure designs of these output structures: A_N Port's output (Figure 4b) is guaranteed to handle –3/+24mA (2.4/0.5V V_{OH}/V_{OL}), and the B_N Port (Figure 4a) can drive greater than –15/+64mA (2.0/0.55V V_{OH}/V_{OL}). The A_N Port is designed to drive the chip side of the PC board to backplane interface, while the B_N Port is capable of driving PC board data transmission lines and backplane signal line with a characteristic impedance as low as 70Ω.

Referring back to Figure 1a, the base drive current for Q9/10/11 comes from either R6 for an inverting output or R7, if the output is non-inverting. For the inverting case, D4 is back-biased when the base voltage applied to Q1 (≥2.0V_{OH}) and Q9 base drive is supplied from R6. Q9's base is clamped at the sum of base-emitter forward biased voltage drops of Q9/10/11 and Q12. Q12's base drive primarily comes from R10/11/12 when Q9/10/11 are ON.

When Q9/10/11 begin to turn-ON, the base drive for Q12 must first overcome the R13/D13 base clamp before current can flow into Q12's base. During the output voltage HIGH to LOW transition, this delay minimizes totem-pole feed-through current into the ground lead by allowing the collector of Q11 (Phase Splitter Transistor – Q_{PS}) to pull down toward 1 V_{BE} + 1 V_{CEsat} and, thereby, turning-OFF the Q13/14 Darlington totem-pole output pull-up driver before Q12 completely turns-ON.

When the gate input switches from V_{IH} to V_{IL} (≤ 0.8V), the charge stored in D2 discharges through the base-emitter of Q2. Q2 (through D3) quickly pulls the bases of Q9/10/11 toward ground. When the collector of Q9 rises high enough (~1.3V) to forward bias the Q12 base clamping network of D9/R8/R9/Q7/Q8, Q12 is quickly turned-OFF before the Q13/14 totem-pole pull-up can turn-ON. This design minimizes feed-through ground during the output voltage LOW to HIGH transition.

The 3-State, totem-pole output structures of both the A_N and B_N ports have Schottky blocking diodes, D15, in their pull-ups. Their purpose is to block leakage current form flowing into the outputs when V_{CC} is either open or shorted to ground. These diodes will not let current flow until the output voltage reaches 5.5V.

The I_{OS} limiting resistors, R15, limit the amount of current that can be sourced from the HIGH to ground. Note that R15 is 12Ω for the A_N outputs. Therefore, under the same conditions, the B_N output pull-up structure will be able to source 2.5 times more current than the A_N outputs.

Minimizing Ground Bounce

Refer to *Application Note AN213 "74F30XXX Family Applications"* for a detailed discussion of "ground bounce" and internal noise generation due to reduced ground lead inductance. When a TTL output switches fro LOW to HIGH or HIGH to LOW, some feed-through or crossover current will be injected into the ground lead of the IC while both the pull-up and pull-down output drive structures are ON simultaneously. The larger the number of switched outputs, the larger the feed-through current and "ground bounce".

"Ground bounce" directly affects the input threshold of a gate, and therefore, its noise sensitivity. The newer output structure design used in the "Light Load" NPN input product line allow all outputs to switch simultaneously with minimal "ground bounce".

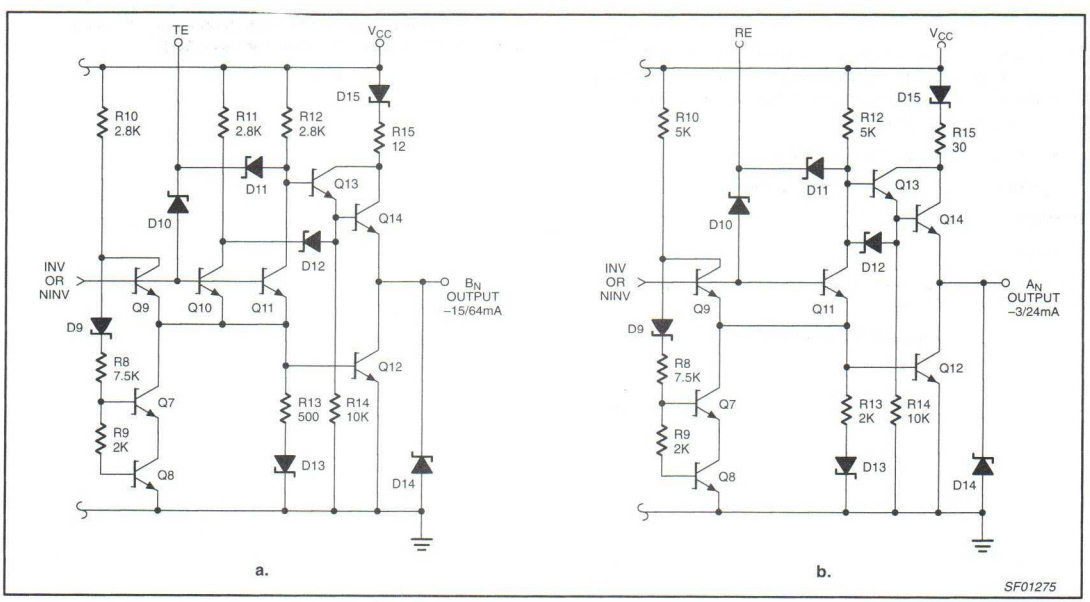


Figure 4. Two Typical "Light Load" Output Structures (74F657)

Table 1. The 74F "Light Load" Input Products

Part Number	# Bits	Polarity	Output	Broad-side	I_{OH}/I_{OL} MIN	Storage	Speed	Parity	Comments
"Light Load" Buffers and Line Drivers									
74F125/6	4-bit	NINV	3-St	No	–15/64mA	None	6.5ns	No	Separate output enables (F125 = $\overline{EN}$; F126 = EN)
74F365/6	6-bit	NINV	3-St	No	–15/64mA	None	7.5ns	No	Common output enable
74F367/8	6-bit	INV	3-St	No	–15/64mA	None	7.5ns	No	Two output enables controlling 3 outputs each
74F455/6	8-bit	INV/NINV	3-St	Yes	–15/64mA	None	7.5ns	Yes	Multiple/Ctr package GND pin, Σ_E, Σ_O = –15/64mA
74F540/1	8-bit	INV/NINV	3-St	Yes	–15/64mA	None	7.5ns	No	Broadside pinout of F240
74655A/6A	8-bit	INV/NINV	3-St	Yes	–15/64mA	None	7.5ns	Yes	Σ_E, Σ_O = –15/64mA
74F804/1804	6-bit	2I-NAND	3-St	No	–48/48mA	None	4.0ns	No	PNP Hex 2-Input NAND gate, F1804 has center supply pins
74F805/1805	6-bit	2I-NOR	3-St	No	–48/48mA	None	4.0ns	No	PNP Hex 2-Input NOR gate, F1805 has center supply pins
74F808/1808	6-bit	2I-AND	3-St	No	–48/48mA	None	5.0ns	No	PNP Hex 2-Input AND gate, F1808 has center supply pins
74F827/8	10-bit	NINV/INV	3-St	Yes	–15/64mA	None	9.0ns	No	
74F832/1832	6-bit	2I-OR	3-St	No	–48/48mA	None	5.5ns	No	PNP Hex 2-Input OR gate, F1832 has center supply pins
74F1240/1	8-bit	INV/NINV	3-St	No	–15/64mA	None	6.5ns	No	Light Load pin replacement for F240/1
74F1244	8-bit	INV/NINV	3-St	No	–15/64mA	None	7.0ns	No	Light Load pin replacement for F244
74F30240/4	8-bit	INV/NINV	OC	Yes	OC/160mA	None	15.0ns	No	Octal, 30Ω PC board data transmission line driver
"Light Load" Registers and Latches									
74F166	8-bit	NINV	3-St	Yes	–1/20mA	S/R	110MHz	No	Serial/Parallel-In, Serial-Out
74F195	4-bit	NINV	3-St	Yes	–1/20mA	S/R	110MHz	No	Serial/Parallel-In, Serial-Out
74F273	8-bit	NINV	3-St	No	–1/20mA	S/R	120MHz	No	D-type flip-flops
74F377	8-bit	NINV	3-St	No	–1/20mA	S/R	100MHz	No	D-type flip-flops
74F595	8-bit	NINV	3-St	Yes	–3/20mA	S/R	80MHz	No	S or P-In, Serial-Out with D-register output storage
74F597	8-bit	NINV	3-St	Yes	–3/20mA	S/R	80MHz	No	S or P-In, Serial-Out with D-register input storage
74F598	8-bit	NINV	3-St	Yes	–3/20mA	S/R	80MHz	No	F597 with multiplexed inputs and outputs
74F821/2	10-bit	NINV/INV	3-St	Yes	–15/64mA	Reg	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enables}}$ & Clock EN inputs
74F823/4	9-bit	NINV/INV	3-St	Yes	–15/64mA	Reg	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enables}}$ & Clock EN inputs
74F825/6	8-bit	NINV/INV	3-St	Yes	–15/64mA	Reg	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enables}}$ & Clock EN inputs
74F841/2	10-bit	NINV/INV	3-St	Yes	–15/48mA	Latch	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enables}}$ & LE Enable inputs
74F843/4	9-bit	NINV/INV	3-St	Yes	–15/48mA	Latch	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enables}}$ & LE Enable inputs
74F845/6	8-bit	NINV/INV	3-St	Yes	–15/48mA	Latch	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enables}}$ & LE Enable inputs

74FXXXX "Light Load" input products

AN215

Part Number	# Bits	Polarity	Output	Broad-side	I_{OH}/I_{OL} MIN	Storage	Speed	Parity	Comments
"Light Load" Transceivers/Latched or Registered Transceivers									
74F545	8-bit	NINV	A_N = 3-St	Yes	–3/24mA	None	7.0ns	No	Pin-for-pin replacement for the Intel 8286
			B_N = 3-St	Yes	–15/64mA	None	7.0ns	No	
74F588	8-bit	NINV	A_N = 3-St	Yes	–3/24mA	None	7.5ns	No	
			B_N = 3-St	Yes	–15/64mA	None	7.5ns	No	IEEE-488/GPIB with output line termination resistors
74F620/23	8-bit	INV/NINV	B_N = 3-St	Yes	–15/64mA	None	7.5ns	No	$A_N \leftrightarrow B_N$, A_N = –3/24mA
74F621/22	8-bit	NINV/INV	B_N = OC	Yes	OC/64mA	None	13.0ns	No	$A_N \leftrightarrow B_N$, A_N = OC/24mA
74F640	8-bit	INV	A/B = 3-St	Yes	–15/64mA	None	7.5ns	No	$A_N \leftrightarrow B_N$
74F641/42	8-bit	NINV/INV	A/B = OC	Yes	OC/64mA	None	13.0ns	No	$A_N \leftrightarrow B_N$
74F646/48	8-bit	NINV/INV	A/B = 3-St	Yes	–15/64mA	2-Reg	11.5ns	No	$A_N \leftrightarrow B_N$, Registers for A_N & B_N ports, 80MHz (Min.)
74F647/49	8-bit	NINV/INV	A/B = OC	Yes	OC/64mA	2-Reg	19.5ns	No	$A_N \leftrightarrow B_N$, Registers for A_N & B_N ports, 40MHz (Min.)
74F651/2	8-bit	INV/NINV	A/B = 3-St	Yes	–15/64mA	2-Reg	12.5ns	No	$A_N \leftrightarrow B_N$, Registers for A_N & B_N ports, 80MHz (Min.)
74F653	8-bit	NINV/INV	B_N = 3-St	Yes	–15/64mA	B_N-Reg	11.0ns	No	$A_N \rightarrow B_N$, B_N port = 85MHz (Min.)
			A_N = OC	Yes	OC/64mA	A_N-Reg	20.0ns	No	$B_N \rightarrow A_N$, A_N port = 45MHz (Min.)
74F657	8-bit	NINV	B_N = 3-St	Yes	–15/64mA	None	8.0ns	Yes	$A_N \leftrightarrow B_N$, Parity I/O, Odd/$\overline{\text{Even}}$ In & $\overline{\text{Error}}$ Out
74F861/2	10-bit	NINV/INV	A/B = 3-St	Yes	–15/64mA	None	10.0ns	No	$A_N \leftrightarrow B_N$
74F863/4	9-bit	NINV/INV	A/B = 3-St	Yes	–15/64mA	None	10.0ns	No	$A_N \leftrightarrow B_N$
74F1242/3	8-bit	INV	A/B = 3-St	No	–15/64mA	None	7.5ns	No	$A_N \leftrightarrow B_N$, Light Load pin replacements for F240/1
74F1245	8-bit	INV	A/B = 3-St	Yes	–15/64mA	None	6.5ns	No	$A_N \leftrightarrow B_N$, Light Load pin replacements for F245
74F30245	8-bit	NINV	B_N = OC	Yes	OC/160mA	None	15.0ns	No	Octal, 30Ω transmission line driver, B_N = 0.6mA I_{IL}
			A_N = 3-St	Yes	–3/24mA	None	7.0ns	No	A_N "Light Load" inputs
74F30640	8-bit	INV	B_N = OC	Yes	OC/160mA	None	15.0ns	No	Octal, 30Ω transmission line driver, B_N = 0.6mA I_{IL}
			A_N = 3-St	Yes	–3/24mA	None	7.0ns	No	A_N "Light Load" inputs
"Light Load" Transceivers/Latched or Registered Transceivers									
74F85	4-bit	INV/NINV	3-St	No	–1/20mA	None	14.5ns	No	4-bit magnitude comparator
74F280B	9-bit	NINV	3-St	Yes	–1/20mA	None	14.5ns	Yes	Parity generator/checker
74F604	16-bit	NINV	3-St/OC	Yes	–3/24mA	D-Reg	80MHz	No	Dual 8-bit registered octal multiplexer

NOTES:
All parameters are worst-case, unless otherwise specified.

3-St = 3-State
OC = Open Collector
Reg = LOW-to-HIGH edge clocked D-type register
Latch = HIGH logic level on the latch enable logic data passes directly through D-type latch
= HIGH-to-LOW logic level transition of the latch enable, data is stored in the D-type latch
S/R = Shift Register

Arbitration in shared resource systems AN216

INTRODUCTION

The need for more powerful and faster systems gave birth to multiprocessing and multi-tasking systems. But to achieve this, cost and reliability were not to be sacrificed. To reduce cost it is vital to share resources, but to do so requires reliable means of arbitration. In a multiprocessing system, a single bus may be shared between various processors or intelligent peripherals. The resources shared by processors (Figure 1) are generally termed as global resources and those shared between the local processor and the peripherals (Figure 2) are typically known as local resources. Whether local or global, there always exists a protocol that will connect and disconnect various devices to and from the shared resources. Various bus architectures in existence today have different ways of doing this.

No matter what the protocol of a specific bus, there is always a method which dictates how arbitration shall be performed between two or more devices. Some systems employ synchronous arbitration and some use an asynchronous approach. The third option is not to use arbitration at all, but instead to employ time-multiplexing. This is used mainly in data communications by dividing the common media into various time slots. Each processor (station) is assigned a predetermined time for using the media. If the station does not need to use the media during its assigned time-slot, it may pass control to the next station. This obviously results in an inefficient use of the bus bandwidth.

Synchronous and asynchronous arbitration have their advantages and disadvantages, and are both used in system designs. Some applications may even use a combination of the two. Generally, synchronous arbitration is used in systems where the designer can take the time to synchronize signals with the master clock. In synchronous arbitration the request is sampled on a clock edge, and therefore if it is asserted close to, but after the sampling clock edge, it will not be recognized until after a whole clock cycle. Today's applications, where speeds are being pushed to their limits, may not find that an optimal solution. Therefore, more and more designers tend towards asynchronous arbitration because it is much faster on the average. Since applications vary drastically from one to another, some may be better served by first-come-first-serve arbitration, some with fixed priority and some with dynamic priority.

In a first-come-first-served scheme, as the name implies, the request to be asserted first is selected first. All other requests made after the first are queued in their respective order of assertion. After the current request is serviced, the request asserted second will be selected, and so on. If the request just serviced is asserted again, before all other active requests are serviced, it will be placed at the end of the queue. In a fixed priority method all inputs have a hard-wired priority and cannot be changed. In a dynamic priority assignment, the user can change the priority depending upon the system needs. For example, processors performing vital tasks may be placed at a higher priority as compared to processors doing background tasks.

Arbitration, whether synchronous or asynchronous, always brings up the question of "metastability". A hard fact that relates itself all the way back to the beginning of the history of electronics. In its simplest definition, it is the state of a flip-flop that is neither a logic "1" nor a logic "0", and is a result of violations of its setup and hold times. This condition must be allowed and dealt with in arbitration and synchronization designs.

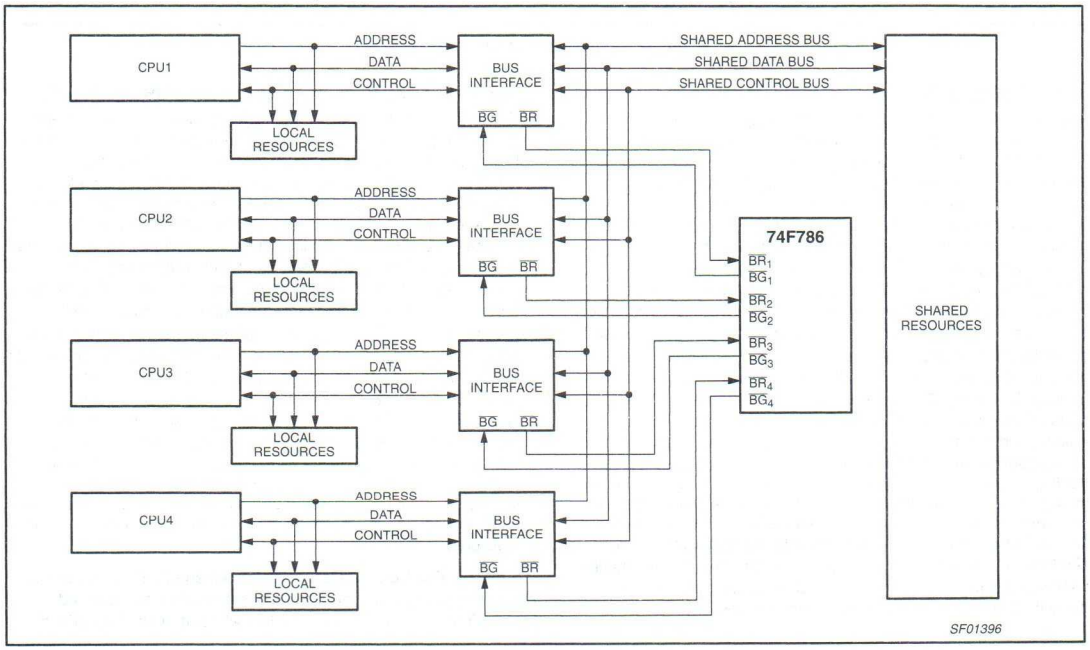


Figure 1. Sharing Global Resources

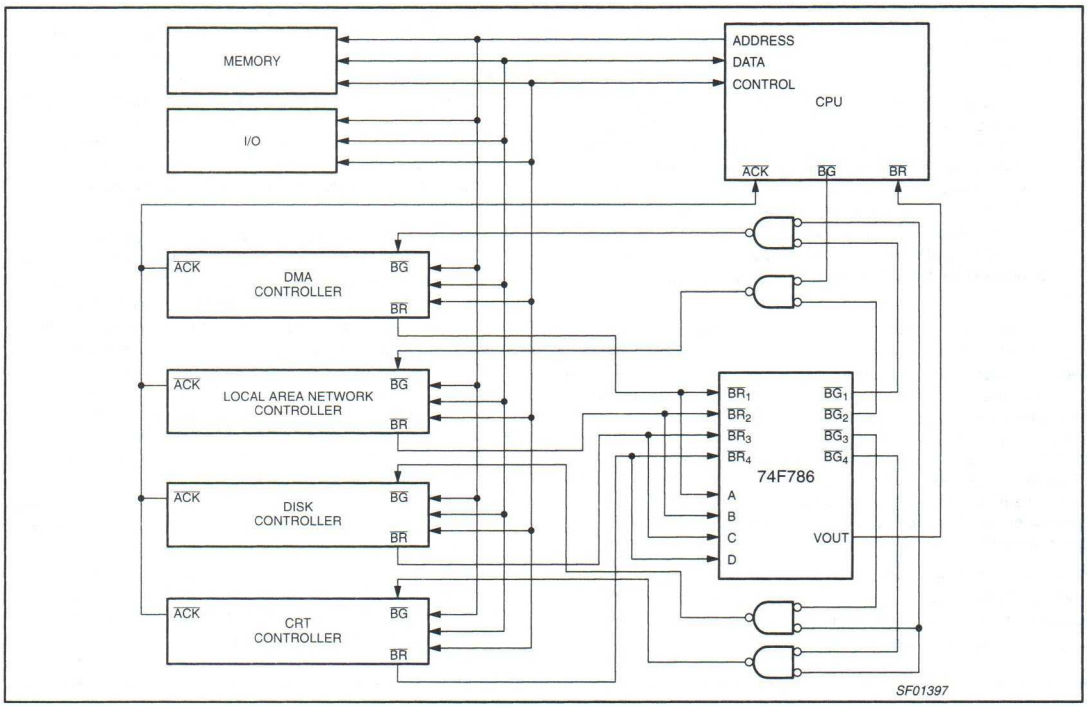


Figure 2. Sharing Local Resources

METASTABILITY

Various publications have discussed this subject and given recommendations for reducing but not completely eliminating this potential problem. Briefly the suggestions consist of using very fast flip-flops (with very small setup and hold times), using multiple flip-flops and delay lines and designing of metastable-hardened flip-flops. Please note that a metastable-hardened flip-flop does not necessarily mean that it will never enter a metastable state, but rather it is a flip-flop that is highly optimized to be used in applications where the system designer cannot guarantee the minimum setup and hold times specified by the manufacturer. Since, as of today, the design of a metastable free flip-flop is not practically possible, the next best thing that could be done is design of a flip-flop with significantly reduced setup and hold times and reduced propagation delays. This will ensure reduced probability of being in a metastable state. Since we still will have some probability of not meeting the minimum setup and hold times and potentially being in a metastable state, another requirement to be imposed on this flip-flop would be to hold its previous state and not to propagate this invalid state to its outputs until it has decided to settle in a "0" or a "1" state. By doing so, it could be guaranteed that the outputs of a flip-flop will never be in an undetermined state even though the flip-flop may internally be in a metastable state. The penalty that the user would expect to pay in such a design will be a propagation delay that can extend beyond the maximum specified in the data sheet.

74F786 — 4-INPUT ASYNCHRONOUS ARBITER

The key consideration when arbitrating for shared resources is that access may not be granted to more than one device at a given time. If this could be guaranteed, it would improve reliability. This Application note describes a product from Philips Semiconductors, which guarantees against simultaneous grants and does so at very high speeds. The Philips Semiconductors 74F786 (Figure 3) is a general purpose asynchronous bus arbiter designed to address the needs for real-time applications, where arbitration is desired between multiple devices sharing common resources. The design goal was to provide for a device, the outputs of which could be guaranteed against logic hazards (glitches), metastability and that no more than one output could be active at a given time. The arbiter has four Bus Request ($\overline{BR}_n$) inputs, which allow arbitration between two to four asynchronous inputs. The priority is determined on a first-come-first-served basis. Corresponding to each input is a separate Bus Grant ($\overline{BG}_n$) output, which indicates which one of the request inputs is served by the arbiter at a given time. All these outputs are enabled by a common enable ($\overline{EN}$) input. Also included on-chip, is a general purpose four-input AND gate that may be used to generate a bus request signal (Figure 2) or as an independent AND gate.

Since the Bus Request inputs have no inherent priority, the arbiter assigns priority to the incoming requests as they are received. Therefore, the first request asserted will have the highest priority.

When a Bus Request is received, its corresponding Bus Grant becomes active, provided $\overline{EN}$ is LOW, and no other Bus Grant is active. Typically, a Bus Grant is selected in 6.6ns from the time of assertion of a request input. If additional Bus Requests are made after the first request goes LOW, they are queued in their respective order, When the first request is removed, the arbiter services the request with the next highest priority, based upon a first-come-first-served algorithm.

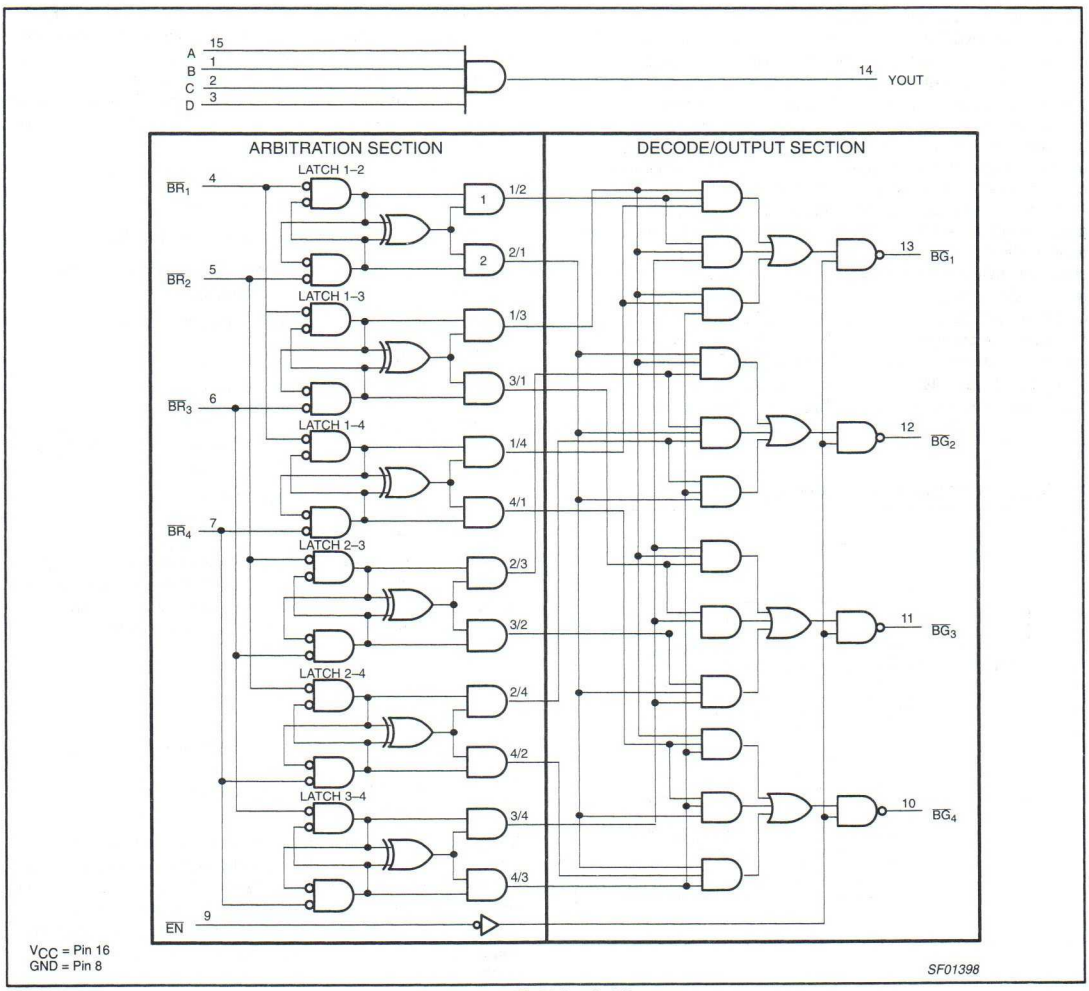
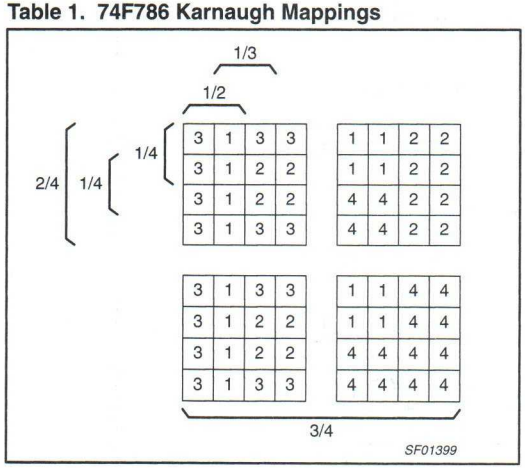


Figure 3. 74F786 Logic Diagram

Metastable-Free Outputs

The 74F786 logic diagram (Figure 3) consists of two sections: the arbitration section and the decoding/output section. Within the arbitration section lie six independent 2-input arbiters, each of which arbitrates between the two Bus Request ($\overline{BR}_n$) inputs connected to that specific arbiter. Each 2-input arbiter is comprised of two cross-coupled NOR gates, an Ex-OR gate and two AND gates. The cross-coupled NOR gates are designed so that they are securely latched when a Schottky diode voltage difference appears between the outputs of these NOR gates. The Ex-OR gate is designed so that its output will remain LOW until there is at least 1Vbe difference between its inputs. This creates a noise-margin of 1Vbe (base to emitter voltage)-1Vsky (Schottky voltage) = 0.3 Volts and assures that the output of the Ex-OR will not go HIGH until after the two NOR gates have resolved any contention problems. This guarantees that neither of the outputs of a 2-input arbiter can be in a metastable state, and also that both outputs cannot be HIGH simultaneously. As is clear from Figure 3, the first 2-input arbiter is responsible for deciding between the $\overline{BR}_1$, and $\overline{BR}_2$ inputs. Since both AND gate outputs cannot be HIGH at the same time, the other three possible configurations are: First, AND gate1 is HIGH indicating that $\overline{BR}_1$ arrived at the latch before $\overline{BR}_2$ (designated 1/2); second, AND gate2 is HIGH indicating BR_2 arrived before BR_1 (designated 2/1); and third, both AND gates are LOW, indicating that neither $\overline{BR}_1$ nor $\overline{BR}_2$ has been latched.

Table 1. 74F786 Karnaugh Mappings



Glitch-Free Outputs

The decode section of the 74F786 is responsible for insuring that the outputs do not glitch or produce a logic hazard. While there are three possible Karnaugh mappings, to produce an optimum decode section with a minimum number of transistors and balanced propagation times, the mapping in Table 1 was chosen. solving Table 1 for $\overline{BG}_1$–$\overline{BG}_4$ yields the following equations:

$$\overline{BG}_1 = 1/2 \cdot 1/3 \cdot 1/4 + 1/2 \cdot 1/3 \cdot 3/4 + 1/2 \cdot 1/4 \cdot 4/3$$

$$\overline{BG}_2 = 2/1 \cdot 2/3 \cdot 2/4 + 2/1 \cdot 2/3 \cdot 3/4 + 2/1 \cdot 2/4 \cdot 4/3$$

$$\overline{BG}_3 = 3/1 \cdot 3/2 \cdot 3/4 + 1/2 \cdot 3/1 \cdot 3/4 + 2/1 \cdot 3/2 \cdot 3/4$$

$$\overline{BG}_4 = 4/1 \cdot 4/2 \cdot 4/3 + 1/2 \cdot 4/1 \cdot 4/3 + 2/1 \cdot 4/2 \cdot 4/3$$

To see if a glitch can occur, let's take the worst possible case, that is, let $\overline{BR}_1$ beat $\overline{BR}_2$, 2 beat 3, 3 beat 4, and 4 beat 1 (a possible situation when all inputs are asserted simultaneously). Also, let's have the outputs of the arbitration section switch sequentially. Initially, all the variables in the equations are false (remember, the outputs of the arbitration section have three possible states). First, when 1/2 goes true, 2/1 must remain false. This eliminates several terms from playing a role in deciding which output becomes active. In fact, $\overline{BG}_2$ has been removed from the list and is no longer a contender. At this point, while all the outputs are HIGH (inactive), we have decided that $\overline{BG}_2$ will remain inactive. This leaves us with the following equations:

$$\overline{BG}_1 = 1/2 \cdot 1/3 \cdot 1/4 + 1/2 \cdot 1/3 \cdot 3/4 + 1/2 \cdot 1/4 \cdot 4/3$$

$$\overline{BG}_3 = 3/1 \cdot 3/2 \cdot 3/4 + 1/2 \cdot 3/1 \cdot 3/4 + \cancel{2/1 \cdot 3/2 \cdot 3/4}$$

$$\overline{BG}_4 = 4/1 \cdot 4/2 \cdot 4/3 + 1/2 \cdot 4/1 \cdot 4/3 + \cancel{2/1 \cdot 4/2 \cdot 4/3}$$

Similarly, when 2/3 goes true, 3/2 must remain false, which further eliminates a term from this set of 3 equations:

$$\overline{BG}_1 = 1/2 \cdot 1/3 \cdot 1/4 + 1/2 \cdot 1/3 \cdot 3/4 + 1/2 \cdot 1/4 \cdot 4/3$$

$$\overline{BG}_3 = \cancel{3/1 \cdot 3/2 \cdot 3/4} + 1/2 \cdot 3/1 \cdot 3/4 + \cancel{2/1 \cdot 3/2 \cdot 3/4}$$

$$\overline{BG}_4 = 4/1 \cdot 4/2 \cdot 4/3 + 1/2 \cdot 4/1 \cdot 4/3 + \cancel{2/1 \cdot 4/2 \cdot 4/3}$$

Now when 3/4 goes true, 4/3 must remain false. This eliminates $\overline{BG}_4$ from the contending list and the contest now is between $\overline{BG}_1$ and $\overline{BG}_3$ as indicated from the following equations:

$$\overline{BG}_1 = 1/2 \cdot 1/3 \cdot 1/4 + 1/2 \cdot 1/3 \cdot 3/4 + \cancel{1/2 \cdot 1/4 \cdot 4/3}$$

$$\overline{BG}_3 = \cancel{3/1 \cdot 3/2 \cdot 3/4} + 1/2 \cdot 3/1 \cdot 3/4 + \cancel{2/1 \cdot 3/2 \cdot 3/4}$$

When 4/1 goes true, 1/4 must remain false. Still no decision has been made, and is dependent on the two 2–4 and 1–3 latches not taken into account yet. In this case, the 2–4 latch status is a Don't Care, so the outcome of the 1–3 latch dictates the Bus Request granted:

$$\overline{BG}_1 = 1/2 \cdot 1/3 \cdot 3/4$$

$$\overline{BG}_3 = 1/2 \cdot 3/1 \cdot 3/4$$

If the 1–3 latch settles in the 1/3 state, $\overline{BR}_1$ gets the grant, and with 3/1 remaining false, $\overline{BG}_3$ will remain inactive. Similarly, if the 1–3 latch goes to the 3/1 state, $\overline{BR}_3$ gets the grant, and with 1/3 remaining false, $\overline{BG}_1$ will remain inactive.

Notice that the Bus Grant was given in this case without regard to the 2–4 latch. In fact, a quick review shows that neither the 2–3 latch nor the 1–4 latch played a role in making the decision. Each grant is dependent on the state of three latches. By the nature of the encoding logic, as the three activating latches are switched, three outputs are forced to remain in an inactive state. This insures a glitch-free output.

Let's assume that in the example above, the 1–3 latch goes to the 1/3 state, and hence, $\overline{BG}_1$ is asserted. At this time the other five latches in the circuit will be in 1/2, 4/1, 2/3, 2/4, and 3/4 states. If at this point $\overline{BR}_3$ is removed, then latch 3–4 changes from 3/4 to 4/3, and hence, $\overline{BR}_4$ steals the grant (with 1/2 · 4/1 · 4/3). This concludes that if three or more requests are asserted precisely at the same time, and one of them is removed prior to being serviced, it may cause premature termination of the present grant and assertion of another grant. Therefore, when using three or more Bus Requests, it is not advised to remove a request before being serviced. On the other hand, arbitration between two requests does not have this restriction. The user, if necessary, may decide to remove an ungranted request at his discretion.

Extended Propagation Delays

Since the outputs of the six 2-input arbiters cannot display a metastable condition, the Bus Grant outputs cannot display a metastable condition because the decoding/output section does not have any storage element to go metastable. Even though the Bus Grant outputs cannot go metastable, the cross-coupled NOR gates can. To determine the metastability characteristics of these NOR gates, the 74F786 was evaluated by Mr. Thomas J. Chaney of Washington University in St. Louis, Missouri, who is considered to be a leading expert in this field. Of the 19 devices supplied to him, Table 2 gives the test results from the fastest, the slowest and a typical package. In order to determine the Mean Time Between Package Unresolved (MTBPU) with the relative arrival times of the two input signal transitions uniformly distributed, the following formula is used:

$$MTBPU = [\exp(t'/\tau)]/[T_0(\text{Input 1 rate})(\text{Input 2 rate})].$$

where:

t' = Time given to resolve contention between inputs after they are asserted,

and τ and T_0 are device parameters derived from tests and can most nearly be defined as:

τ = A function of the rate at which a latch in a metastable state resolves that condition

T_0 = A function of the measurement of the propensity of a latch to enter a metastable state. T_0 is also a very strong function of the normal propagation delay of the device.

Solving for t', the resolving time measured from the arrival of the first input, and setting up the equation so the value of T_0 in Table 2 (given in ns) can be substituted directly, is:

$$t' = (\tau)\ln[(T_0)(3E14)].$$

The implication of the above equation is that, even though typical propagation dely through the arbiter is about 6.6ns, contention between inputs may extend this time significantly and can be calculated from Table 2.

Table 2. 74F786 Test Results for All Latches for Three Packages

All tests with $V_{CC} = 5.0V_{DC}$ and at Room Temperature

PACKAGE	LATCH	OUTPUT MEASURED	τ (ns)	T_0 (ns)	h (ns)	t' FOR 1 FAILURE/CENTURY (inputs at 10E6hz)
FASTEST	1–2	13	0.38	175E2	6.6	16.6
	1–3	13	0.39	79E2	6.6	16.4
	1–4	13	0.39	69E2	6.6	16.4
	2–3	12	0.38	109E2	6.6	16.1
	2–4	12	0.39	68E2	6.6	16.5
	3–4	11	0.38	181E2	6.6	16.3
SLOWEST	1–2	13	0.44	34E2	6.6	18.1
	1–3	13	0.44	17E2	6.6	18.0
	1–4	13	0.43	26E2	6.6	17.8
	2–3	12	0.44	16E2	6.6	17.9
	2–4	12	0.46	8E2	6.6	18.5
	3–4	11	0.44	29E2	6.6	18.2
TYPICAL	1–2	13	0.41	56E2	6.6	17.3
	1–3	13	0.42	24E2	6.6	17.2
	1–4	13	0.43	17E2	6.6	17.5
	2–3	12	0.43	18E2	6.6	17.4
	2–4	12	0.39	72E2	6.6	16.6
	3–4	11	0.41	49E2	6.6	17.2

Where h = typical propagation delay through the device.

Metastability tests for the 74F786 – 4-input asynchronous bus arbiter

AN217

Authors: Charles Dike and Naseer Siddique

INTRODUCTION

Under contract with Signetics, Mr. Thomas J. Chaney of Washington University, St. Louis tested a set of nineteen 74F786 samples (packages) to determine the metastable state recovery statistics for the circuits. The tests were conducted using a procedure described in a paper entitled *"Characterization and Scaling of MOS Flip-Flop Performance"*, (section IV), by T. Chaney and F. Rosenberger, presented at the CalTech Conference on VLSI, January 1979. The general test procedure was to test all 19 packages under one condition, then test the best, worst, and an average package in more detail. According to Mr. Chaney, the test results from the 19 packages formed one of the tightest groupings that he has ever seen. As the parts were numbered, package No. 7 had the fastest resolving times, No. 11 produced some of the slowest resolving times, and No. 1 had resolving times near the middle of the test results. This ranking of the test results from 3 packages remained the same throughout the balance of the test program, which supports the complete testing of only 3 packages. In general, the poorest performance resulted when the packages were heated to near 75°C with $V_{CC} = 4.5V_{DC}$ and the best performance resulted when the packages were cooled to near 0°C with $V_{CC} = 5.5V_{DC}$. The variation within one package caused by the temperature and V_{CC} changes was greater than the variation from package to package. It must be noted that none of the packages tested even approached the data sheet input to output worst case propagation delay of 10.5ns. All the packages tested for a single active output, had propagation delays of about 6ns. Typically, the parts with longer propagation delays also have slower resolving times. Thus, one would expect that the delay time needed to have only one failure in 32 years using a 10ns propagation delay part would be much longer than a value derived from just adding 10–6 = 4ns to the above calculations. thus it appears that the poorest performance measured in this study should be considered a measurement at the edge of the typical range for 74F786 parts.

It must also be noted that the tight grouping of this set of packages means that, when comparing differences between these test results, the measured error, as outlined in *"Measured Flip-Flop Responses to Marginal Triggering"*, IEETC, December 1983, is significant. This is illustrated in association with Table 5.

Test Program and Data

Throughout the test period, the connections to some of the package pins was as shown in Figure 1. The 4 input pins (1, 2, 3, and 15) to the AND gate were all grounded. The output of the AND, Pin 14, was left open. The output enable $\overline{EN}$ pin (9) was grounded. The power ground pin (8) was grounded and the V_{CC} power pin (16) was connected to V_{CC}. The 4 input pins to the arbiter (4, 5, 6, and 7) were treated as a group with two of the pins always receiving an input from the tester and the other two inputs always connected to V_{CC} through 1KΩ resistors. For any arbiter input pair configuration, there are two output (of the set: Pins 10, 11, 12, and 13) active. These two active output pins are each connected to a grounded 510Ω resistor, a grounded 30pF silvered mica capacitor, and a grounded scope probe (13pF). Thus each active output pin has a load of approximately 500Ω to ground and 50pF to ground (43pF plus 5 to 10pF wiring capacitor). In addition, the active output pin being tested was connected to the input of a comparator (3pF max.). The other input to this comparator was referenced to $1.5V_{DC}$. The $1.5V_{DC}$ reference voltage was not varied with V_{CC}. The two arbiter input signals generated by the tester were negative going pulses, each of the same width (approximately 100ns), which were time shifted relative to each other to produce metastable behavior in the arbiter circuit. This form of input causes only one of the two possibly active outputs to switch low.

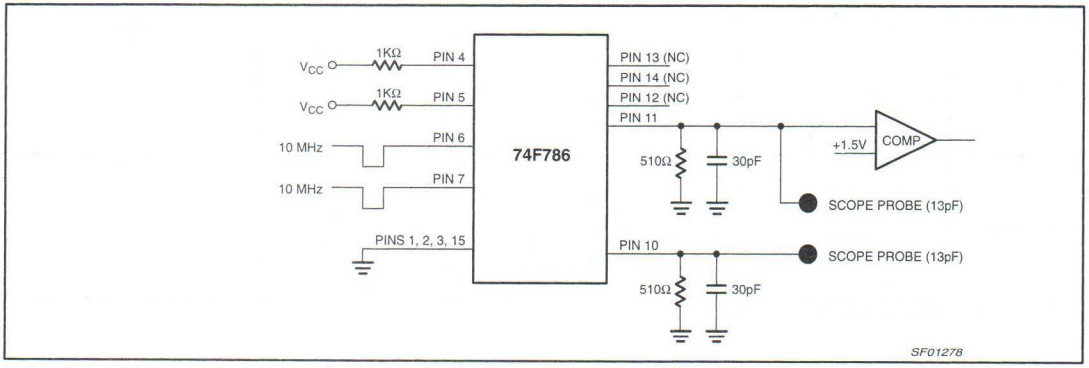


Figure 1. Test Setup for the 74F786

Metastability tests for the 74F786 – 4-input asynchronous bus arbiter

AN217

First Pass Through Packages

The test conditions used for the selection process from the 19 packages is shown in Figure 1 with the results shown in Table 1. The values reported in Table 1 were calculated with t′ (defined later) at 7.60 and 9.93ns. Note that the active inputs are Pins 6 and 7, and the output tested is Pin 11. The last column of this table is the period, after two requests, required to assure that the package would fail to resolve less than once per century. These numbers are based on the assumption that the 2 inputs are not synchronized and both are running at 10MHz (a 100ns clock period). It is assumed that the relative arrival times of the two input signal transitions are uniformly distributed over the clock period. The Mean Time Between Package Unresolved (MTBPU) is then:

$$MTBPU = \{\exp(t'/\tau]/[(T_0)\ (\text{Input1 rate})\ (\text{Input2 rate})]$$

where:

t′ = Time given to resolve contention between inputs after they are asserted and τ and T_0 are device parameters derived from tests and can most nearly be defined as:

τ = A function of the rate at which a latch in a metastable state resolves that condition, and

T_0 = A function of the measurement of the propensity of a latch to enter a metastable state. T_0 is also a very strong function of the normal propagation delay of the device. Also one century = 3E9 seconds.

Solving to t′, the resolving time measured from the arrival of the first request, and setting up the equation so the value of T_0 in Table 1 (given in ns) can be substituted directly gives:

$$t' = (\tau)\ 1n\ [(T_0)\ (3E14)]$$

As a result of the first round of tests, three packages were selected for further testing. Package 7 was selected as the fastest, package 11 as the slowest, and package 1 as a typical package.

Second Set of Tests

Using the logic diagram of the 74F786 (Figure 2), it is possible to construct Table 2. Note from Table 2 that thus far, all testing has been conducted on latch 3–4 (Pins 6 and 7). The second set of tests, conducted only on the 3 packages selected from the first set of tests, involved testing each of the 6 latches in the package to select the poorest performing latch in each package. This step also included testing each of the two active output pins for each input condition to select the path with the longest propagation delay.

The results of this comparison testing is shown in Table 3. The results from the table indicate that latches 1–2 and 3–4 have longer propagation delays than the middle four latches. This propagation delay difference is less than 0.4ns. For each of the conditions tested and reported in Table 3, there is a second active pin that could have been used to measure the performance of the latch under test. For package 1 only, the other active pin was tested for each of the latches. The results of this test are shown in Table 4. In theory, the results should be the same except for possible differences in propagation delay. The value of τ should be the same, but the value of T_0 could be different. In all 6 cases, the active pin previously not tested had a shorter propagation delay (function of T_0) than the active pin that was tested.

Table 4 also indicates something else. That is the accuracy with which the data in this report can be interpreted. Note that τ varies as much as 0.05ns, which is within the 0.06ns measurement error range of the test equipment used.

The results of the second set of tests are:

1. The 6 latches in each of the 3 selected packages behaved the same, relative to each other.
2. In all 3 packages, the latch selected is of little importance, therefore, Latch 1–2 was selected at random for further testing.
3. It was reasonable to continue with the 3 selected packages and to restrict further testing to Latch 1–2 and to only record data from Pin 13.

Table 1. Test Results for Inputs on Pins 6 & 7 and Output Measured at Pin 11

V_{CC} = 5.0V_{DC} at room temperature. t′ = 7.60 and 9.93ns

PACKAGE NUMBER	τ (ns)	T_0 (ns)	h (ns)	t′ FOR 1 FAILURE/CENTURY (INPUTS AT 10E6hz)
1	0.44	17E2	6.6	17.8
2	0.44	15E2	6.6	18.0
3	0.39	12E2	6.6	16.6
4	0.46	9E2	6.6	18.5
5	0.44	9E2	6.6	17.7
6	0.40	63E2	6.6	16.9
7	0.39	103E2	6.6	16.6
8	0.46	8E2	6.6	18.6
9	0.44	22E2	6.6	18.1
10	0.45	9E2	6.6	18.4
11	0.45	18E2	6.6	18.5
12	0.45	14E2	6.6	18.3
13	0.45	11E2	6.6	18.3
14	0.45	15E2	6.6	18.2
15	0.45	11E2	6.6	18.2
16	0.43	30E2	6.6	17.6
17	0.44	16E2	6.6	18.0
18	0.39	126E2	6.6	16.9
19	0.43	31E2	6.6	17.8

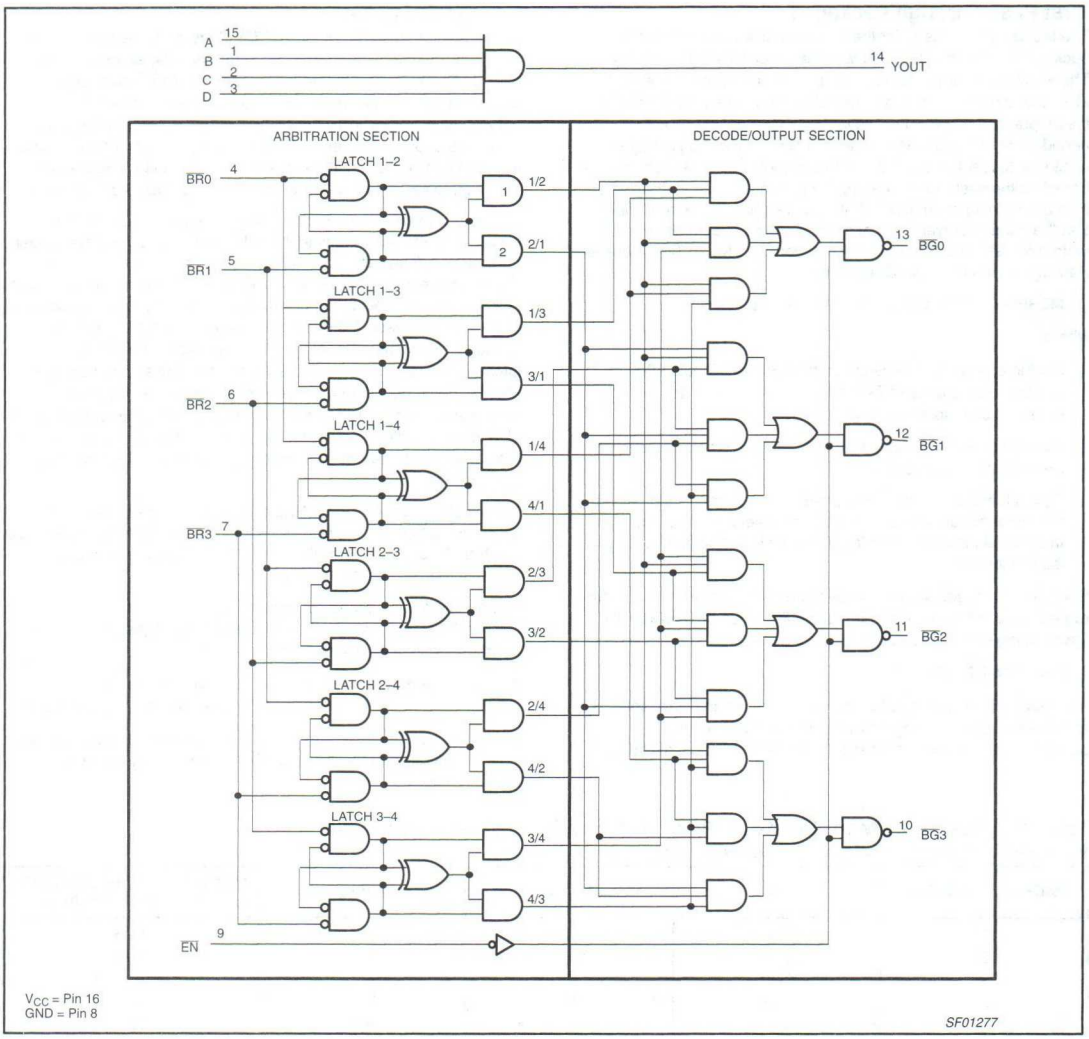


Figure 2. 74F786 Logic Diagram

Table 2. Arbiter Inputs and Corresponding Latches and Output Mapping

INPUT PINS	LATCH UNDER TEST	OUTPUT PINS ACTIVE
4,5	Latch 1–2	13,12 – test pin 13
4,6	Latch 1–3	13,11 – test pin 13
4,7	Latch 1–4	13,10 – test pin 13
5,6	Latch 2–3	12,11 – test pin 12
5,7	Latch 2–4	12,10 – test pin 12
6,7	Latch 3–4	11,10 – test pin 11

Table 3. Test Results for All 6 Latches from Packages 7, 11, and 1

All tests with V_{CC} = 5.0V_{DC} and at room temperature.

PACKAGE NUMBER	LATCH	OUTPUT MEASURED	τ (ns)	T_0 (ns)	h (ns)	t' FOR 1 FAILURE/CENTURY (INPUTS AT 10E6hz)
7	1–2	13	0.38	175E2	6.6	16.6
7	1–3	13	0.39	79E2	6.6	16.4
7	1–4	13	0.39	69E2	6.6	16.4
7	2–3	12	0.38	109E2	6.6	16.1
7	2–4	12	0.39	68E2	6.6	16.5
7	3–4	11	0.38	181E2	6.6	16.3
11	1–2	13	0.44	34E2	6.6	18.1
11	1–3	13	0.44	17E2	6.6	18.0
11	1–4	13	0.43	26E2	6.6	17.8
11	2–3	12	0.44	16E2	6.6	17.9
11	2–4	12	0.46	8E2	6.6	18.5
11	3–4	11	0.44	29E2	6.6	18.2
1	1–2	13	0.41	56E2	6.6	17.2
1	1–3	13	0.42	24E2	6.6	17.2
1	1–4	13	0.43	17E2	6.6	17.5
1	2–3	12	0.43	18E2	6.6	17.4
1	2–4	12	0.39	72E2	6.6	16.6
1	3–4	11	0.41	49E2	6.6	17.2

Table 4. Test Results for All 6 Latches from Package 1, Measured and/or Computed Different Ways

All tests with V_{CC} = 5.0V_{DC} and at room temperature.

PACKAGE NUMBER	LATCH	OUTPUT MEASURED	τ (ns)	T_0 (ns)	h (ns)	t' FOR 1 FAILURE/CENTURY (INPUTS AT 10E6hz)
1	1–2	13	0.41	156E2	6.6	17.3
1	1–2	*13	0.39	160E2	6.6	16.8
1	1–2	12	0.36	390E2	6.6	15.8
1	1–3	13	0.42	24E2	6.6	17.2
1	1–3	*13	0.39	101E2	6.6	16.5
1	1–3	11	0.36	137E2	6.6	15.6
1	1–4	13	0.43	17E2	6.6	17.5
1	1–4	*13	0.40	77E2	6.6	16.7
1	1–4	10	0.35	201E2	6.6	15.3
1	2–3	12	0.43	18E2	6.6	17.4
1	2–3	*12	0.40	63E2	6.6	16.7
1	2–3	11	0.37	88E2	6.6	15.5
1	2–4	12	0.39	72E2	6.6	16.6
1	2–4	*12	0.39	79E2	6.6	16.6
1	2–4	10	0.36	96E2	6.6	15.5
1	3–4	11	0.41	49E2	6.6	17.2
1	3–4	*11	0.40	99E2	6.6	16.9
1	3–4	10	0.36	246E2	6.6	15.7

NOTE:

* These values were computed using the subset of sample times used to measure the response from the other active pin in each case.

Temperature and Power Supply Variation Testing

The temperature and power supply variation testing was conducted on packages 1, 7, and 11. These tests were conducted on latch 1–2 only of each package (inputs 4 and 5, results measured at Pin 13). The results are shown in Table 5. The poorest performance was measured again from package 11. The worst case condition was measured at $V_{CC} = 4.5V_{DC}$ and the case temperature at 75°C and is shown in Table 5 as a **bold** entry. this line gives what could be considered the worst case measured performance from the 19 packages tested.

Table 5. Test Results for Latch 1–2 from Packages 7, 11 and 1

All tests with $V_{CC} = 4.5V_{DC} - 5.0V_{DC}$ and temperatures from 0°C to 75°C.

PACKAGE NUMBER	V_{CC}	TEMPERATURE	τ (ns)	T_0 (ns)	h (ns)	t' FOR 1 FAILURE/CENTURY (INPUTS AT 10E6hz)
7	4.5	3°C	0.37	260E2	6.6	16.3
7	5.5	3°C	0.38	67E2	6.6	15.8
7	4.5	75°C	0.44	70E2	6.6	18.4
7	5.5	75°C	0.43	37E2	6.6	17.7
11	4.5	3°C	0.41	88E2	6.6	17.4
11	5.5	3°C	0.39	64E2	6.6	16.6
11	4.5	Room Temp.	0.42	76E2	6.6	17.9
11	5.5	Room Temp.	0.42	30E2	6.6	17.5
11	4.5	75°C	0.50	15E2	6.6	20.3
11	**4.5**	**75°C**	**0.51**	**8E2**	**6.6**	**20.6**
11	5.5	75°C	0.47	19E2	6.6	19.3
1	4.5	Room Temp.	0.42	93E2	6.6	17.7
1	5.5	Room Temp.	0.42	48E2	6.6	17.1
1	4.5	75°C	0.44	69E2	6.6	18.7
1	5.5	75°C	0.44	37E2	6.6	18.3

A metastability primer

AN219

INTRODUCTION

When using a latch or flip-flop in normal circumstances (i.e., when the device's setup and hold times are not being violated), the outputs will respond to a latch enable or clock pulse within some specified time. These are the propagation delays found in the data sheets. If, however, the setup and hold times are violated so that the data input is not a clear one or zero, there is a finite chance that the flip-flop will not immediately latch a High or Low, but get caught half way in between. This is the metastable state, and it is manifested in a bi-stable device by the outputs glitching, going into an undefined state somewhere between a High and Low, oscillating, or by the output transition being delayed for an indeterminable time.

Once the flip-flop has entered the metastable state, the probability that it will still be metastable some time later has been shown to be an exponentially decreasing function. Because of this property, a designer can simply wait for some added time after the specified propagation delay before sampling the flip-flop output so that he can be assured that the likelihood of metastable failure is remote enough to be tolerable. On the other hand, one consequence of this is that there is some probability (albeit vanishingly small) that the device will remain in a metastable state forever. The designer needs to know the characteristics of metastability so that he can determine how long he must wait to achieve his design goals.

THE CHARACTERISTICS OF METASTABILITY

In order to define the metastability characteristics of a device, three things must be known: first, what is the likelihood that the device will enter a metastable state? This propensity is defined by the parameter "T_0". Second, once the device is in a metastable state, how long would it be expected to remain in that state? This parameter is tau (τ) and is simply the exponential time constant of the decay rate of the metastability. It is sometimes called the metastability time constant. The final parameter is the measured propagation delay of the device. Commonly, the typical propagation delays found in the databook are used for this, and it is designated "h" in the equations (although most designers are familiar with this value as T_{PD}). Now let's see how τ and T_0 are determined by measurements.

A TEST METHOD

Suppose we wanted to measure the metastability characteristics of a fictitious edge-triggered D-type flip-flop and we had a test system that would count each time the flip-flop is found in a metastable state at some time after a clocking edge. The first thing we would like to know about the flip-flop would be the "h" or typical propagation delay. We could measure the delay or look it up in the databook (of course, measuring the actual delay would allow more precise results). this fictitious flip-flop has an h of 7ns. In this test we decide to use a clock frequency of 10 MHz. This frequency is primarily a function of the test system's ability to assimilate the information. The data will run at 5MHz asynchronously to the clock and with a varying period. This frequency was chosen because at two transitions per cycle, the data signal produces 10 million points each second where it is possible for the flip-flop to go into a metastable state, an average of one point for each clock pulse. An important point about the characteristic of the data signal in relation to the clock is that the data transitions must have an equal probability of occurring anywhere within the clock period or the results could be skewed. In other words, we need to have a uniform distribution of random data transitions (High and Low) relative to the clocking edge.

The first measurement we take is to determine the number of times the device is still in a metastable state 8ns after the clock edge. With this device there are 792 failures after 1 billion clock cycles. Changing the time to 9ns, we measure 65 failures after another 1 billion cycles. Because metastability resolves as an exponentially decaying function, the two points define the exponential curve and they can be plotted as shown in Figure 1. An equivalent plot can be made using a semilog scale as in Figure 2. The slope of the line drawn through the two points represents τ. with these two points the τ can be determined by equation (1):

$$\tau = \frac{t_2 - t_1}{ln\ (N_1/N_2)} \quad (1)$$

where N_1 and N_2 are the number of failures at times t_1 and t_2, respectively.

Working through the numbers gives us a τ of 0.40ns. τ of this order is representative of the FAST line of flip-flops.

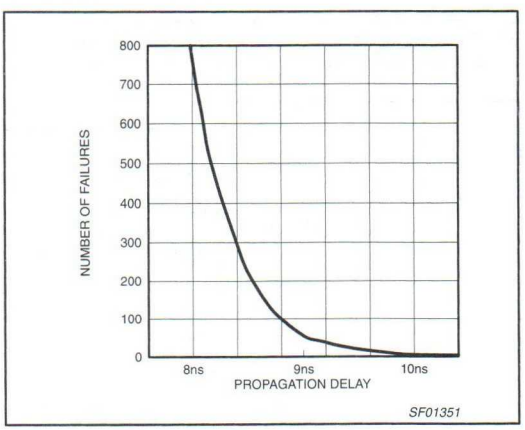


Figure 1. Exponential Decay of Failures

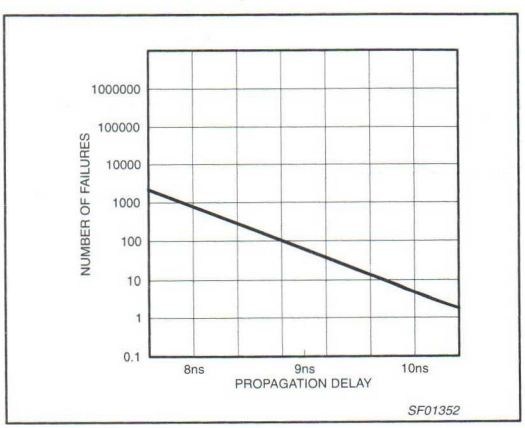


Figure 2. Semi-Log Graph of Failures

Earlier we stated that T_0 is an indicator of the likelihood that the device will enter a metastable state. Now we will attempt to explain it. At 9ns after the clock, we observed 65 failures in 1 billion clock cycles. Since the data transits on average once per clock cycle and the period of this clock is 100ns, from equation (2) we can say that there appears to be an aperture about 0.0065 picoseconds wide at the input of the device that allows metastability to occur for 9 or more nanoseconds. Another way of explaining the same thing would be to suppose that if 1 billion data transitions were uniformly and randomly distributed over a clock period of 100ns, you would expect 65 of these transitions to cause the outputs to go into a metastable state and remain there for at lease 9ns.

$$(2) \qquad T_9 = \frac{N_9 P_C}{N_{C9}}$$

Where N_{C9} is the number of clocking events at 9ns (in this instance, 1 billion), P_C is the period of the clock, and N_9 is the number of failures recorded at 9ns.

By the same reasoning, the window at 8ns appears to be 0.0792 picoseconds wide. It seems to have grown because there are, of course, more failures after 8ns than after 9ns. This aperture has been normalized by researchers to indicate the effective size of the aperture at the clock edge, or time zero. Unfortunately, the normalization process tends to obscure the interpretation of T_0. T_0 can be calculated using equation (3). Figure 3 is an extension of Figure 2 and shows the relationship of T_0, h, and τ.

$$(3) \qquad T_0 = T_8 e^{\left(\frac{8ns}{\tau}\right)}$$

or equivalently,

$$T_0 = T_9 e^{\left(\frac{9ns}{\tau}\right)}$$

In this case T_0 is 38.4 microseconds and this value is again typical of the FAST line of products.

Figure 3 is an extension of Figure 2 and gives a graphic indication of T_0. The number of failures plots on the same scale as the aperture size but the number of failures is dependent on the number of clock cycles used in the test (we always used 1 billion in this paper) and the ratio of data transitions to clock pulses (1:1 in this paper). On the other hand, the aperture size is independent of these things.

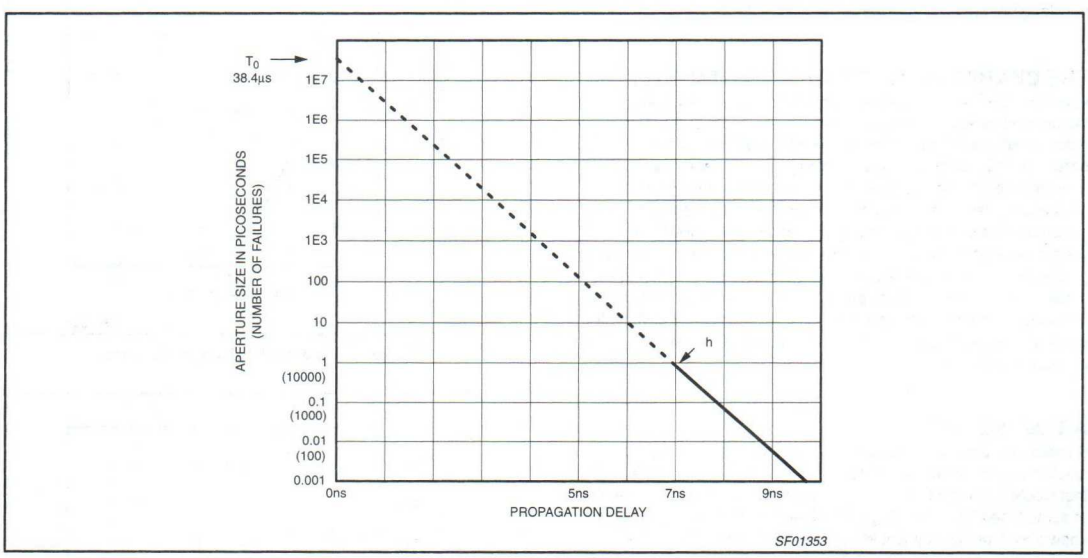


Figure 3. Extended Semi-Log Graph

MTBF

Having determined the T_0 and τ of the flip-flop, calculating the mean time between failures (MTBF) is simple. Suppose a designer wants to use the flip-flop for synchronizing asynchronous data that is arriving at 10MHz, he has a clock frequency of 25MHz, and has decided that he would like to sample the output of the flip-flop 15ns after the clock edge. He simply plugs his numbers into equation (4).

$$\text{(4)} \qquad \text{MTBF} = \frac{e^{\left(\frac{t'}{\tau}\right)}}{T_0 f_C f_i}$$

In this formula, f_C is the frequency of the clock, F_i is the average input event frequency, and t' is the time after the clock pulse that the output is sampled (of course t' > h). In this situation, the f_i will be twice the data frequency because input events consist of both Low and High data transitions. For the numbers above, the MTBF is one million seconds, or about one failure every 11.6 days. If the designer would have tried to sample the data after only 10ns, the MTBF would have been 3.8 seconds.

Metastability literature can be very confusing because several companies use different nomenclature and often the fundamental parameters are obscured by scale factors, so it is important that the user understand MTBF. Let's try a thought experiment to determine the correct MTBF formula. We know the size of the aperture at 8ns, so we need to know how often that window will occur. This is supplied by the clock period. This gives a ratio of window size to clock period and gives us the likelihood of a transition within the clock period causing a metastable state that lasts beyond the 8ns point. Now we need to know the number of input events per clock period to determine the MTBF at 8ns. This is supplied by the average input event period and produces the equation below where P_C and P_i are the periods of the clock and input events, respectively.

$$\text{(5)} \qquad \text{MTBF} = \frac{1}{T_8 \frac{1}{P_C} \frac{1}{P_i}} = \frac{1}{T_8 f_C f_i}$$

This gives the MTBF for 8ns, but how can the formula be developed to handle other times? It has been stated in this paper that the rate of decay of metastable events is an exponential function with a time constant of τ. Using this information gives the equation below, where t' is the time after the clock pulse that the output is sampled.

$$\text{(6)} \qquad \text{MTBF} = e^{\frac{\left(\frac{t'-8ns}{\tau}\right)}{T_8 f_C f_i}} = \frac{e^{\left(\frac{t'}{\tau}\right)}}{T_8 e^{\left(\frac{8ns}{\tau}\right)} f_C f_i} = e^{\frac{\left(\frac{t'}{\tau}\right)}{T_0 f_C f_i}}$$

A point should be made here about MTBF. This is the mean time between failures, and as such, does not indicate the average time between failures. In fact, in this situation, the MTBF is the time before which there is a 63.2% probability that a failure would have occurred. Suppose a device has a MTBF of one million seconds like the example above; because the MTBF is an exponential function, there is a 9.5% probability that a failure will occur in the first 1.16 days of operation. This might cause the user to feel that the device is failing more than expected. The user would find that 50% of his failures would occur within 8 days. Figure 4 gives a visual interpretation of this idea: time constant one represents one million seconds, in this case.

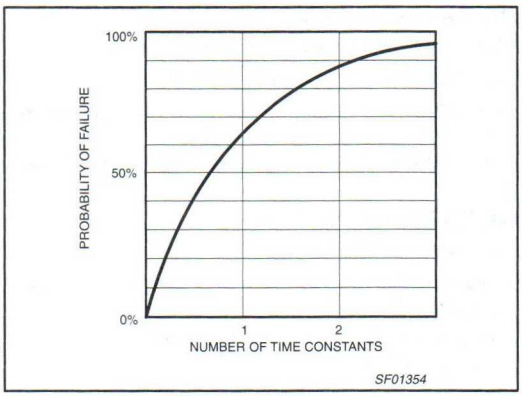


Figure 4.

RECENT DEVELOPMENTS

The quest for better metastability characteristics in flip-flops has recently resulted in the development of flip-flops with τs significantly less than 0.40ns. Perhaps the most notable of these is the Philips Semiconductors 74F50XXX series with typical τs of 135ps. The specifications of these new products can cause confusion among the uninitiated because the typical T_0 on these devices is 9.8 million seconds, or about 113 days. This is an example of how the normalization process obscures the interpretation of T_0. In the newest products, the τs have decreased faster than the normal propagation delays primarily due to speed limitations of the outputs.

Using the example above, and calculating T_7 from equation (3) we see that the window at h is 0.965ps. Now let's assume that we have a device with the same size window (0.965ps) at h, and an h of 7ns. The difference between this device and the previous example is that this device has a τ of 150ps. clearly, if the device has the same h and the same size of window at h but a smaller τ, the device is better. But let's calculate the T_0.

$$\text{(7)} \qquad T_0 = T_7 e^{\left(\frac{7ns}{\tau}\right)}$$

T_0 = 178 million seconds!

Comparing the T_0 of any two devices does not show which device is superior. However, one can expect that the device with the lower τ is superior in all but the most peculiar circumstances.

SUMMARY

This paper is intended to introduce the reader to the terms he will be dealing with regarding metastability and it is hoped that this introduction will help him to digest the more in-depth papers that he will be reading. Philips Semiconductors uses the parameters described by Thomas Chaney of Washington University in St. Louis, Missouri because they are fundamental and the better metastability papers generally use these parameters. For further reading on the subject, the article "Metastable behavior in digital systems" by Lindsay Kleeman and Antonio Cantoni published in *IEEE Design & Test of Computers* in December of 1987, is recommended.

Synchronizing and clock driving solutions – using the 74F50XXX family

AN220

THE 74F50XXX FAMILY

- 74F5074 synchronizing dual D-type flip-flop
- 74F50728 synchronizing cascaded D-type flip-flop
- 74F50729 synchronizing dual D-type flip-flop with edge-triggered set and reset
- 74F50109 synchronizing dual J-$\overline{K}$ positive edge-triggered flip-flop

MAJOR FAMILY FEATURES

- Metastable immune characteristics
- Propagation delay skew and output to output skew guaranteed to be less than 1.5ns
- Balanced output currents for clock driver applications ($I_{OH} = I_{OL} = 20mA$)

INTRODUCTION

The Philips Semiconductors 74F50XXX series of products have been designed to resolve synchronization problems and at the same time produce complementary metastable/immune outputs with remarkably small skews useful in clock driving applications. The 74F5074 and 74F50109 are pin and function compatible replacements of the 74F74 and 74F109 respectively. The 74F50728 consists of two pair of cascaded D-type flip-flops, and the 74F50729 is a pin compatible replacement for the 74F74 with edge-triggered set and reset inputs.

SYNCHRONIZATION

Synchronizing incoming signals to a system clock has proven to be costly, either in terms of time delays or hardware. In order to synchronize a signal, a flip-flop is normally used to 'capture' the incoming signal. When a flip-flop is used in this mode, its setup and hold times are occasionally violated. Whenever this occurs, the flip-flop can enter a metastable state causing the outputs to glitch, oscillate, enter an intermediate state or change state in some abnormal fashion. Any of these conditions could cause a system to crash. To minimize this risk, flip-flops are often cascaded so that the input signal is captured on the first clock pulse and released on the second clock pulse (see Figure 1). This gives the first flip-flop about one clock period minus its propagation delay and minus the second flip-flop's clock-to-Q setup time to resolve any metastable condition. This method greatly reduces the probability that the outputs of the synchronizing device may display an abnormal state, but the trade-off is that one clock cycle is lost to synchronize the incoming signal. Often two separate flip-flop packages are required to produce the cascaded flip-flop circuit.

The 74F50XXX series of products have five design features that cause them to be immune from metastability problems. First, the flip-flops are designed so that their outputs cannot change state until any internal metastability has been resolved. This assures that the outputs will not glitch, oscillate, enter an intermediate state, or change state in some abnormal fashion. Second, the setup and hold time window has been minimized to reduce the likelihood of internal flip-flops entering a metastable state. Third, the internal flip-flops have specifically been designed to exit a metastable state as rapidly as possible. Fourth, the Clock-to-Q propagation delays through the part have been made as short as possible. Finally, Philips Semiconductors has used the best oxide-isolated process available to make these products the best synchronization solutions possible.

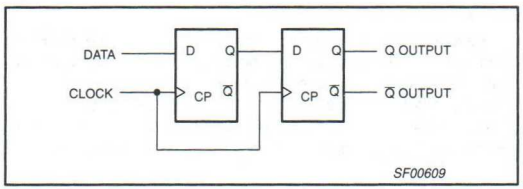


Figure 1. Cascaded Flip-Flops

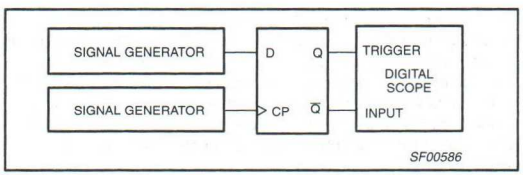


Figure 2. Test Setup

METASTABLE IMMUNITY

Philips Semiconductors uses the term 'metastable immune' to describe characteristics of some of the products in its FAST family, specifically the 74F50XXX family which presently consists of 4 products. This term means that the outputs will not glitch or display an output anomaly under any circumstances including setup and hold time violations. This claim is easily verified on the 74F5074.

When a test is performed (see Figure 2) where two independent signal generators are running at nearly the same frequency (in this case 10MHz clock and 10.02MHz data) the device-under-test operates continuously in the region where metastability can occur. If the Q output is then used to trigger a digital scope set to infinite persistence the $\overline{Q}$ output will build a waveform.

When the device-under-test is a 74F74 (which was not designed with metastable immune characteristics) the waveform appears as shown in Figure 3. This figure clearly shows that the Q output can vary in time with respect to the Q trigger point. It also implies that the Q or $\overline{Q}$ output waveshapes may be distorted. This can be verified on an analog scope with a micro-channel plate CRT. Perhaps of even greater interest are the dots running along the 3.5 volt line in the upper right hand quadrant. These show that the $\overline{Q}$ output did not change state, even though the Q output glitched to at least 1.5 volts, the trigger point of the scope.

When the device-under-test is a metastable immune part, such as the 74F5074, the waveform appears as shown in Figure 4. The 74F5074 $\overline{Q}$ output does not vary with respect to the Q trigger point even when the part is driven into a metastable state. Any tendency towards internal metastability is resolved by Philips Semiconductors patented circuitry. If a metastable event occurs within the flip-flop the only outward manifestation of the event will be an increased Clock-to-Q/$\overline{Q}$ propagation delay. This propagation delay is, of course, a function of the metastability characteristics of the device (see below).

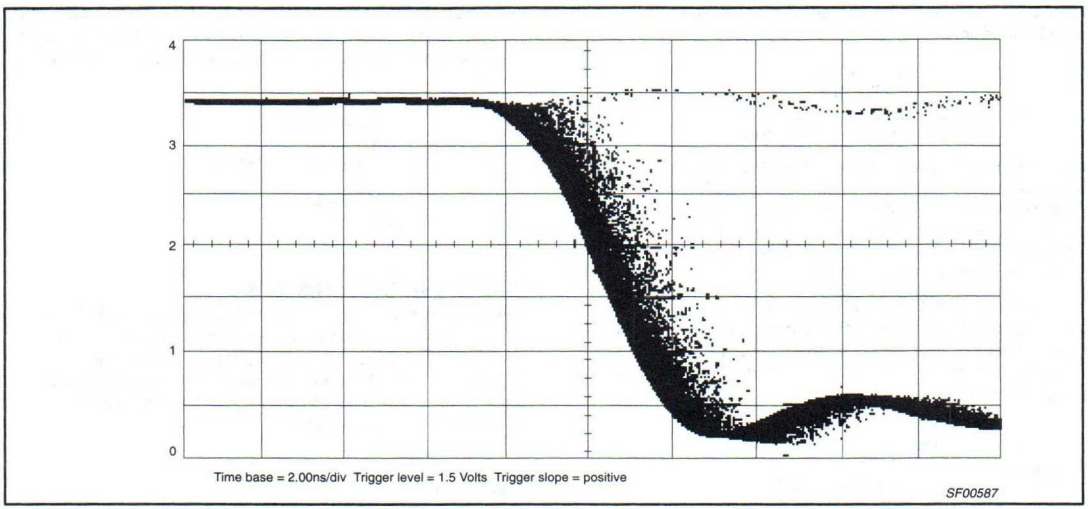


Figure 3. 74F74 $\overline{Q}$ Output Triggered by Q Output, Setup and Hold Times Violated

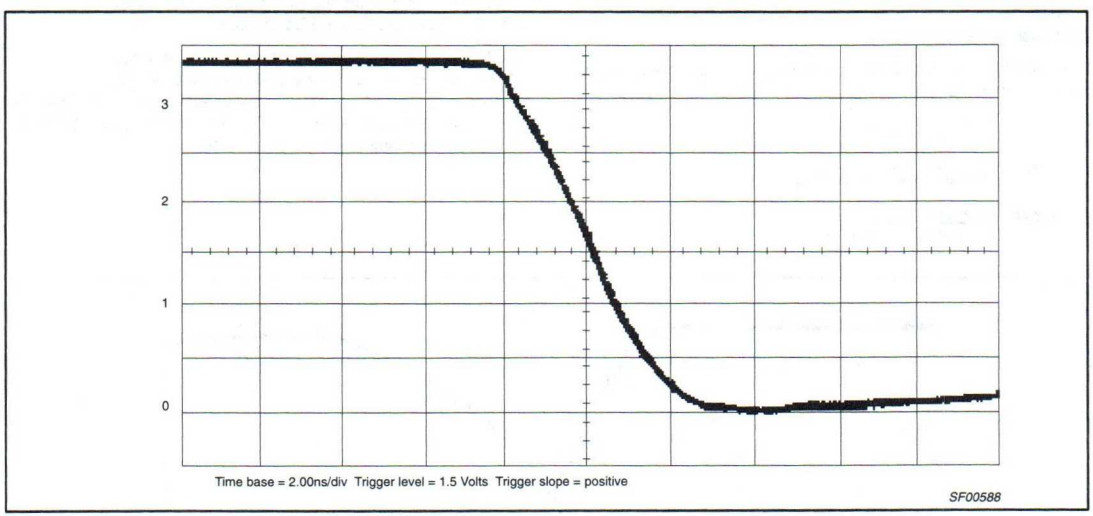


Figure 4. 74F5074 $\overline{Q}$ Output Triggered by Q Output, Setup and Hold Times Violated

METASTABILITY CHARACTERISTICS

In order to define the metastability characteristics of these products, Philips Semiconductors has chosen to use the parameters described by Thomas J. Chaney and Fred U. Rosenberger of Washington University in St. Louis, Missouri in their paper "Characterization and Scaling of MOS Flip-flop Performance in Synchronous Applications" in the *Proceedings of the Caltech Conference on VLSI*, January 1979. These parameters were chosen because they are fundamental and the best papers written on metastability use these parameters.

The first parameter to be considered is T_0. T_0 is a function of the propensity of a latch to enter a metastable state. It is also a very strong function of the normal propagation delay of the device and is generally given in units of seconds. The second parameter is h. It is the propagation delay from Clock-to-Q through a device under normal (i.e., no internal metastability) operation. The final parameter is tau (τ). Tau is the exponential time constant of the rate at which a latch in a metastable state resolves that condition and is typically specified in tenths of nanoseconds. Tau is generally the most important of the defining parameters.

Synchronizing and clock driving solutions – using the 74F50XXX family

AN220

To determine the Mean Time Between Failures (MTBF), the following formula is used:

$$MTBF = \frac{\left[\exp\left(\frac{t'}{\tau}\right)\right]}{[T_0(\text{clock rate})\ (\text{input data rate})]}$$

where t′ is the time given between the flip-flop clock and the output sampling time. This time is always greater than h. One point to keep in mind is that the input data rate is twice the frequency of the input signal because each cycle of the pulse generator produces two data inputs, one High and one Low. A pulse generator operating at 5MHz produces an input data rate of 10MHz.

As an example using the 74F5074, assume that one failure per century is acceptable and both data and the clock are at 10MHz. A typical tau for the 54F5074 is 135 picoseconds with a T_0 of 9.8E6 seconds. Since one century equals about three billion seconds, substituting into the equation above gives:

$$3E9\ \text{sec} = \frac{\left[\exp\left(\frac{t'}{0.135ns}\right)\right]}{[9.8E6(10MHz)\ (10MHz)]}$$

$$t' = 9.5ns$$

If an additional nanosecond were allowed between the clock and the sampling point, one could expect a failure about once every 1.7 million years.

The 74F728 MTBF can be determined by setting the clock period to the t′ so that in the example above the t′ = 100ns. This t′ gives:

$$MTBF = \frac{\left[\exp\left(\frac{100ns}{0.135ns}\right)\right]}{[9.8E6(10MHz)\ (10MHz)]}$$

MTBF = 5.0E321 seconds
or 1.6E312 centuries!

Note that in this case a failure is considered to be any propagation delay beyond the delay expected in a situation where setup and hold times were not violated. Assuming data and clock rates of 100MHz gives:

$$MTBF = \frac{\left[\exp\left(\frac{10ns}{0.135ns}\right)\right]}{[9.8E6(100MHz)\ (100MHz)]}$$

MTBF = 1.5E9 seconds
or 48 years!

SKEW CHARACTERISTICS

One of the requirements for an effective clock driver is that the complementary outputs have a small skew relative to each other. Figure 5 shows a picture of the 74F5074 outputs at room temperature with a 5 volt V_{CC}. Because of Philips Semiconductors patented circuitry the output skews will always remain tightly coupled over temperature and V_{CC}.

SUMMARY

Because of their minimum output skews, metastable immune characteristics, and balanced output drive capabilities, the 74F50XXX series of products offer viable solutions to synchronization and clock driver problems.

For further reading on the metastability problem, Philips Semiconductors recommends Application Note AN219, "A Metastability Primer", and "Metastability Behavior in Digital Systems" by Lindsay Kleeman and Antonio Cantoni in *IEEE Design & Test of Computers*, December 1987, pages 4–19.

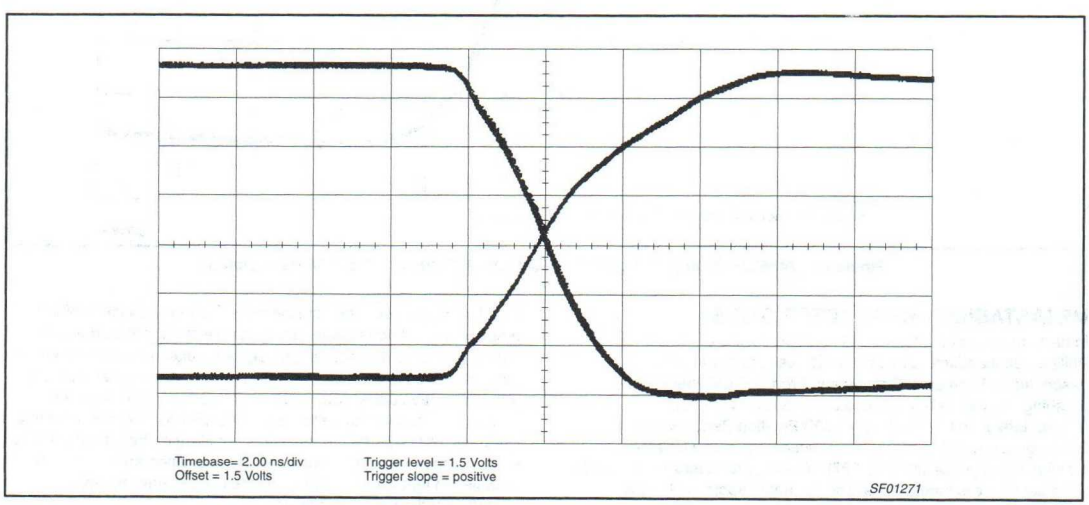


Figure 5. 74F5074 $\overline{Q}$ and Q Outputs Skew Relationship at 5 Volts V_{CC} and Room Temperature

Skew definitions

AN242

INTRODUCTION

Skew specifications are like any other AC electrical specification. The measurements are taken at certain conditions which may or, more likely, may not match a specific condition in a system application. However, like other AC specifications the skew specification is valuable as a "bench mark" for estimating certain circuit characteristics. Skew specifications are most valuable in clock–driving applications and applications where duty cycle characteristics are important. Three specific skew specifications are addressed in this note.

Typical test conditions under which the skews may be tested are:

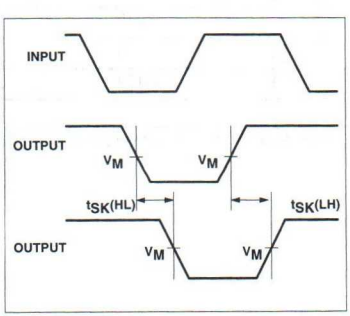
Test load: 50pF, 500Ω
All outputs switching
0°C, 25°C, 70°C
V_{CC} = 4.5V, 5.0V, 5.5V
Input conditions—V_{IL} = 0V to V_{IH} = 3V

Only data paths are tested for skew characteristics (AC measurements such as MR to output are *not* specified).

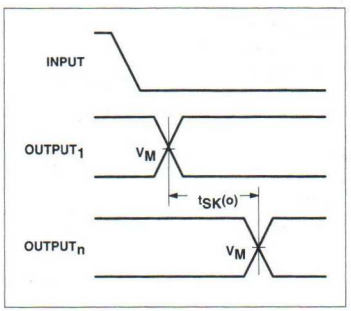
1. Output Skew $t_{SK}(o)$

JEDEC definition: "The difference between two concurrent propagation delay times that originate at either a single input or two inputs switching simultaneously and terminate at different outputs."

This skew generally characterizes like–going edges of a single IC only. It compares t_{PLH} versus t_{PLH} (or t_{PHL} vs. t_{PHL}) for two or more output data paths. This parameter is very useful in describing output distribution capabilities of a device. $t_{SK}(o)$ would be most valuable to customers using the device as a clock driver, distributing clock signals. $t_{SK}(o)$ could be further subdivided into $t_{SK}(LH)$ (output rising edge) and $t_{SK}(HL)$ (output falling edge) skews.



In some instances it may be necessary to compare opposite–going edges as in the case of complementary outputs driving positive–edge and negative–edge triggered clocks. Another case may be a need to simply compare t_{PHL} and t_{PLH} propagation delays on parallel paths.

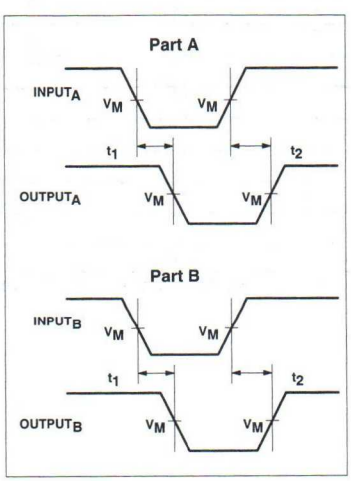


2. Process Skew $t_{SK}(x)$

JEDEC definition: "The difference between identically specified propagation delay times on any two samples of an IC at identical operating conditions."

This parameter addresses the issue of process variations by quantifying the difference between propagation delays that are caused by lot–to–lot variations. It does not include variations due to differences in supply voltage, operation temperature, output load, input edge rates, etc.

This parameter could be viewed as a $t_{SK}(o)$ skew over several like devices.

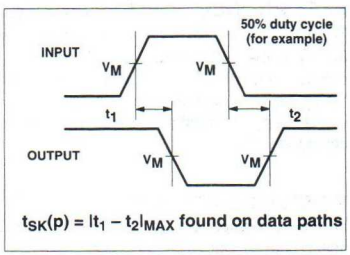


$t_{SK}(x)$ compares t_1 to t_1 and/or t_2 to t_2, etc., under identical conditions.

3. Pulse Skew $t_{SK}(p)$

JEDEC definition: "The difference between the propagation delay times t_{PHL} and t_{PLH} when a single switching input causes one or more outputs to switch."

This parameter is used to quantify duty cycle characteristics. Some applications require a nearly perfect 50% duty cycle. $t_{SK}(p)$ specifies the duty cycle retention characteristics of the device.



In essence this compares the input pulse width to the output pulse width—thus comparing the input duty cycle versus the resulting output duty cycle.

Thermal considerations for FAST logic products

AN2021

INTRODUCTION

Thermal considerations by both supplier and user require more attention as package sizes shrink and operating frequencies increase. This is because an increase in junction temperature (T_j) can adversely affect the long term operating life of an IC. Some of the variables that affect T_j are controlled by the IC manufacturer while others are controlled by the system designer.

With increasingly frequent use of Surface Mount Device (SMD) technology, management of thermal characteristics becomes a growing concern. Not only are the SMD packages much smaller, but the thermal energy is concentrated more densely on the printed circuit board.

FAST PRODUCTS IN SSOP PACKAGE

The FAST product family is a high performance Bipolar Logic Family. In the SMD packages, such as SSOP, it is necessary to estimate operating junction temperatures of the FAST products in the system environment. The information provided herein should assist the system designer with thermal management considerations.

POWER DISSIPATION

The power dissipation equations, definition of terms and the assumptions made in estimating power dissipation are shown below.

The total power is the sum of the static power and dynamic power.

$$P_{total} = P_{static} + P_{dynamic}.$$

The equation for static power dissipation is,

$$P_{stat} = (V_{CC} \times I_{CC})$$

but since I_{CCH}, I_{CCL} and I_{CCZ} are different values, the equation becomes,

$$P_{stat} = V_{CC}[DC_{en}(N_H \times I_{CCH}/N_T + N_L \times I_{CCL}/N_T) + (1\text{-}DC_{en})I_{CCZ}]$$

where:
- DC_{en} = % duty cycle enabled
- N_H = number of outputs in high state
- N_L = number of outputs in low state
- N_T = total number of outputs.

The equation for the dynamic power dissipation is,

$$P_{dyn} = [DC_{en} \times N_{sw} \times V_{CC} \times f1 \times (V_{OH} - V_{OL}) \times C_L] + [DC_{en} \times N_{sw} \times V_{CC} \times f2 \times (ma/MHz/bit)] \times 10^{-3}$$

where:
- DC_{en} = % duty cycle enabled
- N_{sw} = total number of outputs switching
- f1 = operating frequency (in Hz)
- f2 = operating frequency (in MHz)
- C_L = external load capacitance (in F)
- mA/MHz/bit = slope of the I_{CC} vs frequency curve.

Thermal Resistance (Θ_{ja})

The ability of a package to conduct heat from the IC chip inside the package to the environment is expressed in terms of "thermal resistance". It is measured in degrees Centigrade per watt of power dissipated by the chip. Table 1 lists some thermal resistance values for selected FAST products in SSOP packages. The values listed were measured in still air with no traces attached (worst case environment).

Table 1. FAST Products in SSOP Package

PRODUCT	PIN COUNT	Θ_{ja}	mA/MHz/bit (unloaded)
74F245	20	125	0.158
74F244	20	127	0.125
74F2244	20	127	0.045
74F373	20	125	0.158
74F374	20	125	0.102
74F543	24	118	0.512*
74F827	24	121	0.125
74F240	20	124	0.275
74F299	20	121	0.183
74F533	20	124	0.129
74F657	24	113	0.202

* The 74F543 I_{CC} vs Frequency slope increases above 20 MHz. From 20 MHz to 30 MHz, slope = 1.64. From 30 MHz to 40 MHz, slope = 2.55.

Thermal considerations for FAST logic products

AN2021

FACTORS AFFECTING Θ_{ja}

For a given package and lead frame, some factors which affect the thermal resistance (Θ_{ja}) in the application include (1) the die size of the IC chip, (2) the length of the printed circuit board traces attached to IC package on the system board and (3) the amount of airflow across the package.

Figure 1 through Figure 7 provide Θ_{ja} information for the 20 and 24 pin packages as a function of die size, airflow and trace length.

A SAMPLE CALCULATION

An example for the 74F244. Junction temperature is estimated from the equation:

$$T_j = (\Theta_{ja} \times P_{total}) + T_{amb}$$
$$P_{total} = P_{stat} + P_{dyn}$$

Assuming the number of outputs High = 4, V_{CC} at 5.25V, the enable duty cycle (DC_{en}) = 50%, and worst case I_{CC}'s (I_{CCL} = 90 mA, I_{CCH} = 60 mA, I_{CCZ} = 90 mA) the static power calculation is:

$$P_{stat} = (5.25)\{(0.50)[(4)(0.060)/8 + (4)(0.090)/8] + (1-0.50)(0.090)\}$$
$$= (5.25)[(0.0150) + (0.0225) + (0.045)]$$
$$= 0.433 \text{ watts}$$

Assuming the following,

DC_{en}	= 50%	N_{SW}	= 4
f1	= 25 x 10^6 Hz	V_{CC}	= 5.25V
f2	= 25 MHz	ma/MHz/bit	= 0.26
C_L	= 50 pf (50 x 10^{-12}F)	V_{OH}	= 3.4V
		V_{OL}	= 0.4V

the P_{dyn} becomes:

$$P_{dyn} = [(50\%)(4)(5.25)(25x10^6)(3.4-0.4)(50x10^{-12})] + [(50\%)(4)(5.25)(25)(0.26)](10^{-3})$$
$$= (0.0394) + (0.0682)$$
$$= 0.108 \text{ watts}$$

$$P_{total} = 0.433 + 0.108 = 0.541 \text{ watts}$$

The junction temperature estimation then becomes:

$$T_j = (127)(0.541) + T_{amb}$$
$$= 69 + T_{amb}$$

If the system ambient temperature is 55°C, then

$$T_j = 69 + 55 = 124 \text{ °C}.$$

With the junction temperature of a device established for a given system environment the expected operating life of the IC can be determined from the graph in Figure 6.

SYSTEM CONSIDERATIONS

The manner in which an IC package is mounted and positioned in its surrounding environment will have significant effects on operating junction temperatures. These conditions are under the control of the system designer and are worthy of serious consideration in the PC board layout and system ventilation and airflow features.

Forced-air cooling will significantly reduce thermal resistance.

Package mounting can affect thermal resistance. Surface mount packages dissipate significant amounts of heat through the leads that attach to the traces. Trace length is another significant factor.

Thermally conductive adhesive under the surface mount packages can lower thermal resistance by providing a direct heat path from the package to the board.

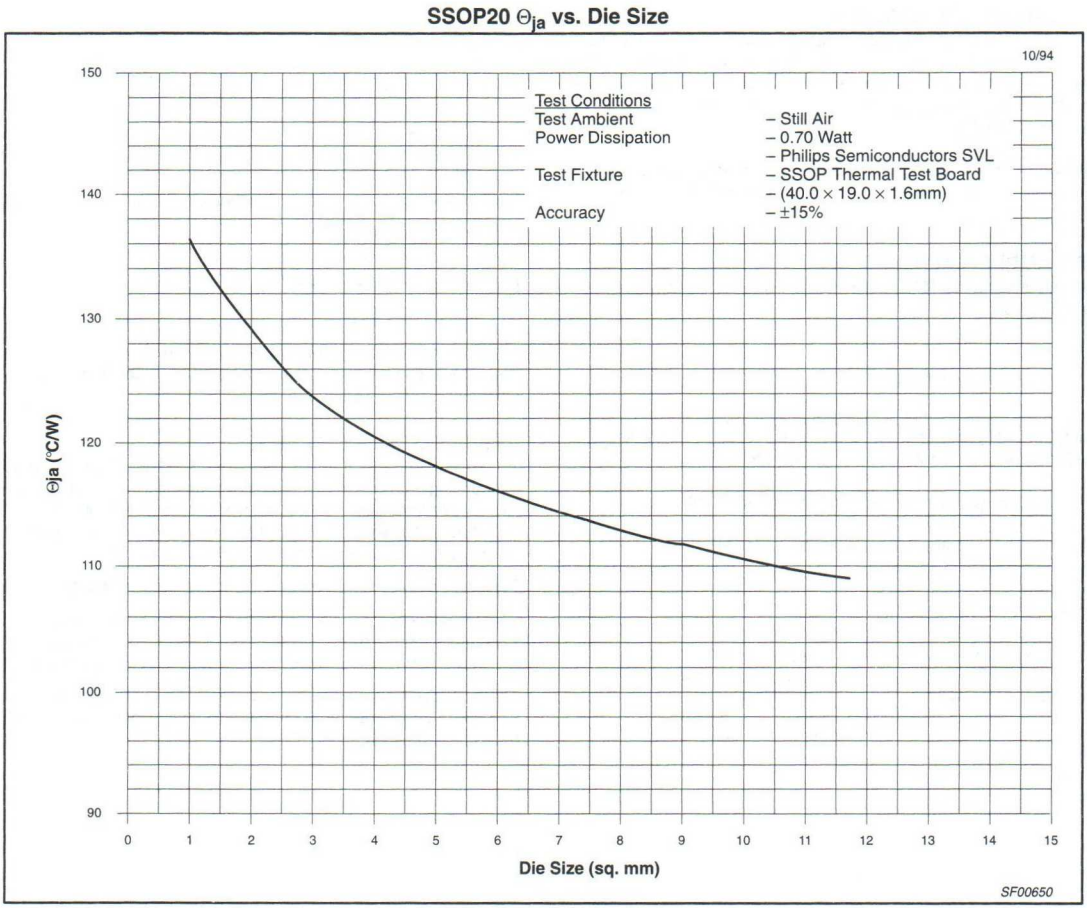

SSOP20 Θja vs. Die Size
10/94
Test Conditions
Test Ambient – Still Air
Power Dissipation – 0.70 Watt
Test Fixture – Philips Semiconductors SVL
– SSOP Thermal Test Board
– (40.0 × 19.0 × 1.6mm)
Accuracy – ±15%
Θja (°C/W)
150
140
130
120
110
100
90
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
Die Size (sq. mm)
SF00650

Figure 1.

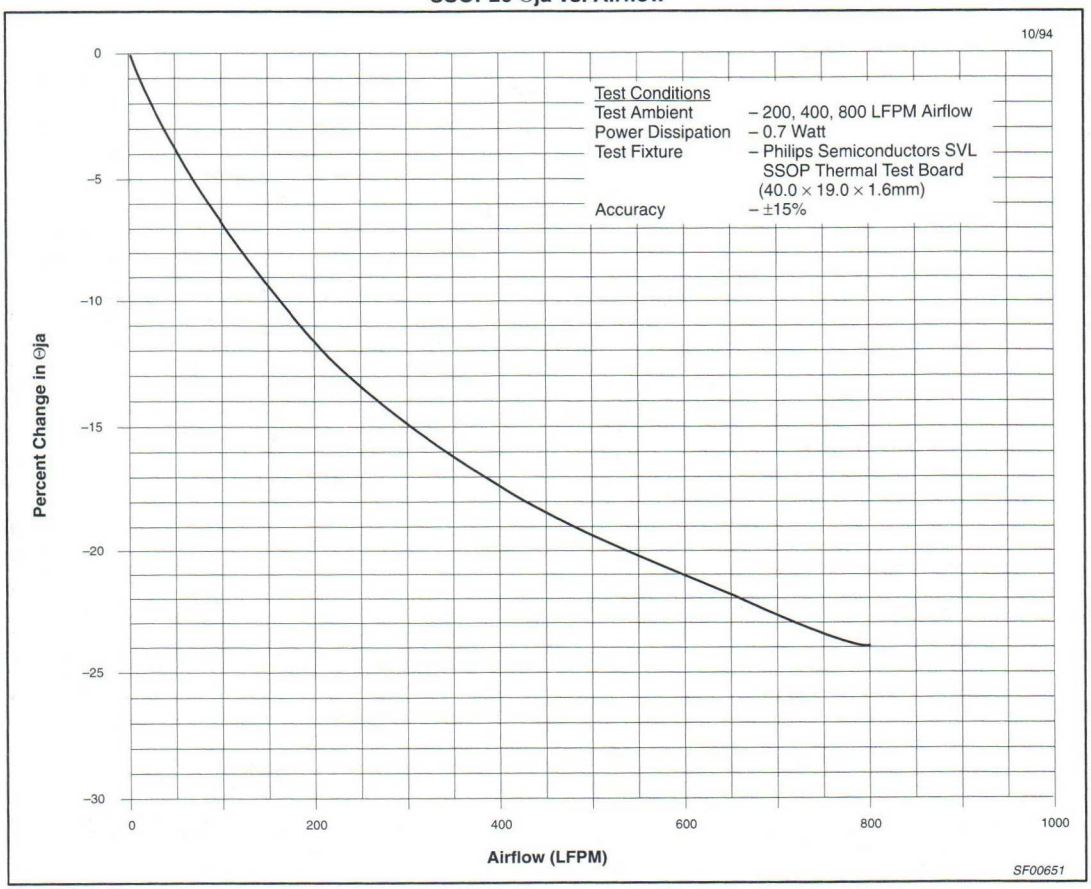

SSOP20 Θja vs. Airflow
10/94
Test Conditions
Test Ambient – 200, 400, 800 LFPM Airflow
Power Dissipation – 0.7 Watt
Test Fixture – Philips Semiconductors SVL SSOP Thermal Test Board (40.0 × 19.0 × 1.6mm)
Accuracy – ±15%
Percent Change in Θja
0
-5
-10
-15
-20
-25
-30
0
200
400
600
800
1000
Airflow (LFPM)
SF00651

Figure 2.

SSOP24 Θja vs. Die Size

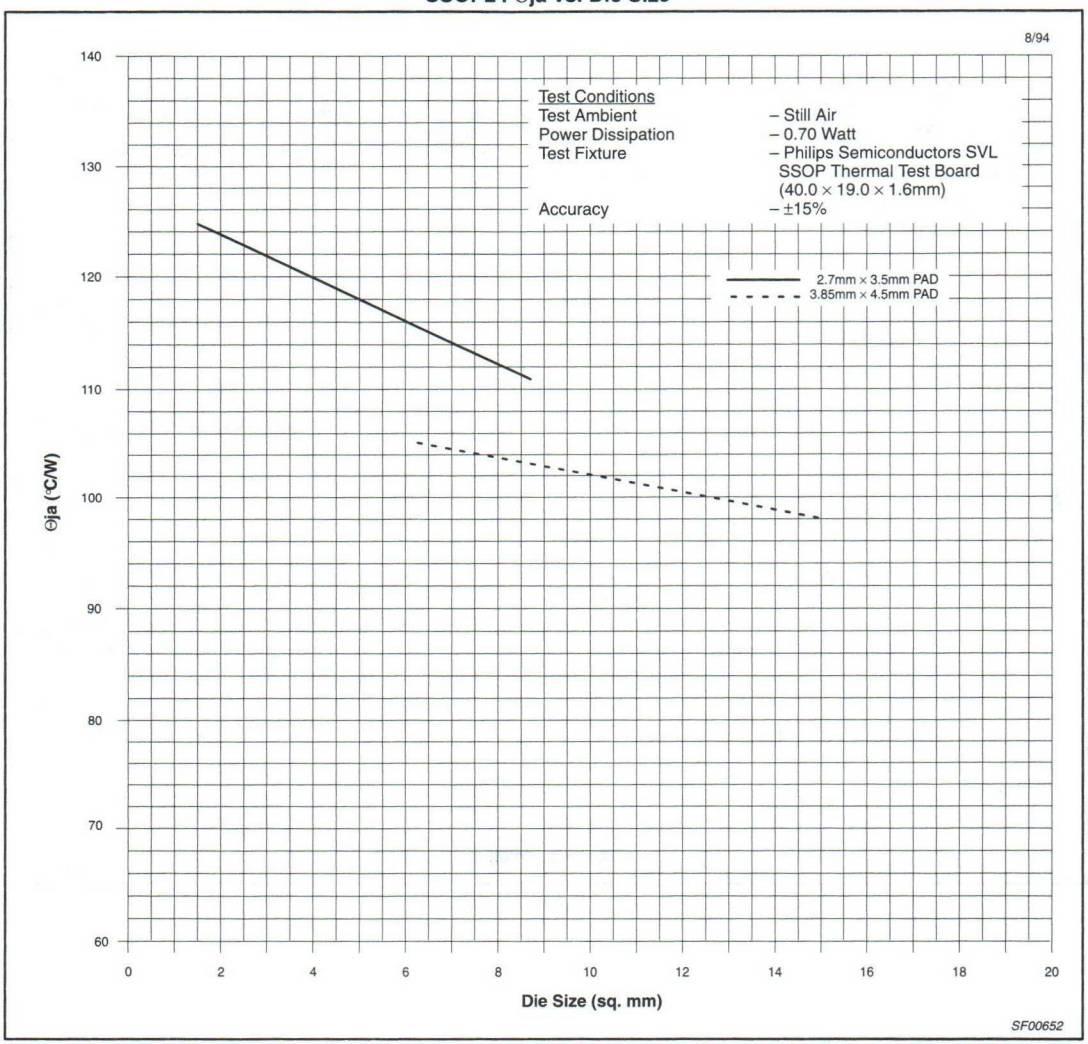


Figure 3.

SSOP24 Θja vs. Airflow

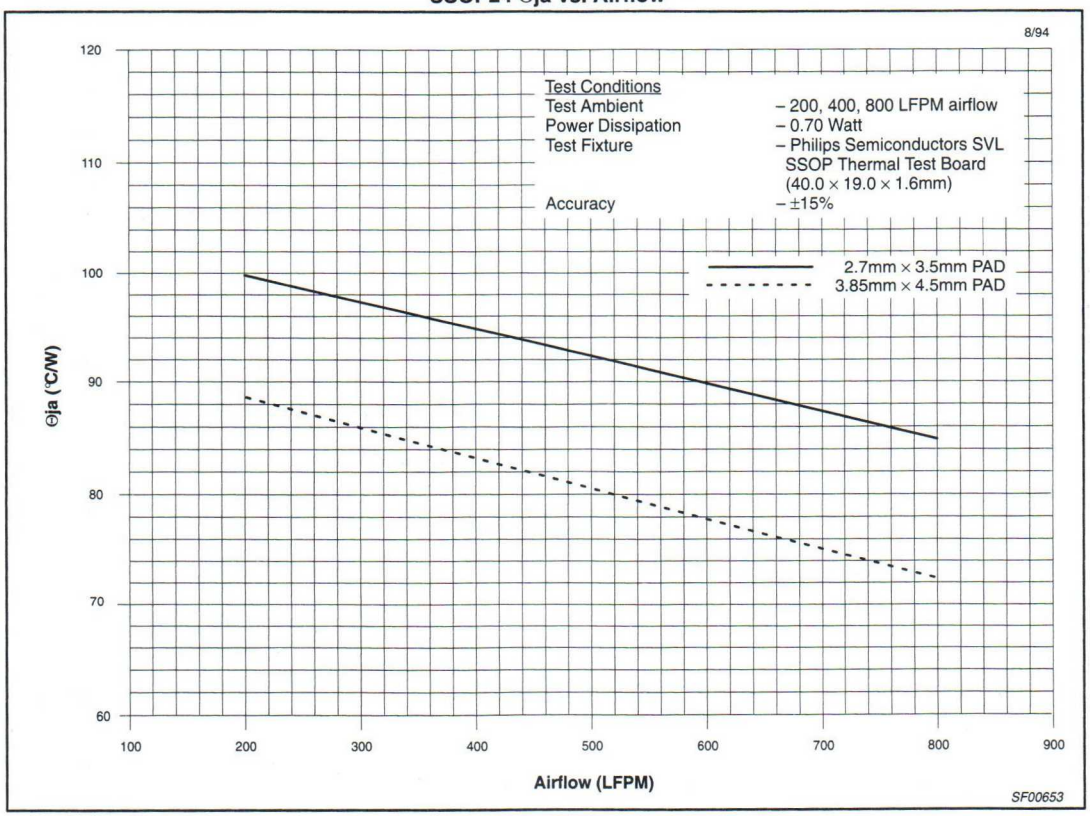


Figure 4.

Effect of Trace Length on Θja

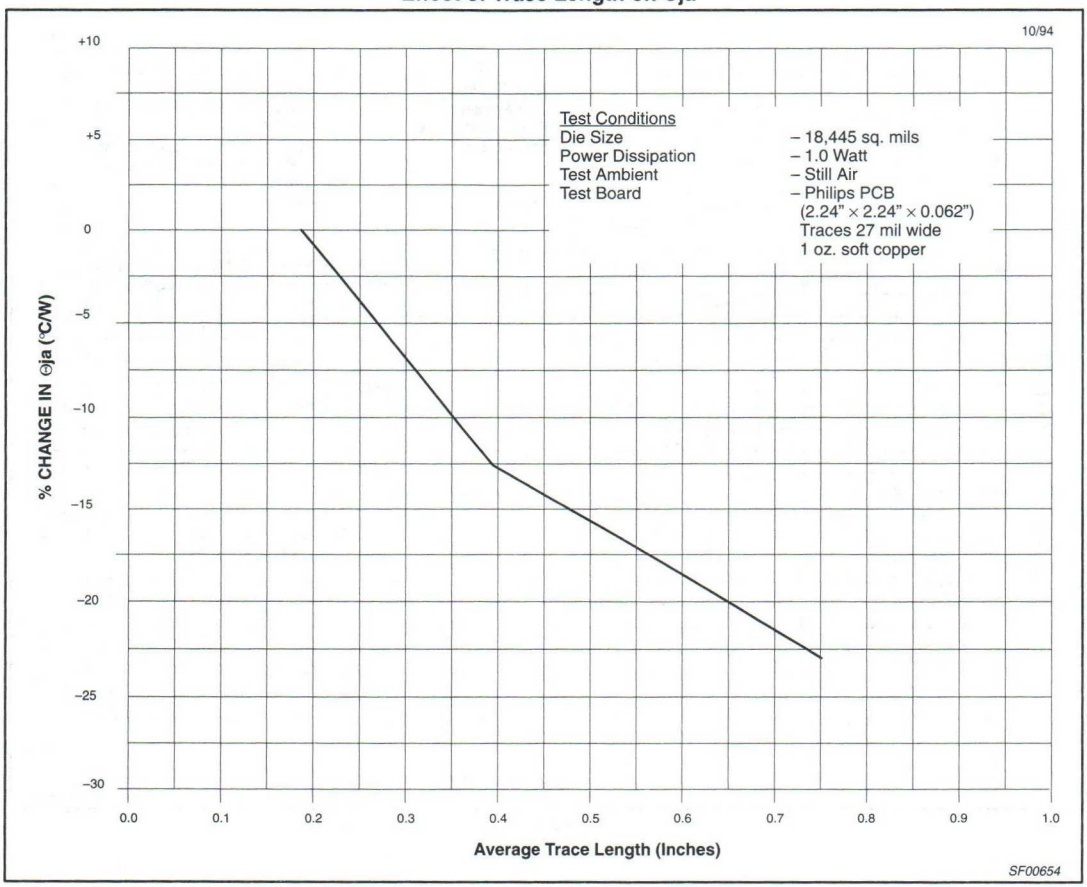


Figure 5.

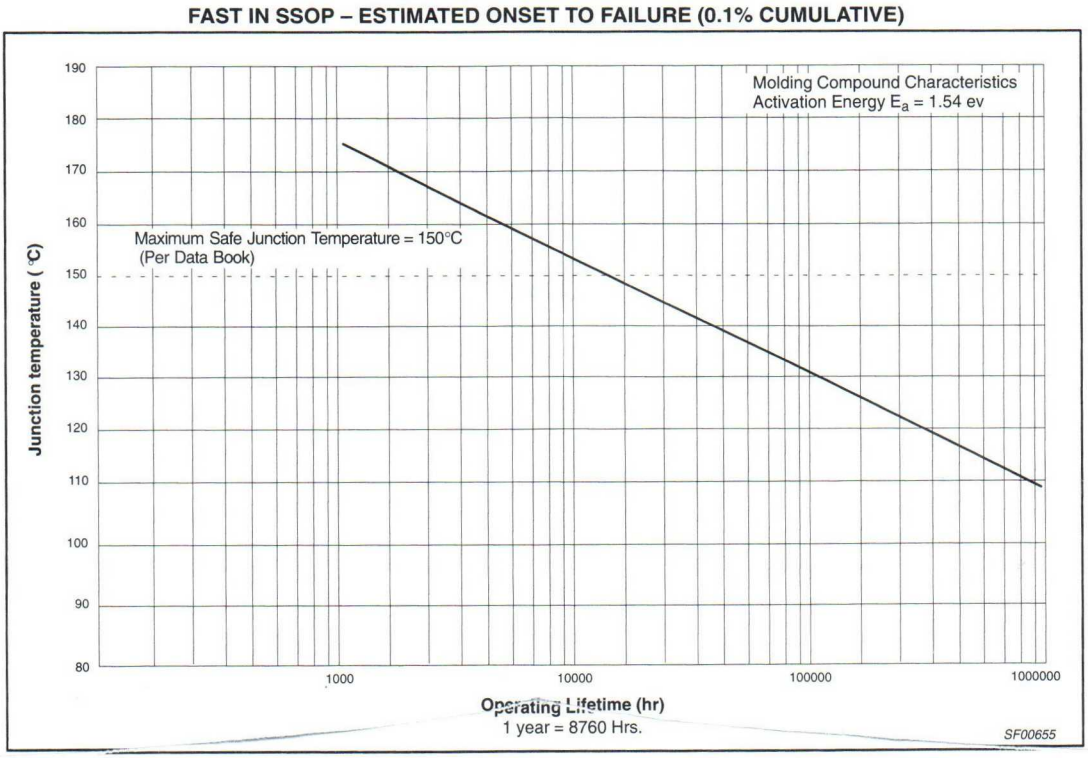

FAST IN SSOP – ESTIMATED ONSET TO FAILURE (0.1% CUMULATIVE)
Molding Compound Characteristics
Activation Energy E_a = 1.54 ev
Maximum Safe Junction Temperature = 150°C
(Per Data Book)
Junction temperature (°C)
190
180
170
160
150
140
130
120
110
100
90
80
1000
10000
100000
1000000
Operating Lifetime (hr)
1 year = 8760 Hrs.
SF00655

Figure 6.

Section 4
Package Information

FAST TTL Logic Series

CONTENTS

Package Information

Soldering Information 928

Package Drawing No.	Description		
SO8:	plastic small outline package; 8 leads; body width 3.9mm	SOT96-1	931
DIP8:	plastic dual in-line package; 8 leads (300 mil)	SOT97-1	932
SO14:	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1	933
DIP14:	plastic dual in-line package; 14 leads (300 mil)	SOT27-1	934
SO16:	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1	935
SO16:	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1	936
DIP16:	plastic dual in-line package; 16 leads (300 mil)	SOT38-4	937
DIP20:	plastic dual in-line package; 20 leads (300 mil)	SOT146-1	938
SO20:	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1	939
SSOP20:	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1	940
PLCC20:	plastic leaded chip carrier; 20 leads	SOT380-1	941
SO24:	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1	942
DIP24:	plastic dual in-line package; 24 leads (300 mil)	SOT222-1	943
SSOP24:	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1	944
SO28:	plastic small outline package; 28 leads; body width 7.5mm	SOT136-1	945
DIP28:	plastic dual in-line package; 28 leads (600 mil); long body	SOT117-2	946
PLCC28:	plastic leaded chip carrier; 28 leads	SOT261-2	947
PLCC44:	plastic leaded chip carrier; 44 leads	SOT187-2	948
DIP48:	plastic dual in-line package; 48 leads (600 mil)	SOT240-1	949

INTRODUCTION

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when though-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

THROUGH-HOLE MOUNTED PACKAGES

Table 1. Types of through-hole mounted packages

TYPE	DESCRIPTION
DIP	plastic dual in-line package
SDIP	plastic shrink dual in-line package
HDIP	plastic heat-dissipating dual in-line package
DBS	plastic dual in-line bent from a single in-line package
SIL	plastic single in-line package

Soldering by dipping or wave

The maximum permissible temperature of the solder is 260°C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24V) to the lead(s) of the package, below the seating plane or not more than 2mm above it. If the temperature of the soldering iron bit is less than 300°C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400°C, contact may be up to 5 seconds.

SURFACE MOUNTED PACKAGES

Table 2. Types of surface mounted packages

TYPE	DESCRIPTION
SO	plastic small outline package
SSOP	plastic shrink small outline package
TSSOP	plastic thin shrink small outline package
VSO	plastic very small outline package
QFP	plastic quad flat package
LQFP	plastic low profile quad flat package
SQFP	plastic shrink quad flat package
TQFP	plastic thin quad flat package
PLCC	plastic leaded chip carrier

Reflow soldering

Reflow soldering techniques are suitable for all SMD packages, ease of soldering varies with the type of package as indicated in Table 3.

The choice of heating method may be influenced by larger plastic packages (QFP or PLCC with 44 leads, or more). If infrared or vapor phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information on moisture prevention, refer to the Drypack chapter in our *"Quality Reference Manual"* (order code 9398 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stenciling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250°C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45°C.

Table 3. Suitability of surface mounted packages for various soldering methods

Rating from 'a' to 'd': **'a' indicates most suitable** (soldering is not difficult); **'d' indicates least suitable** (soldering is achievable with difficulty).

TYPE	REFLOW METHOD					DOUBLE WAVE METHOD
	INFRARED	HOT BELT	HOT GAS	VAPOR PHASE	RESISTANCE	
SO	a	a	a	a	d	a
SSOP	a	a	a	c	d	c
TSSOP	b	b	b	c	d	d
VSO	b	b	a	b	a	b
QFP	b	b	a	c	a	c
LQFP	b	b	a	c	d	d
SQFP	b	b	a	c	d	d
TQFP	b	b	a	c	d	d
PLCC	c	b	b	d	d	b

Wave soldering

Wave soldering is **not** recommended for SSOP, TSSOP, QFP, LQFP, SQFP or TQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- For SSOP, TSSOP and VSO packages, the longitudinal axis of the package footprint must be parallel to the solder flow **and** must incorporate solder thieves at the downstream end.
- For QFP, LQFP and TQFP packages, the footprint must be at and angle of 45° to the board direction **and** must incorporate solder thieves downstream and at the side corners.

Even with these conditions, only consider wave soldering for the following package types:

- SO
- VSO
- PLCC
- SSOP **only with body width 4.4mm**, e.g., SSOP16 (SOT369-1) or SSOP20 (SOT266-1).
- QFP **except** QFP52 (SOT379-1), QFP100 (SOT317-1, SOT317-2 and SOT382-1) and QFP160 (SOT322-1); these are **not** suitable for wave soldering.
- LQFP **except** LQFP32 (SOT401-1), LQFP48 (SOT313-1, SOT313-2), LQFP64 (SOT314-2), LQFP80 (SOT315-1); these are **not** suitable for wave soldering.
- TQFP **except** TQFP64 (SOT357-1), TQFP80 (SOT375-1) and TQFP100 (SOT386-1); these are **not** suitable for wave soldering.

SQFP are **not** suitable for wave soldering.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260°C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150°C within 6 seconds. Typical dwell time is 4 seconds at 250°C.

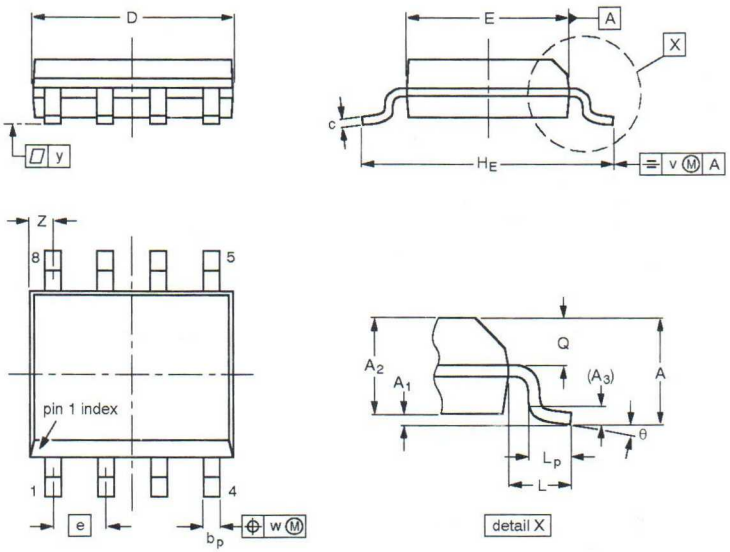
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

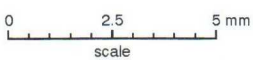
Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300°C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320°C.

Package outlines

SO8: plastic small outline package; 8 leads; body width 3.9mm — SOT96-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

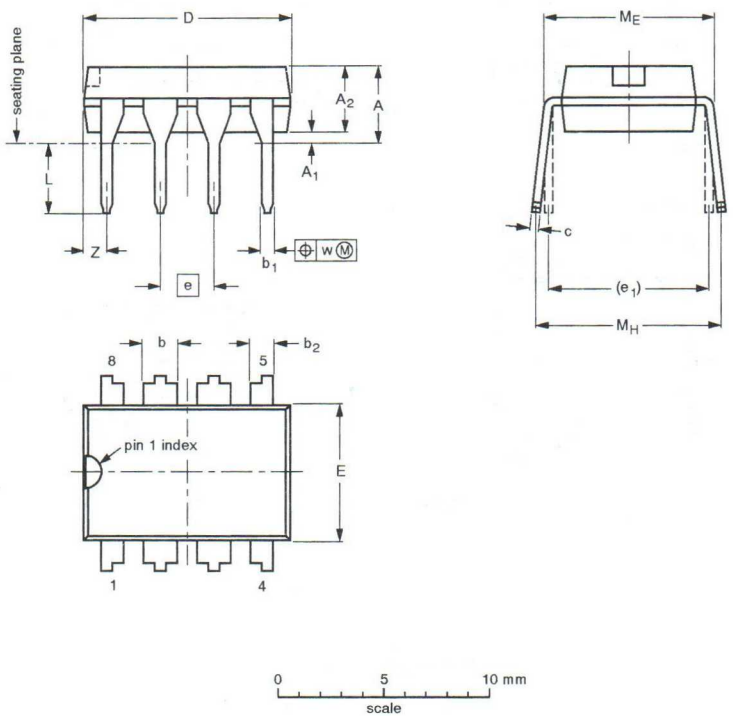
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~95-02-04~~ 97-05-22

Package outlines

DIP8: plastic dual in-line package; 8 leads (300 mil) SOT97-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

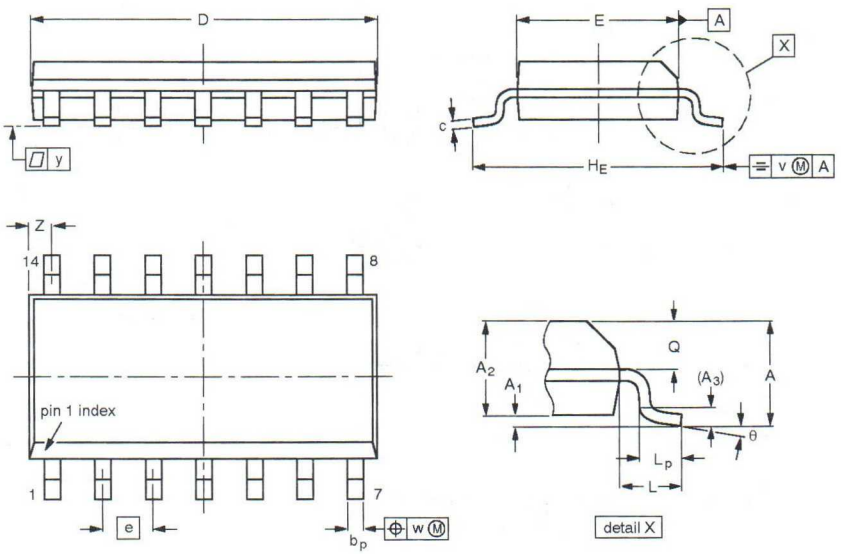
Note

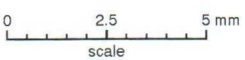
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

Package outlines

SO14: plastic small outline package; 14 leads; body width 3.9 mm — SOT108-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

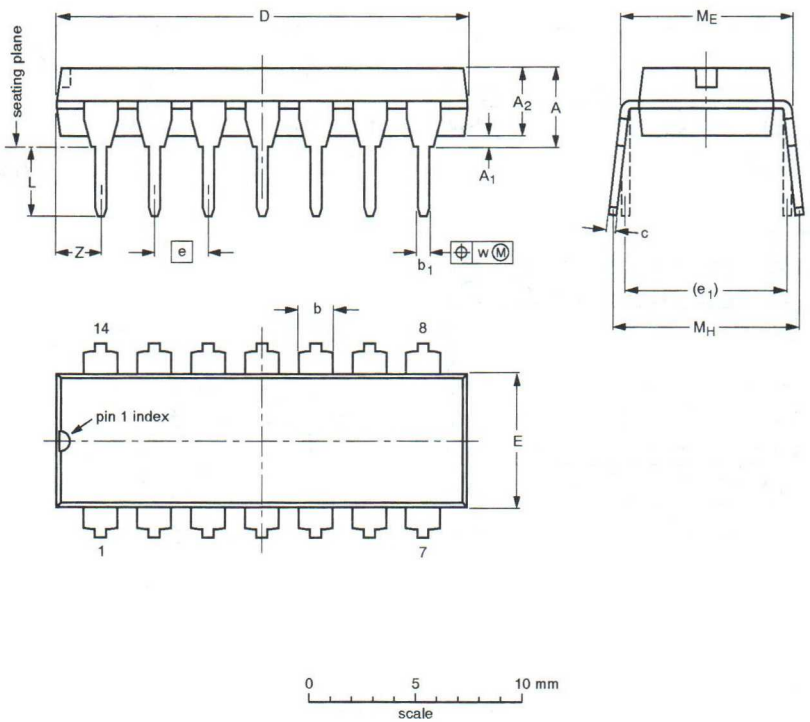
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				~~95-01-23~~ 97-05-22

Package outlines

DIP14: plastic dual in-line package; 14 leads (300 mil) SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

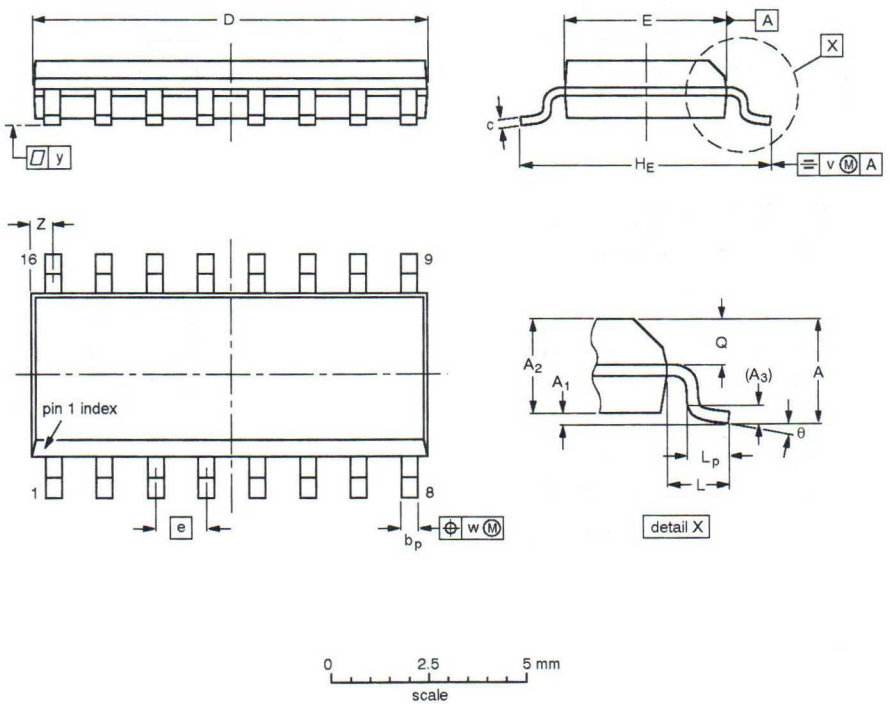
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				~~92-11-17~~ 95-03-11

Package outlines

SO16: plastic small outline package; 16 leads; body width 3.9 mm — SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

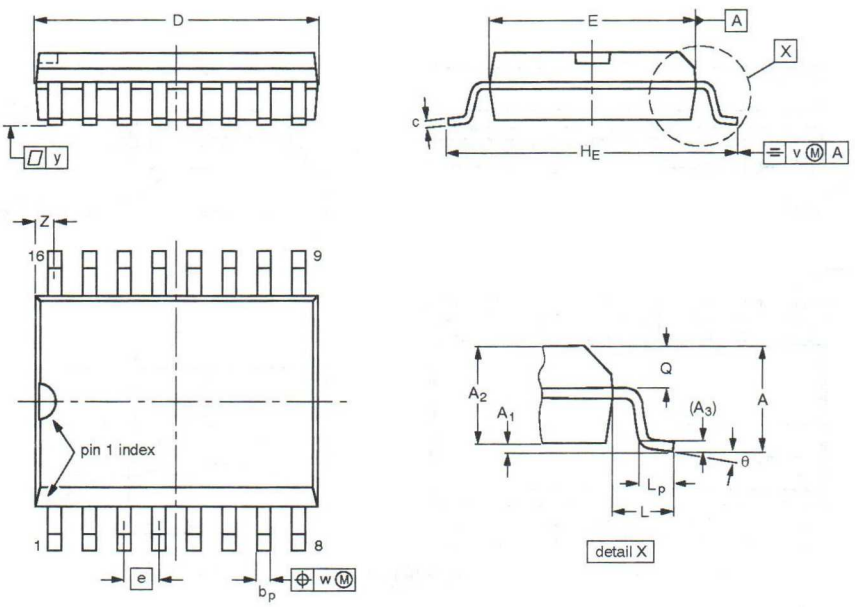
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~95-01-23~~ 97-05-22

Package outlines

SO16: plastic small outline package; 16 leads; body width 7.5 mm — SOT162-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

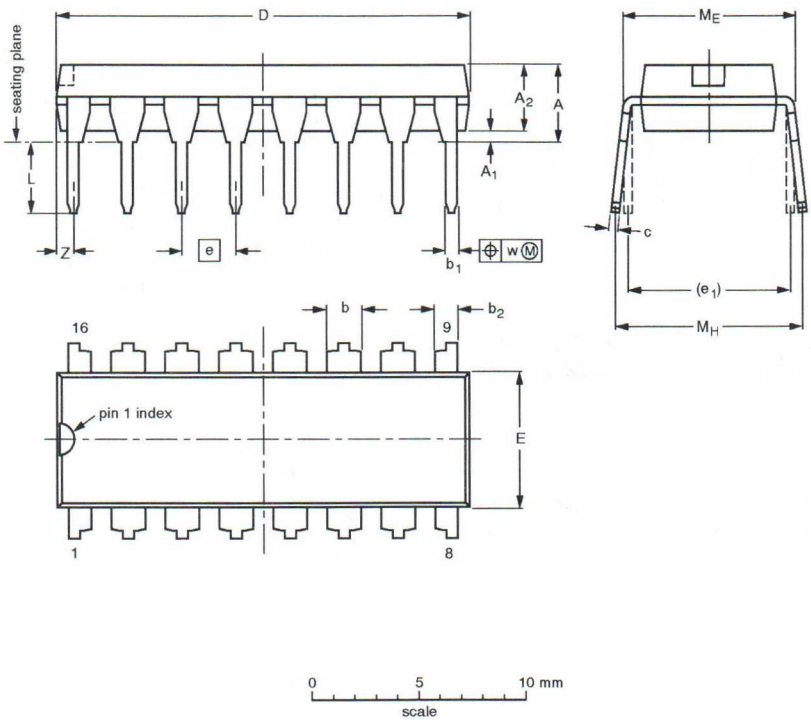
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~95-01-24~~ 97-05-22

Package outlines

DIP16: plastic dual in-line package; 16 leads (300 mil) SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

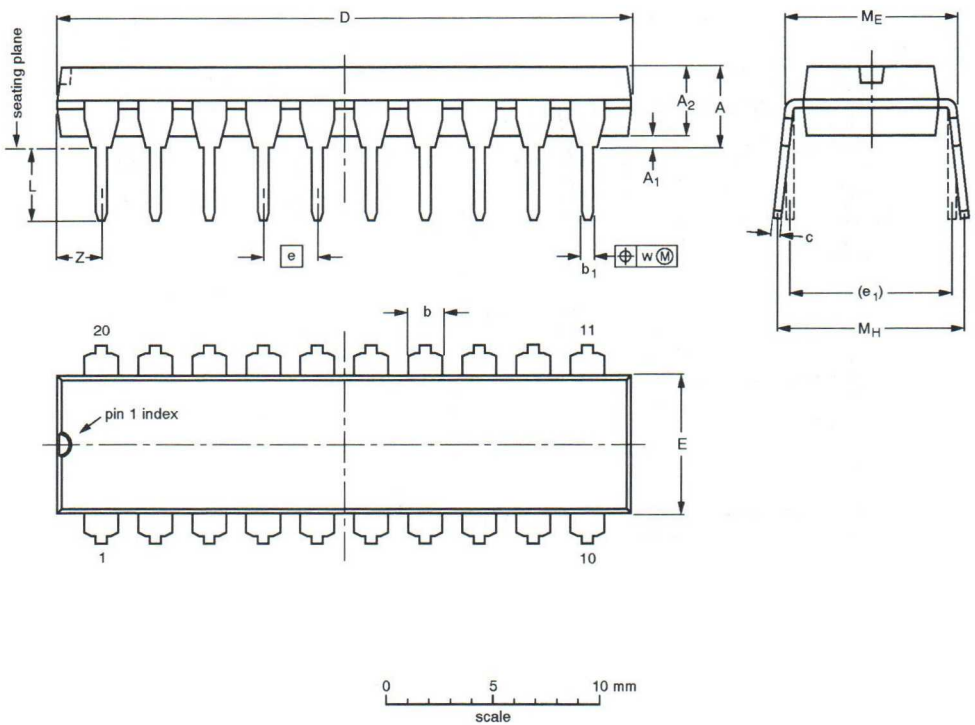
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

Package outlines

DIP20: plastic dual in-line package; 20 leads (300 mil) SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

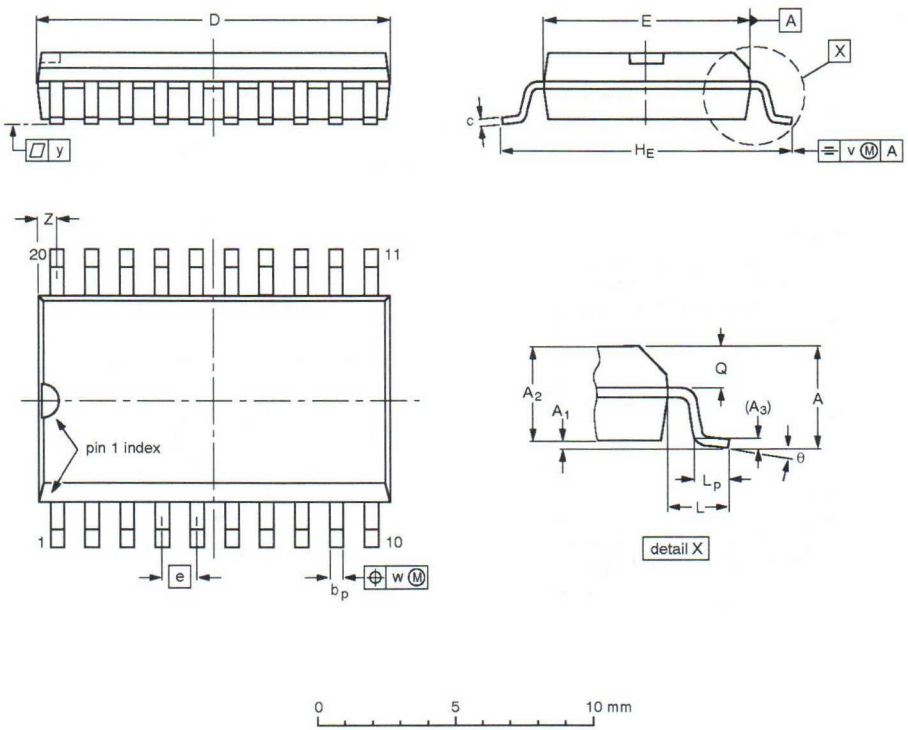
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

Package outlines

SO20: plastic small outline package; 20 leads; body width 7.5 mm — SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

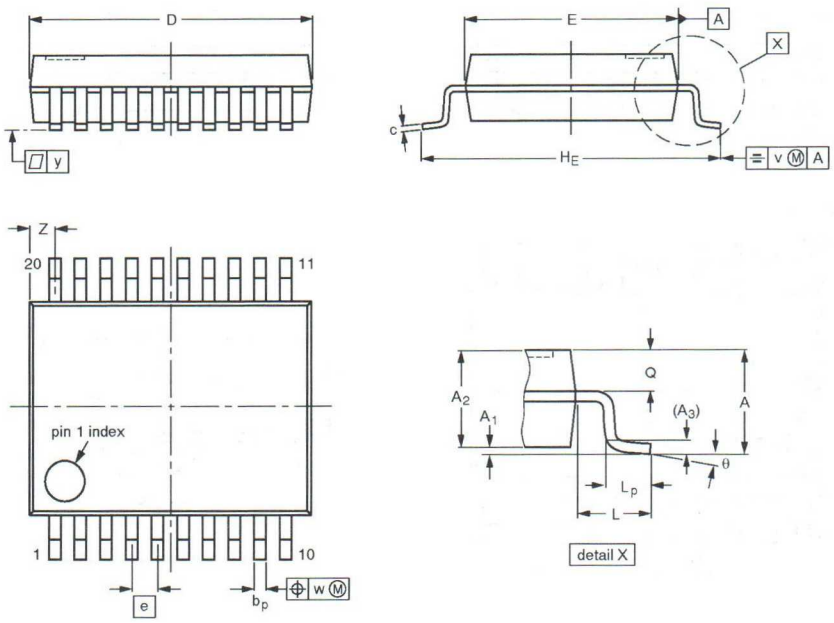
Note

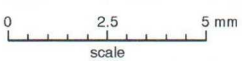
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

Package outlines

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm — SOT339-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

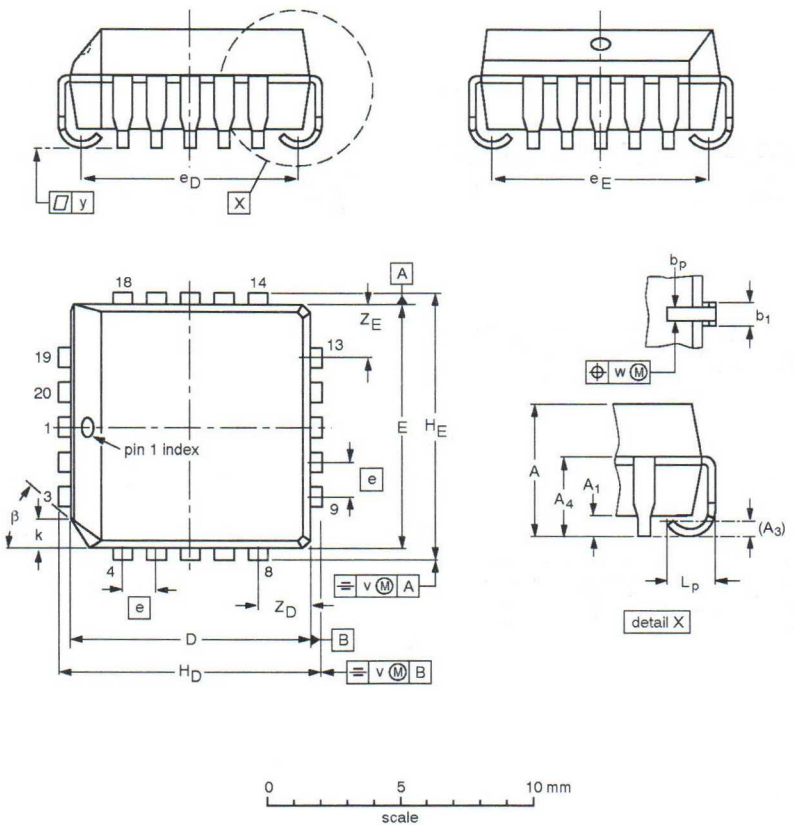
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				~~93-09-08~~ 95-02-04

Package outlines

PLCC20: plastic leaded chip carrier; 20 leads — SOT380-1



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	9.04 8.89	9.04 8.89	1.27	8.38 7.37	8.38 7.37	10.03 9.78	10.03 9.78	1.22 1.07	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.356 0.350	0.356 0.350	0.05	0.330 0.290	0.330 0.290	0.395 0.385	0.395 0.385	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

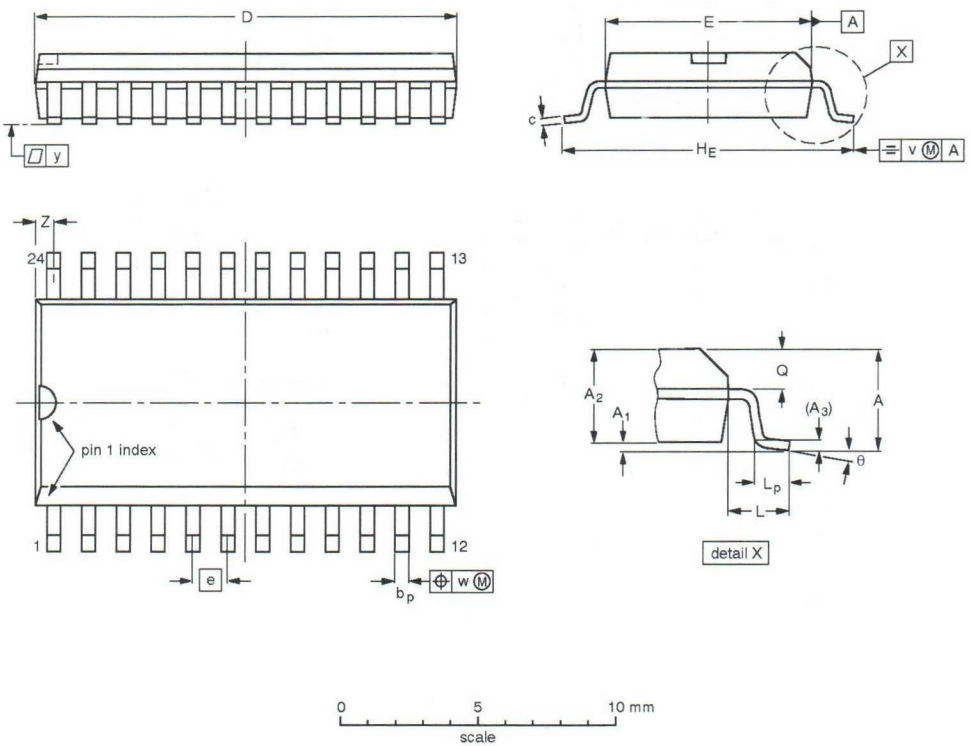
Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT380-1		MO-047AA				~~95-02-25~~ 97-12-16

Package outlines

SO24: plastic small outline package; 24 leads; body width 7.5 mm — SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

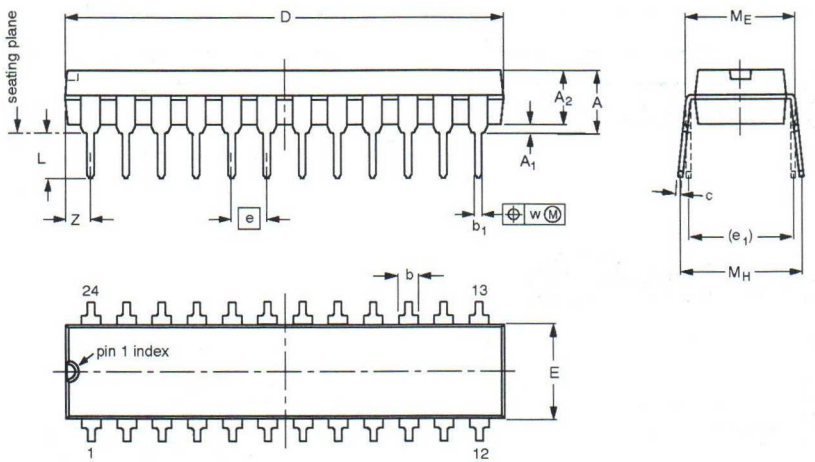
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

Package outlines

DIP24: plastic dual in-line package; 24 leads (300 mil) SOT222-1





DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

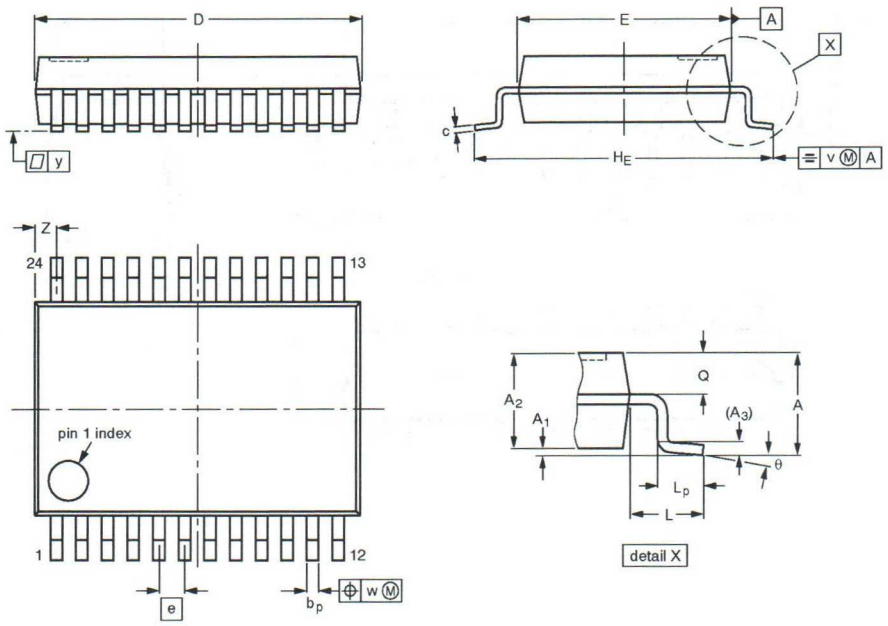
Note

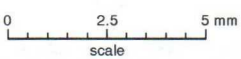
1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

Package outlines

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm — SOT340-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

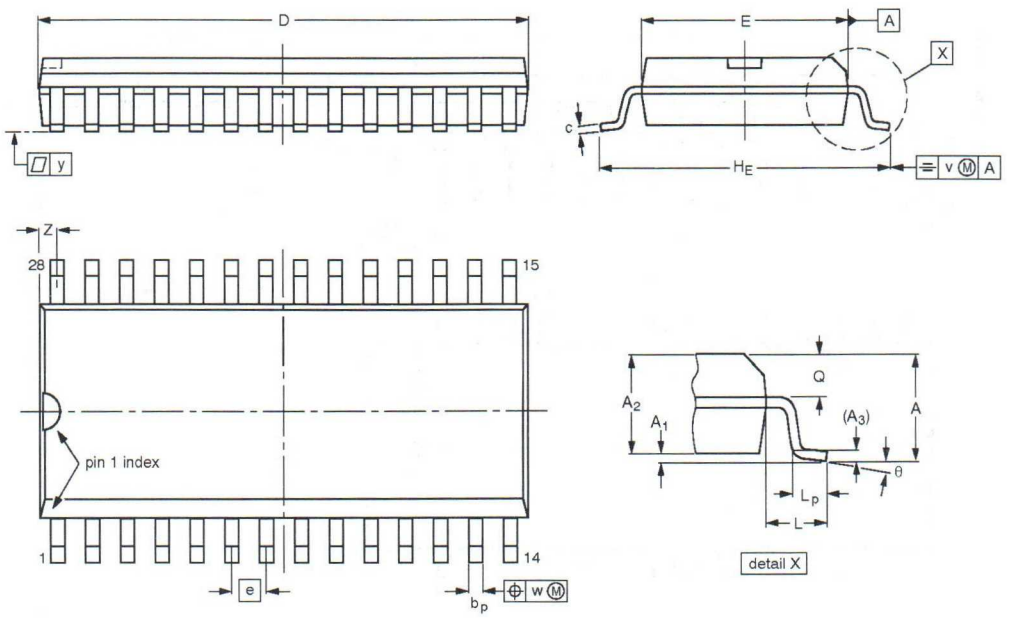
Note

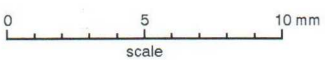
1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				~~93-09-08~~ 95-02-04

Package outlines

SO28: plastic small outline package; 28 leads; body width 7.5mm — SOT136-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

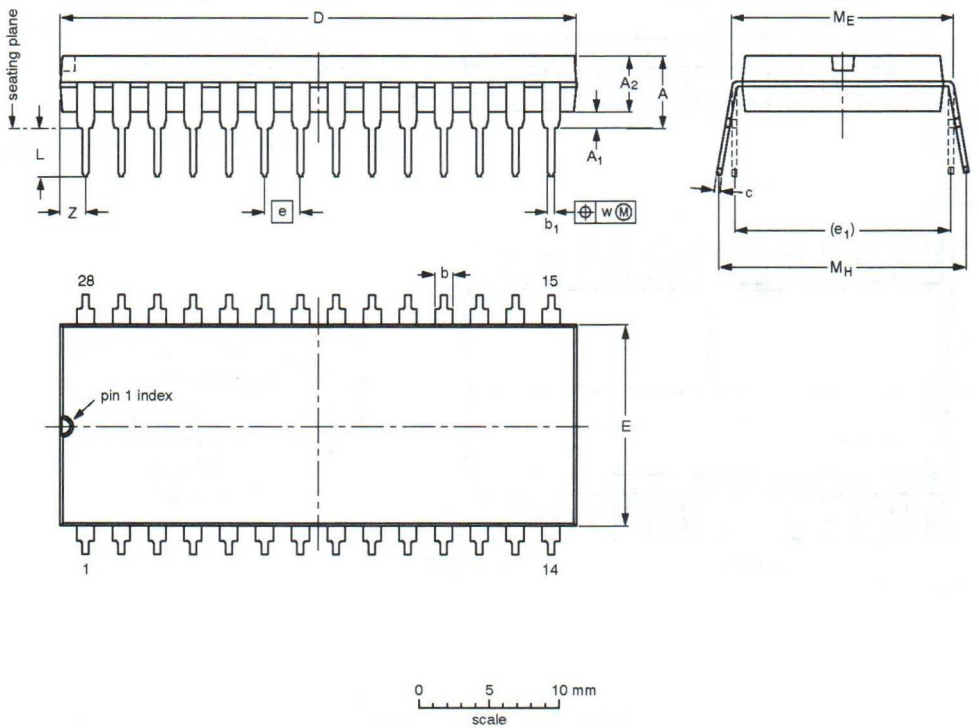
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~95-01-24~~ 97-05-22

Package outlines

DIP28: plastic dual in-line package; 28 leads (600 mil); long body — SOT117-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	3.94	1.63 1.14	0.56 0.43	0.38 0.25	37.08 35.94	14.22 13.84	2.54	15.24	3.51 3.05	15.75 15.24	17.65 15.24	0.25	2.10
inches	0.200	0.020	0.155	0.064 0.045	0.022 0.017	0.015 0.010	1.460 1.415	0.560 0.545	0.100	0.600	0.138 0.120	0.62 0.60	0.695 0.600	0.01	0.083

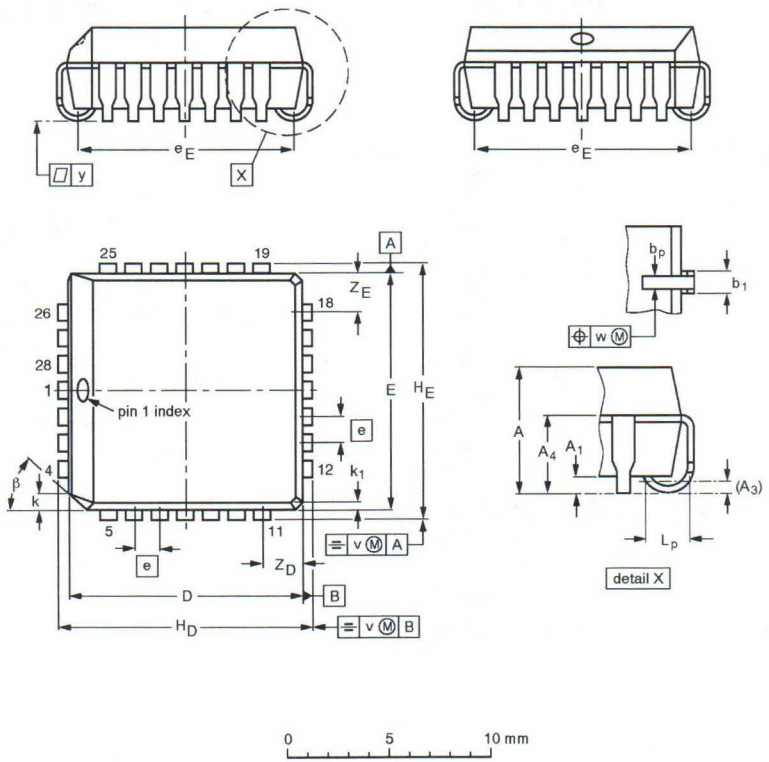
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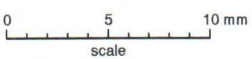
1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-2		MS-011AB				95-03-11

Package outlines

PLCC28: plastic leaded chip carrier; 28 leads — SOT261-2





DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.430 0.390	0.430 0.390	0.495 0.485	0.495 0.485	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

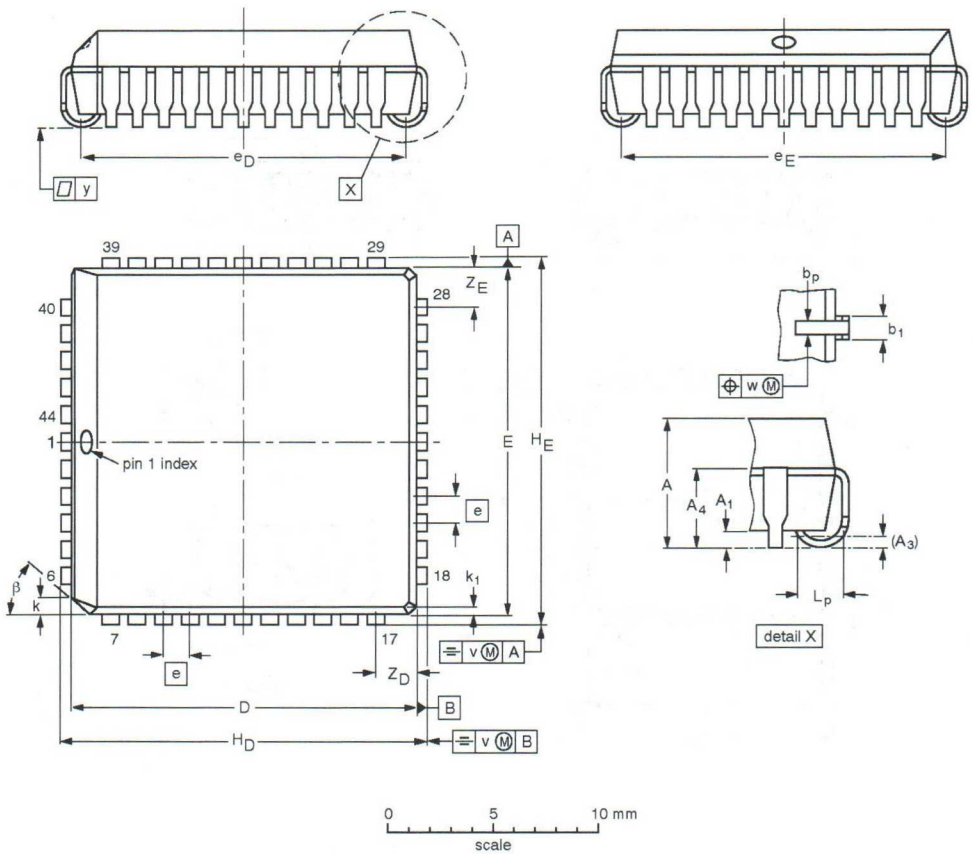
Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT261-2						~~92-11-17~~ 95-02-25

Package outlines

PLCC44: plastic leaded chip carrier; 44 leads — SOT187-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.630 0.590	0.630 0.590	0.695 0.685	0.695 0.685	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

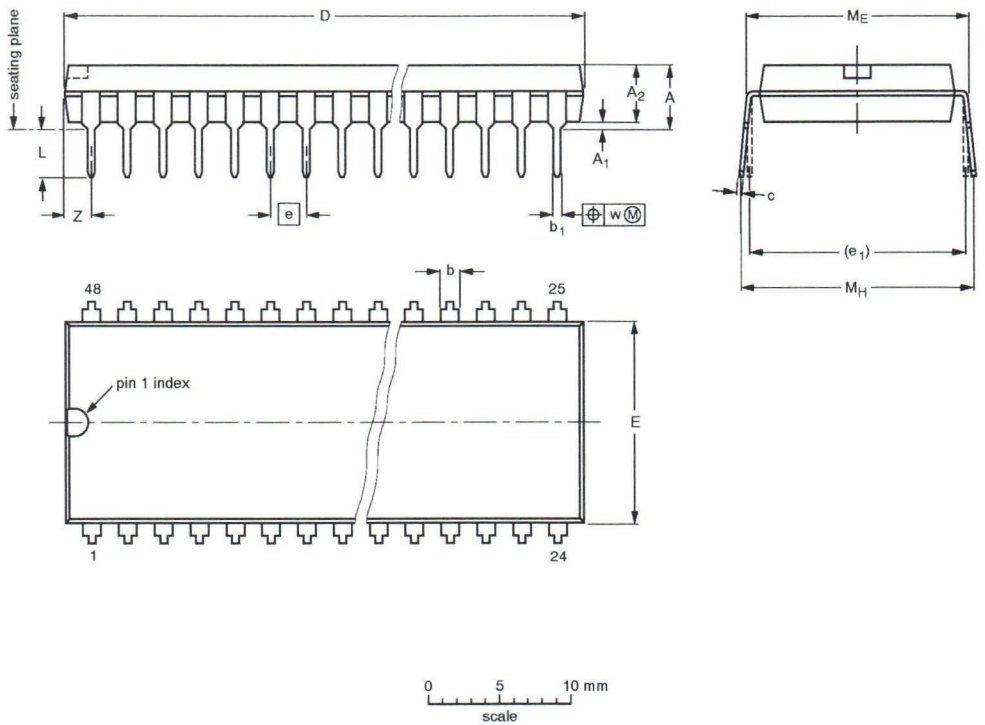
Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT187-2	112E10	MO-047AC				~~95-02-25~~ 97-12-16

Package outlines

DIP48: plastic dual in-line package; 48 leads (600 mil) SOT240-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.9	0.36	4.06	1.4 1.14	0.53 0.38	0.36 0.23	62.60 61.60	14.22 13.56	2.54	15.24	3.90 3.05	15.88 15.24	18.46 15.24	0.254	2.1
inches	0.19	0.014	0.16	0.055 0.045	0.021 0.015	0.014 0.009	2.46 2.42	0.56 0.53	0.10	0.60	0.15 0.12	0.63 0.60	0.73 0.60	0.01	0.083

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT240-1						~~92-11-17~~ 95-01-25

APPENDIX A

DATA HANDBOOK SYSTEM

DATA HANDBOOK SYSTEM

Philips Semiconductors data handbooks contain all pertinent data available at the time of publication and each is revised and reissued regularly.

Loose data sheets are sent to subscribers to keep them up-to-date on additions or alterations made during the lifetime of a data handbook.

Catalogs are available for selected product ranges (some catalogs are also on floppy discs).

Our data handbook titles are listed here.

Integrated Circuits

Book	*Title*
IC01	Semiconductors for Radio, Audio and CD/DVD Systems
IC02	Semiconductors for Television and Video Systems
IC03	Semiconductors for Wired Telecom Systems
IC04	HE4000B Logic Family CMOS
IC05	Advanced Low-power Schottky (ALS) Logic
IC06	High-speed CMOS Logic Family
IC11	General-purpose/Linear ICs
IC12	I^2C Peripherals
IC13	Programmable Logic Devices (PLD)
IC14	8048-based 8-bit Microcontrollers
IC15	FAST TTL Logic Series
IC16	CMOS ICs for Clocks, Watches and Real Time Clocks
IC17	Semiconductors for Wireless Communications
IC18	Semiconductors for In-Car Electronics
IC19	ICs for Data Communications
IC20	80C51-based 8-bit Microcontrollers
IC22	Multimedia ICs
IC23	BiCMOS Bus Interface Logic
IC24	Low Voltage CMOS & BiCMOS Logic
IC25	16-bit 80C51XA Microcontrollers (eXtended Architecture)
IC26	Integrated Circuit Packages
IC27	Complex Programmable Logic Devices

Discrete Semiconductors

Book	*Title*
SC01	Small-signal and Medium-power Diodes
SC03	Power Thyristors and Triacs
SC04	Small-signal Transistors
SC05	Video Transistors and Modules for Monitors
SC06	Power Bipolar Transistors
SC07	Small-signal Field-effect Transistors
SC11	Power Diodes
SC13	PowerMOS Transistors
SC14	RF Wideband Transistors
SC16	Wideband Hybrid Amplifier Modules for CATV
SC17	Semiconductor Sensors
SC18	Discrete Semiconductor Packages
SC19	RF & Microwave Power Transistors, RF Power Modules and Circulators/Isolators

MORE INFORMATION FROM PHILIPS SEMICONDUCTORS?

For more information about Philips Semiconductors data handbooks, catalogs and subscriptions, contact your nearest Philips Semiconductors national organization, select from the **address list on the back cover of this handbook**. Product specialists are at your service and inquiries are answered promptly.

OVERVIEW OF PHILIPS COMPONENTS DATA HANDBOOKS

Our sister product division, Philips Components, also has a comprehensive data handbook system to support their products. Their data handbook titles are listed here.

Display Components

Book	*Title*
DC01	Colour Television and Multimedia Tubes
DC02	Monochrome Monitor Tubes and Deflection Units
DC03	Television Tuners, Coaxial Aerial Input Assemblies
DC04	Colour Monitor and Multimedia Tubes
DC05	Wire Wound Components

Advanced Ceramics & Modules

ACM1 (MA01)	Soft Ferrites
ACM2	Discrete Ceramics
ACM3 (MA03)	Piezoelectric Ceramics and Specialty Ferrites

BC Components

PA01	Electrolytic Capacitors
PA02	Varistors, Thermistors and Sensors
PA03	Potentiometers
PA04	Variable Capacitors
PA05	Film Capacitors
PA06	Ceramic Capacitors
PA06a	Surface Mounted Ceramic Multilayer Capacitors
PA06b	Leaded Ceramic Capacitors
PA08	Fixed Resistors
PA10	Quartz Crystals
PA11	Quartz Oscillators

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