Electronic components and materials

PHILIPS

Buyers & engineers guide

MEMORIES AND MICROPROCESSORS

bipolar and MOS

signetics

CONTENTS

JFP PHILIPSE
7-11-1978

WHEN ORDERING

please quote the ordering code to specify device, temperature range if applicable (prefix N or S), and package (suffix D, E, F, I, K, N, P, T or TA).

examples:

N82S25N	commercial temperature range, plastic DIL package
S82S16F	military temperature range, cerdip DIL package
N74S89N	commercial temperature range, plastic DIL package
S54S89F	military temperature range, cerdip DIL package
2650I	commercial temperature range, metal ceramic DIL package

memories

type index

Bipolar

	RAM			PROM		
technology	capacity	type	page	capacity	type	page
TTL	16 x 4	N3101A	10 – 11	32 x 8	N82S23	12 – 13
	16 x 4	N74S89		32 x 8	N82S123	
	16 x 4	N74S189		256 x 4	N82S27	
	16 x 4	N82S25		256 x 4	N82S126	
	256 x 1	N74S200		256 x 4	N82S129	
	256 x 1	N74S201		256 x 8	N82S114	
	256 x 1	N74S301		512 x 4	N82S130	
	256 x 1	N82S16		512 x 4	N82S131	
	256 x 1	N82S116		512 x 8	N82S115	
	256 x 1	N82S17		512 x 8	N82S140	
	256 x 1	N82S117		512 x 8	N82S141	
	64 x 9	N82S09		512 x 8	N82S146	
	1k x 1	N82S10		512 x 8	N82S147	
	1k x 1	N93415A		1k x 4	N82S136	
	1k x 1	N82S110		1k x 4	N82S137	
	1k x 1	N82LS10		1k x 8	N82S180	
	1k x 1	N82S11		1k x 8	N82S181	
	1k x 1	N93425A		1k x 8	N82S2708	
	1k x 1	N82S111		2k x 4	N82S184	
	1k x 1	N82LS11		2k x 4	N82S185	
	256 x 8	N82S208		2k x 8	N82S190	
	256 x 9	N82S210		2k x 8	N82S191	
	4k x 1	N82S400				
	4k x 1	N82S401				
ECL	16 x 4	GXB10145	14 – 15	32 x 8	GXB10139	14 – 15
	64 x 1	GXB10140		256 x 4	GXB10149	
	64 x 1	GXB10142				
	64 x 1	GXB10148				
	128 x 1	GXB10405				
	256 x 1	GXB10144				
	256 x 1	GXB10410				
	1k x 1	GXB10415				

technology	ROM capacity	type	page	specials capacity		type	page
TTL	256 x 4	**N82S226**	14 – 15	8 x 4	SAM	**N82S12**	14 – 15
	256 x 4	**N82S229**		8 x 4	SAM	**N82S112**	
	256 x 8	**N82S214**		32 x 2	WWRM	**N82S21**	
	512 x 4	**N82S230**		16 x 48 x 8	FPLA	**N82S100**	
	512 x 4	**N82S231**		16 x 48 x 8	FPLA	**N82S101**	
	512 x 8	**N82S215**		16 x 9	FPGA	**N82S102**	
	512 x 8	**N82S240**		16 x 9	FPGA	**N82S103**	
	512 x 8	**N82S241**		16 x 48 x 8	FPLA	**N82S106**	
	1k x 4	**N8228**		16 x 48 x 8	FPLA	**N82S107**	
	1k x 8	**N82S280**		16 x 48 x 8	PLA	**N82S200**	
	1k x 8	**N82S281**		16 x 48 x 8	PLA	**N82S201**	
	2k x 8	**N82S290**					
	2k x 8	**N82S291**					
ECL				8 x 2	CAM	**GXB10155**	14 – 15

memories

type index

MOS

	RAM			EPROM		
technology	capacity	type	page	capacity	type	page
MOS	static					
	256 x 1	**2501**	16 – 17	4k	**2704**	16 – 17
	256 x 1	**25L01**		8k	**2708**	
	256 x 1	**HEF4720B(V)**				
	256 x 4	**2101**				
	256 x 4	**2111**				
	256 x 4	**2112**				
	256 x 4	**2606**				
	256 x 4	**2606-1**				
	1k x 1	**2102**				
	1k x 1	**21F02**				
	1k x 1	**21L02**				
	1k x 1	**2102A/AL**				
	1k x 1	**2115**				
	1k x 1	**2125**				
	1k x 4	**2614**				
	1k x 4	**2624**				
	4k x 1	**2613**				
	4k x 1	**2623**				
	dynamic					
	4k x 1	**2627**	16 – 17			
	4k x 1	**2660**				
	4k x 1	**2680**				
	16k x 1	**2690**				

technology	capacity	type	page	shift registers capacity	type	page
MOS	**ROM**			**static**		
	512 x 8	**2530**	16 – 17	2 x 50	**2509**	18
	1k x 8	**2607**		6 x 32	**2518**	
	1k x 8	**2608**		2 x 100	**2510**	
	2k x 4	**2580**		6 x 40	**2519**	
	2k x 8	**2600**		2 x 128	**2521**	
	2k x 8	**2616**		2 x 132	**2522**	
	2k x 8	**2617**		4 x 80	**2532**	
				2 x 200	**2511**	
				2 x 240	**2529**	
				2 x 250	**2528**	
				2 x 256	**2527**	
				1 x 1k	**2533**	
	character generators			**dynamic**		
	64 x 8 x 5	**2513**	16 – 17	2 x 100	**2506**	18
	64 x 6 x 8	**2516**		2 x 100	**2507**	
	64 x 9 x 9	**2526**		2 x 100	**2517**	
	128 x 7 x 9	**2609**		1 x 512	**2505**	
				1 x 512	**2524**	
				4 x 256	**2502**	
				2 x 512	**2503**	
				1 x 1k	**2504**	
				1 x 1k	**2512**	
				1 x 1k	**2525**	

memories

cross reference

Bipolar

AMD	Signetics
2700/27LS00	82S16
2701/27LS01	82S17
27S08/27LS08	82S23
27S09/27LS09	82S123
27S10	82S126
27S11	82S129
2952	82S10/93415A
2953	82S11/93425A
2980	82S101
2981	82S100
3101	82S25
3101A/27S02	3101A

Fairchild	Signetics
10405	GXB10405
10410	GXB10410/10144
10415	GXB10415
10145A	GXB10145
10149	GXB10149
93403	82S25
93406	82S226
93410	74S301
93411	82S17
93411A	82S117
93415	82S10
93415A	93415A
93415B	82S110
93L415	82LS10
93417	82S126
93419	82S09
93421	82S16
93421A	82S116
93425	82S11
93425A	93425A
93425B	82S111
93L425	82LS11
93427	82S129
93431	82S230
93436	82S130
93438	82S140
93441	82S231
93442	82S241
93446	82S131
93448	82S141
93452	82S136
93453	82S137
93454	82S280
93457	82S226
93464	82S281
93467	82S229

Harris	Signetics
0064	82S25
1024/HM7610	82S129
1024A/HM7611	82S126
2048	82S131
2048A	82S130
HM7602/8256	82S23
HM7603	82S123
HM7615	GXB10149
HM7620	82S130
HM7621	82S131
HM7640	82S140
HM7641	82S141
HM7642	82S136
HM7643	82S137
HM7644	82S115 **
HM7699	82S115 **

Intel	Signetics
2708	82S2708
3101	82S25
3101A	3101A
3106/3106A	82S16
3107/3107A	82S17
3301A	82S226
3302	82S230
3304	82S215 **
3322	82S231
3601	82S126
3602	82S130
3604	82S140
3605	82S136
3621	82S129
3622	82S131
3624	82S141
3625	82S137

** Not pin-for-pin compatible.

Intersil	Signetics
5501	82S25
5503	74S301
55S08(A)	82S10
55S18(A)	82S11
5523A	82S16
5533A	82S17
5600	82S23
5603	82S126
5604A	82S130
5605	82S140
56S06	82S136
5610	82S123
5623A	82S129
5624	82S131
5625	82S141
56S26	82S137

Motorola	Signetics
10139	GXB10139
10140	GXB10140
10142	GXB10142
10144	GXB10144/10410
10145	GXB10145
10146/10415	GXB10415
10147	GXB10405
10148	GXB10148
10149	GXB10149
4004A	82S226
4064	82S25
4256	82S16
5005	82S126
68708	82S2708

MMI	Signetics
10149	GXB10149
6200	82S226
6201	82S229
6205	82S230
6206	82S231
6275	82S290
6276	82S291
6280	82S280
6281	82S281
6300-1	82S126
6301-1	82S129
6305-1	82S130
6306-1	82S131
6330	82S23
6331	82S123
6335	82S114 **
6340	82S140
6341	82S141
6348	82S146
6349	82S147
6352	82S136
6353	82S137
6380	82S180
6381	82S181
6385	82S2708
6530	82S17
6531	82S16
6555	82S09
6560	82S25/3101A
6561	74S189
82S100	82S100
82S101	82S101

National Semiconductor	Signetics
74187	82S226
8573	82S126
8574	82S129
8582	82S17
8588	82S23
86L99	82S25

TI	Signetics
2708	82S2708
	82S400
	82S401
10142	GXB10142
10144	GXB10144/10410
10147	GXB10405
74187	82S226
74S188	82S23
74S189	74S189
74S89	74S89
74S200	74S200
74S201	74S201
74S209	82S11/93425A
74S270	82S230
74S287	82S129
74S288	82S123
74S289	3101A
74S301	74S301
74S309	82S10/93415A
74S370	82S231
74S387	82S126
74S472	82S146
74S473	82S147

** Not pin-for-pin compatible.

memories

cross reference

MOS

AMD	Signetics
2102	2102 21F02 21L02
9216	2617
AM1402APC	2502
AM1403A	2503
AM1404A	2504
AM1507	2517
AM1507T	2506
AM2505K	2505
AM2806HC	2512
AM2807PC	2524
AM2808PC	2525
AM2809	2521
AM2833PC	2533
AM9060	2680
P1101	2501

Electronic Arrays	Signetics
4600	2600
4900	2600

Fairchild	Signetics
2102	2102 21F02 21L02
3343	2521
3344	2522
3347	2532
3349	2518
3533	2533
F4720	HEF4720B

General Instruments	Signetics
2509	2509
2510	2510
2511	2511
2513	2513
2516	2516
2530	2530
2533	2533
2580	2580

Intel	Signetics
2101	2101
2102A	2102 21F02 21L02 2102A
2102AL	2102AL
2107B	2680
2111	2111
2112	2112
2114	2614
2115	2115
2116A	2690
2125	2125
2308	2607
2316E	2616
2704	2704
2708	2607 2708
C1402A	2502
C1403A	2503
M1404A	2504
M1405A	2505
P1101	2501

Intersil	Signetics
IM7501	2501
IM7552	2102
	21F02
	21L02
IM7712C	2512
IM7722C	2525
IM7780C	2532

Mostek	Signetics
29000	2600
MK1007P	2532
MK4007	2501
	25L01
MK4027	2627
MK4096	2660
MK4102	2102
	21F02
	21L02
MK4116	2690

Motorola	Signetics
6570	2609
6830	2608

National Semiconductor	Signetics
MM1101	2501
MM1402A	2502
MM1403A	2503
MM1404A	2504
MM1506H	2506
MM1507H	2517
MM2102	2102
	21F02
	21L02
MM2521	2521
MM2522	2522
MM5058	2533
MM5280	2680

Synertex	Signetics
2316B	2616
4600	2600

Texas Instruments	Signetics
TMS3112NC	2518
TMS3120NC	2532
TMS3128NC	2521
TMS3129NC	2522
TMS3133NC	2533
TMS4035	2102
	21F02
	21L02
TMS4030	2680
TMS4060	2680

memories

technical data

Bipolar

Output structure: OC open collector
TS three-state

	capacity	type	output structure	no. of pins	t_{AA} max ns	input current µA	supply voltage V	max supply current mA	packages
TTL-RAM	16 x 4	**N3101A** *	OC	16	35	100	5	105	N, F
	16 x 4	**N74S89**	OC	16	50	100	5	105	N, F
	16 x 4	**N74S189**	TS	16	35	250	5	110	N, F
	16 x 4	**N82S25**	OC	16	50	100	5	105	N, F
	256 x 1	**N74S200**	TS	16	50	100	5	130	N, F
	256 x 1	**N74S201**	TS	16	50	100	5	130	N, F
	256 x 1	**N74S301**	OC	16	50	100	5	130	N, F
	256 x 1	**N82S16**	TS	16	50	100	5	115	N, F
	256 x 1	**N82S17**	OC	16	50	100	5	115	N, F
	256 x 1	**N82S116**	TS	16	40	100	5	115	N, F
	256 x 1	**N82S117**	OC	16	40	100	5	115	N, F
	64 x 9	**N82S09**	OC	28	45	100	5	190	N, I
	1024 x 1	**N82S10**	OC	16	45	100	5	170	N, F
	1024 x 1	**N82S11**	TS	16	45	100	5	170	N, F
	1024 x 1	**N82S110**	OC	16	35	100	5	170	N, F
	1024 x 1	**N82S111**	TS	16	35	100	5	170	N, F
	1024 x 1	**N93415A**	OC	16	45	100	5	170	N, F
	1024 x 1	**N93425A**	TS	16	45	100	5	170	N, F
	1024 x 1	**N82LS10** *	OC	16	60	100	5	60	N, F
	1024 x 1	**N82LS11** *	TS	16	60	100	5	60	N, F
	256 x 8	**N82S208**	TS	22	60	100	5	185	N, F
	256 x 9	**N82S210**	TS	24	60	100	5	185	N, F
	4096 x 1	**N82S400** *	OC	18	70	150	5	155	I
	4096 x 1	**N82S401** *	TS	18	70	150	5	155	I

* In development.

Military versions of industrial ICs with prefix N have S as a prefix.
Example: industrial version N82S25, military version S82S25.
The specifications shown below apply to industrial versions. There is generally some derating in specification for military versions due to the extended temperature range.

Temperature ranges

C 0 to 75 °C
M −55 to +125 °C

chip enable lines	temp. range	pin compatible types ▲ = fully compatible	second sourced by	pin diagram on page
1	M, C	82S25, 74S89	AMD, Intel, MMI, TI	26
1	M, C	N3101A, 82S25	TI	26
1	M, C	–	MMI, TI	26
1	M, C	N3101A, 74S89	AMD, Fch, Harris, Intel, Intersil, MMI, Mot, National	26
3	M, C	82S16, 82S116, 74S201 ▲	TI	24
3	M, C	82S16, 82S116, 74S200 ▲	TI	24
3	M, C	82S17, 82S117	Fch, Intersil, TI	24
3	M, C	82S116, 74S200, 74S201	AMD, Fch, Intel, Intersil, MMI, Mot	24
3	M, C	82S117, 82S301	AMD, Fch, Intel, Intersil, MMI	24
3	C	82S16, 74S200, 74S201	Fch	24
3	C	82S17, 74S301	Fch	24
1	M, C	–	Fch, MMI	27
1	M, C	82S110, 93415A ▲, 82LS10	AMD, Fch, Intersil, TI	25
1	M, C	82S111, 93425A, 82LS11	AMD, Fch, Intersil, TI	25
1	C	82S10, 93415A, 82LS10	Fch	25
1	C	82S11, 93425A, 82LS11	Fch	25
1	C	82S10 ▲, 82S110, 82LS10	AMD, Fch, TI	25
1	C	82S11 ▲, 82S111, 82LS11	AMD, Fch, TI	25
1	C	82S10, 93415A, 82S110	Fch	25
1	C	82S11, 93425A, 82S111	Fch	25
1	C	–	–	27
1	C	–	–	27
1	C	–	TI	25
1	C	–	TI	25

memories

technical data

Bipolar

Output structure: OC open collector
TS three-state

	capacity	type	output structure	no. of pins	t_{AA} max ns	input current µA	supply voltage V	max supply current mA	packages
TTL-PROM	32 x 8	**N82S23**	OC	16	50	100	5	77	N, F
	32 x 8	**N82S123**	TS	16	50	100	5	77	N, F
	256 x 4	**N82S27**	OC	16	40	1600	5	140	F
	256 x 4	**N82S126**	OC	16	50	100	5	120	N, F
	256 x 4	**N82S129**	TS	16	50	100	5	120	N, F
	256 x 8	**N82S114**	TS	24	60	100	5	180	N, F
	512 x 4	**N82S130**	OC	16	50	100	5	140	N, F
	512 x 4	**N82S131**	TS	16	50	100	5	140	N, F
	512 x 8	**N82S115**	TS	24	60	100	5	180	N, F
	512 x 8	**N82S140**	OC	24	60	100	5	175	N, F
	512 x 8	**N82S141**	TS	24	60	100	5	175	N, F
	512 x 8	**N82S146** *	OC	20	45	–	5	–	N
	512 x 8	**N82S147** *	TS	20	45	–	5	–	N
	1024 x 4	**N82S136**	OC	18	60	100	5	140	F
	1024 x 4	**N82S137**	TS	18	60	100	5	140	F
	1024 x 8	**N82S180**	OC	24	70	100	5	150	F
	1024 x 8	**N82S181**	TS	24	70	100	5	150	F
	1024 x 8	**N82S2708**	TS	24	70	100	5	150	F
	2048 x 4	**N82S184**	OC	18	100	100	5	120	I
	2048 x 4	**N82S185**	TS	18	100	100	5	120	I
	2048 x 8	**N82S190**	OC	24	80	100	5	175	N, F
	2048 x 8	**N82S191**	TS	24	80	100	5	175	N, F

* In development.

Military versions of industrial ICs with prefix N have S as a prefix.
Example: industrial version N82S25, military version S82S25.
The specifications shown below apply to industrial versions. There is generally some derating in specification for military versions due to the extended temperature range.

Temperature ranges

C 0 to 75 °C
M −55 to +125 °C

chip enable lines	temp. range	pin compatible types ▲ = fully compatible	second sourced by	pin diagram on page
1	M, C	–	AMD, Harris, Intersil, MMI, National, TI	21
1	M, C	–	AMD, Harris, Intersil, MMI, TI	21
2	C	82S126, 82S226	–	19
2	M, C	82S226 ▲, 82S27	AMD, Fch, Harris, Intel, Intersil, MMI, Mot, National, TI	19
2	M, C	82S229 ▲	AMD, Fch, Harris, Intel, Intersil, MMI, National, TI	19
2	M, C	82S214 ▲	MMI **	21
1	M, C	82S230 ▲	Fch, Harris, Intel, Intersil, MMI	19
1	M, C	82S231 ▲	Fch, Harris, Intel, Intersil, MMI	19
2	M, C	82S215 ▲	Harris **	22
4	M, C	82S240 ▲	Fch, Harris, Intel, Intersil, MMI	22
4	M, C	82S241 ▲	Fch, Harris, Intel, Intersil, MMI	22
1	C	–	MMI, TI **	22
1	C	–	MMI, TI **	22
2	M, C	–	Fch, Harris, Intel, Intersil, MMI	20
2	M, C	–	Fch, Harris, Intel, Intersil, MMI	20
4	M, C	82S280 ▲	MMI	23
4	M, C	82S281 ▲	MMI	23
1	M, C	–	MMI, (EPROM – Intel, Mot, TI)	23
1	M, C	–	–	20
1	M, C	–	–	20
3	C	82S290 ▲	–	23
3	C	82S291 ▲	–	23

** Not pin-for-pin compatible.

memories

technical data

Bipolar

Output structure: OC open collector OE open emitter
TP totem pole TS three-state

	capacity	type	output structure	no. of pins	t_{AA} max ns	input current µA	supply voltage V	max supply current mA	packages
TTL-ROM	256 x 4	N82S226	OC	16	50	100	5	120	N, F
	256 x 4	N82S229	TS	16	50	100	5	120	N, F
	256 x 8	N82S214	TS	24	60	100	5	175	F
	512 x 4	N82S230	OC	16	50	100	5	135	F
	512 x 4	N82S231	TS	16	50	100	5	135	F
	512 x 8	N82S215	TS	24	60	100	5	175	F
	512 x 8	N82S240	OC	24	60	100	5	175	F
	512 x 8	N82S241	TS	24	60	100	5	175	F
	1024 x 4	N8228	TP	16	70	400	5	170	F, I
	1024 x 8	N82S280	OC	24	70	100	5	150	I
	1024 x 8	N82S281	TS	24	70	100	5	150	I
	2048 x 8	N82S290	OC	24	70	100	5	170	F
	2048 x 8	N82S291	TS	24	70	100	5	170	F
TTL-SAM	8 x 4	N82S12	OC	24	35	250	5	160	N, F
	8 x 4	N82S112	TS	24	35	250	5	160	N, F
TTL-WWRM	32 x 2	N82S21	OC	16	50	1600	5	130	N, F
TTL-FPLA	16 x 48 x 8	N82S100	TS	28	50	100	5	170	N, I
	16 x 48 x 8	N82S101	OC	28	50	100	5	170	N, I
	16 x 48 x 8	N82S106	OC	28	50	100	5	170	N, I
	16 x 48 x 8	N82S107	TS	28	50	100	5	170	N, I
TTL-FPGA	16 x 9	N82S102	OC	28	30	100	5	170	N, I
	16 x 9	N82S103	TS	28	30	100	5	170	N, I
TTL-PLA	16 x 48 x 8	N82S200	TS	28	50	100	5	170	N, I
	16 x 48 x 8	N82S201	OC	28	50	100	5	170	N, I
ECL-RAM	64 x 1	GXB10140	OE	16	15	265	5,2	80 (typ)	D, P
	64 x 1	GXB10142	OE	16	10	265	5,2	100	D, P
	64 x 1	GXB10148	OE	16	15	265	5,2	80 (typ)	D, P
	16 x 4	GXB10145	OE	16	–	220	5,2	145	D, P
	128 x 1	GXB10405	OE	16	15	200	5,2	110	E
	256 x 1	GXB10144	OE	16	30	200	5,2	112	D, E
	256 x 1	GXB10410	OE	16	35	220	5,2	125	E
	1024 x 1	GXB10415 *	OE	16	25	–	5,2	–	E
ECL-PROM	32 x 8	GXB10139	OE	16	20	265	5,2	145	D
	256 x 4	GXB10149	OE	16	20	265	5,2	150	D, E
ECL-CAM	8 x 2	GXB10155	OE	18	13	220	5,2	140	E

* In development.

Military versions of industrial ICs with prefix N have S as a prefix.
Example: industrial version N82S25, military version S82S25.
The specifications shown below apply to industrial versions. There is generally some derating in specification for military versions due to the extended temperature range.

Temperature ranges

TTL – C – 0 to 75 °C
TTL – M – −55 to +125 °C
ECL – C – −30 to + 85 °C

chip enable lines	temp. range	pin compatible types ▲ = fully compatible	second sourced by	pin diagram on page
2	M, C	N82S126 ▲, N82S27	Fch, Intel, MMI, Mot, National, TI	19
2	M, C	N82S129 ▲	Fch, MMI	19
2	M, C	N82S114	–	21
1	M, C	N82S130 ▲	Fch, Intel, MMI, TI	19
1	M, C	N82S131 ▲	Fch, Intel, MMI, TI	19
2	M, C	N82S115 ▲	–	22
4	C	N82S140 ▲	–	22
4	C	N82S141 ▲	Fch	22
–	C	–	–	20
4	M, C	N82S180 ▲	Fch, MMI	23
4	M, C	N82S181 ▲	Fch, MMI	23
3	C	N82S190 ▲	MMI	23
3	C	N82S191 ▲	MMI	23
2 wr. en.	C	–	–	28
2 wr. en.	C	–	–	28
–	C	–	–	28
1	M, C	N82S200 ▲	AMD, MMI	29
1	M, C	N82S201 ▲	AMD, MMI	29
–	C	–	–	29
–	C	–	–	29
1	M, C	–	–	29
1	M, C	–	–	29
1	M, C	N82S100	–	29
1	M, C	N82S101	–	29
2	C	GXB10142, GXB10148	Mot	24
2	C	GXB10140, GXB10148	Mot, TI	24
2	C	GXB10140, GXB10142	Mot	24
1	C	–	Fch, Mot	26
–	C	–	Mot, TI	24
3	C	GXB10410	Fch, Mot, TI	24
3	C	GXB10144	Fch, Mot, TI	24
–	C	–	Fch, Mot	25
1	C	–	Mot	21
1	C	–	Fch, Harris, MMI, Mot	19
–	C	–	–	28

MOS

	capacity	type	no. of pins	tAA typ ns	supply voltage V
Static RAM	256 x 1	**2501**	16	1000	+5, −9
	256 x 1	**25L01**	16	1000	+5, −12
	256 x 4	**2101**	22	450 – 1000	+5
	256 x 4	**2111**	18	450 – 1000	+5
	256 x 4	**2112**	16	450 – 1000	+5
	256 x 4	**2606**	16	750	+5
	256 x 4	**2606-1**	16	500	+5
	1024 x 1	**2102**	16	500 – 1000	+5
	1024 x 1	**21F02**	16	250 – 450	+5
	1024 x 1	**21L02**	16	400 – 1000	+5
	1024 x 1	**2102A/AL**	16	150 – 650	+5
	1024 x 1	**2115**	16	35 – 75	+5
	1024 x 1	**2125**	16	35 – 75	+5
	1024 x 4	**2614** *	18		+5
	1024 x 4	**2624** *	18		+5
	4096 x 1	**2613** *	18		+5
	4096 x 1	**2623** *	18		+5
LOCMOS static RAM	256 x 1	**HEF4720B(V)**	16	150 – 450	+3 to +15
Dynamic RAM	4096 x 1	**2660**	16	200 – 350	+12, +5, −5
	4096 x 1	**2680**	22	200 – 350	+12, +5, −5
	4096 x 1	**2627**	16	150 – 250	+12, +5, −5
	4096 x 1	**2390** *	16	150 – 250	+12, +5, −5
ROMs and character generators p-channel	512 x 8	**2530**	24	700	+5, −12
	2048 x 4	**2580**	24	950	+5, −12
	64 x 8 x 5	**2513**	24	600	+5, −12
	64 x 6 x 8	**2516**	24	600	+5, −12
	64 x 9 x 9	**2526**	24	700	+5, −12
n-channel	1024 x 8	**2607**	24	450	+5
	1024 x 8	**2608**	24	550	+5
	2048 x 8	**2600**	24	300	+5
	2048 x 8	**2616**	24	300	+5
	2048 x 8	**2617**	24	450	+5
	4096 x 8	**2632** *	24		+5
	4096 x 8	**2633** *	24		+5
	128 x 7 x 9	**2609**	24	500	+5
EPROM	4096	**2704**	24	450	+12, +5, −5
	8192	**2708**	24	450	+12, +5, −5

* In development.

Temperature range
C = 0 to +70 °C
XC = −40 to +85 °C

chip enable lines	temp. range	pin compatible types	second sourced by	pin diagram on page
–	C	25L01	AMD, Intel, Intersil, Mostek, National	30
1	C	2501	Mostek	30
2	C	–	Intel	32
2	C	–	Intel	32
1	C	–	Intel	33
1	C	2606-1	–	33
1	C	2606	–	33
1	C	21F02, 21L02, 2102A/AL	AMD, Fch, Intel, Intersil, Mostek, National, TI	30
1	C	2102, 21L02, 2102A/AL		30
1	C	2102, 21F02, 2102A/AL		30
1	C	2102, 21F02, 21L02	Intel	30
1	C	2125	Intel	31
1	C	2115	Intel	31
–	C	2624	Intel	33
–	C	2614	Intel	33
–	C	2623	Intel	31
–	C	2613	Intel	31
1	XC	–	Fch	30
1	C	–	Mostek	34
1	C	–	AMD, Intel, National, TI	34
1	C	–	Mostek	34
1	C	–	Intel, Mostek	34
1	C	–	GI	35
4	C	–	GI	36
1	C	–	GI	38
1	C	–	GI	38
1	C	–	–	38
2	C	–	Intel	35
4	C	–	Motorola	35
2	C	–	Electronic Arrays, Mostek, Synertex	36
3	C	–	Intel, Synertex	37
3	C	–	AMD	37
–	C	–	–	37
–	C	–	will be industry standard	–
4	C	–	Motorola	39
1	C	–	Intel	39
1	C	–	Intel	39

memories

technical data

MOS

Several types can be made available in Cerdip (F package) and metal ceramic (I package).

Static shift registers – one clock (TTL compatible)
– power supplies +5 and –12 V; 2509/10/11 also –5 V

capacity	type	output structure	on-chip recirculate	package leads	typ speed MHz	second sourced by	pin diagram on page
hex 32 bits	2518	bare drain	yes	N-16	3,0	Fch, TI	40
hex 40 bits	2519	bare drain	yes	N-16	3,0	–	40
dual 50 bits	2509	three-state	yes	N-14, K	3,0	GI	40
quad 80 bits	2532	push-pull	yes	N-16	3,0	Fch, Intersil, Mostek, TI	41
dual 100 bits	2510	three-state	yes	N-14, K	3,0	GI	40
dual 128 bits	2521	push-pull	yes	N-8	3,0	AMD, Fch, National, TI	41
dual 132 bits	2522	push-pull	yes	N-8	3,0	Fch, National, TI	41
dual 200 bits	2511	three-state	yes	N-14, K	3,0	GI	40
dual 240 bits	2529	push-pull	yes	N-8	3,0	–	41
dual 250 bits	2528	push-pull	yes	N-8	3,0	–	41
dual 256 bits	2527	push-pull	yes	N-8	3,0	–	41
1024 bits	2533	push-pull	jumper	N-8	2,0	AMD, Fch, GI, National, TI	41

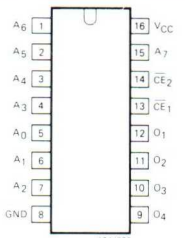
Dynamic shift registers – two clocks (not TTL compatible)
– power supplies +5 and –5 V

dual 100 bits	2517	20 kΩ PD	no	T, N-8	4,0	AMD, National	42
dual 100 bits	2507	7,5 kΩ PD	no	T, N-8	4,0		42
dual 100 bits	2506	bare drain	no	T, N-8	4,0	AMD, National	42
quad 256 bits	2502	bare drain	no	N-16	10,0	AMD, Intel, National	42
512 bits	2524	bare drain	yes	N-8	5,0	AMD	42
512 bits	2505	bare drain	yes	K	3,0	AMD, Intel	43
dual 512 bits	2503	bare drain	no	TA, N-8	10,0	AMD, Intel, National	43
1024 bits	2525	bare drain	yes	N-8	5,0	AMD, Intersil	42
1024 bits	2512	bare drain	yes	K	3,0	AMD, Intersil	43
1024 bits	2504	bare drain	no	TA, N-8	10,0	AMD, Intel, National	43

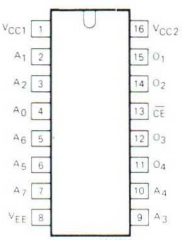
pin diagrams — second sources

Bipolar

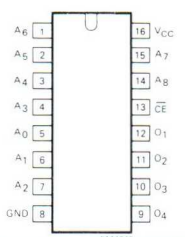
ROMs and PROMs 4 bits wide



type	capacity/output structure	second source
82S27	256 x 4 PROM/OC	–
82S126	256 x 4 PROM/OC	AMD 27S10, Fch 93417, Harris 1024A/7611, Intel 3601, Intersil 5603, MMI 6300-1, Mot 5005, National 8573, TI 74S387
82S129	256 x 4 PROM/TS	AMD 27S11, Fch 93427, Harris 1024/HM7610, Intel 3621, Intersil 5623A, MMI 6301-1, National 8574, TI 74S287
82S226	256 x 4 ROM/OC	Fch 93406, Intel 3301A, MMI 6200, Mot 4004A, National 74187,
82S229	256 x 4 ROM/TS	TI 74187 Fch 93467, MMI 6201



GXB10149	256 x 4 PROM/OE	Fch 10149, Harris HM7615, MMI 10149, Mot 10149



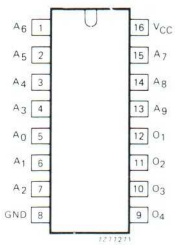
82S130	512 x 4 PROM/OC	Fch 93436, Harris HM7620, Intel 3602, Intersil 5604A, MMI 6305-1
82S131	512 x 4 PROM/TS	Fch 93446, Harris HM7621, Intel 3622, Intersil 5624, MMI 6306-1
82S230	512 x 4 ROM/OC	Fch 93431, Intel 3302, MMI 6205, TI 74S270
82S231	512 x 4 ROM/TS	Fch 93441, Intel 3322, MMI 6206, TI 74S370

memories

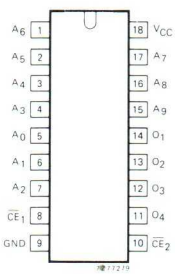
pin diagrams — second sources

Bipolar

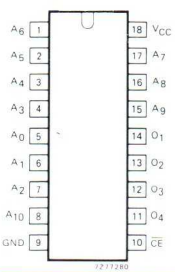
ROMs and PROMs 4 bits wide



type	capacity/output structure	second source
8228	1024 x 4 ROM/TP	–

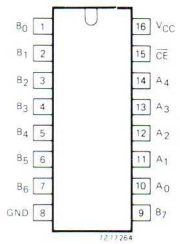


82S136	1024 x 4 PROM/OC	Fch 93452, Harris HM7642, Intel 3605, Intersil 56S06, MMI 6352
82S137	1024 x 4 PROM/TS	Fch 93453, Harris HM7643, Intel 3625, Intersil 56S26, MMI 6353

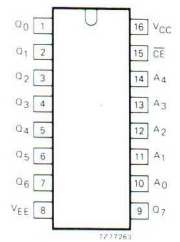


82S184	2048 x 4 PROM/OC	–
82S185	2048 x 4 PROM/TS	–

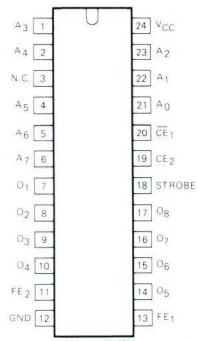
ROMs and PROMs 8 bits wide



type	capacity/output structure	second source
82S23	32 x 8 PROM/OC	AMD 27S08/27LS08, Harris HM7602/8256, Intersil 5600, MMI 6330, National 8588, TI 74S188
82S123	32 x 8 PROM/TS	AMD 27S09/27LS09, Harris HM7603, Intersil 5610, MMI 6331, TI 74S288



GXB10139	32 x 8 PROM/OE	Mot 10139



82S114	256 x 8 PROM/TS	MMI 6335**
82S214	256 x 8 ROM/TS	

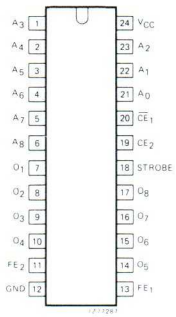
** Not pin-for-pin compatible.

memories

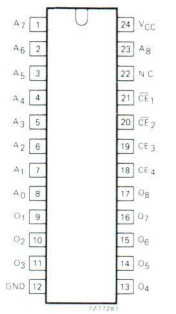
pin diagrams — second sources

Bipolar

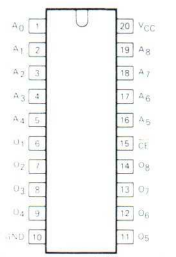
ROMs and PROMs 8 bits wide



type	capacity/output structure	second source
82S115	512 x 8 PROM/TS	Harris HM7644**/HM7699**
82S215	512 x 8 ROM/TS	—

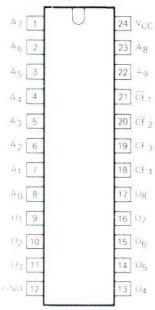


82S140	512 x 8 PROM/OC	Fch 93438, Harris HM7640, Intel 3604, Intersil 5605, MMI 6340
82S141	512 x 8 PROM/TS	Fch 93448, Harris HM7641, Intel 3624, Intersil 5625, MMI 6341
82S240	512 x 8 ROM/OC	—
82S241	512 x 8 ROM/TS	Fch 93442

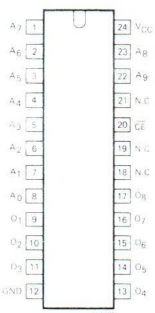


82S146	512 x 8 PROM/OC	MMI 6348, TI 74S472**
82S147	512 x 8 PROM/TS	MMI 6349, TI 74S473**

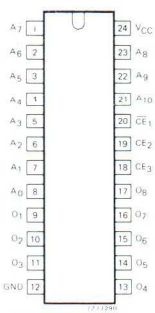
** Not pin-for-pin compatible.



type	capacity/output structure	second source
82S180	1024 x 8 PROM/OC	MMI 6380
82S181	1024 x 8 PROM/TS	MMI 6381
82S280	1024 x 8 ROM/OC	Fch 93454, MMI 6280
82S281	1024 x 8 ROM/TS	Fch 93464, MMI 6281



82S2708	1024 x 8 PROM/TS	MMI6385, EPROM – Intel 2708, Mot 68708, TI 2708



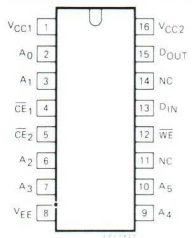
82S190	2048 x 8 PROM/OC	–
82S191	2048 x 8 PROM/TS	–
82S290	2048 x 8 ROM/OC	MMI 6275
82S291	2048 x 8 ROM/TS	MMI 6276

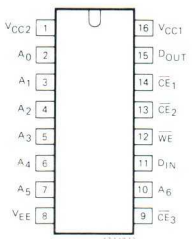
memories

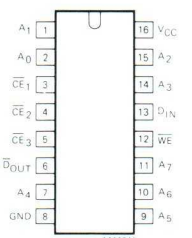
pin diagrams — second sources

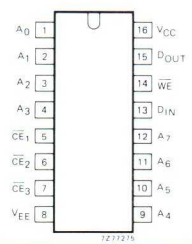
Bipolar

RAMs 1 bit wide



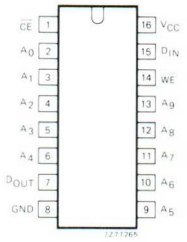




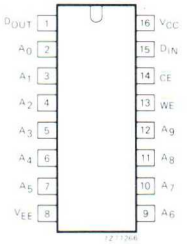


type	capacity/output structure	second source
GXB10140	64 x 1/OE	Mot 10140
GXB10142	64 x 1/OE	Mot 10142, TI 10142
GXB10148	64 x 1/OE	Mot 10148
GXB10405	128 x 1/OE	Mot 10147, TI 10147
74S200	256 x 1/TS	TI 74S200
74S201	256 x 1/TS	TI 74S201
74S301	256 x 1/OC	Fch 93410, Intersil 5503, TI 74S301
82S16	256 x 1/TS	AMD 2700/27LS00, Fch 93421, Intel 3106/3106A, Intersil 5523A, MMI 6531, Mot 4256
82S116	256 x 1/TS	Fch 93421A
82S17	256 x 1/OC	AMD 2701/27LS01, Fch 93411, Intel 3107/3107A, Intersil 5533A, MMI 6530
82S117	256 x 1/OC	Fch 93411A
GXB10144	256 x 1/OE	Fch 10410, Mot 10144, TI 10144
GXB10410	256 x 1/OE	Fch 10410, Mot 10144, TI 10144

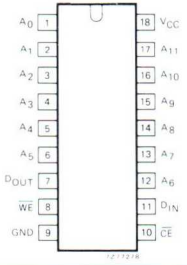
RAMs 1 bit wide



type	capacity/output structure	second source
82S10	1024 x 1/OC	AMD 2952, Fch 93415, Intersil 55S08(A), TI 74S309
82S110	1024 x 1/OC	Fch 93415B
82S11	1024 x 1/TS	AMD 2953, Fch 93425, Intersil 55S18(A), TI 74S209
82S111	1024 x 1/TS	Fch 93425B
82LS10	1024 x 1/OC	Fch 93L415
82LS11	1024 x 1/TS	Fch 93L425
93415A	1024 x 1/OC	AMD 2952, Fch 93415A, TI 74S309
93425A	1024 x 1/TS	AMD 2953, Fch 93425A, TI 74S209



GXB10415	1024 x 1/OE	Fch 10415, Mot 10146/10415

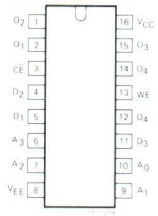


82S400	4096 x 1/OC	TI 2708
82S401	4096 x 1/TS	TI 2708

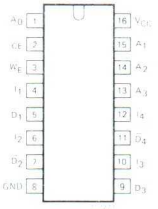
pin diagrams — second sources

Bipolar

RAMs 4 bits wide

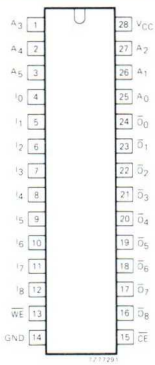


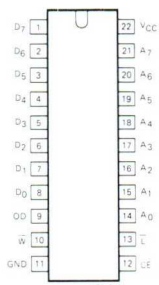
type	capacity/output structure	second source
GXB10145	16 x 4/OE	Fch 10145A, Mot 10145,

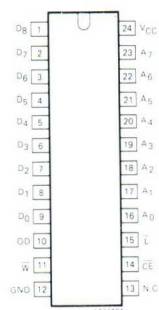


82S25	16 x 4/OC	AMD 3101, Fch 93403, Harris 0064, Intel 3101, Intersil 5501, MMI 6560, Mot 4064, National 86L99
74S89	16 x 4/OC	TI 74S89
74S189	16 x 4/TS	MMI 6561, TI 74S189
3101A	16 x 4/OC	AMD 3101A/27S02, Intel 3101A, MMI 6560, TI 74S289

RAMs 1 byte (8 or 9 bits) wide



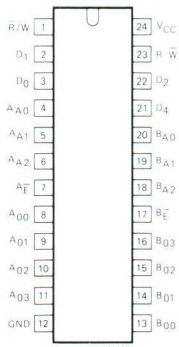




type	capacity/output structure	second source
82S09	64 x 9/OC	Fch 93419, MMI 6555
82S208	256 x 8/TS	–
82S210	256 x 9/TS	–

Bipolar

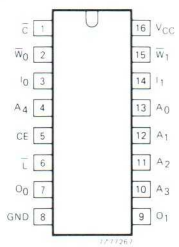
Specials (SAM, WWRM, CAM)



type	capacity/output structure	second source
82S12	8 x 4 SAM/OC	–
82S112	8 x 4 SAM/TS	–

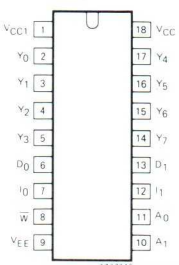
A **S**imultaneous **A**ddressable **M**emory or multiport memory is one in which different locations can be selected at the same time.

The 82S12/112 SAM-element has two independent sets of address-decoders and outputs.



82S21 32 x 2 WWRM/OC –

A **W**rite **W**hile **R**ead **M**emory element is a RAM provided with output latches, in such a way that (read out) data may be retained in the latches either when the chip is disabled or when new information has to be written in the memory.

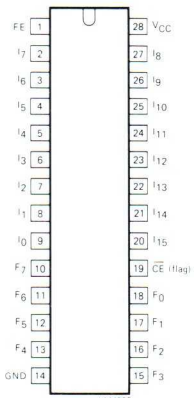


GXB10155 8 x 2 CAM/OE –

In a **C**ontent **A**ddressable **M**emory or association memory the address information is associated with the memory content to search whether and/or in which location this information is stored; data is searched in parallel.

The normal functions of read-out and write-in can also be performed.

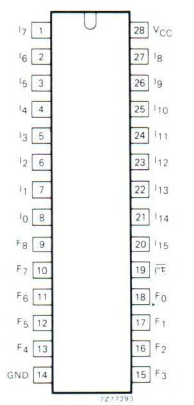
Specials (PLA, FPLA, FPGA)



type	capacity/output structure	second source
82S100	16 x 48 x 8 FPLA/TS	AMD 2981, MMI 82S100
82S101	16 x 48 x 8 FPLA/OC	AMD 2980, MMI 82S101
82S200	16 x 48 x 8 PLA/TS	–
82S201	16 x 48 x 8 PLA/OC	–
82S106	16 x 48 x 8 FPLA/OC	–
82S107	16 x 48 x 8 FPLA/TS	–

In the 82S106/107, the chip enable input is replaced by a "flag" output indicating whether a programmed product term is activated.

The Programmable Logic Array is a two level AND-OR/AND-NOR combinational logic element, consisting of a system of logic gates with programmable inputs and outputs in order to generate series of product-terms according to customer requirements. Programming can either be done during production (PLA) or by the customer in the field (FPLA).

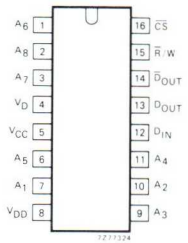


82S102	16 x 9 FPGA/OC	–
82S103	16 x 9 FPGA/TS	–

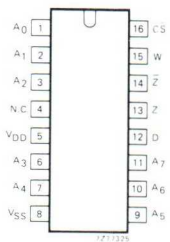
The Field Programmable Gate Array is a one-level AND/NAND logic element with programmable inputs and outputs to generate several AND/NAND functions according to customer requirements.

MOS

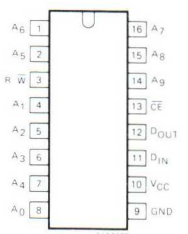
Static RAMs 1-bit wide



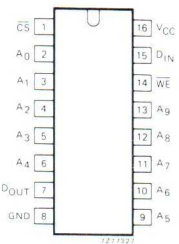
type	capacity	second source
2501	256 x 1	AMD P1101, Intel P1101, Intersil IM7501, Mostek MK4007, National MM1101
25L01	256 x 1	Mostek MK4007



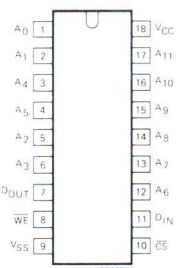
HEF4720B(V)	256 x 1	Fch F4720



2102	1024 x 1	AMD 2102, Fch 2102, Intel 2102A, Intersil IM7552, Mostek MK4102, National MM2102, TI TMS4035
21F02	1024 x 1	
21L02	1024 x 1	
2102A	1024 x 1	Intel 2102A
2102AL	1024 x 1	Intel 2102AL



type	capacity	second source
2115	1024 x 1	Intel 2115
2125	1024 x 1	Intel 2125



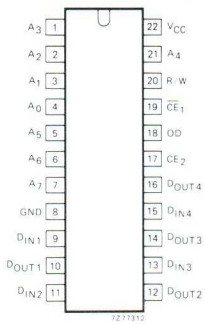
2613	4096 x 1	Intel
2623	4096 x 1	Intel

memories

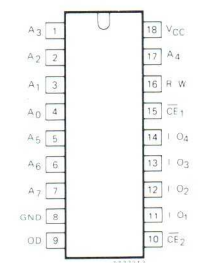
pin diagrams — second sources

MOS

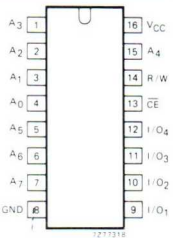
Static RAMs 4-bits wide



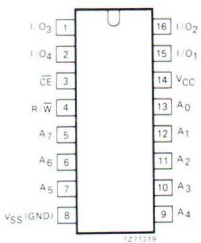
type	capacity	second source
2101	256 x 4	Intel 2101



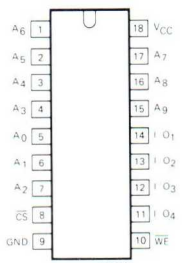
2111	256 x 4	Intel 2111



type	capacity	second source
2112	256 x 4	Intel 2112



2606	256 x 4	–
2606-1	256 x 4	–



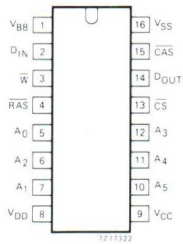
2614	1024 x 4	Intel 2114
2624	1024 x 4	Intel

memories

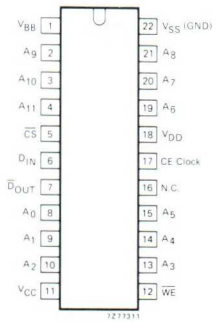
pin diagrams — second sources

MOS

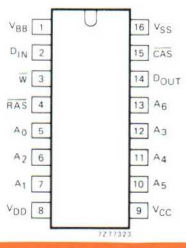
Dynamic RAMs 1-bit wide



type	capacity	second source
2627	4096 x 1	Mostek MK4027
2660	4096 x 1	Mostek MK4096

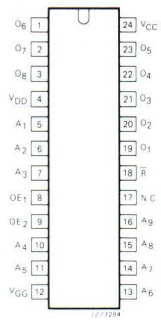


2680	4096 x 1	AMD 9060, Intel 2107B, National MM5280, TI TMS4060, TMS4030

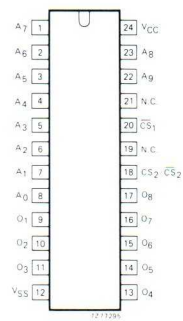


2690	16384 x 1	Intel 2116A, Mostek MK4116

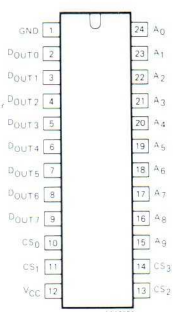
ROMs 8-bits wide



type	capacity	second source
2530	512 x 8	General 2530



2607	1024 x 8	Intel 2308, EPROM – Intel 2708



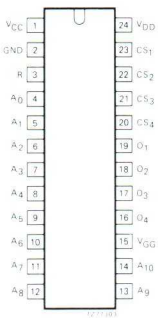
2608	1024 x 8	Motorola 6830

memories

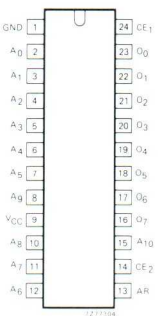
pin diagrams — second sources

MOS

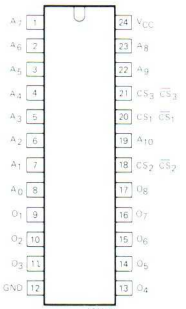
ROMs 4 and 8-bits wide

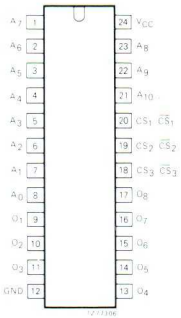


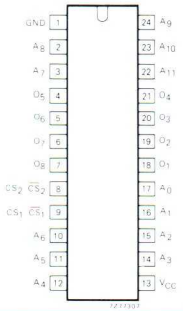
type	capacity	second source
2580	2048 x 4	General 2580



2600	2048 x 8	Electronic Arrays 4600 and 4900, Mostek 29000, Synertex 4600







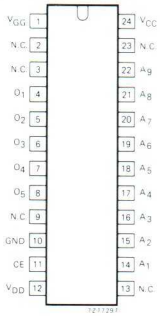
type	capacity	second source
2616	2048 x 8	Intel 2316E, Synertex 2316B
2617	2048 x 8	AMD 9216
2632	4096 x 8	–

memories

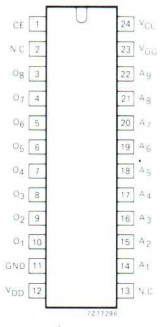
pin diagrams — second sources

MOS

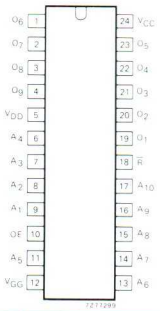
Character generators



type	capacity	second source
2513	64 x 8 x 5	General 2513

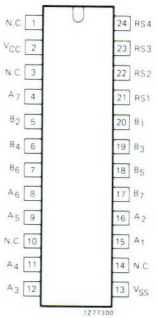


2516	64 x 6 x 8	General 2516

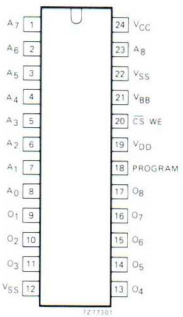


2526	64 x 9 x 9	—

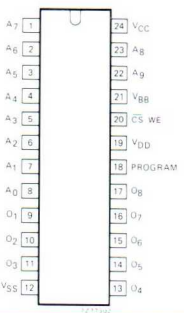
EPROMs



type	capacity	second source
2609	128 x 7 x 9	Motorola 6570



2704	4096	Intel 2704



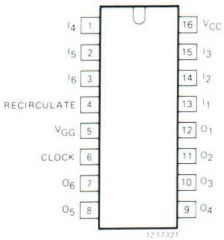
2708	8192	Intel 2708

memories

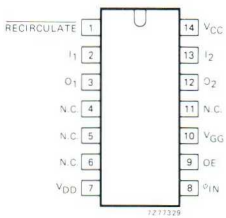
pin diagrams — second sources

MOS

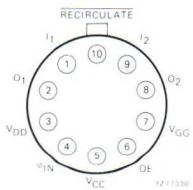
Static shift registers

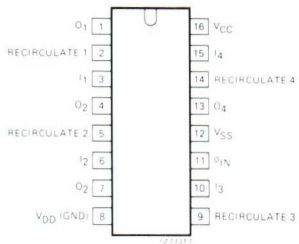


type	capacity	second source
2518	6 x 32	Fch 3349, TI TMS3112NC
2519	6 x 40	—

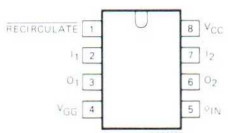


2509	2 x 50	General 2509
2510	2 x 100	General 2510
2511	2 x 200	General 2511

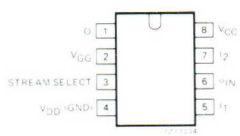




type	capacity	second source
2532	4 x 80	Fch 3347, Intersil IM7780C Mostek MK1007P, TI TMS3120NC



2521	2 x 128	AMD AM2809, Fch 3343, National MM2521, TI TMS3128NC
2522	2 x 132	Fch 3344, National MM2522, TI TMS3129NC
2529	2 x 240	–
2528	2 x 250	–
2527	2 x 256	–

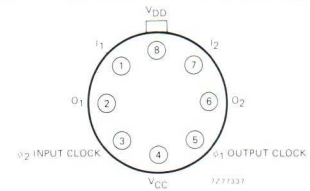


2533	1024	AMD AM2833PC, Fch 3533, General 2533, National MM5058, TI TMS3133NC

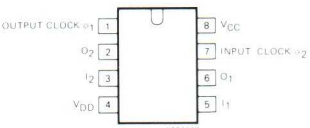
pin diagrams — second sources

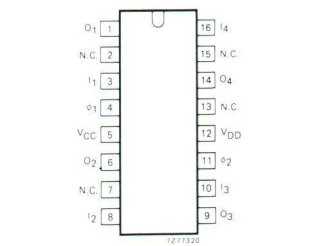
MOS

Dynamic shift registers

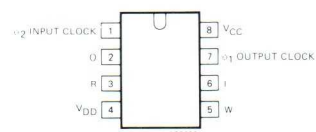


type	capacity	second source
2506	2 x 100	AMD AM1507T, National MM1506H
2507	2 x 100	–
2517	2 x 100	AMD AM1507, National MM1507H

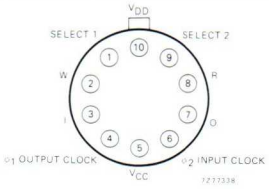


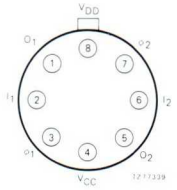


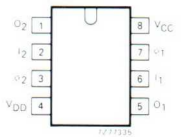
2502	4 x 256	AMD AM1402APC, Intel C1402A, National MM1402A

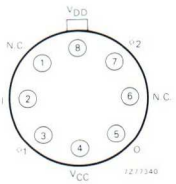


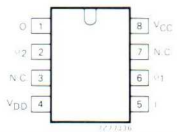
2524	512	AMD AM2807PC
2525	1024	AMD AM2808PC, Intersil IM7722C











type	capacity	second source
2505	512	AMD AM2505K, Intel M1405A
2512	1024	AMD AM2806HC, Intersil IM7712C
2503	2 x 512	AMD AM1403A, Intel C1403A, National MM1403A
2504	1024	AMD AM1404A, Intel M1404A, National MM1404A

microprocessors

type index

cross reference

Type index

Bipolar		MOS	
AMD	Signetics	National	Signetics
2901A	N2901-1	2650	2650
Intel	Signetics		
3001	N3001		
3002	N3002		

8X300 fixed instruction set bipolar microprocessor

The Signetics 8X300 is a monolithic, high-speed microprocessor implemented with bipolar Schottky technology. As the central processing unit, CPU, it allows 16-bit instructions to be fetched, decoded and executed in 250 ns. A 250 ns instruction cycle requires maximum memory access of 65 ns, and maximum I/O device access of 35 ns.

Instructions operate on an 8-bit byte. Input data can be rotated and masked before being subjected to an arithmetic or logic operation. Output data can be shifted and merged with the input data before being applied to external logic. This allows 1 to 8-bit I/O and data memory fields to be accessed and the resulting data to be processed in a single instruction cycle.

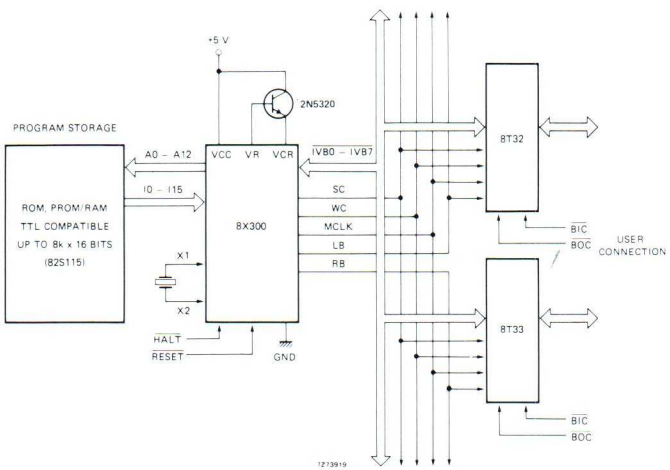
Features

- 185 ns instruction decode and execute delay (with Signetics 8T32/33 I/O port)
- Eight 8-bit working registers
- Single instruction access to 1-bit, 2-bit, 3-bit ... or 8-bit field on I/O bus
- Separate instruction address, instruction, and I/O data busses
- On-chip oscillator
- Bipolar Schottky technology
- TTL inputs and outputs
- Three-state output on I/O data bus
- +5 V operation from 0 to 70 °C

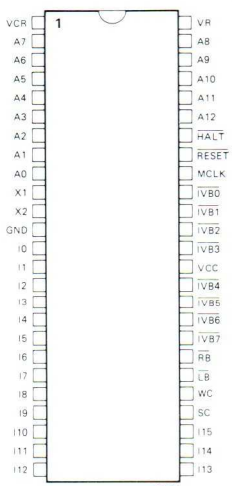
8X300 Instruction Set

- General purpose instruction set with substantial capabilities in arithmetic, byte and bit manipulation and I/O processing
- 16-bit instruction word
- 13 bits allow 8k program words
- Eight instruction classes: MOVE, ADD, AND, XOR, XEC, NZT, XMIT and JMP

Typical system configuration



Pin configuration – I package



8X300KT100SK designer's evaluation kit for fixed instruction bipolar microprocessor

The Signetics 8X300 Fixed Instruction Bipolar Microprocessor provides new levels of high performance to microprocessor applications not previously possible with MOS technology.

In the majority of cases, the choice of a bipolar microprocessor slice, as opposed to a MOS device, is based on speed. The 8X300 processor, combined with high-speed memory and I/O devices, is capable of executing all instructions in 250 ns.

The 8X300 is optimized for control and data movement applications. It has a 13-bit address bus for selecting instructions from program storage and a separate input bus for entering 16-bit instruction words. Data handling and I/O device addressing are accomplished via the 8-bit Interface Vector (IV) bus. The IV bus is supported by four additional control lines and a clock.

The unique features of the 8X300 IV bus and instruction set permit 8-bit parallel data to be rotated or masked before undergoing arithmetic or logic operations. Then, the data may be shifted and merged into any set of from 1 to 8 contiguous bits at the destination. The entire process of input, shifting, processing and output is done in 1 instruction cycle time. The 250 ns cycle time makes the 8X300 ideally suited for high-speed applications.

The evaluation board contains all the elements which a designer needs to judge the suitability of the 8X300 for his systems applications. Included with the 8X300 are 4 I/O ports for external device interface, 256 bytes of temporary (working) data storage, and 512 words of program storage all properly connected to the 8X300 to allow immediate exercising of the board. For this purpose, the PROMs are preprogrammed with the I/O control, RAM control, and RAM integrity diagnostic programs. With the remaining PROM space, the designer may enter his own benchmark, test, or development routines.

The board design allows complete flexibility in access to the address, instruction and IV busses as well as all controls and signals of the 8X300. The IV bus, I/O port user connection, clock signals control lines, address bus and instruction bus are wired to output pins, the board edge connector and flat cable connectors.

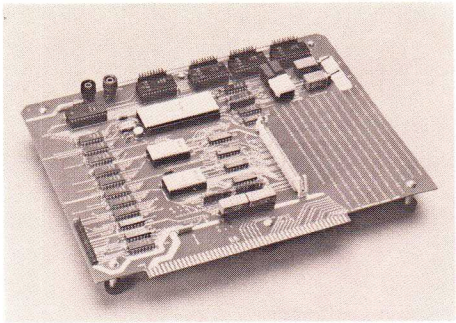
The board layout permits variations and/or expansions of the basic design. In addition to the access to all signals for transfer off the board, a wire wrap area is provided so that the designer may add to the board circuitry as he desires.

The addition may include memory, additional interfaces, or special circuits which meet specific user requirements.

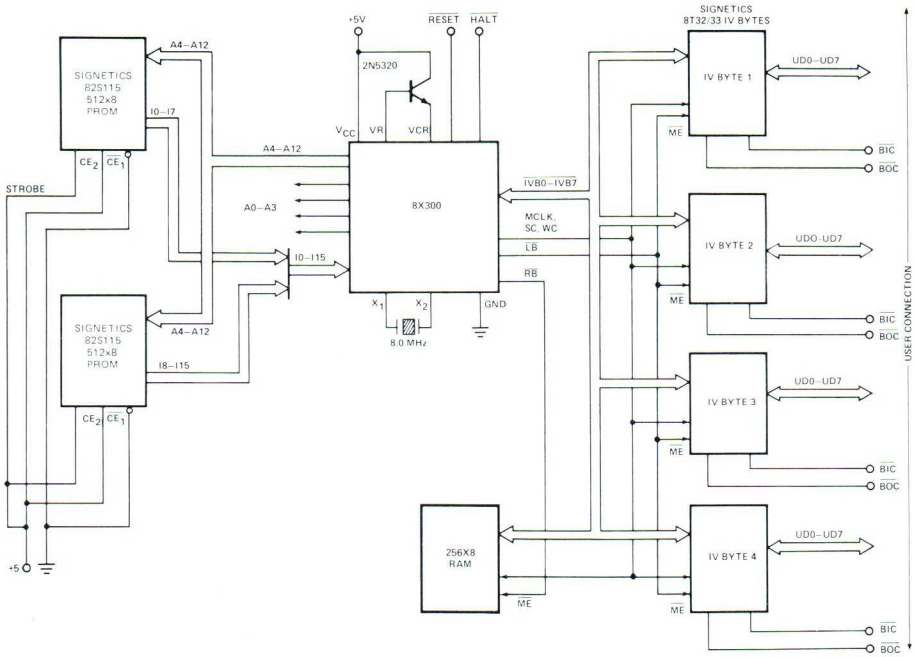
Controls are also provided for diagnostic and instructional purposes by allowing various operating modes. In the WAIT mode, the program may be single-stepped for ease of checkout. The one-shot instruction jamming allows control of the program start location, changes of program flow, changing or examining the internal registers, or testing of simple sequences. The repeated instruction jamming provides a means of repetitive execution of an instruction so that the I/O bus and the control lines may be examined without software changes. In both of these jam cases, the jammed instruction is selected by board-mounted switches.

Features

- 250 ns CPU with crystal
- 4 I/O ports (32 lines)
- 256 bytes data storage
- 512 words program storage
- run/wait control
- single step
- instruction jamming, one-shot instruction jam repeated jam
- all busses to output pins
- firmware diagnostics
- wire wrap area
- edge connector
- flat cable connectors
- wire wrap posts for bus lines



Assembled kit 8X300KT100SK



8X300 KIT CONFIGURATION

Contents

1 each 8X300
8 each 82S116 (256 x 1 RAM)
2 each 82S115 (512 x 8 PROM)
4 each 8T32 (addressable bidirectional I/O port)
1 each 8T31 (bidirectional I/O port)
2 each 8T26A (quad bus transceiver)
4 each 74157 (quad 2-input data selector)
2 each 7474 (dual D flip-flop)
2 each 7400 (quad NAND gate)
1 each 7427 (3-input NOR gate)
1 each p.c. board
miscellaneous parts
1 each introductory manual, assembly instructions, code listings and schematics

8X01 CRC generator/checker

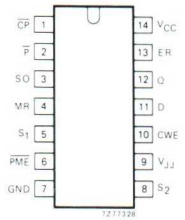
Objective specification

The CRC Generator/Checker circuit is used to provide an error detection capability for serial digital data handling system. The serial data stream is divided by a selected polynomial and the division remainder is transmitted at the end of the data stream as a Cyclic Redundancy Check Character (CRCC). When the data is received, the same calculation is performed. If the received message is error-free, the calculated remainder should satisfy a predetermined pattern. In most cases, the remainder is zero except in the case where Synchronous Data Link Control type protocols are used whereby the correct remainder is checked for 1111000010111000 ($X^0 - X^{15}$).

8 polynomials are provided and can be selected via a 3-bit control bus. Popular polynomials such as CRC-16 and CCITT are implemented. Polynomials can be programmed to start with either all zeros or all ones.

Automatic right justification for polynomials of degree less than 16 is provided.

Pin configuration – F, N packages



Features

- I^2L technology
- TTL inputs/outputs
- 5 MHz (max) data rate
- total power dissipation = 175 mW (max)
- V_{CC} = 5,0 V
- V_{JJ} = 1,0 V
- separate preset and reset controls
- SDLC specified pattern match
- automatic right justification

Typical applications

- floppy and other disc systems
- digital cassette and cartridge systems
- data communication systems

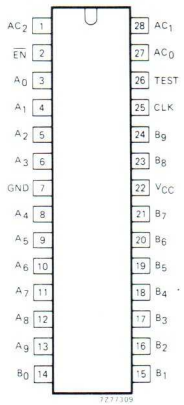
Objective specification

The Signetics 8X02 is a Low-Power Schottky LSI device intended for use in high performance microprogrammed systems to control the fetch sequence of microinstructions. When combined with standard ROM or PROM, the 8X02 forms a powerful microprogrammed control section for computers, controllers, or sequenced logic.

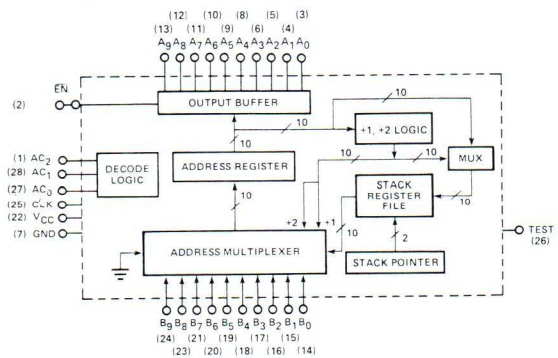
Features

- low-power Schottky process
- 50 ns cycle time (typ)
- 1024 microinstruction addressability
- N-way branch
- 4-level stack register file (LIFO type)
- automatic push/pop stack operation
- "test & skip" operation on test input line
- 3-bit command code
- three-state buffered outputs
- auto-reset to address 0 during power up
- conditional branching, pop stack and push stack
- positive edge trigger (low-to-high transition)

Pin configuration — N, I packages



Block diagram



8-bit latched addressable bidirectional I/O ports

8T32 Three-state, synchronous user port
8T33 Open collector, synchronous user port
8T35 Open collector, asynchronous user port
8T36 Three-state, asynchronous user port

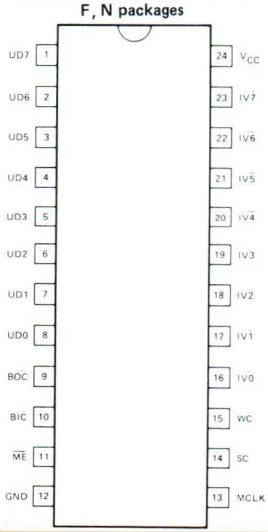
The interface vector (IV) byte is an 8-bit bidirectional data register designed to function as an I/O interface element in microprocessor systems. It contains 8 data latches accessible from either a microprocessor (IV) port or a user port. Separate I/O control is provided for each port. The 2 ports operate independently, except when both are attempting to input data into the IV byte. In this case, the user port has priority.

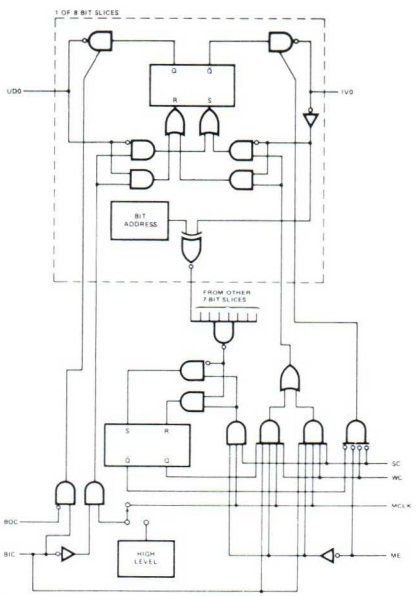
A unique feature of the 8T32/33/35/36 IV byte is the way in which it is addressed. Each IV byte has an 8-bit, field programmable address, which is used to enable the microprocessor port. When the SC control signal is HIGH, data at the microprocessor port is treated as an address. If the address matches the IV byte's internally programmed address, the microprocessor port is enabled, allowing data transfer through it.

Features

- A field-programmable address allows 1 of 512 IV bytes on a bus to be selected, without decoder
- Each byte has 2 ports, one to the user, the other to a microprocessor. IV bytes are completely bidirectional
- Ports are independent, with the user port having priority for data entry
- A selected IV byte de-selects itself when another IV byte address is sensed
- User data input available as synchronous (8T32, 8T33) or as asynchronous (8T35, 8T36) function
- The user data bus is available with three-state (8T32, 8T36) or open collector (8T33, 8T35) outputs
- At power up, the IV byte is not selected and the user port outputs are HIGH
- Three-state TTL outputs for high drive capability
- Directly compatible with the 8X300 interpreter
- Operates from a single 5 V power supply over a temperature range of 0 to 70 °C

F, N packages





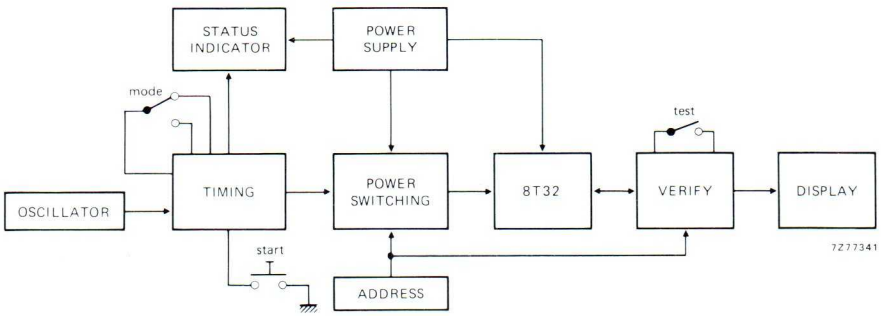
8T32KT1000SK programming kit for 8T32 addressable I/O port

This kit provides signals and levels required for programming the select addresses of the 8T32, 8T33, 8T35 and 8T36 I/O ports. Controls are provided for programming, testing and isolating the nichrome fuses which determine the device address.

Contents

1 x NE556A timer
2 x 74LS74 latch
1 x 74 LS93 counter
1 x 74LS154 decoder
4 x 8T26AB transceiver
2 x 74LS08 AND gate
1 x 8T80A NAND gate
1 x 74LS04 inverter
6 x 75450BA driver
2 x LM309DA regulator
printed circuit board and associated components

Block diagram



8T39 bus expander

The Bus Expander is specifically designed to increase the I/O capability of 8X300 systems previously limited by fan-out considerations. The bus expander serves as a buffer between the 8X300 and blocks of I/O devices. Each bus expander can buffer a block of 16 I/O ports while only adding a single load to the 8X300.

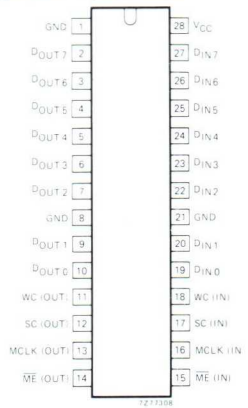
Features

- 15 ns propagation delay
- bidirectional
- three-state outputs on both ports
- pre programmed address range

Applications

The bus expander is not limited to use with the 8X300, but may be applied in any system which uses a combined address/data bus.

Pin configuration – I, N packages



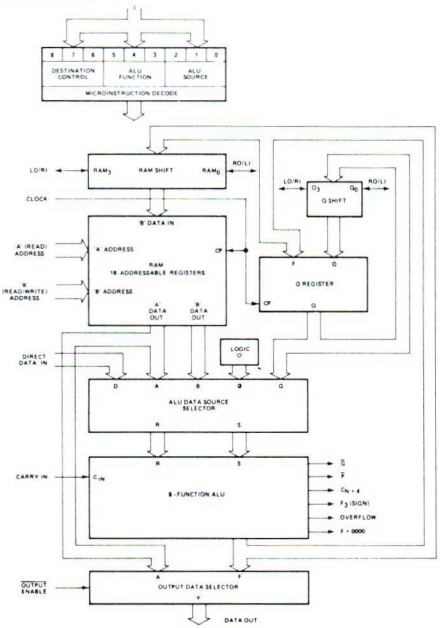
N2901-1 bipolar microprocessor processing element

Objective specification

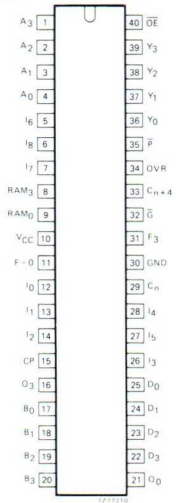
The 4-bit bipolar microprocessor slice is designed as a high-speed cascadable element intended for use in CPUs, peripheral controllers, programmable microprocessors and numerous other applications. The microinstruction flexibility of the 2901-1 will allow efficient emulation of almost any digital computing machine.

The device, as shown in the block diagram below, consists of a 16-word by 4-bit 2-port RAM, a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The 9-bit microinstruction word is organized into 3 groups of 3 bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable with full look-ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU. Advanced low-power Schottky processing is used to fabricate this 40-lead LSI chip.

Block diagram



Pin configuration – I, N packages



Features

- 80 ns cycle time
- 2-address architecture
  independent simultaneous access to 2 working registers saves machine cycles
- 8-function ALU
  performs addition, 2 subtraction operations, and 5 logic functions on 2 source operands
- flexible data source selection
  ALU data is selected from 5 source ports for a total of 203 source operand pairs for every ALU function
- left/right shift independent of ALU
  add and shift operations take only 1 cycle
- 4 status flags
  carry, overflow, zero, and negative
- expandable
  connect any number of 2901-1s together for longer word lengths
- microprogrammable
  3 groups of 3 bits each for source operand, ALU function, and destination control

Microprogram control unit N3001

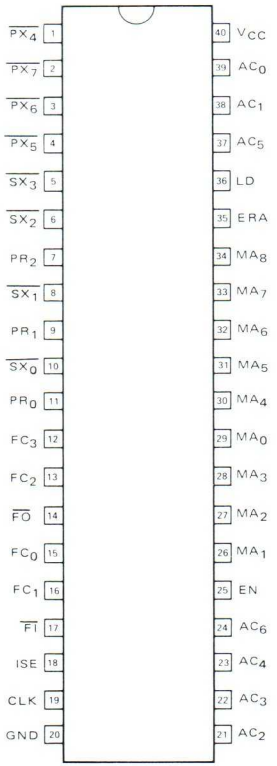
The N3001 MCU is one element of a bipolar microcomputer set. When used with the 3002, 74S182, ROM or PROM, a powerful microprogrammed computer can be implemented. The 3001 MCU controls the fetch sequence of microinstructions from the microprogram memory. Functions performed by the 3001 include:

- maintenance of microprogram address register
- selection of next microinstruction address
- decoding and testing of data supplied via several input busses
- saving and testing of carry output data from the central processing (CP) array
- control of carry/shift input data to the CP array
- control of microprogram interrupts

Features

- Schottky TTL process
- 45 ns cycle time (typ)
- direct addressing of standard bipolar PROM or ROM
- 512 microinstruction addressability
- advanced organization:
  9-bit microprogram address register and bus organized to address memory by row and column
  4-bit program latch
  2 flag registers
- 11 address control functions
- flight flag control functions:
  4 flag input functions
  4 flag output functions

Pin configuration – I, N packages



Central processing element N3002

3000KT1000 prototyping kit.

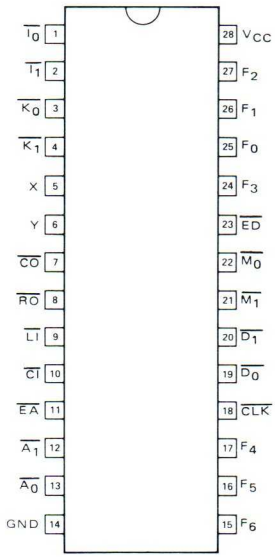
The N3002 central processing element (CPE) is one part of a bipolar microcomputer set. The N3002 is organized as a 2-bit slice and performs the logical and arithmetic functions required by microinstructions. A system with any number of bits in a data word can be implemented by using multiple N3002s, the N3001 microcomputer control unit, the N74S182 carry look-ahead unit and ROM or PROM.

Features

- 45 ns cycle time (typ)
- easy expansion to multiple of 2 bits
- 11 general purpose registers
- full function accumulator
- useful functions include:

  2's complement arithmetic
  logical AND, OR, NOT, EXCLUSIVE-NOR
  increment, decrement
  shift left/shift right
  bit testing and zero detection
  carry look-ahead generation
  masking via K-bus
  conditioned clocking allowing non-destructive testing of data in accumulator and scratchpad
- 3 input busses
- 2 output busses
- control bus

Pin configuration – I, N packages



3000KT1000 – 12 package prototyping kit

Central processing unit		
• microprogram control unit	N3001I	(1 x)
• central processing element	N3002I	(4 x)
• carry look-ahead	N74S182B	(1 x)
Microprogram memory		
• 256 x 8 PROM	N82S114I	(3 x)
Input/output		
• 8-bit bidirectional I/O port with latches	N8T31N	(1 x)
• 4-bit bus transceiver	N8T26AB	(2 x)

3000KT8080SK bipolar emulation kit for the 3000 series 8080A system emulator

The 8080 Emulation Kit is a microprogrammable microprocessor utilizing Schottky LSI components to implement an emulation of an Intel 8080A microcomputer system. The emulation is functionally equivalent to a microprocessor system incorporating the following Intel devices: 8080A, 8228, 8224 and 8212. The kit provides the standard address, data, status and control busses as defined in the Intel 8080 Microcomputer System Manual. Since the kit uses bipolar LSI elements, the emulator lacks the two-phase non-overlapping clock. Furthermore, those signals emanating from the 8080 during SYNC time are not provided, but rather the useful status signals provided by the 8228 system controller are implemented. The emulation also provides an extension of the 8228 operation during multi-byte interrupts. This is realized by allowing any 8080 program branch instruction to be inserted during interrupts rather than restricting multi-byte instructions to CALL during interrupts. Finally, a non-standard status signal, RTRAP, is provided which indicates that the present instruction is a reserved or undefined instruction. After this indication, the processor will enter the normal HALT routine and await an interrupt. (Intel 8080A operation during undefined instructions is undefined.) Thus all 12 of the unused instructions in the 8080 instruction set are reserved for future instruction set expansion. These unused codes may be used at any time to extend the usual instruction set without requiring any reprogramming of the bipolar PROMs used for microprogram memory. Finally, the emulator is fully static so that the clock may be adjusted from a typical cycle time of 150 ns to d.c.

The kit contains all the parts necessary to construct the emulator and includes preprogrammed PROMs. The kit is designed to be assembled by a skilled technician in about 8 hours.

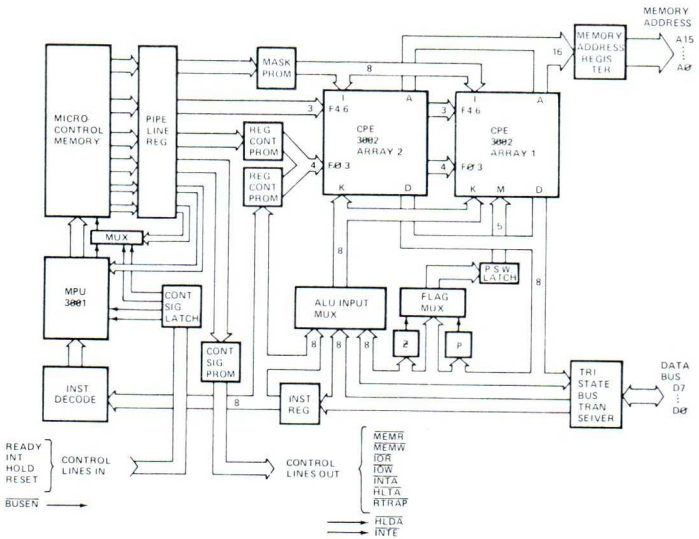
Features

- full emulation of 8080A system
- speed increase by factor of 2 to 9,2 over 8080A system
- static operation; microcycle time d.c. to 150 ns
- operation from single +5 V supply
- executes all 8080 instructions
- hardware multiply and divide
- microprogram expandable
- includes single-phase clock
- full vectored interrupt to any location within 64k memory

Kit contents

1 each	N74123
1 each	N3001
8 each	N3002
7 each	N82S115
1 each	N82S23
2 each	N82S123
2 each	N82S126
3 each	N8263
3 each	N74S182
1 each	N74S280
2 each	N7475
1 each	DM8613
11 each	N74S174
2 each	N8T28
3 each	N8T97
1 each	N74S153
2 each	N74S157
1 each	N7400
1 each	N74S02
3 each	N74S04
1 each	N74S08
1 each	N74S10
1 each	N74S133
2 each	resistor networks 1 kΩ, 16 pin
1 each	P.C. board
1 each	manual
1 each	schematic
1 each	set of microprogram listings
plus:	over 25 miscellaneous resistors, capacitors and other parts

Block diagram



8-bit MOS microprocessors 2650, 2650A

The 2650 processor is a general purpose, single chip, fixed instruction set, parallel 8-bit binary processor. It can perform any data manipulations through execution of a stored sequence of machine instructions. The processor has been designed to closely resemble conventional binary computers, but executes variable length instructions of one to three bytes in length. BCD arithmetic is made possible through use of a special "DAR" machine instruction.

The 2650 is manufactured using Signetics' n-channel silicon gate MOS technology. N-channel provides high carrier mobility for increased speed and also allows the use of a single 5 V power supply. Silicon gate provides for better density and speed. Standard 40-pin dual in-line packages are used for the processor.

The 2650 contains a total of seven general purpose registers, each eight bits long. They may be used as a source or destination for arithmetic operations, as index registers and for I/O transfers.

The processor can address up to 32 768 bytes of memory in four pages of 8 192 bytes each. Processor instructions are one, two or three bytes long, depending on the instruction. Variable length instructions tend to conserve memory space since a one or two-byte instruction may often be used rather then a three-byte instruction. The first byte of each instruction always specifies the operation to be performed and the addressing mode to be used. Most instructions use six of the first eight bits for this purpose, with the remaining two bits forming the register field. Some instructions use the full eight bits as an operation code.

The most complex direct instruction is three bytes long and takes 9,6 μs to execute assuming that the processor is running at its maximum clock rate and has an associated memory with cycle and access times of 620 ns or less. The minimum instruction execution time is 4,8 μs.

The clock input to the processor is a single phase pulse train and uses only one interface pin. It requires a normal TTL voltage swing, so no special clock driver is required.

The Data Bus and Address signals are three-state to provide convenience in system design. Memory and I/O interface signals are synchronous so that Direct Memory Access (DMA) and multiprocessor operations are easy to implement.

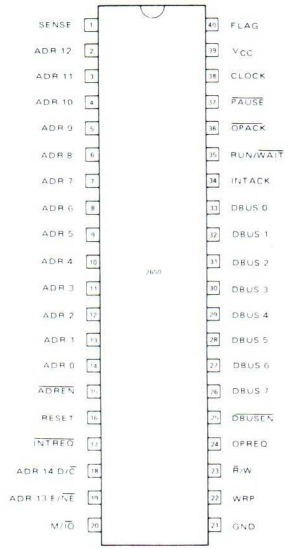
The interrupt mechanism is implemented as a single level, address vectoring type. Address vectoring means that an interrupting device can force the processor to execute code at a device-determined location in memory.

The 2650A is a functional equivalent of the 2650 with a new mask design which provides improved device-operating margins. Both versions are pin-for-pin compatible.

Features

- general purpose processor
- single chip
- fixed instruction set
- parallel 8-bit binary operations
- 40-pin dual in-line package
- n-channel silicon gate MOS technology
- TTL compatible inputs and outputs
- single power supply of +5 V
- seven general purpose registers
- return address stack, 8 deep, on chip
- 32k byte addressing range
- separate address and data lines
- variable length instructions of 1, 2 or 3 bytes
- 75 instructions
- machine cycle time of 2,4 μs at clock frequency of 1,25 MHz
- direct instructions take 2, 3, or 4 cycles
- single phase TTL level clock input
- static logic
- three-state output buses
- register, immediate, relative, absolute, indirect, and indexed addressing modes
- vector interrupt format

Pin configuration – I package



Addressing modes

The 2650 processor can develop addresses in eight ways:

- register addressing
- immediate addressing
- relative addressing
- relative, indirect addressing
- absolute addressing
- absolute, indirect addressing
- absolute, indexed addressing
- absolute, indirect, indexed addressing

Interface signal definition

ADR0-ADR12 – The low order 13 bits of address for memory access are on these pins. ADR0-ADR7 are also used in two-byte I/O instructions. These outputs are three-state buffers controlled by ADREN.

ADR13-E/$\overline{NE}$ – This multiplexed output signal delivers the ADR13 address bit when M/IO is in the M phase or discriminates between Extended and Non-Extended I/O instructions when M/IO is in the I/O phase.

ADR14-D/$\overline{C}$ – Address 14 or Data/Control is a multiplexed output signal. This pin delivers the ADR14 address bit when M/IO is in the M phase or discriminates between Data and Control I/O instructions when M/IO is in the I/O phase.

$\overline{ADREN}$ – Address Bus Enable is an input providing the external control for the ADR0-ADR12 three-state buffer drivers.

DBUS0-DBUS7 – This is the 8-bit, bidirectional three-state bus over which data is communicated into or out of the processor.

$\overline{DBUSEN}$ – Data Bus Enable is an input that controls the three-state buffer drivers for DBUS0 to DBUS7.

OPREQ – Operation Request is an output signal that informs external devices that the information on other output pins is valid.

$\overline{OPACK}$ – Operation Acknowledge is an input which is used by external devices to end an I/O or memory signalling sequence.

M/$\overline{IO}$ – Memory/Input-Output. This output informs external devices whether Memory or Input/Output functions are being performed.

$\overline{R}$/W – This output signal describes an I/O or memory operation as Read or Write, and defines whether the bidirectional DBUS is transmitting or receiving.

WRP – This Write Pulse is generated during write sequences and may be used to strobe memory or I/O devices.

SENSE – Is an input, independent of the other I/O signals, that provides a direct input to the processor.

FLAG – This pin provides a direct output signal that is completely independent of the other I/O signals.

$\overline{INTREQ}$ – Interrupt Request. This input is used by external devices to force the processor into the interrupt sequence.

INTACK – Interrupt Acknowledge is the signal used by the processor to inform external devices that it has entered an interrupt sequence.

$\overline{PAUSE}$ – Pause is used to temporarily stop the processor at the end of the current instruction. It may stop processing for an indefinite length of time and is available to use for DMA (Direct Memory Access).

RUN/$\overline{WAIT}$ – Informs external circuits as to the Run/Wait status of the 2650 processor.

RESET – Is an input that resets the program counter to zero and clears the interrupt inhibit bit.

CLOCK – This is the only clock input to the processor. It accepts standard TTL levels.

V_{CC} – +5 V power.

GND – The logic and power supply ground for the processor.

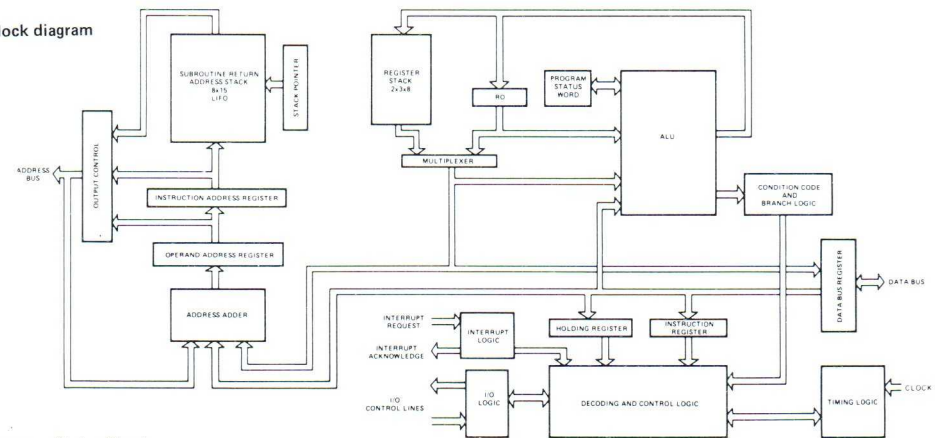
Processor hardware architecture

A block diagram of the processor is shown below. The first, second, and third bytes of instructions are read into the processor on the data bus and loaded into the Instruction Register, Holding Register, and Data Bus Register, respectively. The instructions are decoded through a combination of ROM and random logic.

The ALU performs arithmetic, Boolean, and combinatorial shifting functions. It operates on eight bits in parallel and utilizes carry-look-ahead logic. A second adder is used to increment the instruction address register and to calculate operand addresses for the indexed and relative addressing modes. This separate address adder allows complex addressing modes to be implemented with no increase in instruction execution time.

The General Purpose Register Stack and the Subroutine Return Address Stack are implemented with static RAM cells. The Register Stack consists of seven 8-bit registers. The Subroutine Stack can contain eight 15-bit addresses, thereby allowing eight levels of subroutine nesting. Placing the Subroutine Stack on the chip allows efficient ROM-only systems to be implemented in some applications. Separate 15-bit Instruction Address and Operand Address Registers are provided. The 2650 is an 8-bit binary processor with BCD capability.

Block diagram



Program Status Word

The Program Status Word (PSW) increases the flexibility and processing power of the 2650. The PSW is a special purpose register within the processor that contains status and control bits.

It is divided into two registers called the Program Status Upper (PSU) and Program Status Lower (PSL). The PSW bits may be tested, loaded, stored, preset, or cleared using the instructions which affect the PSW. The bits are utilized as follows:

PSU

7	6	5	4	3	2	1	0
S	F	II	Not Used	Not Used	SP2	SP1	SP0

S Sense
F Flag
II Interrupt Inhibit
SP2 Stack Pointer Two
SP1 Stack Pointer One
SP0 Stack Pointer Zero

PSL

7	6	5	4	3	2	1	0
CC1	CC0	IDC	RS	WC	OVF	COM	C

CC1 Condition Code One
CC0 Condition Code Zero
IDC Interdigit Carry
RS Register Bank Select
WC With/Without Carry
OVF Overflow
COM Logical/Arith. Compare
C Carry/Borrow

technical data – MOS

Instruction set

	mnemonic		op code	format*	description of operation	affects	cycles
Load/Store	LOD	Z	000 000	1Z	Load Register Zero	CC (Note 1)	2
		I	000 001	2I	Load Immediate	CC (Note 1)	2
		R	000 010	2R	Load Relative	CC (Note 1)	3
		A	000 011	3A	Load Absolute	CC (Note 1)	4
	STR	Z	110 000	1Z	Store Register Zero ($r \neq 0$)	CC (Note 1)	2
		R	110 010	2R	Store Relative	–	3
		A	110 011	3A	Store Absolute	–	4
Arithmetic	ADD	Z	100 000	1Z	Add to Register Zero w/wo Carry	C, CC (Note 1), IDC, OVF	2
		I	100 001	2I	Add Immediate w/wo Carry	C, CC (Note 1), IDC, OVF	2
		R	100 010	2R	Add Relative w/wo Carry	C, CC (Note 1), IDC, OVF	3
		A	100 011	3A	Add Absolute w/wo Carry	C, CC (Note 1), IDC, OVF	4
	SUB	Z	101 000	1Z	Subtract from Register Zero w/wo Borrow	C, CC (Note 1), IDC, OVF	2
		I	101 001	2I	Subtract Immediate w/wo Borrow	C, CC (Note 1), IDC, OVF	2
		R	101 010	2R	Subtract Relative w/wo Borrow	C, CC (Note 1), IDC, OVF	3
		A	101 011	3A	Subtract Absolute w/wo Borrow	C, CC (Note 1), IDC, OVF	4
	DAR		100 101	1Z	Decimal Adjust Register	CC (Note 2)	3
Logical	AND	Z	010 000	1Z	AND to Register Zero ($r \neq 0$)	CC (Note 1)	2
		I	010 001	2I	AND Immediate	CC (Note 1)	2
		R	010 010	2R	AND Relative	CC (Note 1)	3
		A	010 011	3A	AND Absolute	CC (Note1)	4
	IOR	Z	011 000	1Z	Inclusive OR to Register Zero	CC (Note 1)	2
		I	011 001	2I	Inclusive OR Immediate	CC (Note 1)	2
		R	011 010	2R	Inclusive OR Relative	CC (Note 1)	3
		A	011 011	3A	Inclusive OR Absolute	CC (Note 1)	4
	EOR	Z	001 000	1Z	Exclusive OR to Register Zero	CC (Note 1)	2
		I	001 001	2I	Exclusive OR Immediate	CC (Note 1)	2
		R	001 010	2R	Exclusive OR Relative	CC (Note 1)	3
		A	001 011	3A	Exclusive OR Absolute	CC (Note 1)	4
Compare	COM	Z	111 000	1Z	Compare to Register Zero Arithmetic/Logical	CC (Note 3)	2
		I	111 001	2I	Compare Immediate Arithmetic/Logical	CC (Note 4)	2
		R	111 010	2R	Compare Relative Arithmetic/Logical	CC (Note 4)	3
		A	111 011	3A	Compare Absolute Arithmetic/Logical	CC (Note 4)	4
Rotate	RRR		010 100	1Z	Rotate Register Right w/wo Carry	C, CC, IDC, OVF	2
	RRL		110 100	1Z	Rotate Register Left w/wo Carry	C, CC, IDC, OVF	2
Branch	BCT	R	000 110	2R	Branch On Condition True Relative	–	3
		A	000 111	3B	Branch On Condition True Absolute	–	3
	BCF	R	100 110	2R	Branch On Condition False Relative	–	3
		A	100 111	3B	Branch On Condition False Absolute	–	3
	BRN	R	010 110	2R	Branch On Register Non-Zero Relative	–	3
		A	010 111	3B	Branch On Register Non-Zero Absolute	–	3
	BIR	R	110 110	2R	Branch On Incrementing Register Relative	–	3
		A	110 111	3B	Branch On Incrementing Register Absolute	–	3

	mnemonic		op code	format*	description of operation	affects	cycles
Branch	BDR	R	111 110	2R	Branch On Decrementing Register Relative	–	3
		A	111 111	3B	Branch On Decrementing Register Absolute	–	3
	ZBRR		100 110 11	2ER	Zero Branch Relative, Unconditional	–	3
	BXA		100 111 11	3EB	Branch Indexed Absolute, Unconditional (Note 5)	–	3
Subroutine branch/return	BST	R	001 110	2R	Branch To Subroutine On Condition True, Relative	SP	3
		A	001 111	3B	Branch To Subroutine On Condition True, Absolute	SP	3
	BSF	R	101 110	2R	Branch To Subroutine On Condition False, Relative	SP	3
		A	101 111	3B	Branch To Subroutine On Condition False, Absolute	SP	3
	BSN	R	011 110	2R	Branch To Subroutine On Non-Zero Register, Relative	SP	3
		A	011 111	3B	Branch To Subroutine On Non-Zero Register, Absolute	SP	3
	ZBSR		101 110 11	2ER	Zero Branch To Subroutine Relative, Unconditional	SP	3
	BSXA		101 111 11	3EB	Branch To Subroutine, Indexed, Absolute Unconditional (Note 5)	SP	3
	RET	C	000 101	1Z	Return From Subroutine, Conditional	SP	3
		E	001 101	1Z	Return From Subroutine and Enable Interrupt, Conditional	SP, II	3
Input/Output	WRTD		111 100	1Z	Write Data	–	2
	REDD		011 100	1Z	Read Data	CC (Note 1)	2
	WRTC		101 100	1Z	Write Control	–	2
	REDC		001 100	1Z	Read Control	CC (Note 1)	2
	WRTE		110 101	2I	Write Extended	–	3
	REDE		010 101	2I	Read Extended	CC (Note 1)	3
Misc.	HALT		010 000 00	1E	Halt, Enter Wait State	–	2
	NOP		110 000 00	1E	No Operation	–	2
	TMI		111 101	2I	Test Under Mask Immediate	CC (Note 6)	3
Program status	LPS	U	100 100 10	1E	Load Program Status, Upper	F, II, SP	2
		L	100 100 11	1E	Load Program Status, Lower	CC, IDC, RS, WC, OVF, COM, C	2
	SPS	U	000 100 10	1E	Store Program Status, Upper	CC (Note 1)	2
		L	000 100 11	1E	Store Program Status, Lower	CC (Note 1)	2
	CPS	U	011 101 00	2EI	Clear Program Status, Upper, Masked	F, II, SP	3
		L	011 101 01	2EI	Clear Program Status, Lower, Masked	CC, IDC, RS, WC, OVF, COM, C	3
	PPS	U	011 101 10	2EI	Preset Program Status, Upper, Masked	F, II, SP	3
		L	011 101 11	2EI	Preset Program Status, Lower, Masked	CC, IDC, RS, WC, OVF, COM, C	3
	TPS	U	101 101 00	2EI	Test Program Status, Upper, Masked	CC (Note 6)	3
		L	101 101 01	2EI	Test Program Status, Lower, Masked	CC (Note 6)	3

* Format code: The number indicates the number of bytes. The letter(s) indicate the format type(s).

Notes:

1. Condition code (CC1, CC0): 01 if positive, 00 if zero, 10 if negative.
2. Condition code is set to a meaningless value.
3. Condition code (CC1, CC0): 01 if R0 > r, 00 if R0 = r, 10 if R0 < r.
4. Condition code (CC1, CC0): 01 if r > V, 00 if r = V, 10 if r < V.
5. Index register must be register 3 or 3'.
6. Condition code (CC1, CC0): 00 if all selected bits are 1s, 10 if not all selected bits are 1s.

Programmable Communications Interface (PCI) 2651

Applications

- intelligent terminals
- network processors
- front end processors
- remote data concentrators
- computer to computer links
- serial peripherals

The Signetics 2651 PCI is a universal synchronous/asynchronous data communications controller chip designed for microcomputer systems. It interfaces directly to the Signetics 2650 microprocessor and may be used in a polled or interrupt driven system environment. The 2651 accepts programmed instructions from the microprocessor and supports many serial data communication disciplines, synchronous and asynchronous, in the full or half-duplex mode.

The PCI serializes parallel data characters received from the microprocessor for transmission. Simultaneously, it can receive serial data and convert it into parallel data characters for input to the microcomputer.

The 2651 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode.

The PCI is constructed using Signetics' n-channel silicon gate depletion load technology and is packaged in a 28-pin DIP.

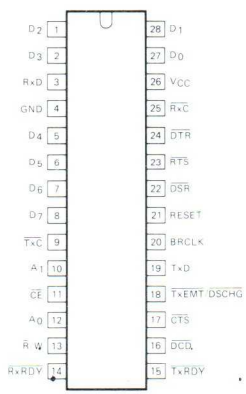
Features

- Synchronous operation
  5 to 8-bit characters
  single or double SYN operation
  internal character synchronization
  transparent or non-transparent mode
  automatic SYN or DLE-SYN insertion
  SYN or DLE stripping
  odd, even, or no parity
  local or remote maintenance loop back mode
  baud rate: d.c. to 0,8M baud (1x clock)
- Asynchronous operation
  5 to 8-bit characters
  1, 1½ or 2 stop bits
  odd, even, or no parity
  parity, overrun and framing error detection
  line break detection and generation
  false start bit detection
  automatic serial echo mode
  local or remote maintenance loop back mode
  baud rate: d.c. to 0,8M baud (1x clock)
  d.c. to 50k baud (16x clock)
  d.c. to 12,5k baud (64x clock)

Pin designation

pin no.	symbol	name and function	type
27, 28, 1, 2, 5-8	D_0-D_7	8-bit data bus	I/O
21	RESET	Reset	I
12, 10	A_0-A_1	Internal register select lines	I
13	$\overline{R}/W$	Read or write command	I
11	$\overline{CE}$	Chip enable input	I
22	$\overline{DSR}$	Data set ready	I
24	$\overline{DTR}$	Data terminal ready	O
23	$\overline{RTS}$	Request to send	O
17	$\overline{CTS}$	Clear to send	I
16	$\overline{DCD}$	Data carrier detected	I
18	$\overline{TxEMT}/\overline{DSCHG}$	Transmitter empty or data set change	O
9	$\overline{TxC}$	Transmitter clock	I/O
25	$\overline{RxC}$	Receiver clock	I/O
19	TxD	Transmitter data	O
3	RxD	Receiver data	I
15	$\overline{TxRDY}$	Transmitter ready	O
14	$\overline{RxRDY}$	Receiver ready	O
20	BRCLK	Baud rate generator clock	I
26	V_{CC}	+5 V supply	I
4	GND	Ground	I

Pin configuration – I package

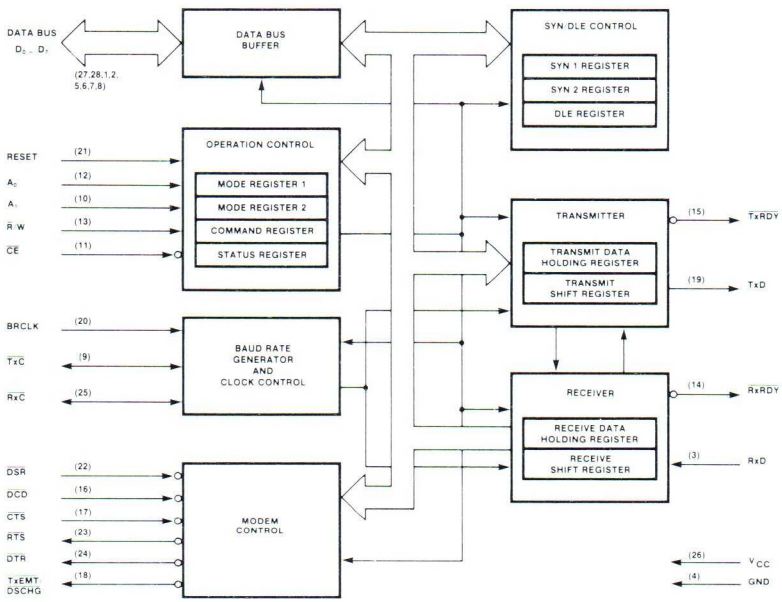


Block diagram

The PCI consists of six major sections. These are the transmitter, receiver, timing, operation control, modem control and SYN/DLE control. These sections communicate with each other via an internal data bus and an internal control bus. The internal data bus interfaces to the microprocessor data bus via a data bus buffer.

Other features

- internal or external baud rate clock
- 16 internal rates – 50 to 19 200 baud
- double buffered transmitter and receiver
- full or half-duplex operation
- fully compatible with 2650 CPU
- TTL compatible inputs and outputs
- single 5 V power supply
- no system clock required
- 28-pin dual in-line package



Programmable Communications Interface (continued)

Table 1 Baud rate generator characteristics — crystal frequency = 5,0688 MHz

baud rate	theoretical frequency 16x clock	actual frequency 16x clock	percentage error	duty cycle %	divisor
50	0,8 kHz	0,8 kHz	–	50/50	6336
75	1,2	1,2	–	50/50	4224
110	1,76	1,76	–	50/50	2880
134,5	2,152	2,1523	0,016	50/50	2355
150	2,4	2,4	–	50/50	2112
300	4,8	4,8	–	50/50	1056
600	9,6	9,6	–	50/50	528
1 200	19,2	19,2	–	50/50	264
1 800	28,8	28,8	–	50/50	176
2 000	32,0	32,081	0,253	50/50	158
2 400	38,4	38,4	–	50/50	132
3 600	57,6	57,6	–	50/50	88
4 800	76,8	76,8	–	50/50	66
7 200	115,2	115,2	–	50/50	44
9 600	153,6	153,6	–	48/52	33
19 200	307,2	316,8	3,125	50/50	16

Note
16x clock is used in asynchronous mode. In synchronous mode clock multiplier is 1x and duty cycle is 50% for any baud rate.

Table 2 CPU-related signals

pin name	pin no.	input/output	function
V_{CC}	26	I	+5 V supply input.
GND	4	I	Ground.
RESET	21	I	A high on this input performs a master reset on the 2651. This signal asynchronously terminates any device activity and clears the Mode, Command and Status registers. The device assumes the idle state and remains there until initialized with the appropriate control words.
A_1-A_0	10, 12	I	Address lines used to select internal PCI registers.
$\bar{R}/W$	13	I	Read command when low, write command when high.
$\overline{CE}$	11	I	Chip enable command. When low, indicates that control and data lines to the PCI are valid and that the operation specified by the $\bar{R}/W$, A_1 and A_0 inputs should be performed. When high, places the D_0-D_7 lines in the three-state condition.
D_7-D_0	8, 7, 6, 5 2, 1, 28, 27	I/O	8-bit, three-state data bus used to transfer commands, data and status between PCI and the CPU. D_0 is the least significant bit; D_7 the most significant bit.
$\overline{TxRDY}$	15	O	This output is the complement of Status Register bit SR0. When low, it indicates that the Transmit Data Holding Register (THR) is ready to accept a data character from the CPU. It goes high when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open drain output which can be used as an interrupt to the CPU.
$\overline{RxRDY}$	14	O	This output is the complement of Status Register bit SR1. When low, it indicates that the Receive Data Holding Register (RHR) has a character ready for input to the CPU. It goes high when the RHR is read by the CPU, and also when the receiver is disabled. It is an open drain output which can be used as an interrupt to the CPU.
$\overline{TxEMT}/\overline{DSCHG}$	18	O	This output is the complement of Status Register bit SR2. When low, it indicates that the transmitter has completed serialization of the last character loaded by the CPU, or that a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs has occurred. This output goes high when the Status Register is read by the CPU, if the TxEMT condition does not exist. Otherwise, the THR must be loaded by the CPU for this line to go high. It is an open drain output which can be used as an interrupt to the CPU.

Multi-Protocol Communications Controller (MPCC) 2652

The 2652 Multi-Protocol Communications Controller (MPCC) is a monolithic n-channel MOS LSI circuit that formats, transmits and receives synchronous serial data while supporting bit-oriented or byte control protocols. The chip is TTL compatible, operates from a single +5 V supply, and can interface to a processor with an 8 or 16-bit bidirectional data bus.

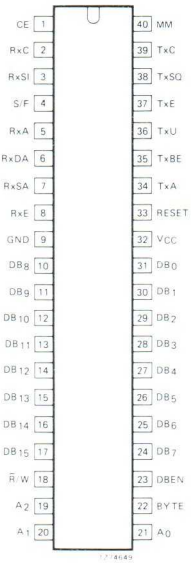
Features

- d.c. to 500k bps data rate
- protocol management
  bit-oriented protocols (BOP): SDLC, ADCCP, HDLC
  byte-control protocols (BCP): BI-SYNC, DDCMP
- programmable operation
  8 or 16-bit three-state data bus
  protocol selection – BOP or BCP
  error control –CRC or VRC or no error check
  character length – 1 to 8-bits for BOP or 5 to 8 bits for BCP
  SYNC or secondary station address comparison for BCP-BOP
  idle transmission of SYNC/FLAG or MARK for BCP-BOP
- automatic detection and generation of special BOP control sequences, i.e., FLAG, ABORT, GA
- zero insertion and deletion for BOP
- short character detection for last BOP data character
- SYNC generation, detection, and stripping for BCP
- maintenance mode for self-testing
- common parameter control registers
- independent status and data registers for receive and transmit
- status indicator signals can be used as CPU interrupts
- TTL compatible
- 40-pin package
- single +5 V supply

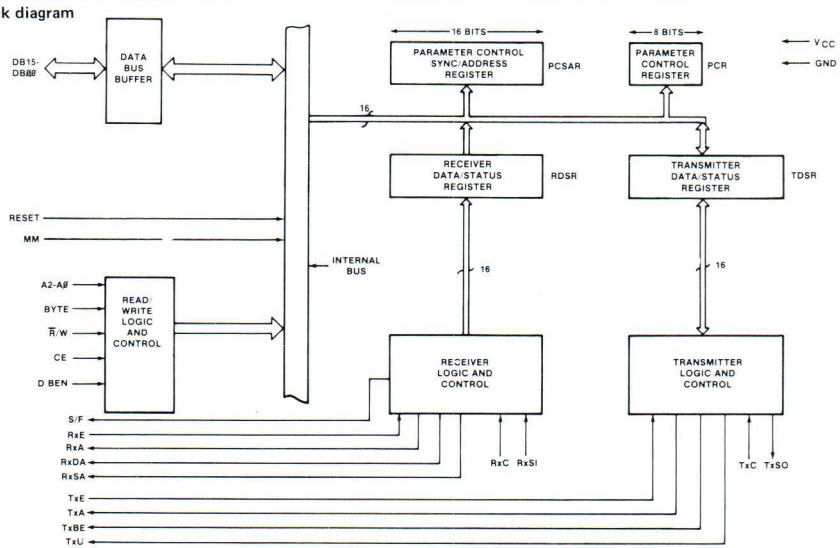
Applications

- intelligent terminals
- network processors
- front end communications
- remote data concentrators
- communication test equipment
- computer to computer links

Pin configuration – I package



MPCC block diagram



Pin designation

mnemonic	pin no.	type	name and function
DB15-DB00	17-10 24-31	I/O	**Data Bus.** DB07-DB00 contain bidirectional data while DB15-DB08 contain control and status information to or from the processor. Corresponding bits of the high and low order bytes can be WIRE OR'ed into an 8-bit data bus.
A2-A0	19-21	I	**Address Bus.** A2-A0 select internal registers. The four 16-bit registers can be addressed on a word or byte basis. See Register Address section.
BYTE	22	I	**Byte.** Single byte (8-bit) data bus transfers are specified when this input is high. A low level specifies 16-bit data bus transfers.
CE	1	I	**Chip Enable.** A high input permits a data bus operation when DBEN is activated.
R/W	18	I	**Read/Write.** $\overline{R}$/W controls the direction of data bus transfer. When high, the data is to be loaded into the addressed register. A low input causes the contents of the addressed register to be presented on the data bus.
DBEN	23	I	**Data Bus Enable.** After A2-A0, CE, BYTE and $\overline{R}$/W are set up, DBEN may be strobed. During a read, the three-state data bus (DB) is enabled with information for the processor. During a write, the stable data is loaded into the addressed register and TxBE will be reset if TDSR was addressed.
RESET	33	I	**Reset.** A high level initializes all internal registers and timing.
MM	40	I	**Maintenance Mode.** MM internally gates TxSO back to RxSI and TxC to RxC for off-line diagnostic purposes. The RxC input is disabled when MM is asserted.

Multi-Protocol Communications Controller (continued)

Pin designation

mnemonic	pin no.	type	name and function
RxE	8	I	**Receiver Enable.** A high level input permits the processing of RxSI data. A low level disables the receiver logic and initializes all receiver registers and timing.
RxA	5	O	**Receiver Active.** RxA is asserted when the first data character of a message is ready for the processor. In the BOP mode this character is the address. The received address must match the secondary station address if the MPCC is a secondary station. In BCP mode, if Strip-SYNC ($PCSAR_{13}$) is set, the first non-SYNC character is the first data character; if Strip-SYNC is zero, the character following the second SYNC is the first data character. In the BOP mode, the closing FLAG resets RxA. In the BCP mode, RxA is reset by a low level at RxE.
RxDA*	6	O	**Receiver Data Available.** RxDA is asserted when an assembled character is in $RDSR_L$ and is ready to be presented to the processor. This output is reset when $RDSR_L$ is read.
RxC	2	I	**Receiver Clock.** RxC (1x) provides timing for the receiver logic. The positive-going edge shifts serial data into the RxSR from RxSI.
S/F	4	O	**SYNC/FLAG.** S/F is asserted for one RxC clock time when a SYNC or FLAG character is detected.
RxSA*	7	O	**Receiver Status Available.** RxSA is asserted when there is a zero to one transition of any bit in $RDSR_H$ except for RSOM. It is cleared when $RDSR_H$ is read.
RxSI	3	I	**Receiver Serial Input.** RxSI is the received serial data. Mark = '1', space = '0'.
TxE	37	I	**Transmitter Enable.** A high level input enables the transmitter data path between $TDSR_L$ and TxS0. At the end of a message, a low level input causes TxS0 = 1 (mark) and TxA = 0 after the closing FLAG (BOP) or last character (BCP) is output onTxS0.
TxA	34	O	**Transmitter Active.** TxA is asserted when TxE is high and TSOM ($TDSR_8$) is set. This output will reset when TxE is low and the closing FLAG (BOP) or last character (BCP) has been output on TxS0.
TxBE*	35	O	**Transmitter Buffer Empty.** TxBE is asserted when the TDSR is ready to be loaded with new control information or data. The processor should respond by loading the TDSR which resets TxBE.
TxU*	36	O	**Transmitter Underrun.** TxU is asserted during a transmit sequence when the service of TxBE has been delayed for more than one character time. This indicates the processor is not keeping up with the transmitter (TxS0 depends on $PCSAR_{11}$). TxU is reset by RESET or setting of TSOM ($TDSR_8$).
TxC	39	I	**Transmitter Clock.** TxC (1x) provides timing for the transmitter logic. The positive-going edge shifts data out of the TxSR to TxS0.
TxSO	38	O	**Transmitter Serial Output.** TxS0 is the transmitted serial data.
V_{CC}	32	PS	+5 V power supply.
GND	9	GND	0 V reference ground.

* Indicates possible interrupt signal.

Programmable Peripheral Interface (PPI) 2655

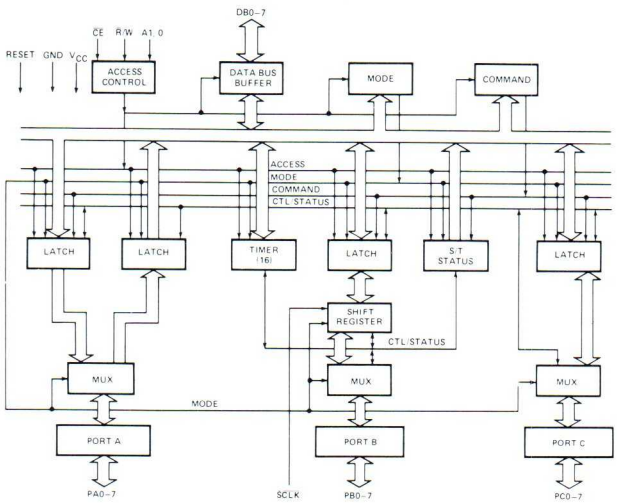
The 2655 PPI is designed for 2650 microcomputer systems. It consists of three ports (24 I/O pins), which can be individually programmed to function as input, output or bidirectional ports. Interface with the 2650 is via an eight-bit bidirectional data bus.

The PPI may be programmed for five major modes of operation: static I/O, strobed I/O, bidirectional I/O, serial I/O, or serial/timer I/O. In the serial/timer mode, parallel-to-serial or serial-to-parallel conversion of data operates simultaneously with the timer on one of the three ports.

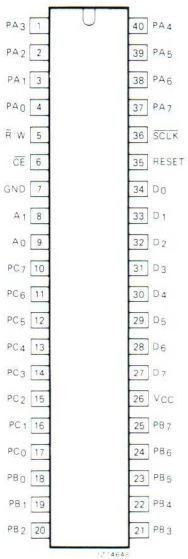
Features

- five selectable major operating modes:
  static I/O
  strobed I/O
  bidirectional I/O
  serial I/O
  serial/timer I/O
- three ports (A, B and C) with 24 programmable I/O pins
- completely TTL compatible
- 3 MHz programmable timer or event counter
- fully compatible with the 2650 microprocessor
- direct bit set/reset capability of each bit for all three ports
- ability to source 1 mA at 1,5 V
- 300 ns port read/write access time
- operates in a polled or interrupt driven system environment
- 40-pin dual in-line package
- single +5 V supply

Block diagram



Pin configuration — I package



Programmable Peripheral Interface (continued)

Operation

The following is a functional description of the five operating modes of the PPI. Each mode is selected via a mode control word. Interrupt generation and interrupt enable/disable functions are available with each mode except the static mode which operates entirely under program control.

Static mode

All three ports can operate in the static I/O mode. This mode allows each pin of each port to be either an input pin or an output pin. A logic '1' written to a pin of a selected port from the 2650 will condition that pin to be an input or output pin. Writing a logic '0' to the pin conditions that pin to be an output pin only. Outputs are latched while inputs are not. Each pin may be set or reset on an individual basis by a "set/reset" command.

Strobed I/O mode

In this mode, data may be transferred to or from a specified port in conjunction with strobe or "handshaking" signals. Ports A and B can operate in the strobed I/O mode and port C bits are used as control and status bits. In this mode both inputs and outputs are latched, and each port can be either an input or output.

Bidirectional I/O mode

This mode provides a means for communicating with a peripheral device over a single eight-bit bus with both transmitting and receiving capability. Port A operates in this mode with Port C pins providing "handshaking" signals for status and control. Both inputs and outputs are latched and port direction is determined by a control signal from the peripheral.

Serial I/O mode

This mode provides a means for communicating with a peripheral device on a bit serial basis through Port B. Parallel data from the CPU will be shifted out to the peripheral over the least significant bit of Port B (PB0). Eight clocks will be required for a complete character transfer. The eight-bit character will be repeatedly shifted out until the CPU presents another character to Port B.

For the serial in mode, data is input from the peripheral at the most significant bit of Port B (PB7). Eight clocks will be required to assemble the eight-bit character. An interrupt request will signal the CPU for character transfer.

Timer mode

This mode enables the PPI to perform time interval measurements, pulse width measurements, and event counting. This timing function is performed during the serial/timer mode, and is restricted to Port B only. The mode is initiated by selecting the desired operation and loading a 16-bit down counter with an initial value. The counter does not start counting until the upper eight bits have been loaded. An interrupt can be generated to signal the CPU when the timer reaches a zero count.

Pin definitions

pin no.	pin name	type	function
27-34	D7-D0	I/O	Eight-bit three-state bidirectional data bus. All data and command transfers are made using this bus. D0 is the least-significant bit; D7 is the most-significant bit.
35	Reset	I	Resets all internal storage elements, including the data latches and command registers. Resets ports A, B and C to accept input data, and operating mode to static mode. A functionally equivalent on-chip power-on reset is also provided.
8, 9	A1, A0	I	Address lines used to select internal PPI modes or registers. Indicates control or data words to be placed on the data bus. Used in conjunction with the $\overline{R}$/W line.
5	$\overline{R}$/W	I	When low, gates the selected register to the data bus. When high, gates the contents of the data bus into the selected register.
6	$\overline{CE}$	I	When low, identifies that control and data lines to the PPI are valid.
36	$\overline{SCLK}$	I	Provides a serial clock for the parallel-to-serial or serial-to-parallel conversion.
37-40 1-4	PA7-PA0	I/O	An eight-bit three-state quasi-bidirectional port.* PA0 is the least-significant bit; PA7 is the most-significant bit.
25-18	PB7-PB0	I/O	An eight-bit quasi-bidirectional port.* PB0 is the least-significant bit; PB7 is the most-significant bit. Port B also has parallel-to-serial or serial-to-parallel conversion capability with PB0, 7 being either the serial output or input respectively. Data is double buffered. Port B can also operate as a 16-bit binary timer, as an event counter, or as a pulse width indicator. An output is generated whenever the counter is decremented to the all-zero state.
10-17	PC7-PC0	I/O	A eight-bit quasi-bidirectional port.* PC0 is the least-significant bit; PC7 is the most-significant bit. Port C bits are also used as control and status signals in conjunction with ports A and B. When the pin bit is used as a strobe input, the line receives an external strobe input which clocks information from port A or port B into the port A or port B data latches. When the pin is used as a status line, the line indicates port A or port B status condition which may be used as an interrupt input to the 2650.
26	V_{CC}	I	+5 V supply.
7	GND	I	Ground.

* A quasi-bidirectional port allows each bit to be designated as input or output under program control. If any bit of the port is set to a '1', that bit becomes an input or output depending on the usage of the port pin. If the peripheral is driving the port bit (i.e. overriding the logic '1' condition produced by the internal port pull-up resistor), then the bit is an input. If the peripheral is receiving from the port bit, then a '0' or '1' written to the port will be transmitted to the peripheral.

System Memory Interface (SMI)
2656

The 2656 System Memory Interface (SMI) is a mask programmable circuit with on-chip memory, I/O, and timing (clock) functions. It is usable either in 2-chip or multi-chip microcomputer systems. Used with the 2650 microprocessor, it provides a 2-chip microcomputer. This 2-chip microcomputer offers the user 2kx8 bits of ROM, 128x8 bits of RAM, and an 8-bit multi-function I/O port.

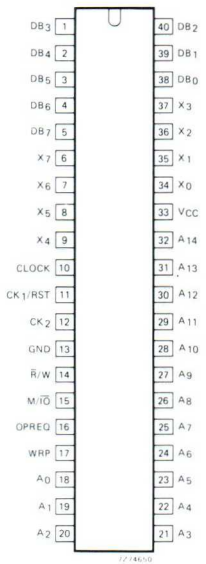
Used as a system interface in a multi-chip microcomputer, with large memory and/or additional peripheral requirements, the programmable versatility of the SMI provides decoded chip enable outputs. These outputs connect directly to other memory or I/O functional blocks with few, if any, requirements for additional interfacing chips. This reduces both chip count and cost in complex microcomputer systems.

The 2656 is processed using Signetics' n-channel silicon gate technology. Only a single power supply of +5 V is needed.

Features

- 2kx8 mask programmable ROM
- 128x8 static RAM
- 8 multi-purpose pins for either chip enables or I/O bits
- 8-bit latch for either I/O or MPU storage
- internal clock generator with crystal, RC, or external timing source
- system power-on reset
- 40-pin dual in-line package
- single +5 V supply
- 2-chip microcomputer
- system control for multi-chip microcomputers – eliminates or reduces TTL support circuitry for memory and I/O device selection
- from small (2k-2 chip) to 32k microprocessor-based systems.

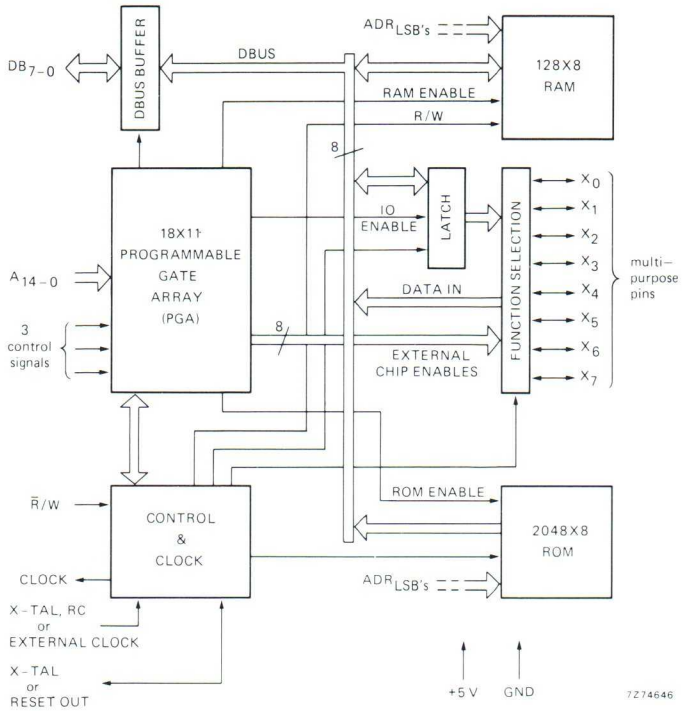
Pin configuration – I package



Pin definitions

pin no.	pin name	function
38-40, 1-5	DB_0-DB_7	8-bit bidirectional data bus. All data transfers between the MPU and ROM, RAM, Latch and X pins are made using this bus.
15-32	PGA inputs	18 PGA inputs that are used to determine SMI operation during the current MPU cycle. These inputs should include:
18-32	A_0-A_{14}	• MPU address bus. Address bus inputs occupy contiguous bit positions with A_0 as the least-significant address bit.
16	OPREQ	• A control signal that specifies the valid state of address and control bus.
15, 17	M/$\overline{IO}$, WRP	• Optional signals. Possibilities include Memory or I/O (M/$\overline{IO}$), Write Pulse (WRP), external control signals, or additional high order address bits.
14	$\overline{R}$/W	A control signal from the MPU that indicates whether the requested operation is to be a Read or Write (0 or 1 respectively). This signal must not change while OPREQ is true.
10	CLOCK	Output clock to the MPU. The frequency is determined by the timing element and the mask programmable divisor (divided by 1, 2, 3, 4).
11, 12	CK_1/RST, CK_2	Connections for the timing element. Only CK_2 is necessary for an RC or external timing source. The CK_1/RST pin then becomes a power-on RESET output. Two pins are necessary for direct connection of a crystal.
33, 13	V_{CC}, GND	Power supply connection and ground.
34-37, 9-6	X_0-X_7	Multi-purpose I/O pins. These pins can be mask programmed as external memory or I/O Chip Enables, or bidirectional I/O Port data bits, or any combination of the two.

System Memory Interface (continued)



Functional block descriptions

Data Bus Buffer

A three-state bidirectional 8-bit bus transceiver for data transfer between the SMI and MPU.

Programmable Gate Array (PGA)

Provides select signal outputs for the internal ROM, RAM, Latch, and up to 8 multi-purpose I/O pins that are mask-programmed as Chip Enables. A PGA output is active when the input variables match any one of 11 corresponding mask-programmed product terms. The 18 input variables are normally address and control bus signals from the MPU and may be programmed as '1', '0', and 'don't care'. Each product term is a specified combination of the input variables.

Control and Clock

Generates the CLOCK output signal to the MPU and control signals for the ROM, RAM, and LATCH. A mask programmable frequency divider provides input frequency division by 1, 2, 3 or 4. The timing source is mask programmable and may be a crystal, RC, or external oscillator. If either of the latter two are designated as a timing source, the second timing pin becomes a RESET output to the MPU.

ROM

2 048 bytes of mask-programmable Read Only Memory for storage of instructions and constants. The ROM base address is PGA mask programmable over the entire MPU address range. The ROM can be disabled by a mask option.

RAM

128 bytes of Read/Write Memory for MPU data storage and retrieval. The RAM base address is PGA mask programmable over the entire MPU address range. RAM dominates over ROM if address overlap is intentionally mask programmed. The RAM can be disabled by a mask option.

Function Select (FS)

A 1 x 8 Function Select array of mask-programmable contacts determine the function of each of the multi-purpose I/O pins (X_0-X_7). Two modes exist:

1. CE – The X pin is an active low Chip Enable ($\overline{CE}$) for either external memory or an I/O port. PGA inputs receive the external address and MPU control signals required to generate the $\overline{CE}$ output.
2. P – The X pin is a bidirectional I/O Port Data bit. A portion of the PGA provides the control signal to select the Port.

Latch

Holds output data for the multi-purpose I/O pins mask programmed as a mode P. The latch continues to function as a read/write element even if all multi-purpose I/O pins are programmed as chip enables. Thus, any X pin that is programmed as an external chip enable can have corresponding latch bits available for temporary data storage or software flags. To read an input pin, the corresponding latch bit must first be written to a '1' by the MPU program. This is done to disable all active outputs, changing them to passive pull-up outputs. This permits inputs to be sensed on the same pin. Subsequent reads of the same pin do not have to be preceded by a write if the state of the latch pin remains a '1'.

2650PC4000 Emulator board for 2656

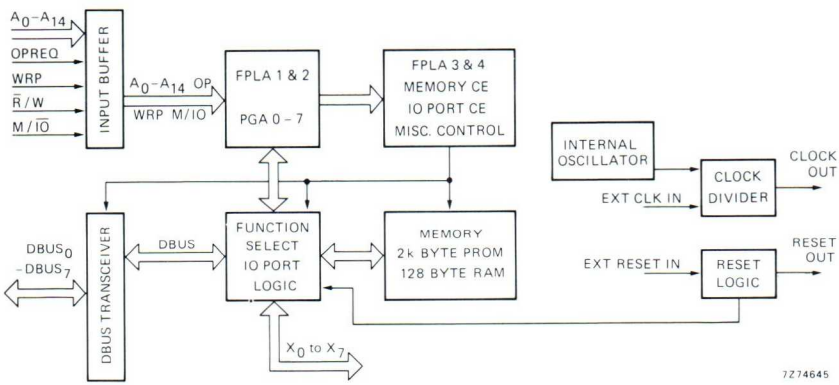
The PC4000 is a circuit emulation of the 2656, a 40-pin NMOS-LSI system memory interface chip. The PC4000, in circuit board form, offers the engineer a system design aid. By designing with the PC-board emulator, specific ROM and PGA (programmable gate array) patterns can be determined for the user's application.

In utilizing the PC4000, the engineer-designer is able to implement the same functions as the 2656. Through a cable and 40-pin plug with a pin configuration identical to the 2656, the user connects the PC4000 directly into his prototype system. He can access the 128x8 RAM, the preprogrammed ROM, and the gate array. The user can simulate the eight multi-function ports either as I/O ports or chip enables, the power-on reset, and the clock generator and divider.

The PC4000 emulator contains the same circuits that are available to the user on the 2656 Systems Memory Interface chip. Functionally the PC4000 replaces the 2656 in the user's prototyping system through a pin-for-pin compatible plug and its 40-wire ribbon cable attached to the PC4000. Identical circuit functionality of the 2656 chip is provided to the user by the functions of the PC Board.

In emulating the 2656, the speed of the board circuitry is equivalent to or faster than the on-chip circuitry. ROM is implemented with bipolar PROMs and on-chip RAM is implemented with the bipolar RAM packages. The programmable gate array (PGA) for the selection of the ROM and RAM enables and the I/O function selects are implemented with field programmable logic arrays (FPLAs).

The oscillator provided on the PC4000 has the same frequency dividers available as on the 2656. The oscillator divide ratio is implemented by the toggle switch settings.



Functional block descriptions

Input Buffer

This circuitry buffers the incoming signals from the MPU (specifically for the 2650 MPU, the addresses, A0-A14, and the 4 control signals, OPREQ, WRP, $\overline{R}$/W and M/$\overline{IO}$).

Data Bus Transceiver

This circuitry buffers the incoming 8-bit data bus from the MPU, and provides output drivers to the data bus.

FPLAs 1 and 2

FPLAs 1 and 2 represent a portion of the programmable gate array of the 2656 SMI chip. These 2 FPLAs decode the chip enable signals.

FPLAs 3 and 4

These FPLAs represent the remainder of the gate array. FPLA 3 and a portion of FPLA 4 generate the on-board ROM, RAM and port enable signals. The remainder of FPLA 4 is used to generate the data bus control signals.

Function Select and I/O Port Logic (via FPLAs 1-4)

The function select and I/O port logic allow the multi-purpose pins of the 2656 to be individually selected as either an I/O port or a chip enable via eight switches, FS0-FS7. When assigned as chip enables, they must be programmed in FPLAs 1 and 2. When a multi-purpose pin is assigned as I/O or as an input port, the port address is programmed in FPLAs 1 and 2. When the FS switch is ON, the corresponding pin of the 2656 is selected as an I/O port. When the FS switch is OFF, the corresponding pin is selected as a chip enable.

Memory

Both ROM and RAM memory functions are implemented in bipolar PROM and RAM respectively. The memory chip enables are programmed in FPLAs 3 and 4. (See the PROGRAMMING section.)

Clock Divider, Reset Logic, and Internal Oscillator

This circuitry provides an internal oscillator with switches for frequency divide by 1, 2, 3 or 4. Reset logic is provided on the PC4000 to allow the user to reset the system during debug via an external switch closure, without the need for powering down. The reset logic is used when the RC or external oscillator modes are selected.

If the RC or crystal internal oscillator mode is desired, the frequency determining components must be installed on the emulator PCB. The pins on the header that correspond to the RC and Crystal pins are not used in this mode, and only the external Reset function is provided.

Part list

part number	quantity	description
7403	2	Open Collector Quad Nand
7404	3	Hex Inverter
7405	2	Open Collector Hex Inverter
74LS14	1	Hex Schmitt Trigger Inverter
7432	1	Quad 2-Input OR gate
74LS86	1	Quad 2-Input XOR
74109	1	Dual JK Flip-Flop
74116	1	Dual Quad D Latch with Clear
74126	4	Quad Three-state Buffer
74163	1	4-bit Binary Counter
8T28B	2	Bidirectional Data Bus Driver Receiver
8T97B	5	Three-state Hex Buffer
8T98B	2	Three-state Hex Inverter Buffer
82S101	4	Open Collector FPLA
82S115	4	512x8 PROM
82S09	2	64x9 BIPOLAR RAM
NE555	1	Timer
761-1-51,0 kΩ	4	Resistor Dip Pak
	1	10 kΩ Resistor
	1	100 kΩ Resistor
	1	220 Ω Resistor
		Note: All Resistors ¼ watt
	1	150 pF Capacitor
	2	0,01 μF Capacitor
	5	4,7 μF Capacitor
	14	0,1 μF Capacitor
	1	Edge Connector AMP 225-21021-401-117
	2	8-Position Dip Switch
	1	PC Board 2650/PC4000
	4	24-pin Dip Socket
	4	28-pin Dip Socket
	1	40-pin Dip Socket
	1	Cable Assembly

Required but not supplied:
Timing element for oscillator.

Emulator board for 2656 (continued)

40-core cable pin configuration

The interface from the PC4000 to the user's system is a 40-core cable with 40-pin DIP plugs at both ends.

function	pin no.	pin no.	function
DBUS3	1	40	DBUS2
DBUS4	2	39	DBUS1
DBUS5	3	38	DBUS0
DBUS6	4	37	X3
DBUS7	5	36	X2
X7	6	35	X1
X6	7	34	X0
X5	8	33	NC*
X4	9	32	ADDR14
CLK OUT	10	31	ADDR13
CLK 1	11	30	ADDR12
CLK2	12	29	ADDR11
VSS GND	13	28	ADDR10
R/W	14	27	ADDR9
M/I/O	15	26	ADDR8
OPREQ	16	25	ADDR7
WRP	17	24	ADDR6
ADDR0	18	23	ADDR5
ADDR1	19	22	ADDR4
ADDR2	20	21	ADDR3

* VDD for chip, no connection for board.

Note: Timing Element pins have alternative functions determined by connections W on the printed circuit board.
CLK 1 is external reset out. To use, connect W (4) to W (5).
CLK 2 is external clock in. To use, connect W (2) to W (3).
CLK 2 not used: To use internal RC oscillator connect W (1) to W (2).
To use internal XTAL oscillator connect W (2) to W (8).

Edge connector

The edge connector for the 2650PC4000 is an AMP 225-21021-4-01-117 edge connector. This edge connector has 20 pins on 0,156 inch centres with the following pin configuration:

GND	1	A	GND
GND	2	B	GND
	3	C	C2X
	4	D	
	5	E	RESET OUT**
	6	F	CLK OUT**
	7	H	RESET IN**
CK	8	J	OSC**
VCC	9	K	VCC
VCC	10	L	VCC

** Factory test only – do not use.

Microprocessor prototyping card 2650PC1001

The 2650PC1001 is a complete microcomputer on a single printed circuit board. The heart of this computer is Signetics' 2650 Microprocessor; a single chip, n-channel MOS Integrated Circuit which contains the CPU and control sections of the classical general purpose computer architecture.

In addition to the Microprocessor, the 2650PC1001 contains both control and read/write memory, I/O ports, clock, and all the necessary buffering and interface circuits to permit data transfer both on and off the p.c.b.

Features

- 2650 Microprocessor
- 1k bytes of ROM with PIPBUG*
- 1k bytes of RAM (off-board expandable)
- 1 MHz crystal oscillator
- serial I/O (either TTY 20 mA current loop or RS232 – selectable by jumper wire)
- 2 eight-bit output ports
- 2 eight-bit input ports
- DMA capability
- LED display indicators
- data bus and address bus test points
- buffered data and address outputs
- single power supply (+5 V)**

* Signetics' Loader and Debugging Program. (See appl. note SS50)

** Assumes RS232 I/O port is not used.

Memory

The memory of the 2650PC1001 is divided into two segments:

a. ROM with PIPBUG

b. RAM (Read/Write Memory)

The Read-Only Memory supplied with the card is the 82S129 Field Programmable type (PROM). Eight of these 256x4 devices are arranged to provide a 1kx8 memory array. The 2650PC1001 is supplied with the PIPBUG loader and debugger already programmed into the ROM. Since the devices are loaded into sockets, however, they can be easily replaced with other ROMs or PROMs programmed by the user.

The 1kx8 array is constructed with 2606 NMOS RAM devices. Since the 2606 is a 256x4 device, again 8 devices are used in the array.

Serial I/O

The serial I/O capability of the 2650PC1001 utilizes a unique serial I/O feature of the basic 2650 microprocessor. This feature allows serial data to be transferred directly into the 2650 under program control by using the sense and flag pins on the microprocessor.

Two types of serial I/O ports are available. The first is a teletype interface which can be directly connected to a teletype 20 mA current loop. The second is an RS232 interface which provides a connection for voltage-driven peripheral equipment. The selection of the particular interface to be used is made by connecting a jumper wire directly from the microprocessor flag and sense lines to the appropriate output port. If the RS232 interface is used, +12 and −12 V supplies are required in addition to the +5 V supply which operates the rest of the board.

Parallel I/O

Parallel I/O channels using the 2650's unique Non-Extended I/O mode are also provided. This mode allows a single byte instruction to select one of two distinct I/O devices. On the 2650PC1001, these two devices are represented by four separate data channels; two for reading and two for writing. The output (or write) channels are fully latched and buffered. The input (or read) channels are fully buffered. One read and one write channel represent a single I/O device. In addition to the Non-Extended I/O ports, the data and address buses, plus the appropriate control signals, are also available to provide the full extended I/O capability.

Microprocessor prototyping card (continued)

Other I/O

A complete listing of the I/O pins, plus a brief description of any I/O signal not detailed above, is as follows:

1,2	Ground
4-11	Processor Data Bus*
12	Strobe to Enable Input Data Port
13	D/C Output*
14	DMA Control Input
15	Extended/Non-Extended Output*
16	Interrupt Acknowledge Output*
17	R/W Output*
18	Write Pulse Output*
19	Run/Wait Output*
20	Operation Request Output*
21	Memory/IO Output*
22	Operation Acknowledge Input*
23	Clock Output (or Input if on-board clock not used)
24	Operation Request Input for DMA
25	Reset Input*
26	Interrupt Request Input*
27	Pause Input*
28-32	Unused
33-47	Address Bus*
48	+12 V for RS232
49	−12 V for RS232
50	+5 V
A, B	Ground
C	Not used
D-M	Non Extended Output Port "D"
N	Clock to load data into Output Port "D"
P	TTY serial data input (+)
R	TTY serial data input (−)
S	TTY serial data Output pull-up resistor (current loop +)
T	TTY serial data Output; TTL Level, open collector (current loop return)
U	RS232 ground
V	RS232 Output
W	TTY tape reader Output; TTL Level, open collector (+)
X	TTY tape reader Output pull-up resistor (−)
Y	RS232 Input
Z	Clock to load data into Output Port "C"
a-h	Non-Extended Output Port "C"
j	Strobe to enable Input Port Control
k-u	Non-Extended Input Port "D"
v-c	Non-Extended Input Port "C"
d	+12 V for RS232
e	−12 V for RS232
f	+5 V

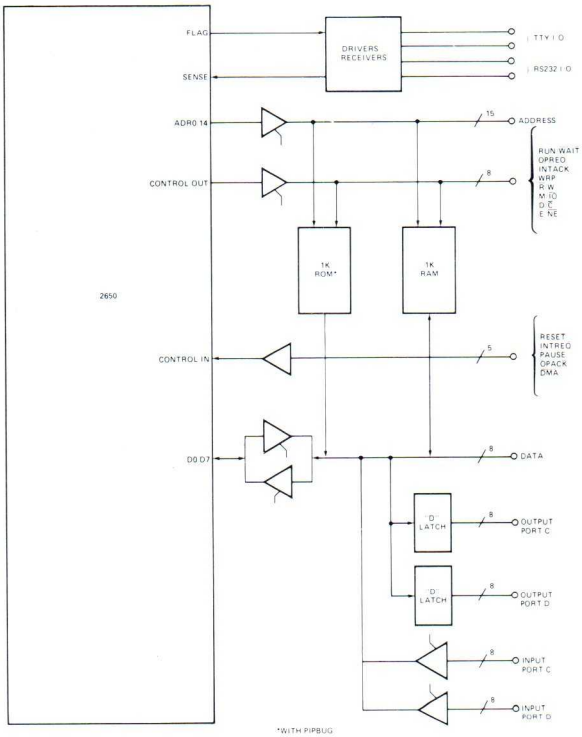
Summary

The above is intended to provide a brief description of Signetics' 2650PC1001 Prototyping Board. More detailed information can be obtained from the following:

SS50	PIPBUG Application Note
SP50	2650PC1001 Manual (Detailed Description)
AS50	Serial I/O using Sense and Flag Application Note
2650BM 1000	Basic 2650 Microprocessor Manual

* Buffered 2650 microprocessor outputs.

PC1001 Block diagram



Adaptable Board Computer (ABC) prototyping system
2650PC1500
2650KT9500

The Adaptable Board Computer, ABC 1500, is a modular microcomputer containing a CPU, memory, I/O ports and support circuitry. It is designed to cover a broad range of applications from software development to system hardware prototyping. Cost performance trade-offs have been carefully considered to achieve maximum flexibility and allow the card to be tailored to a variety of individual requirements.

The basic configuration consists of the 2650 8-bit microprocessor, 512 bytes of read/write memory (four 2112 static RAMs), 1k bytes of 2608 ROM with PIPBUG*, two 8T31 I/O ports and buffering on data, address and control lines. A single +5 V supply will be required to power the card and communicate with a serial 20 mA current loop terminal.

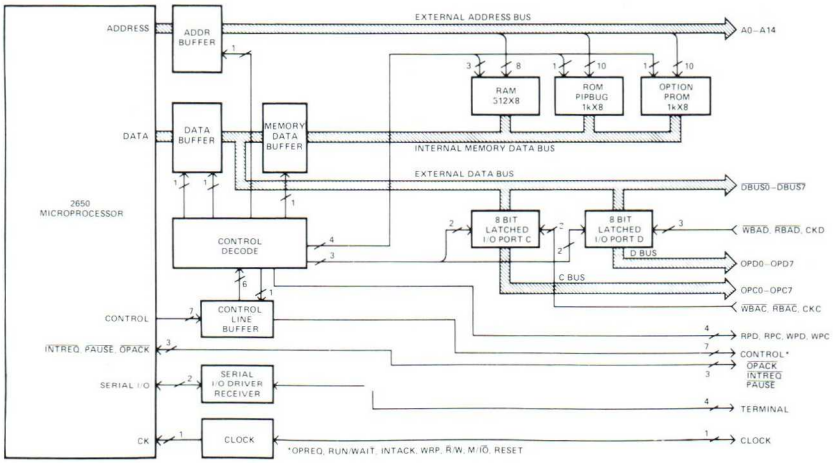
Modifications to the basic system can be easily made to allow for various memory configurations and operating modes. Unused plated-through holes are provided for the PROM memory chips (82S115s). Other options are jumper selectable. The area on the card associated with each jumper is identified with a "Wx" mnemonic.

The ABC 1500 is sold either as a completely assembled and tested card (2650PC1500) or in kit form (2650KT9500).

Features

- expandable printed circuit card: unused area on card filled with plated-through holes on 7,5 mm centres for wire-wrap sockets
- 1k bytes of PIPBUG* ROM (in socket)
- 512 bytes of RAM
- two latched I/O ports
  – four non-extended I/O read/write user strobes
- three-state buffers on data, address and control lines
- serial input/output port
- single +5 V supply requirement (1,7 A max) for card and 20 mA current loop interface (±12 V supply for RS232 interface)
- simple memory and I/O port decoding with two 16-pin DIPs
- interrupt and single step capability
- simple clock configured from dual monostable multivibrator
- 24k memory expansion capability
- directly compatible with 4k RAM card (2650PC2000) and power supply demonstration base (2650DS2000)
- card dimensions: 20 cm by 17,5 cm with a 100-pin connector along the 20 cm dimension

* PIPBUG is a loader, editor, and debug program. See Table 1.



Options

- 1k bytes of PROM in place of ROM
- 512 bytes of PROM or ROM in place of RAM
- asynchronous operation capability
- external clock input
- interrupt vector from port C

Interface

- terminal interface jumper selectable
  a. W4 to W5 and W6 to W7 jumpers select the 20 mA current loop mode
  b. W3 to W4 and W7 to W8 jumpers select the RS232 mode
- normally high input lines (10 kΩ pull-up resistor on each): $\overline{\text{INTREQ}}$, $\overline{\text{PAUSE}}$, $\overline{\text{RESET}}$, $\overline{\text{WBAC}}$, $\overline{\text{WBAD}}$, CKC, CKD
- plated-through holes are available at each connector pin to allow for insertion of wire-wrap pins
- edge connector supplied with card
- to allow for external clock input, remove jumper W9-W10
- asynchronous operation by removing jumper W1 to W2 and driving $\overline{\text{OPACK}}$
- during vectored interrupts, it is possible to allow port C to place the interrupt address on the data bus by removing jumper W21-W22 and jumpering W22-W23

Table 1 PIPBUG commands

alpha character input	command
A	alter memory
B	set breakpoint
C	clear breakpoint
D	dump memory to papertape
G	go to address
L	load memory from papertape
S	see and alter registers

Note: The program is entered by resetting the card. The terminal will then respond with an asterisk (*).

Memory configuration

All of page 0 is reserved for on-card memory (0 to 8191_{10}). Address lines A9, A11 and A12 are not decoded (Don't care signals) allowing two ICs to perform not only memory decoding but also I/O port decoding. As an added benefit, usable memory space exists at the top of page 0 (see memory map) due to the interleaving effect between the ROM and RAM memories. This memory space can be used as interrupt vector address locations in a negative direction from address location "0" (a negative relative instruction from address location "0" wraps around the first 8k page).

There is a total of two blocks in the RAM structure, each of which contains 256 bytes of RAM. Since PIPBUG uses the first 63 RAM locations for temporary storage, the first actual user location is 1087_{10} ($43F_{16}$) (there are seven other address locations corresponding to the first user location – see memory map). Starting at $43F_{16}$, the range for on card RAM extends to address 1535_{10} ($5FF_{16}$), giving a total usable on-card space of 449 bytes.

The first external memory location for add-on memory is 8192_{10} (2000_{16}). All of page 1, 2, and 3 are available, giving a total memory expansion capability of 24k.

Memory options

Modifications to the basic configuration can be made to provide a mix of RAM/PROM/ROM memories. PROM memories can be used in place of the PIPBUG ROM by removing the ROM from its socket and adding one or two 82S115 PROMs (512x8). Area and plated-through holes are provided on the card for insertion of sockets for the PROMs or the PROMs themselves. Decoding for the PROMs has been provided by ABC 1500 logic.

Data and address lines for 2112 RAMs and 82S129 PROMs or 82S229 ROMs are identical. It is, therefore, possible to use PROMs and/or ROMs in place of RAM. This option will require removal of the RAMs (two per block), and changing the jumper for each 256 byte block of PROM or ROM added. The jumper needed for each block of memory is as follows:

memory section	RAM jumper	PROM/ROM jumper
first block	W12-W13	W11-W13
second block	W15-W16	W14-W16

Adaptable Board Computer (ABC) prototyping system (continued)

I/O Port configuration

Two ports (C and D) are implemented with 8T31 bidirectional ports and can be used for general purpose I/O. Each consists of 8 clocked latches with two sets of bidirectional inputs/outputs. Data written into one side of the port will appear inverted at the other side.

One side of each port (Bus B of the 8T31) is tied to the external data bus ($\overline{DBUSX}$). The 2650 communicates with each port over this bus with one byte, non-extended I/O instructions. During 2650 activity with the ports, the ABC 1500 will provide four output strobes indicating the nature of the operation.

Table 2 Page 0 memory map

ADDRESS LINES						DECIMAL ADDRESS	ORGANIZATION	HEX ADDRESS
A14	A13	A12	A11	A10	A9			
						8k		1FFF
0	0	X	X	1	X		SECOND BLOCK RAM	
							FIRST BLOCK RAM	
							SECOND BLOCK RAM	
						7k	FIRST BLOCK RAM	1BFF
0	0	X	X	0	X		PIPBUG ROM	
						6k		17FF
0	0	X	X	1	X		SECOND BLOCK RAM	
							FIRST BLOCK RAM	
							SECOND BLOCK RAM	
						5k	FIRST BLOCK RAM	13FF
0	0	X	X	0	X		PIPBUG ROM	
						4k		0FFF
0	0	X	X	1	X		SECOND BLOCK RAM	
							FIRST BLOCK RAM	
							SECOND BLOCK RAM	
						3k	FIRST BLOCK RAM	0BFF
0	0	X	X	0	X		PIPBUG ROM	
						2k		07FF
0	0	X	X	1	X		SECOND BLOCK RAM	06FF
							FIRST BLOCK RAM	05FF
							SECOND BLOCK RAM	04FF
						1k	FIRST BLOCK RAM	03FF
0	0	X	X	0	X		PIPBUG ROM	
						0		0000

Notes

1. * = Don't care for ROM and RAM; ** = Don't care for RAM.
2. Each block of RAM = 256 bytes.

strobe	function	strobe pulse width
WPC	write to Port C	duration of WRP
WPD	write to Port D	duration of WRP
RPC	read Port C	duration of OPREQ
RPD	read Port D	duration of OPREQ

The other side of each port (Bus A of the 8T31) is controlled by the user. Four control lines are used to read, write or three-state the buses.

control line				function
$\overline{WBAD}$	(1)	$\overline{RBAD}$	(0)	Read Port D
$\overline{WBAD}$	(0)	$\overline{RBAD}$	(0)	Write to Port D
$\overline{WBAD}$	(1)	$\overline{RBAD}$	(1)	Three-state D Bus
$\overline{WBAC}$	(1)	$\overline{RBAC}$	(0)	Read Port C
$\overline{WBAC}$	(0)	$\overline{RBAC}$	(0)	Write to Port C
$\overline{WBAC}$	(1)	$\overline{RBAC}$	(1)	Three-state C Bus

If no external logic is connected each port will be in the "read" mode ($\overline{WBAX}$ lines pulled high). The $\overline{RBAX}$ lines are tied to ground to allow read/write control of the buses with just the $\overline{WBAX}$ lines. To allow control for three-stating the buses, the following jumpers must be removed:

Line	Jumper
$\overline{RBAC}$	W19-W20
$\overline{RBAD}$	W17-W18

The clock for each port (CKC-Port C clock, CKD-Port D clock) is available at a connector pin for external control. These normally "high" lines can be pulled low to disable writing to the ports from either the 2650 or the external device.

ABC 1500 edge connector signal list

pin no.	function	pin no.	function	pin no.	function	pin no.	function
1	GND	26	$\overline{INTREQ}$	A	GND	d	OPC 3
2	GND	27	$\overline{PAUSE}$	B	GND	e	OPC 4
3	NC*	28	NC*	C	NC*	f	OPC 5
4	$\overline{DBUS0}$	29	$\overline{RBAD}$	D	OPD 0	g	OPC 6
5	$\overline{DBUS1}$	30	NC*	E	OPD 1	h	OPC 7
6	$\overline{DBUS2}$	31	$\overline{RBAC}$	F	OPD 2	j	NC*
7	$\overline{DBUS3}$	32	NC*	H	OPD 3	k	RPD
8	$\overline{DBUS4}$	33	A11	J	OPD 4	m	$\overline{WBAD}$
9	$\overline{DBUS5}$	34	A13-E/$\overline{NE}$	K	OPD 5	n	WPD
10	$\overline{DBUS6}$	35	A12	L	OPD 6	p	CKD
11	$\overline{DBUS7}$	36	A14-D/$\overline{C}$	M	OPD 7	r	NC*
12	NC*	37	A9	N	NC*	s	NC*
13	A14-D/$\overline{C}$	38	A10	P	TTY serial in +	t	NC*
14	NC*	39	A8	R	TTY serial in −	u	NC*
15	A13-E/$\overline{NE}$	40	A7	S	TTY serial out +	v	RPC
16	INTACK	41	A6	T	TTY serial out −	w	$\overline{WBAC}$
17	$\overline{R}$/W	42	A5	U	RS232 ground	x	WPC
18	WRP	43	A3	V	RS232 output	y	CKC
19	RUN/$\overline{WAIT}$	44	A0	W	NC*	z	NC*
20	OPREQ	45	A1	X	NC*	$\overline{a}$	NC*
21	M/$\overline{IO}$	46	A4	Y	RS232 input	$\overline{b}$	NC*
22	$\overline{OPACK}$	47	A2	Z	NC*	$\overline{c}$	NC*
23	CLOCK	48	+12 V	a	OPC 0	$\overline{d}$	+12 V
24	TS	49	−12 V	b	OPC 1	$\overline{e}$	−12 V
25	$\overline{RESET}$	50	+5 V	c	OPC 2	$\overline{f}$	+5 V

Adaptable Board Computer (ABC) prototyping system (continued)

ABC 1500 parts list

quantity	description
1	PC1500 printed circuit board
1	edge connector – AMP 225-804-50
1	2650 8-bit static microprocessor
1	N7402 quad 2-input NOR gate – I/O strobe logic
1	N7416 hex inverter buffer – current loop interface
1	N74123 monostable multivibrator – clock for 2650
1	N74S138 3 line to 8 line decoder – control decode
1	8T15 – EIA line driver – R232 driver
4	8T26 quad three-state driver/receiver – data and memory data buffer
2	8T31 – bit latched bidirectional I/O port
4	8T97 hex three-state driver – address and control line buffer
1	2608 static ROM (1024x8) – PIPBUG ROM – CN0035
4	2112 static RAM (256x4) – organized as 512 byte RAM
1	82S123 PROM (32x8) coded PROM CD 1500 – control decode
4	1N914 diode
1	2N2222 transistor
1	50 pF capacitor
1	300 pF capacitor
13	0,1 μF capacitor
3	4,7 μF capacitor
2	220 Ω resistor
6	1 kΩ resistor
2	2 kΩ resistor
1	3,3 kΩ resistor
8	10 kΩ resistor
1	20 kΩ resistor
1	24-pin 2608 ROM socket – Robinson-Nugent ICN 246-54

Resident Assembler Board 2650PC1600

Features

- 3-pass Resident Assembler
- 5,5k bytes assembler program
- socket for 512 bytes user defined PROM
- 2k bytes RAM
- 365 user-definable symbols
- 20 pre-defined symbols
- generation of error messages
- LIBR directive to create subroutine libraries
- compatible with PC1001, ABC1500 and DS2000
- paper tape editor facility
- single +5 V supply requirement (4 A max)
- card dimensions 20 cm by 17,5 cm with a 100-pin connector along the 20 cm dimension

The 2650PC1600 is a resident assembler to be used with the PC1001 or ABC1500 prototyping boards. It also fits into the DS2000 power supply base.

The system consists of a printed-wiring board on which 11 PROMs containing the assembler program are mounted, together with 16 RAM ICs for use as storage during program assembly. The assembler has been designed for use with paper tape and so input and output are transmitted via a teletype. Alternatively, a fast paper tape reader may be used to advantage. An extra socket has been included on the PC1600 board for PROM containing a tape-reader control program.

The PC1600 resident assembler accepts a program written in 2650 Assembly Language as input and produces a tape containing a hexadecimal translation of the program. This hexadecimal tape has a format suitable for input to the PC1001 or ABC1500 prototyping boards via the PIPBUG control program which is included on both these boards. The assembler is a three-pass type, that is the entire assembly language program is scanned three times by the assembler. On the first pass all the symbols defined by the user (up to a maximum of 365) are assigned values and stored in the RAMs on the PC1600 board and simple errors such as invalid symbols detected. During the second pass the internal logic of the program is checked and any further errors detected, the line-by-line assembly is performed and a full listing of the program, including any error messages, is printed out. On the third pass the hexadecimal tape is punched and a corresponding hexadecimal listing produced for reference.

The assembler program introduces several additional features over the cross assembler, the most important being four new error messages, 20 pre-defined symbols and a new assembler directive LIBR. This directive enables the user to assemble several tapes into one hexadecimal tape as part of the same program, this facilitates the creation of subroutine "libraries". The assembler also makes patching of a program in RAM easier by assembling the correct number of bytes for a line containing an error, so that these bytes may be altered without changing the memory locations of the rest of the bytes of the program.

PC1600 edge connector signal list

pin no.	function
1	GND
2	GND
4	DBUS0
5	DBUS1
6	DBUS2
7	DBUS3
8	DBUS4
9	DBUS5
10	DBUS6
11	DBUS7
17	R/W
18	WRP
20	OPREQ
21	M/IO
33	ABUS11
34	ABUS13
35	ABUS12
36	ABUS14
37	ABUS9
38	ABUS10
39	ABUS8
40	ABUS1
41	ABUS6
42	ABUS5
43	ABUS3
44	ABUS0
45	ABUS1
46	ABUS4
47	ABUS2
50	+5 V
A	GND
B	GND

4k Memory Card
2650PC2000

The 2650PC2000 is a 4k Memory Card designed to be compatible with the 2650 microprocessor. It is composed of 32 NMOS, 1k by 1 bit static RAMs, 21L02, and organized in four groups of one kilobyte each. Decoding is provided to select one of the four groups and also distinguish the card in multi-card configurations. In a system application utilizing up to 8 cards (32k), each card is uniquely identified by hardwired jumpers. No external decoding is required.

The decoding logic is sectioned into two blocks. The first block determines if the address identifies that card as being part of the 8k page address. (The 2650 memory scheme is organized into 4 pages of 8k each.) The second block uniquely locates 1k bytes of memory on the board in the 8k bytes of memory of the selected page. Each 1k bank is individually selected by hardwired jumpers to the decoder.

Features

- requires only single +5 V supply
- industry standard 21L02 memories
- fully decoded for 32k memory organization
- data bus buffered with three-state drivers/receivers
- accessable from microprocessor or DMA controller
- TTL compatible
- dimensions are 20 x 17,5 cm with a 50-pin edge connector along 20 cm dimension
- typical power consumption of 4,5 W

Signal definition

Memory control signals and address lines between the 2650 microprocessor and the 2650PC2000 are indicated in the block diagram. The $\overline{\text{OPEX}}$ control line is reserved for use with DMA controllers. Its function is similar to that of the OPREQ line from the 2650. When either of these lines are true and a memory operation is specified (M/$\overline{\text{IO}}$ = High) the memory card is enabled to decode address lines A0-A14. When a bank is selected, the selected card control logic block allows the read-write line ($\overline{\text{R}}$/W) and write pulse (WRP) to pass to the memory array and also enable the external data bus drivers. When the operation is complete the memory card responds with a true condition on $\overline{\text{OPACK}}$.

Jumper address decoding

Jumpers are applied to designated plated-through holes identified by a "Wn" mnemonic. To identify the card to be part of a particular page, jumper point W5 to one of the following:

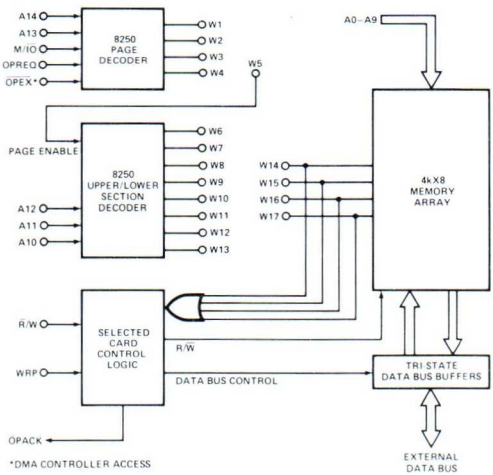
W1 for page 0
W2 for page 1
W3 for page 2
W4 for page 3

To locate each of the 1k bytes of the memory card in the selected memory page, four bank jumpers are required. The outputs of the decoder used to select one of eight 1k byte memory segments (W6-W13) must be connected to the selected 1k bytes of memory on the 2650PC2000 (W14-W17).

Factory installed jumpers allow for immediate connection to a Demo System (DS1000/2000) which has 2k of memory. These jumpers have been connected as follows:

W1 to W5 (page 0)
W8 to W14
W9 to W15
W10 to W16
W11 to W17

2650PC2000 block diagram



2650PC2000 edge connector

pin no.	function	pin no.	function
1,2, A, B	GROUND	34	ABUS13
4	$\overline{\text{DBUS0}}$	35	ABUS12
5	$\overline{\text{DBUS1}}$	36	ABUS14
6	$\overline{\text{DBUS2}}$	37	ABUS9
7	$\overline{\text{DBUS3}}$	38	ABUS10
8	$\overline{\text{DBUS4}}$	39	ABUS8
9	$\overline{\text{DBUS5}}$	40	ABUS7
10	$\overline{\text{DBUS6}}$	41	ABUS6
11	$\overline{\text{DBUS7}}$	42	ABUS5
17	$\overline{\text{R}}$/W	43	ABUS3
18	WRP	44	ABUS0
20	OPREQ	45	ABUS1
21	M/$\overline{\text{IO}}$	46	ABUS4
22	$\overline{\text{OPACK}}$	47	ABUS2
24	$\overline{\text{OPEX}}$	50, f	VCC +5 V
33	ABUS11		

Microprocessor Demonstration System 2650DS2000

The Demo System 2000 (2650DS2000) is a hardware base for use with the 2650 CPU printed circuit board (PC1001) and allows the exercising of this card with user defined options. When the DS2000 is combined with a CPU board (PC1001) and a teletype (TTY), the user is equipped with everything he needs to exercise any of the software or hardware features of the 2650. The DS2000 has a built-in power supply.

Features

- user-defined expansion capability from connector supplying address, data and control lines
- RS232 and TTY interface
- two extended and two non-extended I/O ports
- single step capability for program debugging
- display of address bus, data bus and the two non-extended I/O ports

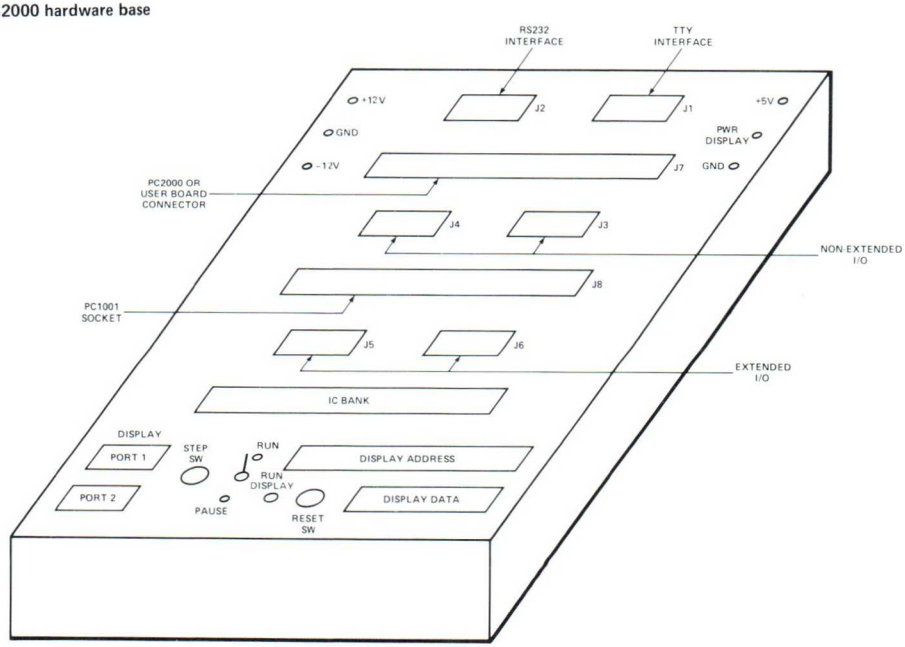
Connectors

The 2650 CPU Board (PC1001) is inserted into the J8 connector to complete the demo system. The user printed circuit board is inserted into the J7 connector. Both connectors are the same type (100 Pin Amphenol, series 225) and the numbered pins J7 and J8 have the same signals (except pin 12). The lettered pins of J7 (pins A to g) are not used.

Displays

The address and data bus led displays reflect the information on these buses during each OPREQ (beginning of an external operation). Latches store the information until another OPREQ is received. The two non-extended port displays represent data on channel C (port 2) and channel D (port 1) during the OPREQ for each I/O operation. A logic one on these displays will turn "on" the leds and a logic zero will turn them "off".

DS2000 hardware base



Controls

The pause and step logic allows one instruction to be executed at a time by pushing the 'step' button when the Run/Pause switch is in the pause position. In this mode the Run/$\overline{\text{Wait}}$ display led will go off. The reset switch will reset the display latches and place all zeros in the 2650 instruction address register.

Connections to sockets J7 and J8

pin no.	function (J7 and J8)	pin no.	function (J7 and J8)	pin no.	function (J8 only)*	pin no.	function (J8 only)*
1	GND	26	$\overline{\text{INTREQ}}$	A	GND	d	OPC 3
2	GND	27	$\overline{\text{PAUSE}}$	B	GND	e	OPC 4
3	NC**	28	NC	C	NC	f	OPC 5
4	$\overline{\text{DBUS0}}$	29	NC	D	OPD 0	g	OPC 6
5	$\overline{\text{DBUS1}}$	30	NC	E	OPD 1	h	OPC 7
6	$\overline{\text{DBUS2}}$	31	NC	F	OPD 2	j	EIPC
7	$\overline{\text{DBUS3}}$	32	NC	H	OPD 3	k	IPD 0
8	$\overline{\text{DBUS4}}$	33	ABUS 11	J	OPD 4	m	IPD 1
9	$\overline{\text{DBUS5}}$	34	ABUS 13	K	OPD 5	n	IPD 2
10	$\overline{\text{DBUS6}}$	35	ABUS 12	L	OPD 6	p	IPD 3
11	$\overline{\text{DBUS7}}$	36	ABUS 14	M	OPD 7	r	IPD 4
12*	EIPD	37	ABUS 9	N	COPD	s	IPD 5
13	D/$\overline{\text{C}}$	38	ABUS 10	P	TTY serial in +	t	IPD 6
14	$\overline{\text{DMA}}$	39	ABUS 8	R	TTY serial in –	u	IPD 7
15	E/$\overline{\text{NE}}$	40	ABUS 7	S	TTY serial out +	v	IPC 0
16	INTACK	41	ABUS 6	T	TTY serial out –	w	IPC 1
17	$\overline{\text{R}}$/W	42	ABUS 5	U	RS232 ground	x	IPC 2
18	WRP	43	ABUS 3	V	RS232 output	y	IPC 3
19	RUN/$\overline{\text{WAIT}}$	44	ABUS 0	W	TTY tape reader out +	z	IPC 4
20	OPREQ	45	ABUS 1	X	TTY tape reader out –	$\overline{\text{a}}$	IPC 5
21	M/$\overline{\text{IO}}$	46	ABUS 4	Y	RS232 input	$\overline{\text{b}}$	IPC 6
22	$\overline{\text{OPACK}}$	47	ABUS 2	Z	COPC	$\overline{\text{c}}$	IPC 7
23	CLOCK	48	+12 V	a	OPC 0	$\overline{\text{d}}$	+12 V
24	$\overline{\text{OPEX}}$	49	–12 V	b	OPC 1	$\overline{\text{e}}$	–12 V
25	$\overline{\text{RESET}}$	50	+5 V	c	OPC 2	$\overline{\text{g}}$	+5 V

* J7 has no connections to these pins.

** NC = No Connection.

Microprocessor Demonstration System (continued)

Extended I/O DIL sockets			Non-extended I/O DIL sockets		
pin no.	function J5	function J6	pin no.	function J3	function J4
1	$\overline{\text{DBUS0}}$	ABUS 0	1	(Output Port C) 0	(Output Port D) 0
2	$\overline{\text{DBUS1}}$	ABUS 1	2	OPC 1	OPD 1
3	$\overline{\text{DBUS2}}$	ABUS 2	3	OPC 2	OPD 2
4	$\overline{\text{DBUS3}}$	ABUS 3	4	OPC 3	OPD 3
5	$\overline{\text{DBUS4}}$	ABUS 4	5	OPC 4	OPD 4
6	$\overline{\text{DBUS5}}$	ABUS 5	6	OPC 5	OPD 5
7	$\overline{\text{DBUS6}}$	ABUS 6	7	OPC 6	OPD 6
8	$\overline{\text{DBUS7}}$	ABUS 7	8	OPC 7	OPD 7
9	$\overline{\text{OPACK}}$	ABUS 8	9	Clock Output Port C	Clock Output Port D
10	M/$\overline{\text{IO}}$	ABUS 9	10	Enable Input Port C	Enable Input Port D
11	OPREQ	ABUS 10	11	(Input Port C) 7	(Input Port D) 7
12	RUN/$\overline{\text{WAIT}}$	ABUS 11	12	IPC 6	IPD 6
13	WRP	ABUS 12	13	IPC 5	IPD 5
14	$\overline{\text{R}}$/W	ABUS 13	14	IPC 4	IPD 4
15	INTACK	ABUS 14	15	IPC 3	IPD 3
16	E/$\overline{\text{NE}}$	$\overline{\text{PAUSE}}$	16	IPC 2	IPD 2
17	$\overline{\text{DMA}}$	$\overline{\text{INTREQ}}$	17	IPC 1	IPD 1
18	D/$\overline{\text{C}}$	CLOCK	18	IPC 0	IPD 0

TTY interface DIL socket		RS232 interface connector	
pin no.	function J1	pin no.	function J2
1	TTY serial in +	1	RS232 ground
2	TTY serial in –	2	RS232 input
8	TTY tape reader out –	3	RS232 output
9	TTY tape reader out +	5	jumper
13	TTL serial out –	6	jumper
14	TTL serial out +	7	RS232 ground
		8	jumper
		20	jumper

Intelligent Typewriter Controller
2650PC3000

The 2650PC3000 is a basic text generating system requiring only six integrated circuits including one 2650 microprocessor. The serial communication link between the 2650 and the users terminal is accomplished with the flag and sense lines on the microprocessor. The 2650PC3000 is used to control the storage of characters entered from a terminal with either a current loop or voltage swing capability (±7,5 V min).

Control Characters allow the text to be printed out on the terminal with the capability for inserting unique characters at locations identified during text generation. When the text is printed out the entire text will be output unless a control character is detected. The microprocessor then stops the print-out and the operator enters the desired unique information. Another control character is then given to continue printing the text until all characters stored in memory are printed or until another stop character is detected. The stop character is recorded in memory just like any other character; however, it is not printed during text print-out.

Additional control characters allow for the erasure of the previous character typed or the erasure of the entire memory.

Features

- total of six IC packages
- operates at +5 V at a max of 500 mA
- interface to either current loop or device capable of sending and receiving a minimum voltage swing of ±7,5 V referenced to signal ground
- 250 character storage capability
- card size less than 7,5 x 10 cm with four screwed-on stand-offs at corners
- 1 MHz clock implemented with 74123 one-shot
- variable baud rate between 110 and 300 baud by trimmer pot adjustment of clock
- PROM mounted in 24-pin socket
- card edge connector supplied with each card
- inputs provided for an external system reset

Parts descriptions

2650	8-bit TTL compatible N-Channel Microprocessor incorporating a serial I/O Port. (See 2650 Hardware Specification Manual for complete description – 2650BM1000.)
2606	1024-bit static MOS, TTL compatible RAM memory organized as 256 words by 4 bits/word
82S115	4096-bit Bipolar TTL compatible PROM organized as 512 words by 8 bits/word
N7426	Quad 2-input high voltage NAND gate with open collector capable of driving voltage and current loop interfaces (20 mA max)
74123	Dual retriggerable monostable multivibrator with clear configured as a clock for 2650
Potentiometer	Helipot series 91C 50 kΩ, 9,5 mm cermet trimming potentiometer
PC edge connector	Amphenol – 225-21021-401-117 Cinch – 251-10-30-160

Miscellaneous components consist of eleven ¼ W and two ½ W resistors, and two mica, one ceramic and one tantalum capacitor.

The following are required to make the board functional but are not supplied with the card:
RS232 type connector for voltage swing interface: DB25P or DB25S
Reset switch – (normally open, connected to +5 V)
Power supplies: +5 V
±15 V

Intelligent Typewriter Controller (continued)

Terminal interface
voltage mode terminal connection

The voltage mode interface is very similar to the standard RS232 interface except that the "signal" ground cannot be connected to "protective" ground. When a Cinch type 25-pin connector (DB25P or DB25S) is used on an RS232 compatible terminal, the PC3000 should be connected as follows:

DB25P (DB25S) pin no.	PC3000 edge connector pin no.	PC3000 signal name
1	no connection	–
3	6	VS out +
2	J	VS in +
7	K	VS out – (signal GND)
5, 6, 8, 20	connect together	–

on card – jumper point A to C
and point D to E.

current loop terminal connection

When a terminal is used that employs current loop transmission techniques the four wires from the terminal should be connected to the corresponding four pins on the PC3000 card: TTY out +, TTY out –, TTY in +, and TTY in–.
on card – jumper point A to B
and point D to F.

PC3000 command summary

key	function
Rubout (delete)	Erase last character in memory and echo the erased character. Additional preceding characters can be erased by continuing to depress the delete key.
Control and E	Erase entire memory.
Control and B	Used to indicate beginning of inserted message. Is not printed but stored in memory. Stops print-out when read from memory. Required once from each unique information entry.
Control and C	Continues print-out of memory after entry of unique information.
Control and P	Prints out contents of terminal memory.
Control and R	Software reset.

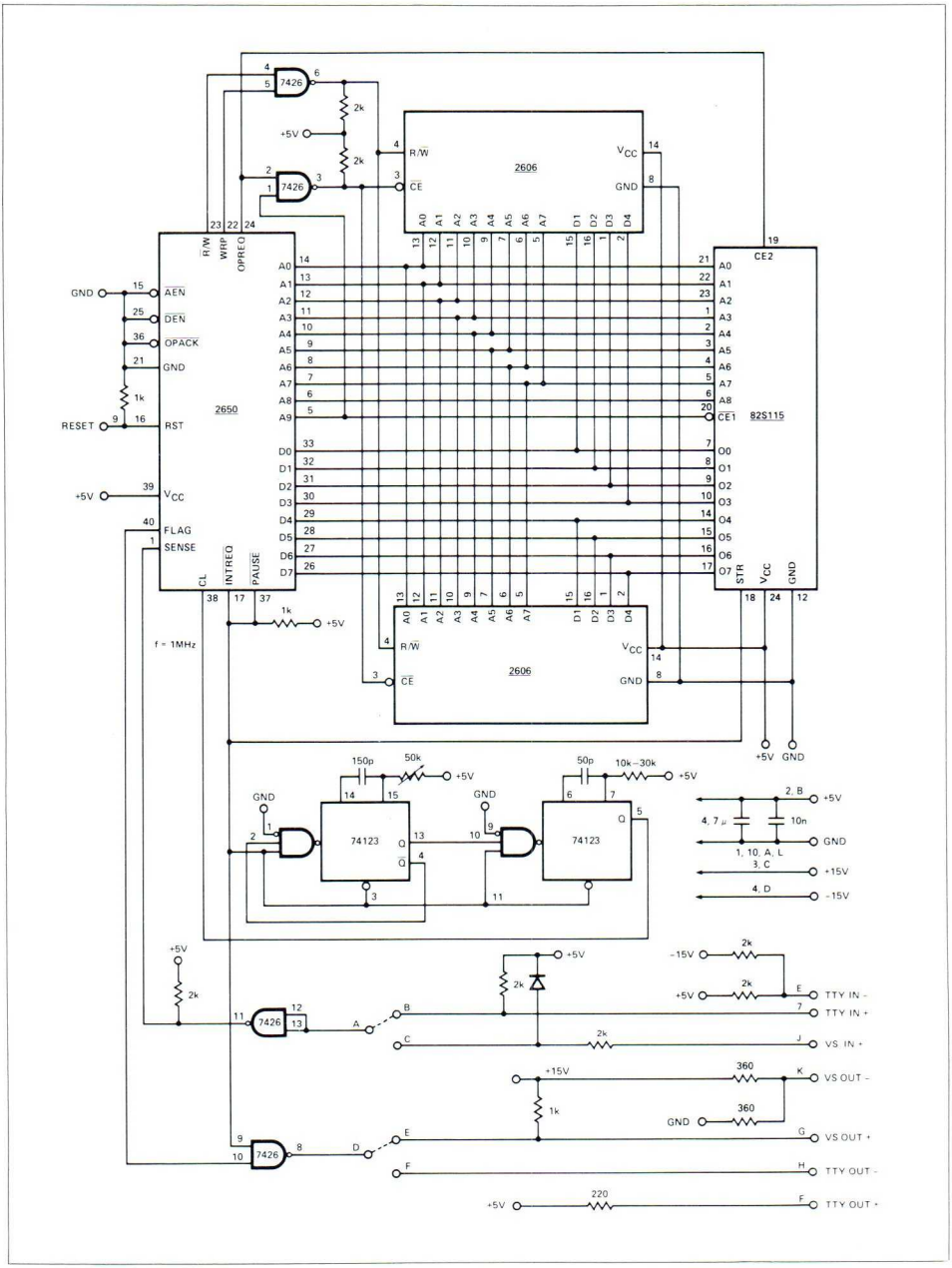
Note:
Bell will ring if any of the following are true
1. Entering more than 250 characters in memory.
2. Requesting print-out of an empty buffer.
3. Attempting to delete more characters than there are in memory.

PC3000 connector pin assignment

pin no.	function	pin no.	function
1	GND	A	GND
2	+5	B	+5
3	+15	C	+15 V
4	–15	D	–15
5	–	E	TTY in –
6	VS out +	F	TTY out +
7	TTY in +	H	TTY out –
8	–	J	VS in +
9	RESET	K	VS out – (Signal Ground)
10	GND	L	GND

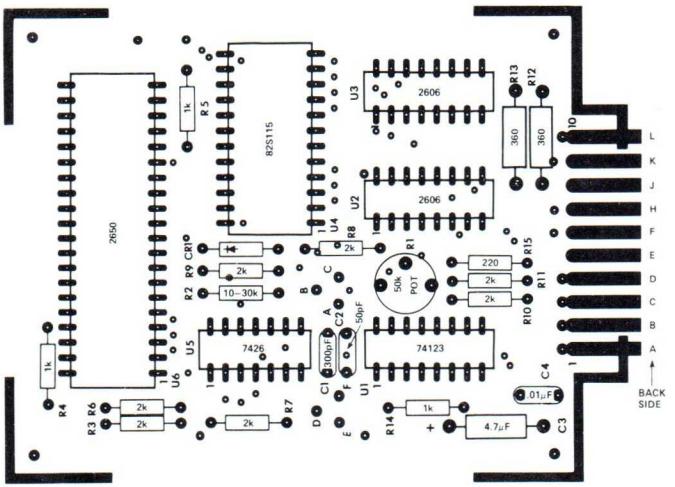
VS – Voltage Swing

Intelligent typewriter controller

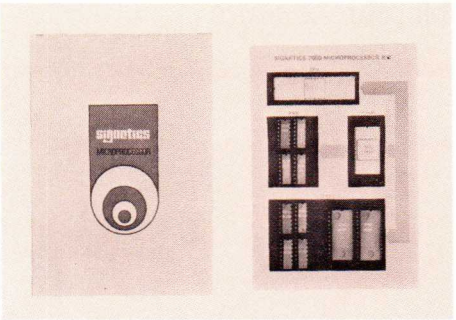


Intelligent Typewriter Controller (continued)

Intelligent typewriter controller board layout



Microprocessor Prototyping Kit
2650KT9100



The KT9100 kit contains a 2650 microprocessor and enough chips to implement a small development system. Since the interface requirements of the 2650 are completely TTL compatible, no attempt has been made to limit the user's flexibility by dictating a fixed logic configuration. There is complete freedom in using standard SSI or MSI logic to adapt the microprocessor to the memory, I/O devices, or clock.

Several simple system examples are presented to enable quick set up and evaluation. Other configurations to adapt to individual requirements should become evident from these examples.

Parts descriptions

2112: The 2112 is a static 1024-bit RAM organized as 256 words by 4 Bits/Word. It is manufactured with n-channel, silicon gate, MOS technology and achieves an access time of less than 800 ns. No clocks are required, and the chip is powered from a single 5 V source.

82S115I: The 82S115I is a 4096-bit Schottky-Clamped, bipolar PROM incorporating on-chip data output registers. It is field-programmable and fully TTL compatible with on-chip decoding and two chip enable inputs for easy memory expansion. Inputs to the device are pnp transistors with a maximum current requirement of 100 μA.

8T31: The 8T31 is an 8-bit Bidirectional I/O Port designed to function as a general purpose I/O interface element. It consists of 8 clocked latches with two sets of bidirectional Inputs/Outputs allowing master control from either the microprocessor or from the I/O device.

8T26B: The 8T26B consists of four pairs of inverting three-state logic elements configured as Quad Bus Drivers/Receivers with separate buffered receiver enable and driver enable lines. Both the driver and receiver gates have three-state outputs and low-current pnp inputs.

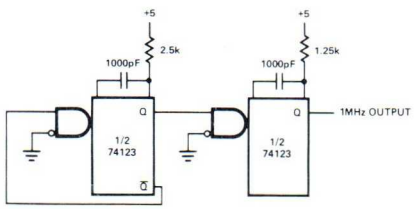
Circuit examples

Two circuit configurations are presented to indicate a possible program checkout approach. The first allows the use of RAM for program debugging. The second figure represents a possible final system configuration with the program fixed in PROM. Both circuits use the 8T26s as bus buffers.

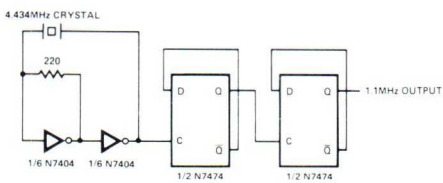
Parts list

part no.	qty	description
2650	1	CPU
2112	4	256 x 4 RAM
82S115I	1	4k PROM (Unprogrammed) 512 x 8
8T31I	2	8-bit Bidirectional I/O Port
8T26B	4	Quad Bus DR/REC

One-shot clock oscillator circuit

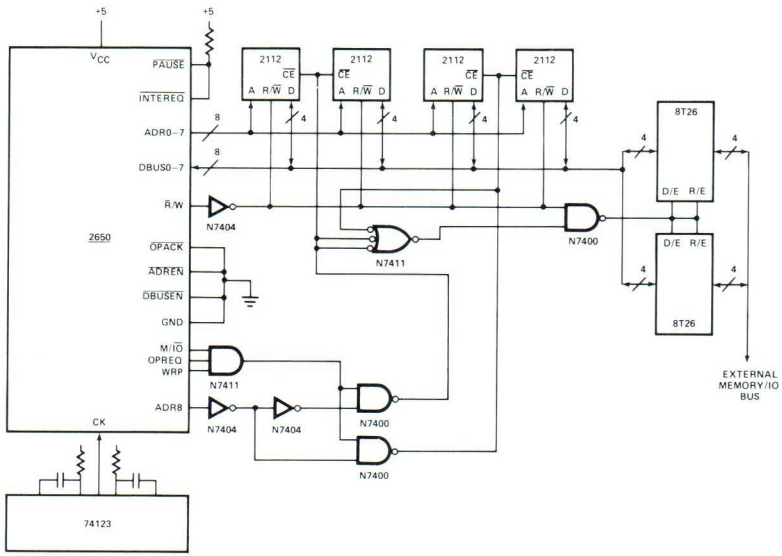


Crystal oscillator circuit

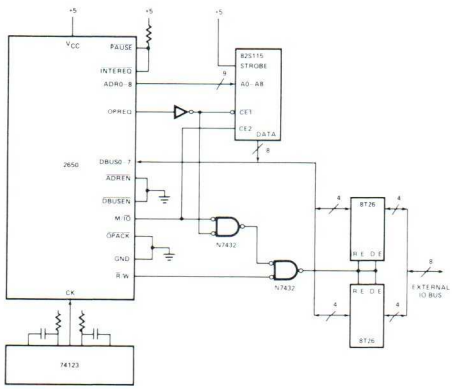


Microprocessor Prototyping Kit (continued)

Example of initial program checkout configuration



Finalized configuration with program fixed in PROM



2650 Assembler Version 3.2
2650AS1000/1100

The 2650 assembly language (PIPHASM) is a symbolic language designed specifically to facilitate the writing of programs for the 2650 microprocessor.

The AS1000 is for 32-bit or larger machines and the AS1100 is for 16-bit machines.

The 2650 assembler is a program which accepts symbolic source code as input and produces a listing and/or an object module "Hexadecimal" format compatible to the two tape punching programs PIPHTAP (for acceptance by PIPBUG), PIPSTAP (for PROMs) and also to the simulator, PIPSIM.

The assembler is written in standard Fortran IV and is approximately 1 250 Fortran card images in length. It is modular and may be executed in an overlay mode should memory restrictions make that necessary. It operates in a two-pass mode to build a symbol table, to issue helpful error messages, produce an easily readable program listing and output a computer-readable object module. This version of the assembler compiles into a 12k word load module on the PDP-11/40 (16-bit words) and executes under DOS (8k) within a 28k memory.

Availability

The 2650 assembler is available on both NCSS and GE timeshare. It is also available from Signetics on 9-track magnetic tape written in EBCDIC in 80-character unblocked records at a density of 800 bpi.

Features

- forward references
- pseudo-ops to aid programming
- self-defining constants
- symbolic machine operation codes
- free format source code
- syntax error checking
- symbolic address assignment and references
- data creation statements
- storage reservation statements
- assembly listing control statements
- addresses can be generated as constants
- character codes may be specified as ASCII or EBCDIC
- comments and remarks may be encoded for documentation

Language requirements

I. Input requirements

Input to the assembler consists of a sequence of characters combined to form assembly language elements. These language elements include symbols, instruction mnemonics, constants and expressions which make up the individual program statements that comprise a source program.

A. Characters

alphabetic:	A-Z
numeric	0-9
special characters	blank
	(left parenthesis
	) right parenthesis
	+ add or positive value
	– subtract or negative value
	* asterisk
	' single quote
	, comma
	/ slash
	$ dollar sign
	< less than sign
	> greater than sign

B. Symbols

Symbols are formed from combination of characters. Symbols provide a convenient means of identifying program elements so they can be referenced by other elements.

C. Constants

A constant is a self-defining language element. Unlike a symbol, the value of a constant is its own "face" value and is invariant. Internal numbers are represented in 2s complement notation. There are two forms in which constants may be written: the Self-Defining Constant and the General Constant.

Self-Defining Constant

The self-defining constant is a form of constant which is written directly in an instruction and defines a decimal value.

General Constant

The general constant is also written directly in an instruction, but the interpretation of its value is dictated by a code character and delimited by quotation marks. Its form can be binary, octal, decimal, hexadecimal, EBCDIC or ASCII.

D. Expressions

An expression is an assembly language element that represents a value. It consists of a single term or combination of terms separated by arithmetic operators. A term may be a valid symbolic reference, a self-defining constant or a general constant.

2650 Assembler Version 3.2 (continued)

II. Fields

A statement prepared for processing by the assembler is logically divided into four fields, as indicated below. They are free form and are separated by at least one blank character. The name must begin in logical column 1.

Label	Operation	Operand	Comments
name	opcode	operand(s)	

Where:

Label field — contains an optional label which the assembler will assign as the symbolic address of the first byte of the instruction.

Operation field — contains any of the 2650 processor mnemonic operation codes or any assembler Directive. This field may include an expression which specifies a register or value as required by the instruction. All symbols used in this field must have been previously defined, i.e. no symbolic forward references are allowed.

Operand field — contains one or more operand elements such as indirect address indicator, operand expression, index register specification, auto-increment/auto-decrement indicator, constant specification, etc. depending on the requirements of the particular instruction.

Comments field — any characters following the operand field will be reproduced in the assembly listing without processing. The Comments Field must be separated from the argument field by at least one blank.

III. Directives

There are eleven directives which the assembler will recognize. These assembler directives, although written much like processor instructions, are simply commands to the assembler instead of to the processor. They direct the assembler to perform specific tasks during the assembly process, but have no meaning to the 2650 processor. These assembler directives are:

ORG	Set location counter
EQU	Specify a symbol equivalence
ACON	Define address constant
DATA	Defines memory data
RES	Reserve memory storage
END	End of assembly
EJE	Eject the listing page
PRT	Printer control
SPC	Space control
TITL	Title
PCM	Punch control

2650 Simulator Version 1.2
2650SM1000/1100

The 2650 Simulator (PIPSIM) is a Fortran IV program which allows a user to simulate the execution of his program without utilizing the 2650 processor. The simulator executes the 2650 program via host computer software by maintaining its own internal Fortran storage registers to describe the 2650 program, the microprocessor registers, the ROM/RAM memory configuration, and the input data to be read dynamically from I/O devices. Inputs to the simulator are the object module (or the 2650 program in object format) produced by the 2650 assembler and a deck of user commands. The simulator can accommodate an object module of up to 8192 Bytes.

The output consists of a listing of the user's commands and a print out of both static and dynamic information as requested by the commands. The user may request traces of the processor status, dumps of the contents of memory, and recording of program timing statistics. Multiple simulations of the same program with different parameters may be executed during one simulation run.

The SM1000 is configured to operate on 32-bit or larger machines and executes under DOS (8k) within a 28k memory. The SM1100 is configured for 16-bit machines and compiles into a 16k word load module on a PDP-11/40.

Availability

The 2650 Simulator is available on both NCSS and GE timeshare. It is also available from Signetics on a 9-track magnetic tape written in EBCDIC in 80-character unblocked records at a density of 800 bpi.

Features

- cycle counter for timing estimates
- instruction fetch break points
- operand fetch break points
- trace facilities
- snapshot dumps
- patching facility
- statistical information generated
- easy-to-use command language
- optionally selected start and end addresses
- simulated registers may be displayed while the simulation program is executed
- simulated registers may be altered while the program is executing
- maintains a 2k cell (easily modified to 8k) to simulate a read/write RAM
- capability exists for configuring parts of simulator memory to look like ROM
- incorporates a 200-byte first in, first out (FIFO) buffer to store the data read from a simulated input device
- establishes initial program conditions
- monitors execution sequences

User commands

Commands specify how the program is to run and what data is to be recorded. The simulator accepts information in card image form. The entire card is read in Fortran "A" format, and one command must be complete on one card. Comments may appear in any order within a command set.

The basic manual set (2650BM1000) contains a complete description of the user commands and the general operation of the simulator.

2650 Simulator Version 1.2 (continued)

command name	parameters	description
DUMP	LOC, FWA-LWA(;....;LOC, FWA-LWA)	Display the area of memory, FWA-LWA, whenever the instruction at LOC executes.
REND	NONE	Execute the last simulation and terminate the entire run.
INPUT	VALUE (;....;VALUE)	Define the data to be read by simulated I/O instructions.
INSTR.	LOC(;....;LOC)	Display the processor state whenever the instruction at LOC executes.
LIMIT	NO	Specify the total number of instructions executed.
PATCH	LOC, VALUE(;....;LOC,VALUE)	Initialize each memory location, LOC, to VALUE
REFER.	LOC(;....;LOC)	Display the processor state whenever the instruction at LOC is referenced by another instruction.
SETP.	LOC(,PSL=VALUE), (,PSU=VALUE)	Set the program status byte (lower and/or upper) to VALUE whenever the instruction at LOC executes.
SETR.	LOC (9, RO=VALUE)...(R6=VALUE)	Set the general purpose registers to VALUE whenever the instruction at LOC executes.
SROM	FWA-LWA	Specify the boundaries of Read-Only Memory.
START	LOC	Start the simulated program execution at LOC.
STAT	None	Display instruction statistics at end of program execution.
STOP.	LOC(;....;LOC)	Terminate the program execution when the instruction at LOC executes.
TEND	None	Execute the last simulation and prepare to read the User Commands for the next simulation.
TRACE.	FWA-LWA(;....;FWA-LWA)	Display the processor state whenever an instruction executes, which lies within the area of memory, FWA-LWA.

Higher Level Language (PLμS)
2650PL1000

The higher level language is designed for use with the 2650 microprocessor. This language allows the programmer to reduce programming effort while retaining the control and efficiency of assembly language. It is written in ANSI standard Fortran IV and will execute on most machines without alteration. Programs written in this language tend to be self-documenting and are easily altered.

The higher level language is a sequence of "Declarations" and "Executable Statements".

The declarations allow the programmer to control allocation of storage, define simple textual substitutions (Macros), and define procedures. The language is "Block Structured": procedures may contain further declarations which control storage allocation and define other procedures.

The procedure definition facility of the language allows modular programming: a program can be divided into sections (e.g. teletype input, conversion from binary to decimal forms, and printing output messages). Each of these sections is written as a language procedure. Such procedures are conceptually simple, easy to formulate and debug and easily incorporated into a large program. They may form a basis for a procedure library, if a family of similar programs is being developed. Procedures may be individually compiled.

The language handles two kinds of data, its two basic "Data Types": byte and address. A byte variable or constant is one that can be represented as an 8-bit quantity; an address variable or constant is a 16-bit or double-byte quantity. The programmer can declare variable names to represent byte or address values. One can also declare vectors (or arrays) or type byte or address.

In general, executable statements specify the computational processes that are to take place. To achieve this, arithmetic, logical (Boolean), and comparison (relational) operators are defined for variables and constants of both types (BYTE and ADDRESS). These operators and operands are combined to form EXPRESSIONS, which resemble those of elementary algebra. Expressions are a major component of language statements.

A simple statement form is the assignment statement, which computes a result and stores it in a memory location defined by a variable name. Other statements in the language perform conditional tests and branching, loop control, and procedure invocation with parameter passing. The flow of program execution is specified by means of powerful control structures that take advantage of the block-structured nature of the language. Input and output statements read and write 8-bit values from and to input and output ports. Procedures can be defined which use these basic input and output statements to perform more complicated I/O operations.

A method of automatic text-substitution (more specifically, a "compile-time macro facility") is also provided. A programmer can declare a symbolic name to be completely equivalent to an arbitrary sequence of characters. As each occurrence of the name is encountered by the compiler, the declared character sequence is substituted, so the compiler actually processes the substituted character string instead of the symbolic name.

The compiler supports compile time expression evaluation and conditional compilation which allows selective compilation of code depending on an input parameter at compile time.

The language generates absolute and/or relocatable code. The relocatable modules may be linked by a powerful linkage editor at load time.

Additionally the language contains all machine independent features of the PL/M language as a subset, thereby enhancing portability of programs.

Availability

The higher level language is available on NCSS timeshare. It is also available from Signetics on magnetic tape for 16 and 32-bit machines.

Features

- written in free-form
- adaptable to both 16 and 32-bit machines
- block structured
- employs procedure calls
- byte and address data elements
- based variables
- in-line assembly language
- Macro capability
- generates relocatable code supported by a relocating loader
- includes PL/M as a subset
- allows separate compilation of program modules
- has improved control structure over PL/M
- conditional compilation
- compile time expression evaluation

Microcomputer Prototype Development System TWIN

The Microprocessor Prototype Development System is a modular system designed to support development and implementation of 2650 microcomputer systems.

A typical system consists of three hardware elements: a Prototype Development Computer (PDC), a floppy disk storage subsystem, and a system console (typically an ASR33 teletype). The PDC includes an integral MOS and bipolar PROM programmer and an in-circuit emulation/hardware debug facility. A wide range of PDC cards and system peripherals are available.

System software includes an Operating System, File Management, Debug Software, Text Editor, and 2650 Resident Assembler. These programs provide the user with the tools to perform his software development easily and quickly. These software capabilities, together with the capacity and performance of the floppy disk subsystem, and the in-circuit emulation/hardware debug capability significantly reduce the time and cost of a microcomputer system development project.

The Microprocessor Prototype Development System introduces a unique new Multiprocessor architecture for prototyping systems. This architecture provides users with the benefits of maximum availability of common (user) memory space and a Master processor/Operating System that is isolated and independent from the user system in the in-circuit emulation/hardware debug mode.

The Microprocessor Prototype Development System will have a long life cycle, since it is designed with the capability of supporting future microprocessors, additional peripherals and expanded software support and hardware debug capabilities.

Hardware features

Modular microprocessor prototype development system to support development, implementation and check out of 2650 microcomputer systems.

Powerful new Multiprocessor architecture provides maximum memory space to user and a protected environment for the Master processor/Operating System at all times.

The 2650 microprocessor –5 V only, fully TTL compatible, 2,4 µs cycle time, easy-to-learn instruction set – is used for the Master and Slave microprocessors.

Hardware interfaces and software drivers provided for floppy disk storage subsystem, TTY, CRT terminal, paper tape reader, line printer and EIA RS232 terminals.

In-circuit emulation/hardware debug and powerful debug software provides extensive emulation and diagnostic facilities for the user system.

Integral MOS and bipolar PROM programmers.

User/Common memory of 16k bytes, expandable to 64k bytes.

Two universal bus structures with multiprocessor and DMA capabilities.

Eight-level maskable priority interrupt system available to the user.

Software features

System software provided with the Prototype Development System includes the Signetics Disk Operating System (SDOS), text editor, debug package, 2650 assembler and linkage editor.

The Signetics Disk Operating System (SDOS) provides complete control over operation of all portions of the Prototype Development System. All functions relating to file handling, loading and execution are included, as well as provision for invoking the debug system and PROM programming functions.

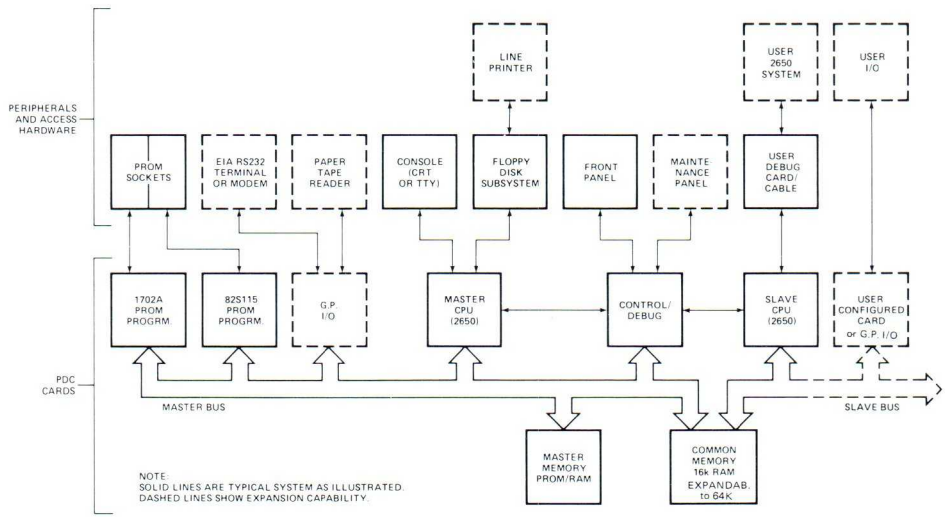
The SDOS software has been designed to allow the user to create, edit, and assemble files; obtain object and listing outputs; load and execute programs; and through the debug system, check out programs in a most efficient manner.

SDOS provides a powerful procedure capability which gives the user the capability of creating powerful and customized operating system commands dynamically.

Programs may be read and written in either hexadecimal or SMS (Signetics Memory Services) format for (P)ROM programming.

The SDOS software provides a flexible input/output system which is organized through logical channels allowing the user to dynamically assign any logical channel to any physical device or file within the system. Thus, system I/O devices may be dynamically assigned using SDOS commands either from the console or from within a user's program.

Typical system



SDOS assumes a dual CPU environment with one CPU designated as a master and the other as a slave. SDOS resides in a dedicated memory consisting of ¼k PROM and 16k of RAM running under the master CPU.

SDOS will control a multidrive floppy disk subsystem (up to 8 drives), a line printer, a high speed paper tape reader and an ASR-33TTY compatible console. Drivers are provided within SDOS for these I/O devices. In addition, the user may write his own driver for other peripheral devices and easily link them into the SDOS system.

The Prototype Development System Resident Assembler translates symbolic 2650 assembly language instructions into appropriate machine language code.

Microcomputer Prototype Development System (continued)

The Assembler produces absolute object code. The absolute object code produced is in hexadecimal format which may be converted by an SDOS command to SMS format for PROM or ROM programming.

The Text Editor is a comprehensive software package which allows the user to enter and modify text files. The Text Editor is line oriented and accepts inputs from an input file, performs modifications in a work space and outputs the revised text to an output file.

The Debug System is a software program which will provide the user with run-time program debug capabilities within a hardware environment. It utilizes special hardware features built into the program development system to control the execution of the user's program. User programs operating under the debug system will have dynamic program trace, breakpoint capabilities, memory modification capabilities, and status reporting on the memory, program, and internal processor status.

All of the above-described software will be supplied in object format on diskette and is provided with each Prototype Development System.

PDC cards

Master CPU
System Crystal Clock
Master 2650
UART/TTY Interface
Real Time Clock
Disk/Paper tape Port

Control/debug
Debug Logic
Master/Slave Interaction
Interrupt Logic
Front Panel Interface

Slave CPU
Slave 2650
User Cable Interface

Master memory
4k-Byte Static NMOS RAM
2k-Byte 1702A Erasable PROM

Common memory – 4k RAM
4k-Byte Static NMOS RAM

Common memory – 16k RAM
16k-Byte Dynamic NMOS RAM

General purpose I/O
EIA Interface
Four Output Ports
Four Input Ports
8 Interrupt Lines

1702 PROM programmer

82S115 PROM programmer

User configurable card
For interfacing directly with users own I/O devices.
Extender card

Peripherals

Floppy disk subsystem
Expandable to 8 drives

Line printer (optional)

High speed paper tape reader (optional)

Teletype (optional)

CRT terminal (optional)

A.C. power requirements
50 Hz or 60 Hz, 115/230 VAC

documentation

Technical manuals

2650 Microprocessor Manual (bound manual) – Contains the complete specifications for the 2650 microprocessor. Describes the instruction set, interface signals, the internal organization, and the electrical characteristics. Includes user guides to the 2650 Assembler Language and the 2650 Simulator.

2650 Registered Microprocessor Manual Set (loose-leaf) – Same as above with the addition of all Signetics microprocessor application memos with automatic updating service. Order No. 2650BM1000.

Signetics TWIN 2650 Assembly Language Manual – A user's guide to the 2650 Assembly Language for the TWIN Prototype Development System. Order No. TW09005000.

TWIN Operator's Guide – Describes all aspects of TWIN system operation, from unpacking, through switches and indicators, to the use of the various system development programs. Order No. TW09003000.

TWIN System Reference Manual – Describes each board in the TWIN system, with functional descriptions and a theory of operation at the block diagram level. A knowledge of microcomputer development systems and the 2650 microprocessor is assumed. Order No. TW09004000.

Designing with Microcomputers – An introductory text on microcomputer fundamentals for electronic circuit and system designers and managers.

Data sheets

TWIN Microcomputer Prototype Development System
PC1001 Microprocessor Prototyping Card
PC1500/KT9500 Adaptable Board Computer (ABC) Prototyping System
PC1600 Resident Assembler Board
PC2000 4k Memory Card
PC4000 Emulator Board for 2656
DS2000 Microprocessor Demonstration System
KT9100 Microprocessor Prototyping Kit
AS1000/1100 2650 Assembler Version 3.2
SM1000/1100 2650 Simulator Version 1.2
PL1000 Signetics Higher Level Language (PLμS)
2651 Programmable Communications Interface (PCI) Integrated Circuit
2652 Multi Protocol Communications Controller (MPCC) Integrated Circuit
2655 Programmable Peripheral Interface (PPI) Integrated Circuit
2656 System Memory Interface (SMI) Integrated Circuit

Brochure

Signetics TestWare Instrument (TWIN)

Application notes

no.	title	summary
AS50	Serial Input/Output	Describes how the Sense/Flag capability of the 2650 can be used for serial I/O interfaces.
AS51	Bit & Byte Testing Procedures	Describes several methods of testing the contents of the internal registers in the 2650.
AS52	General Delay Routines	Describes several ways of writing software time delay routines for the 2650, including formulae for calculating the delay time.
AS53	Binary Arithmetic Routines	Provides examples for processing binary arithmetic addition, subtraction, multiplication, and division with the 2650.
AS54	Conversion Routines	Describes routines for converting: Eight-bit unsigned binary to BCD Sixteen-bit signed binary to BCD Signed BCD to ASCII ASCII to BCD Hexadecimal to ASCII ASCII to Hexadecimal
AS55	Fixed Point Decimal Arithmetic Routines	Describes methods of performing addition, subtraction, multiplication and division of binary-coded-decimal (BCD) numbers with the 2650.
SP50	2650 Evaluation Printed Circuit Board (PC1001)	Provides a detailed description of the PC1001, an evaluation and design tool for the 2650.
SP51	2650 Demo System	Provides a detailed description of the Demo System, a hardware base for use with the 2650 CPU prototyping board (PC1001 or PC1500).
SP52	Support Software for use with the NCSS Timesharing System	Provides step-by-step procedures for generating, editing, assembling, punching, and simulating Signetics 2650 programs using the NCSS timesharing service.
SP53	Simulator, Version 1.2	Summarizes the features and characteristics inherent in version 1.2 of the 2650 simulator.
SP54	Support Software for use with the General Electric Mark III Timesharing System	Provides step-by-step procedures for generating, editing, assembling, simulating, and punching Signetics 2650 programs using General Electric's Mark III timesharing system.
SP55	The ABC 1500 Adaptable Board Computer	Describes the various components and applications of the ABC (Adaptable Board Computer) 1500 system development card.
SS50	PIPBUG	Provides a detailed description of PIPBUG, a monitor program designed for use with the 2650.
SS51	Absolute Object Format	Describes the absolute object code format for the 2650.
MP51	Initialization	Describes the procedures for initializing the 2650 microprocessor, memory, and I/O devices to their described initial states.
MP52	Low-Cost Clock Generator Circuits	Describes several clock generator circuits that may be used with the 2650. These circuits are standard TTL logic elements (7400 series). They include RC, LC and crystal oscillator types.
MP53	Address and Data Bus Interfacing Techniques	Provides several examples of interfacing the 2650 address and data buses with ROMs and RAMs, such as the 2608, 2606 and 2602.
MP54	2650 Input/Output Structures and Interfaces	Examines the use of the 2650s versatile set of I/O instructions and the interface between the 2650 and I/O ports. A number of application examples for both serial and parallel I/O are given.

courses

Microprocessor courses
A series of one, two and three-day courses have been arranged and will be given in Eindhoven, The Netherlands. They will cover all aspects of the Signetics 2650 MOS and 8X300 bipolar microprocessors. The course language will be English. Apart from these, local courses are also being held.

Description of the courses

Introduction to Microcomputers (1-day Course)
This basic course is intended for those engineers, salesmen, and managers who are not familiar with logic design. As a background, the course presents the developments that have made microprocessors possible and focuses on the advantages of microprocessor-based design and the trade-offs between microprocessor-based solutions and the more conventional ones. The use of microprocessors from three different viewpoints – design, marketing and production – is described and the course reviews the fundamental concepts of the development cycle.

Designing with Microprocessors (1-day Course)
This course has a two-fold objective. That of familiarization of engineers and programmers with microprocessor fundamentals, and demonstrating the application of Signetics 2650 microprocessors to system design. A real-life design problem – an intelligent typewriter system – is posed and solved. This design example also serves to illustrate the important differences between microprocessor and random logic techniques, and illustrates the simplicity of using the Signetics 2650 microprocessor.

2650 Intensive Workshop (3-day Course)
This intensive workshop of lectures and laboratory work is intended primarily for logic designers. Divided into several sections, the course describes the 2650 instruction repertoire including instruction formats and addressing, the software development cycle, interface requirements and the design of interface circuits. The objective of this course is to provide participants with the knowledge and experience necessary to apply the 2650 microprocessor to the solution of real-life design problems. Accordingly, practical work also assumes a major role in this course.

2650 System Design Workshop (3-day Course)
For those who have completed the three-day intensive workshop, or for those familiar with the 2650 but lack design experience, the workshop offers mainly practical work. Problem solving with a microcomputer system, standard hardware interfacing methods, hardware system design and the program development are all included. This is a course only for those with a good 2650 background, but lack experience in tackling a design problem. Taking both courses gives complete capability to produce one's own system designs.

TWIN System User Course (2-day Course)
This course is principally for engineers and programmers familiar with the 2650 microprocessor and its instruction repertoire. The course develops a practical understanding of Signetics TWIN Prototype Development System. This system includes a development computer, dual floppy disk unit, display terminal with keyboard, high speed printer and in-circuit emulator TWICE. Laboratory work enables participants to execute a hardware/software development cycle.

8X300 Intensive Workshop (2-day Course)
This course is intended for users of the bipolar 8X300 microprocessor and provides a theoretical and practical background to 8X300 hardware, software and interface circuits. Each participant has the personal use of an 8X300 system development computer for course work. Participants can gain the knowledge necessary for using the 8X300 to solve real-life design problems.

PLμS Course (3-day Course)
The PLμS course (Programming Language for Micro Systems) is an introduction to high level language programming for hardware-oriented designers. Trade-offs between high level and assembly languages are discussed, including basic concepts of high level language programming. High level language enables a designer to develop machine language code with less effort and fewer statements than with assembly language.

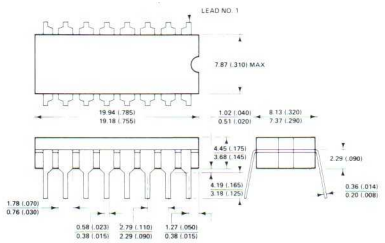
packages

The package types indicated in the technical data are listed in the table.
Packages D, E and P are not illustrated as their dimensions are similar to those of F, I and N, respectively.
Dimensions shown are mm with inches in parenthesis.

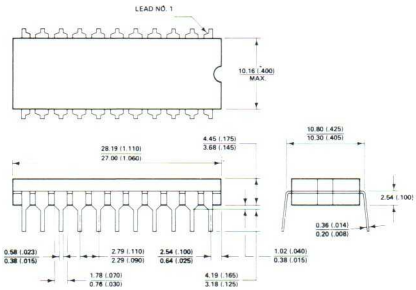
package type	construction	no. of pins
D	cerdip DIL	16
E	metal ceramic DIL	16, 18
F	cerdip DIL	16, 18, 22, 24
I	metal ceramic DIL	16, 18, 24, 28, 40, 50
K	metal can	10
N	plastic DIL	8, 14, 16, 20, 22, 24, 28, 40
P	plastic DIL	16
T	metal can	8
TA	metal can	8

packages

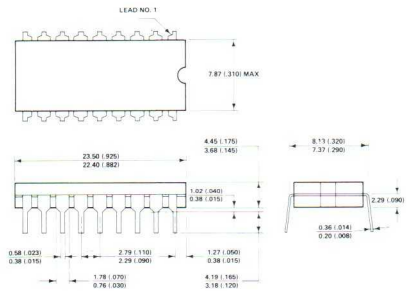
F package 16 pin



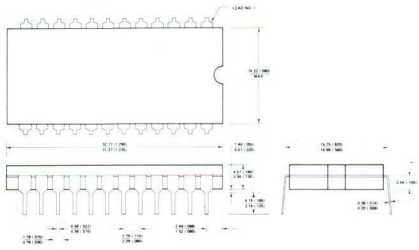
F package 22 pin



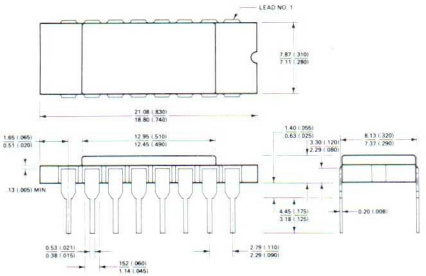
F package 18 pin



F package 24 pin



I package 16 pin



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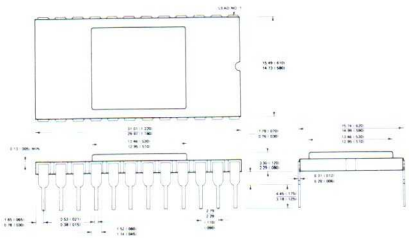
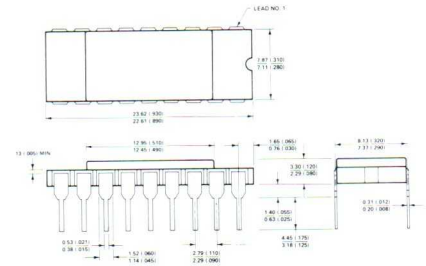
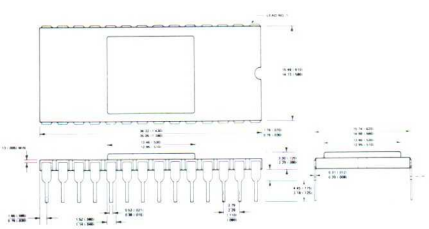


I package 18 pin

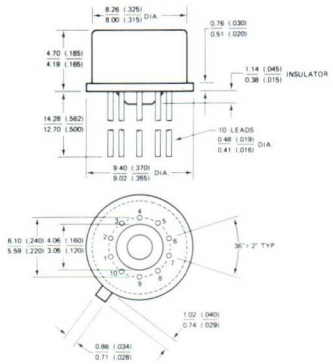


I package 28 pin

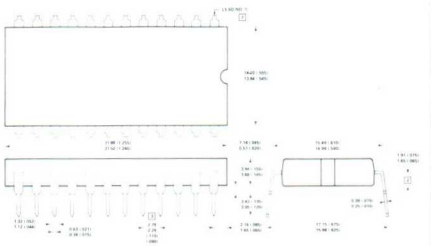


packages

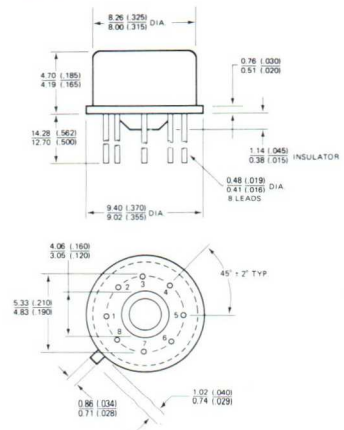
K package



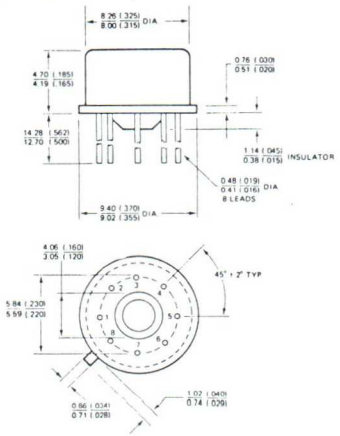
N package — 24 pin as an example



T package



TA package



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