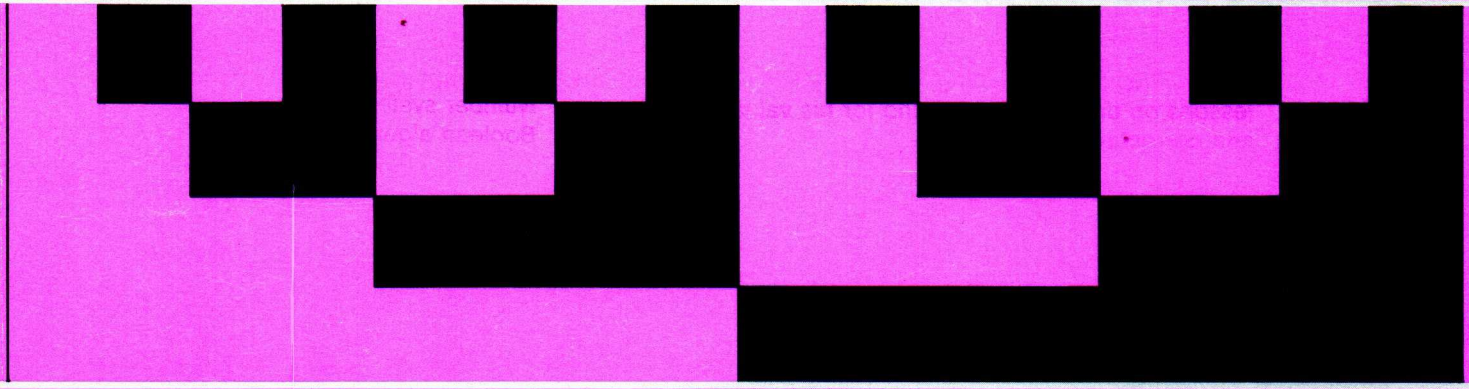
PHILIPS

digital instrument course

Part 2 DIGITAL COUNTERS AND TIMERS



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Second edition

The front cover shows the pattern of the BCD 1, 2, 4, 8 code and the 9-digit, 7-segment display of the Philips counter PM 6650.

DIGITAL INSTRUMENT COURSE

Part 2. Digital counters and timers

by A. J. Bouwens


PM 6613 universal counter 200MHz
PHILIPS
DISPLAY TIME
SENSITIVITY
100000000
520000000
999999999

Contents list

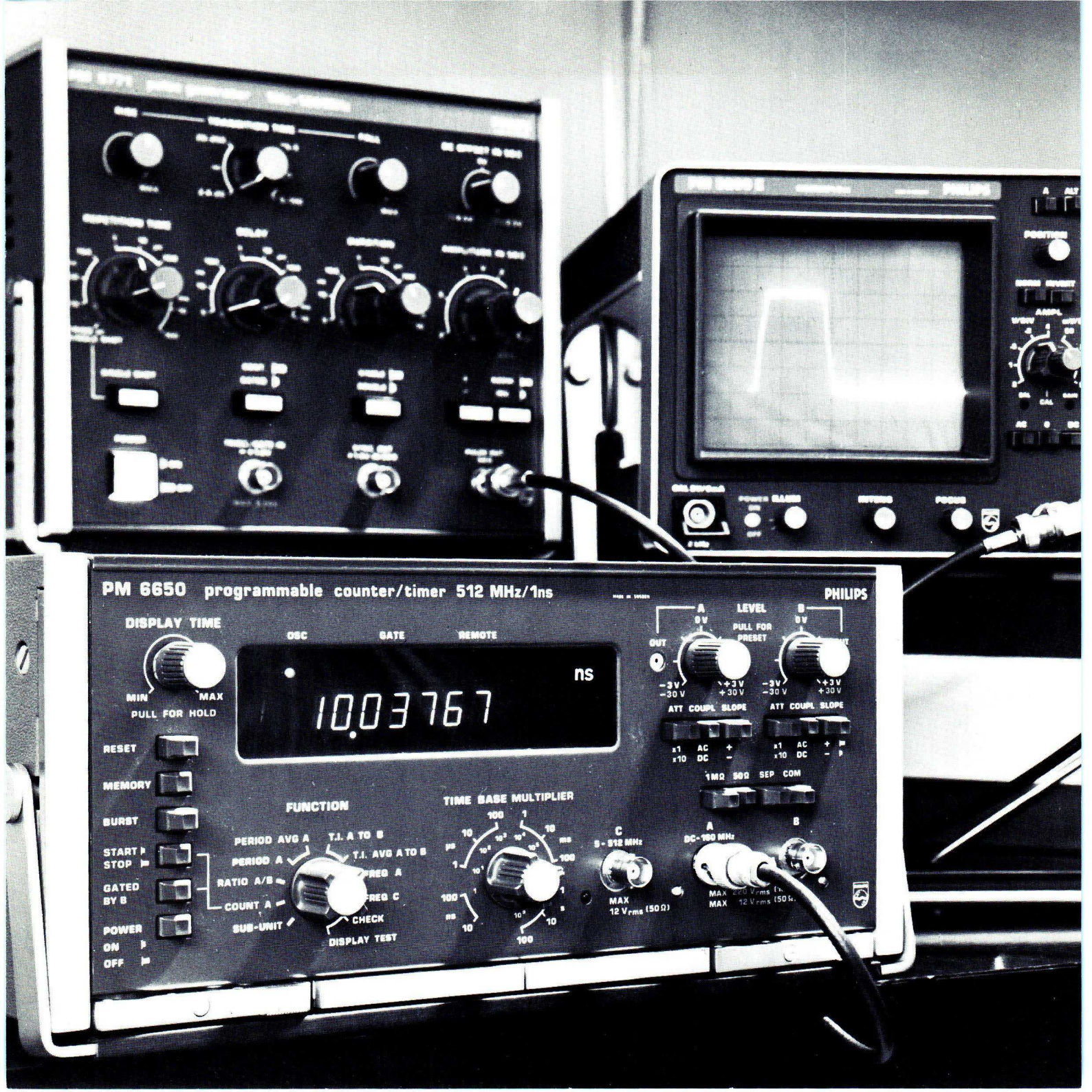

programmable counter/timer 512 MHz/1ns
DISPLAY TIME
470.25257
MHz
FUNCTION
TIME BASE MULTIPLIER
LEVEL
PERIOD AVG A
RATIO A/B
DISPLAY TEST

Foreword

With the aid of the theoretical knowledge of digital circuits gained in the first part of this course, we are now in a position to proceed to a discussion of electronic digital counters. Though digital counters have not been with us for very long, their introduction has caused a revolution in the electronic measuring world since they make it relatively simple to reach an accuracy that could only be realised under carefully standardized laboratory conditions in the old days.

The first generation of counters was introduced about 20 years ago. They were equipped with vacuum tubes and were thus bulky and heavy, and consumed a lot of power. The second generation was introduced in the early sixties and was considerably smaller, thanks to the use of transistorized circuitry. However, the basic specifications of the instruments remained more or less the same as for the tube versions.

The availability of digital integrated circuits at the end of the sixties led to the birth of the third generation, while further developments in integration (MOS circuits, where the whole circuitry of a digital counter can be contained on a single chip, large scale integration) are fostering the next generation, the first few members of which have already appeared on the market.


PM 6650 programmable counter/timer 512 MHz/1ns
PHILIPS
DISPLAY TIME
MIN
MAX
PULL FOR HOLD
OSC
GATE
REMOTE
ns
10.03767
RESET
MEMORY
BURST
START
STOP
GATED BY B
POWER
ON
OFF
FUNCTION
PERIOD AVG A
PERIOD A
RATIO A/B
COUNT A
SUB-UNIT
T.I. A TO B
T.I. AVG A TO B
FREQ A
FREQ C
CHECK
DISPLAY TEST
TIME BASE MULTIPLIER
C
5 - 512 MHz
MAX
12 Vrms (50Ω)
A
B
DC-100 MHz
A
LEVEL
B
OUT
0V
PULL FOR PRESET
−3V
−30 V
+3V
+30 V
ATT COUPL SLOPE
x1
x10
AC
DC
1MΩ 50Ω SEP COM

Chapter 1
Basic counter circuitry

The word counter in fact covers a wide variety of different modes of operation, such as the totalizing (counting) of input events, and the measurement of frequency, time, time interval or pulse width. Special counters can also average over a number of measurements, carry out simple computing operations, compare two signals, etc.

The basic counter functions will be discussed in this chapter, while the various modes of operation and other aspects of counter techniques will be dealt with in following chapters.

A counter contains 5 basic units (fig. 1.1.):

1. Input circuit
2. Main gate
3. Decimal counting unit (DCU) and display
4. Time-base circuit
5. Control circuit

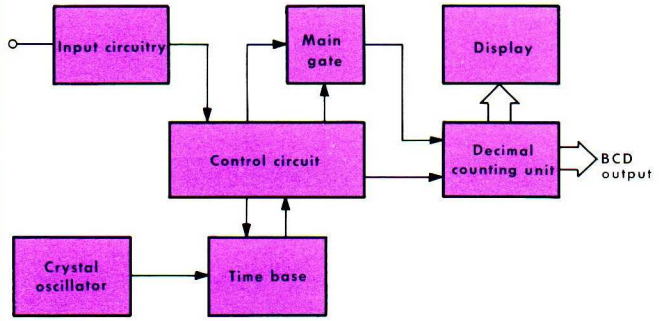


Fig. 1.1. Block diagram of a counter

Input circuitry

The input circuitry is mainly intended as a signal conditioner: it converts the (analog) signal to be counted (sine waves, pulses etc.) into a form compatible with the logic circuitry in the rest of the digital counter. In other words, it converts the signal into "1" 's and "0" 's.

Such an input channel consists mainly of the following stages:

- ☐ An AC/DC coupling circuit
- ☐ An input attenuator
- ☐ A voltage limiter for circuit protection
- ☐ An impedance converter with level adjustment (for the selection of the optimum trigger point).
- ☐ A Schmitt trigger, which converts the signal into logic pulses.

Fig. 1.2. shows the simplified circuit diagram of a typical input channel. The signal applied to the input is fed to the AC/DC switch. In the DC position the signal is passed on directly to the voltage divider (attenuator), and in the AC position via the coupling capacitor C_1. In this example the attenuator has three steps (e.g. x 100, x 10 and x 1).

As can be seen from the diagram, in the most sensitive position the input signal is fed directly via the series resistor to the input FET (which causes hardly any attenuation, because of its high input impedance).

Directly following the attenuator is the limiter circuit, consisting of the diodes D_{1-4}. This protects the input stage against overloading (negative or positive). Input voltages exceeding the Zener voltage of D_1 or D_2 are bypassed by these diodes. The input amplifier consists of two field-effect transistors, which convert the high input impedance into a low output impedance. The gate of TS_2 is connected to the level potentiometer, by means of

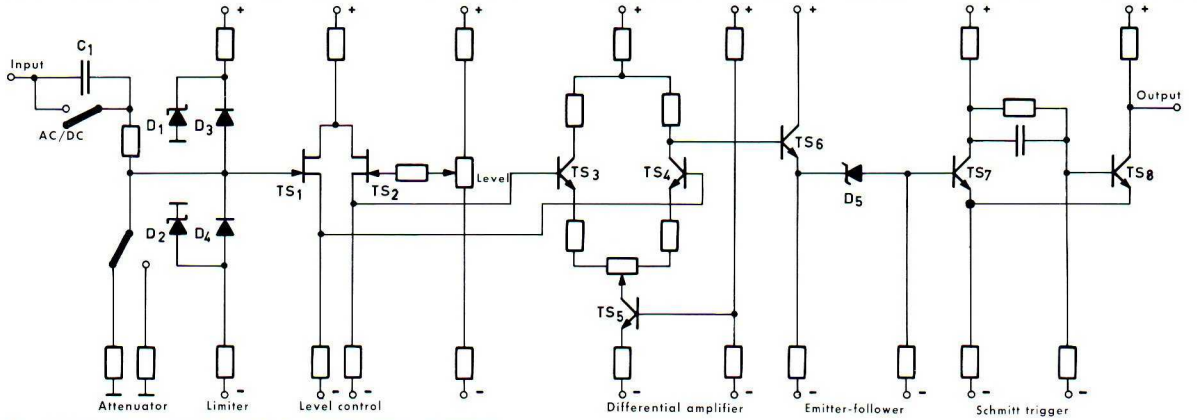


Fig. 1.2. Simplified circuit diagram of a typical input channel

which the trigger point may be shifted from positive voltages to negative ones, via zero. The signal from the input stage goes to the differential amplifier (TS_3 TS_4), the total emitter current being kept constant by the current source TS_5. The current distribution between the two transistors is made symmetrical by means of the potentiometer in the emitter leads. Because this total current is kept constant, a current increase in one transistor leads to a decrease in the other.

The output voltage of one of the transistors of the differential pair is fed via an emitter-follower (TS_6) and a Zener diode D_5 (to compensate for the differences in voltage level between the stages) to the Schmitt trigger (TS_7 TS_8).

A high voltage level at the input of the Schmitt trigger will make transistor TS_7 conducting. The base voltage of TS_8 will then drop, causing a lower level at the emitter of TS_7 which will therefore conduct even more. The Schmitt trigger will thus arrive at a stable position (a "1"), which will also appear at the output. When a low level is applied to the input the mechanism will work in the opposite direction, resulting in a low level at the output. The advantage of this circuit is that the levels of the two stable states "1" and "0" are more or less defined by the supply voltage. Proper selection of the supply voltages can thus make the output compatible with the logic levels used later on in the circuit.

An important property of the Schmitt trigger, the trigger hysteresis or the trigger window, determines the sensitivity of the counter to a certain extent and provides some noise immunity.

As can be seen from fig. 1.3a, when the amplitude of the input signal (shown here as a sine wave, though any waveform is possible) increases, the Schmitt trigger flops into a stable 1 position when the voltage reaches point A. A further increase in input amplitude does not change the output pulse at all. When the signal amplitude decreases again, the trigger does not switch over at point A' but (owing to the hysteresis) at point B (it takes a somewhat lower voltage to get the circuit working again). Similarly, the Schmitt trigger next switches over at C (not at B'), and so on. When however the amplitude of the signal applied to the Schmitt trigger is smaller than the trigger window so that the signal is contained entirely within the window nothing happens (left-hand waveform in fig. 1.3b).

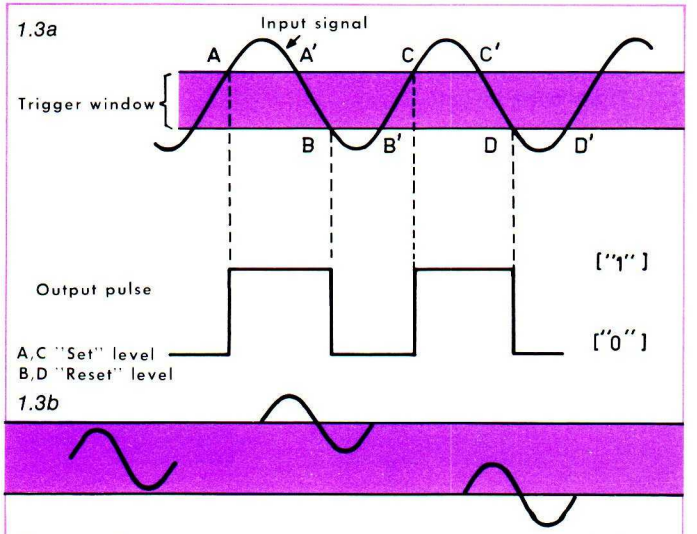
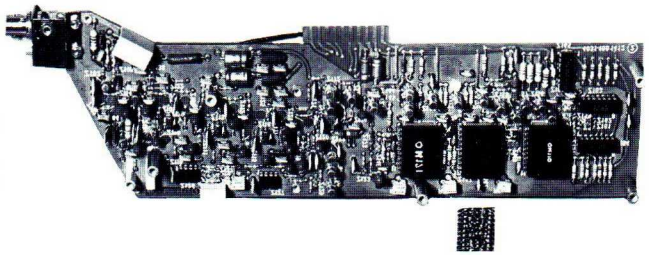


Fig. 1.3. Effect of trigger window on counter operation: when the input amplitude is large enough (1.3a), a correct output pulse train is produced, but when the input amplitude is too small (1.3b) no output pulses at all are produced.



Input channel of Philips VHF counter PM 6645

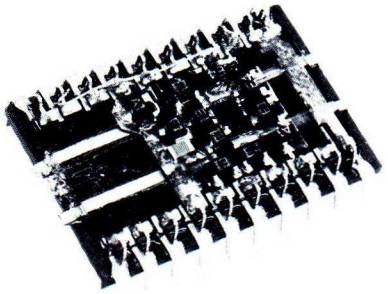
When a positive DC shift is applied to the signal (middle waveform), the Schmitt trigger will go high ("1") but will remain there, so no pulse appears at the output here either. Similarly with a negative DC shift the Schmitt trigger will stay low or go low ("0") and remain there, without delivering any pulses at the output.

We have assumed that the time the Schmitt trigger needed to pass to the "1" state or back to the "0" state was more or less infinitely small. In practice, however, it takes some time for the Schmitt trigger to change state. As the frequency of the input signal (or the repetition rate of the voltage changes) increases, a moment will come where the Schmitt trigger can no longer follow the input, for instance the input signal may start going up again while the Schmitt trigger is still tending to the "0" state; in this case some pulses will not be counted. It is therefore good practice to specify the pulse-pair resolution of a counter: this gives a clearer impression of the capabilities of the input circuitry than just stating the maximum input frequency.

Main gate

The signal conditioned in the input circuit is passed to the main gate, which is mostly a standard dual-input logic gate. One of its inputs is for the information signal while the other receives the gate control signal.

When the gate is turned "0N" the incoming pulses pass through the gate to the next stage the decimal counting unit. Just like the Schmitt trigger, the main gate also has a frequency limit beyond which it can no longer follow the input signal completely, so pulses can get lost here too. As at high frequencies, standard IC gates tend to be too slow; special circuits built with discrete components (mostly using thinfilm techniques) has been developed to solve this problem.



High-frequency main gate in thin-film technique

Decimal counting unit and display

The heart of the digital counter is the decimal counting unit (DCU), which usually consists of a number of counter decades in cascade. Each decade consists of five basic units: a decade counter, a memory, a BCD-to-decimal decoder, a numerical indicator driver (low-to-high-level converter) and the numerical indicator. This combination functions as follows.

The input signal is counted (see part 1 of this course, chapter 5) in the normal way* and as soon as the first counter goes from 9 back to 0 a carry (from flip-flop D) is presented to the next decade. This thus counts one for every ten input pulses (indicating the tens). Similarly the third decade register indicates the hundreds, the fourth the thousands, and so on.

When counting has finished, the various decades are steady and contain some BCD-coded information. As can be seen from fig. 1.4, each output of the decades is connected to one AND gate, which on its turn is connected to the input of a D-type flip-flop (memory). The other input of the AND gates, which are all in parallel, is connected to the transfer line. As long as the transfer line is LOW the AND gates are closed and nothing happens; when, however, the transfer line is made HIGH the information from the counting decades will be transferred to the D flip-flops (independent of the previous content of the memory). When the transfer line is made LOW again, the decade is disconnected from the memory and can start counting again after a reset pulse, while the memory retains the last information. When the next count is finished and the transfer pulse is given, only those memory flip-flops for which the new content differs from the old will change. The advantage of the use of the memory is a quite, steady display without continuous changing of digits. Furthermore, the off time of the counter decades can be kept short because part of the read (display) time is in the measuring time.

If it is desired to follow the instantaneous changes in the digits (e.g. for tuning a circuit to a certain frequency), the memory can be switched off and the transfer line made HIGH by means of a manual switch. The D flip-flops in the memory then follow the states of the various flip-flops in the decades continuously.

In most counters the outputs of the memory are (or can be) led to an output connector, giving a parallel BCD output which can be used e.g. for driving a digital printer.

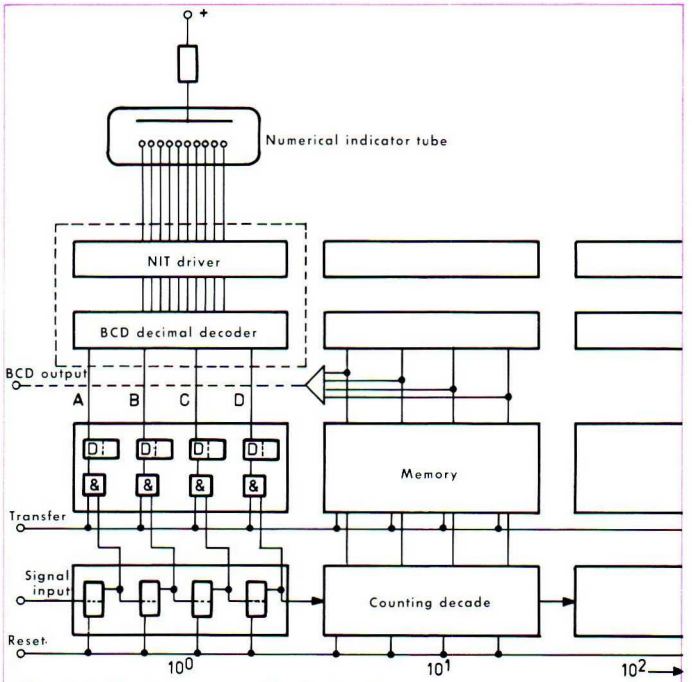


Fig. 1.4. Block diagram of a decimal counting unit and display.

When the BCD data are stored in the memory, the next step is the conversion to normal decimal information. As can be seen from fig. 1.4., the output of the D flip-flops is connected to the BCD-to-decimal converter, whose outputs are connected via the level converters in the drivers to the numerical indicator (NIT). In most instruments the decoder and the driver are combined in one integrated circuit.
In the above example use is made of a static display, i.e.

* For the sake of clarity, the special gates for the 9-to-0 jump have been omitted from the diagram (fig. 1.4.).

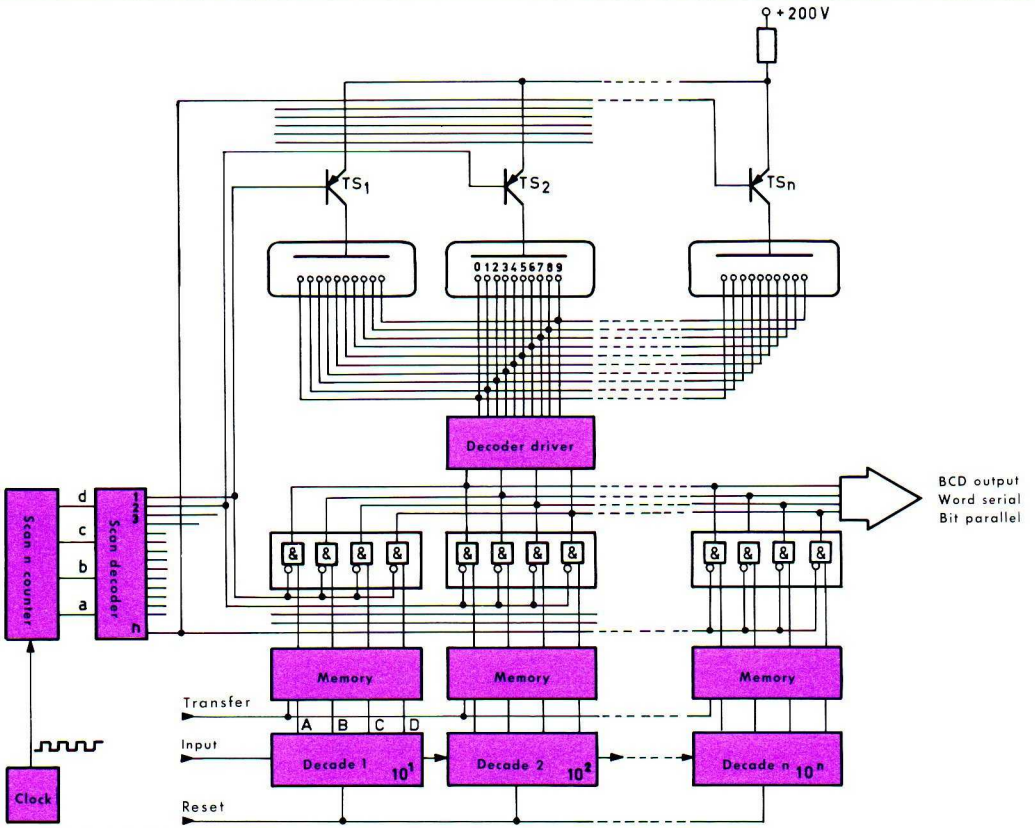


Fig. 1.5. Block diagram of a dynamic display. For symplicity only 3 decades are shown.

each indicator tube is connected via its own driver decoder to the appropriate memory flip-flop and decade. With e.g. the 9-digit counter, all 9 indicator tubes will display the appropriate figures at the same time.

In the dynamic display method, on the other hand, only one decoder driver is used and the indicator tubes display their contents one after the other. The speed of switching from one tube to the other is chosen so as to eliminate flickering. With e.g. a 9-digit counter, each digit is glowing only 11% (= 1/9) of the display time, resulting in a much lower brightness. This can however be compensated for by passing a higher current through the tube during the short time it is burning.

The display method has the advantage than only one (rather expensive) decoder driver is needed. However, some additional circuitry is needed to take care of the "scanning" of the various display tubes, which adds again to the cost of the circuit. It can be shown that for 3-5 digits the static method is the cheapest, while for 8 digits or more the dynamic method is best. The economic cross-point is somewhere around 6-7 digits.

A dynamic display functions as follows (fig. 1.5.):

Just as in the static display method, first the counter decades count the pulses, then the transfer pulse is given and the information contained in the counter decades is transferred to and stored in the memory.

As can be seen from fig. 1.5., each memory output is connected to an AND gate.

All A,B, C and D lines are then grouped together in "WIRED OR" logic and connected to the A, B, C and D inputs of one single decoder driver. The other input of each group of the 4 (decade) AND gates is connected via an invertor and a separate line to the scan decoder. The outputs of the decoder driver are connected to the numerical indicator tubes, the identical cathodes of which are also connected in parallel - so all the "1" 's, "2" 's, "6" 's and so on are "tied" together.

The anodes, however, are connected separately to the HIGH voltage via a transistor, and each transistor in its turn is connected to the above mentioned scan decoder, which is connected via a normal counter to a clock generator. If not more than 10 digits are to be displayed, a normal decade counter and BCD-to-decimal decoder can be used, while if more than 10 digits are needed special binary counters and decoders are necessary.

The scan counter drives the scan decoder. As soon as the first count is registered, output 1 of the decoder becomes LOW, the anode switch (TS_1) is closed and the four AND gates of the first decade are opened. The data in the memory are then transferred to the decoder driver (Note: all the AND gates of the other decades remain closed), the BCD data are decoded to the appropriate decimal digit and all the cathodes (n_1) corresponding to this digit are made LOW. However, only the cathode in the indicator tube of which the anode switch is closed (in our example the first tube) will light up and display the required number. After the next clock pulse the "1" line of the decoder will go HIGH again and line "2" will go LOW, initiating the operation described above for the second decade and so on until the data in the last decade (LSD) have been displayed. A new cycle starts immediately and the digits are continuously displayed.

The BCD information of the various decades present at the decoder/driver input can also be made available at an output connector. Since this information is presented in a serial mode, the information from the scan decoder must also be available at the output connector (directly or in order to save output lines also in BCD form), in order to indicate which decade a given decimal digit belongs to.

The clock-pulse frequency must be high enough to eliminate flicker. In dynamic display, the maximum pulse frequency is determined by the ignition delay and the time needed for the glow discharge to spread across the whole numeral. The duty cycle and the anode current pulses must be chosen to give good character brilliance.

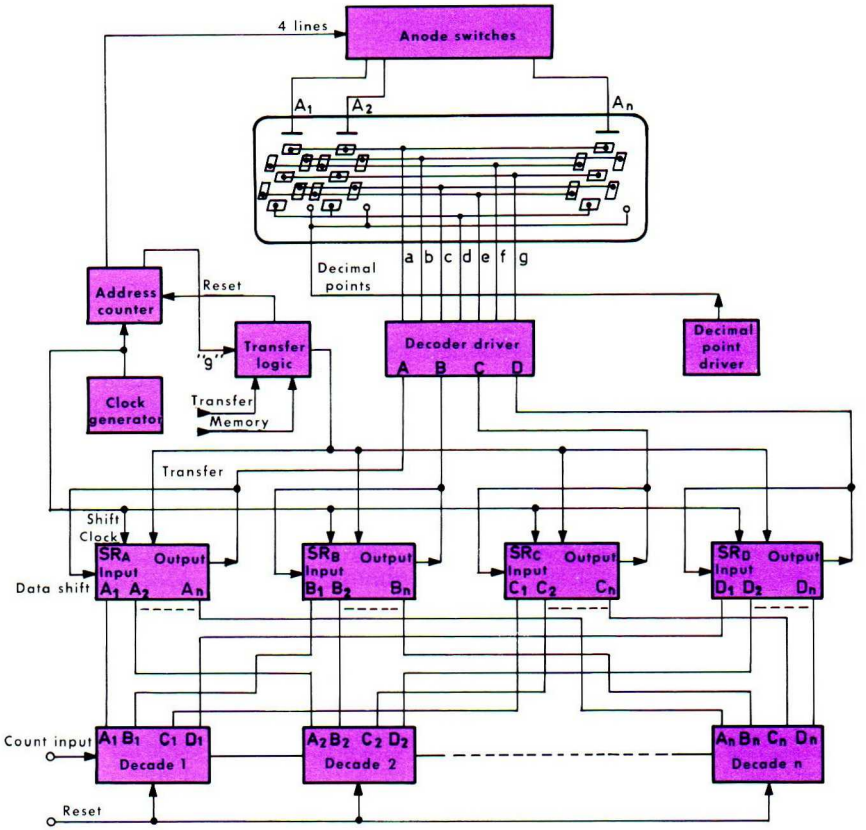


Fig. 1.6. Dynamic display with 7-segment PANDICON®

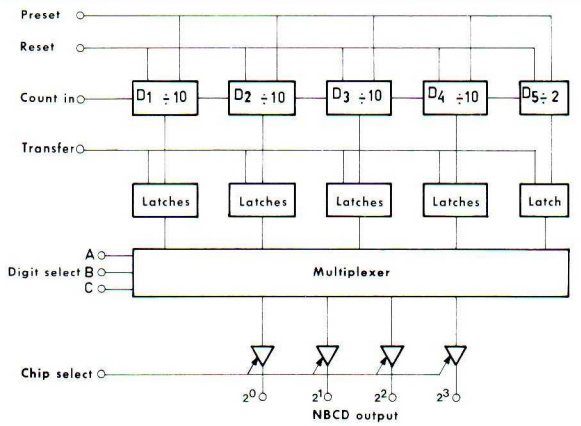


Fig. 1.7. Quad decade counter LSI.

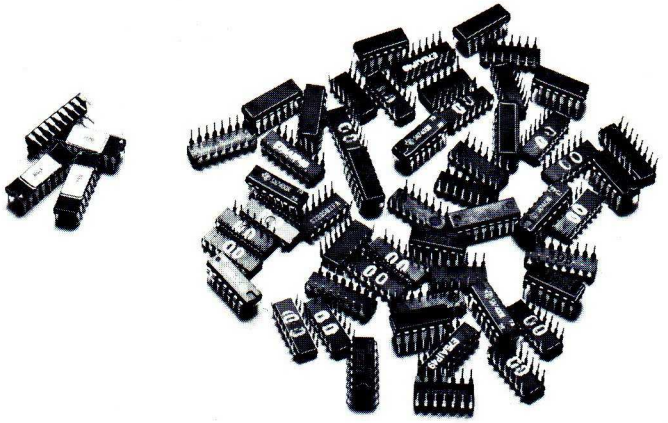


Fig. 1.8. Four LSI quad decades as used in the Philips PM 6610 series replace fifty two TTL integrated circuits!

In fact, the dynamic display system described above is more complicated than found in practice, in the interests of clear explanation of the display principe. The memory of a real dynamic display can generally be built up of 4-parallel n-bit shift-register chains. (The "4-parallel" refers to A, B, C and D data, and the n to the number of decades.)

The operation of such a system is as follows (fig. 1.6.):

When counting is finished the data are transferred to the shift register (memory) in the normal way. The decoder driver is connected directly to the output of the shift registers and the numeral belonging to the last decade is decoded and displayed. Then a shift pulse is given, the contents of the shift registers are shifted one step and the next last decade is displayed and so on. This process continues until the original contents of the shift registers are back where they started, and the next cycle can start. Alhough the data in the various registers are shifted round all the time, nothing is lost and the shift register retains its function as a memory.

In the example of fig. 1.6 a 7-segment multi-digit PANDICON^{R} is used. Dynamic display is the only possible method here, because - owing to the limited pin connections possible in one single envelope - all the cathodes of the same kind are tied together internally and connected to the outside world via one pin.

Modern counters like those of the Philips PM 6610 series use inhouse manufactured large - scale C-MOS integrated circuits wich drastically reduce the number and bulk of the digital components required. One such LSI is the Quad decade fig. 1.7. and fig. 1.8. which is used in the DCU and in the time-base circuitry.

Time-base circuitry

Basically a digital counter counts pulses, as its name would suggest. We have seen how the pulses are counted, stored and displayed in a modern counter. Indeed, the first electronic counters worked in much the same way in this respect. Modern counters, however, have many more facilities (measurement of frequency, time etc.).

Frequencies are measured basically by counting a number of input pulses during a precisely defined time interval. For example, if the main gate is kept open for exactly 1 second and the numbers of pulses counted is 12500, the frequency is 12500 Hz. Time intervals are measured by means of trains of pulses of exactly known frequency, which are counted accurately during the time that the main gate is kept open by control signals related to the time interval to be measured; for example, if the pulses to be counted have a pulse repetition frequency of 1 MHz (so the distance between pulses is 1 μs) and 7500 pulses are counted between the opening and closing of the main gate, the time interval measured is 7500 μs.

The various modes of operation will be discussed in greater detail in the next chapter; however, a few general remarks are in place here. It will be clear that for both frequency and time measurements a time reference of great accuracy and stability is needed. Furthermore it will be necessary - in order to have different opening times of the main gate and timing pulses with different repetition frequencies - to derive a number of other reference frequencies from this time reference.

Decade counters as applied in the DCU are therefore also used for scaling the reference frequency in steps of 10.

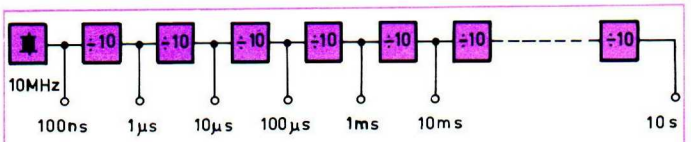


Fig. 1.9. Crystal oscillator and time-base divider

Most counters have a time-base range from 100 ns up to 10 sec in decade steps. The basic time reference is generally a very stable crystal (quartz) oscillator, which is followed by the above-mentioned decade scalers (fig. 1.9.).

No matter how well the associated circuitry is designed, the performance of this time standard is ultimately limited by the characteristics of the quartz oscillator. Two of these characteristics should be mentioned here.

a. Temperature stability

The resonant frequency of a crystal oscillator depends on the temperature. Around the "turning point" this temperature dependance has a parabolic form for the type of crystals used in digital counters (see fig. 1.10.). At the "turning point" temperature T, the temperature coefficient is zero. If, however, the crystal temperature varies by as little as 0. 1°C from the turning point the frequency can change by a factor of the order of 10^{-9}. For this reason, in high-quality counters the crystal oscillator is built into an oven with accurate proportional control. With this method frequency stabilities of the order of 10^{-10}/°C can be achieved. Another type of oscillator - used in cheaper digital counters - is the TXCO, where the frequency drift due to temperature variations is compensated by another temperature-dependent element in the circuit which drives the frequency in the opposite direction.

The average temperature stability possible with a TXCO (temperature compensated crystal oscillator) is of the order of 5×10^{-8}/°C.

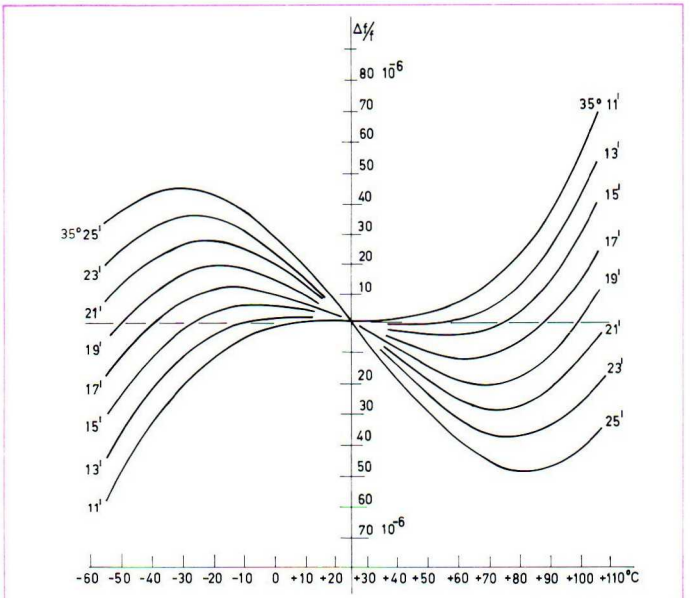


Fig.1.10. The relationship between crystal temperature and frequency

b. Aging of long-term stability

The aging of a crystal oscillator is generally taken to refer to the average trend in the value of the output frequency as a function of time. This trend depends strongly on the type of crystal, its age and the operating conditions. High-quality crystal oscillators have an aging of the order of 10^{-9} per 24 hours, while lower-quality ones are 10 to 100 times worse. Of course the aging can always be compensated for by means of a simple trimmer and a good frequency standard. This process, which must be carried out at sufficiently frequent intervals, is called recalibration of the crystal.

(See also chapter 4 on the accuracy of crystal oscillators).

The control circuit

This can be regarded as the "brain" of the counter. Depending on the operating mode, various commands are given automatically, manually or by remote control. During a measuring cycle the operating conditions must be controlled in such a way that the measuring process can proceed without disturbance. The control circuit exercises the following functions:

— control of the main gate
— generation of the reset pulses for the counting decades and the time-base dividers
— control of the main-gate signal lamp
— control of the display time
— generation of the memory transfer pulse
— generation of the clock pulses needed for a dynamic display
— control of printer or other device which may be connected to the BCD output.

As the precise way in which these functions are performed depends on the measuring mode involved, further details about the control circuit will be left till the next chapter.

Questions

Q.1.1. The trigger window of the input circuit of a digital counter is decreased by a factor of 4. This will increase the input sensitivity of the counter

A. By a factor of 4
B. By a factor of 2
or decrease the sensitivity
C. By a factor of 4

A	
B	
C	

Q.1.2. The main gate in a medium-frequency counter is

A. An AND gate
B. An OR gate
C. Could be either

A	
B	
C	

Q.1.3. In a multi-digit display tube like the PANDICON[R], the display system is

A. Dynamic
B. Static
C. Could be either

A	
B	
C	

Q.1.4. The memory in a digital counter is built in

A. To drive a printer
B. For convenient operation
C. To improve the accuracy

A	
B	
C	

Q.1.5. The maximum counting speed of the decimal counting unit is determined by

A. The first decade
(seen from the input)
B. All decades
C. The main gate only

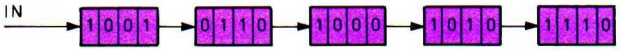
A	
B	
C	

Q.1.6. In a decimal counter the memory transfer pulse is given

A. Before
B. After
C. At the same moment as the decade counter reset pulse

A	
B	
C	

Q.1.7. The varous flip-flops of a 5-digit DCU are in the states shown below.

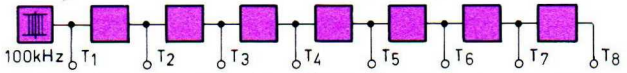


The display driven by this DCU will show the following decimal number:

A. 74896
B. 75169
C. 96157

A	
B	
C	

Q.1.8. The time references at outputs T_1, T_5 and T_8 of the time-base divider shown below are:



A. $T_1 = 10\ \mu s$ C. $T_1 = 10\ \mu s$
$T_5 = 10$ ms $T_5 = 100$ ms
$T_8 = 10$ s $T = 1$ s
B. $T_5 = 10\ \mu s$
$T_5 = 100$ ms
$T_8 = 100$ s

A	
B	
C	

Q.1.9. An accuracy of 10^{-7} is required of a digital counter with a crystal oscillator having an aging rate of $3 \times 10^{-9}/24$ hours. The crystal oscillator should then be recalibrated once a

A. Week
B. Month
C. Year

A	
B	
C	

Q.1.10. When the transfer pulse input fig. 1.4. of a DCU is kept HIGH continuously during counting, the display will

A. Show only zeros
B. Show only zeros until the reset pulse is given
C. Follow the counting continuously

A	
B	
C	


PM 6645 frequency counter 30 Hz - 512 MHz
PHILIPS
PM 6634 frequency converter 1-12.6 GHz
03.03 7421
GHz
DISPLAY TIME
FREQUENCY PRESET
03,0 GHz
INPUT A

Chapter 2
Modes of operation

As we mentioned in the previous chapter, electronic counters can perform various different functions, such as totalizing (counting) of input events, measurements of frequency or time, time averaging and so on. Not all counters will have all these modes; the choice depends mainly on the price or application area.

The most obvious operating mode is of course:

Totalizing (or counting) of (electrical) input events.
The functioning of the counter in this mode is quite simple, as can easily be seen from the block diagram of fig. 2.1. After being shaped by the input circuit, the input pulses pass through the main gate (which is simply an ON/OFF switch in this case) to the decimal counting unit. The control unit realises the necessary circuit connections and at the same time sets the transfer line in the display section to HIGH, to ensure that the counted events are displayed directly.

The counter is generally started and stopped with a simple two-position switch (for manual control) or with a start-stop pulse when the instrument is remote-controlled.

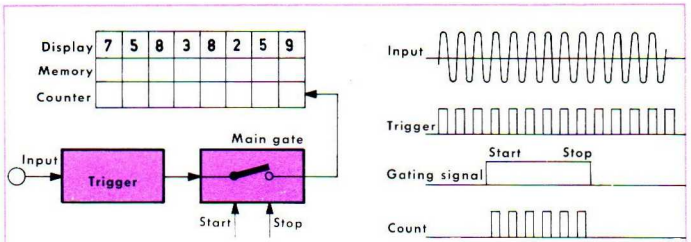


Fig. 2.1. Simplified block diagram and signal flow for the totalizing mode

Frequency measurements
As frequency is defined as "the number of events per time interval", the only thing we have to do to make a frequency meter from our totalizer is to keep the main-gate switch closed during a precisely known time interval.

For example, if the switch is closed for 1 second the frequency is displayed in Hz, while if it is closed for 1 ms the frequency is given in kHz. Of course, this reference time interval must be very accurately determined.
This is done with a crystal oscillator (described in the previous chapter, where we also saw how the various time references can be derived from the crystal oscillator by means of decimal dividers). The functioning of the counter in this measuring mode is illustrated in fig. 2.2.

Of course, quite a lot of switching and programming is required to set the instrument in this mode; the function of the control circuit in this connection has already been discussed in the previous chapter.

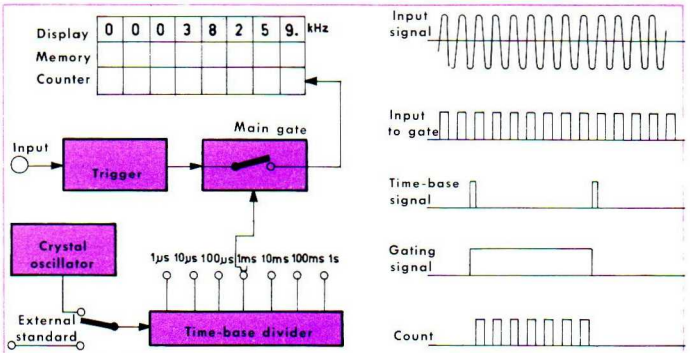


Fig. 2.2. Simpliifed block diagram and signal flow for the frequency mode

The operation of the control circuit is as follows (see fig. 2.3.).

When the instrument is switched to the FREQUENCY mode, input ① of gate I is made HIGH, so the reference pulses from the time-base generator ② can pass AND gate I. The output signal from this gate ③ is fed to the clock input of the D flip-flop A (main-gate flip-flop); as $D = \overline{Q}_A = 1$ flip-flop A will switch over, making $\overline{Q}_A$ low. The output $\overline{Q}_A$ ④ is fed to the inhibit input of the main gate (MG), thus causing the latter to pass the input signals of the decade counters which will go on counting until the main gate is closed again on arrival of the next clock pulse (T_2) (which causes flip-flop A to toggle again). The measuring time T_m is finished now and the next part of the programme is the display time. When flip-flop A returns to its initial state, a positive edge ④ is presented to the clock input of D flip-flop B (the display flip-flop) which will toggle, making $\overline{Q}_B$ low. The output of the display flip-flop is fed via the pulse shaper PS to the transfer gate (IV) (a NAND gate), closing the latter and giving a positive pulse at the output ⑦. This positive transfer pulse ensures that the information stored in the counting decades is shifted into the memory (see fig. 1.5.); after processing of these data (decoding and level converting) the appropriate numerals in the display unit are lit up. At the same time as $\overline{Q}_B$ is going LOW, the display multivibrator (MV) is started and produces a ramp ⑧, the slope of which (and hence the time required to reach the switch-over point) is determined by the display-time potentiometer. When the display multivibrator reaches the switch-over point (time T_3 in fig. 2.3.) a negative-going pulse is produced and initiates quite a number of operations. First of all, gate V is closed, giving a positive-going output pulse ⑨ which resets the decade counters to zero; secondly the display flip-flop (B) is reset again; and finally the output of NAND gate VI ⑩ goes LOW (after being HIGH during the display time, for presetting of the time-base dividers) and via the invertor VII making output ⑪ HIGH and actuating the RESET input of the main-gate flip-flop A.

The reason for the last two control operations is as follows.

As we can see from the pulse diagram, the complete timing sequence during the measuring and display periods is governed by the time-base generator. If we now assume (worst case) that the time-base interval (T_1-T_2) is 10 seconds and the display time is e.g. 1 second then we will have to wait nearly 9 seconds before a new sequence starts again, because the time-base divider will have to go to full dividing range before it gives a new timing pulse. If however we apply a preset pulse to the time-base dividers during the display time in such a way that all time-base decades are set to 9 (BCD 1001), then directly after the display time is finished, the next pulse from the crystal oscillator (which has a repetition period of e.g. 1 μs) will set all dividers to 0 (= 10) and the first clock pulse T_1 will be delivered, in other words a new measurement can start directly after the display time is finished.

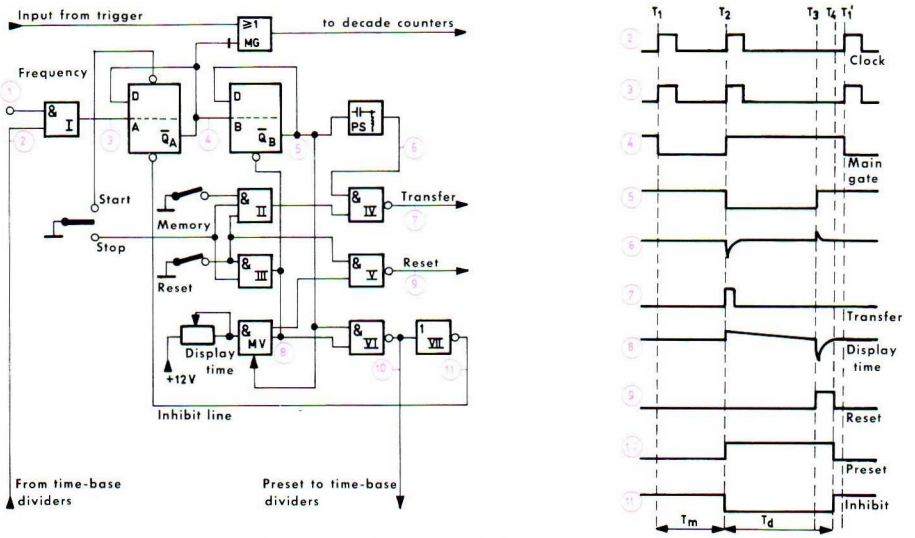


Fig. 2.3. Simplified block diagram and signal flow for the control circuit

On the other hand, when the time interval between the clock pulses (T_1-T_2) is shorter than the display time a new measuring cycle can never start before the display time is finished, because the time-base dividers are constantly preset to 9 so no time-base pulses can be generated. In order to prevent unwanted setting of the main-gate flip-flop (resulting in opening of the main gate) an inhibiting signal ⑪ is applied to the RESET input of the main-gate flip-flop, keeping the latter in the "0" position.

As can be seen from fig. 2.3, closing the MEMORY switch makes the output of gate II LOW so that the output of gate IV ⑦ goes HIGH, making the transfer line HIGH too, so the display follows the counting continuously.

When the RESET button is depressed, the output of AND gate III goes to LOW, reset pulses are applied to the decade counters and to flip-flop B, a preset pulse is applied to the time-base dividers and a transfer pulse is produced.

The circuit of fig. 2.3. can also operate in the TOTALIZING mode. When the instrument is in this mode, input ① is LOW (because it is NOT FREQUENCY), and pushing the START/STOP switch to START causes flip-flop A to toggle so that the main gate is opened. Switching to STOP at the end of the measuring cycle gives the normal sequence of reset signals, as can easily be seen from the figure.

Another point we must mention is the position of the decimal point. In most counters a decimal point is placed between each pair of digits and the appropriate one is lit up depending on the positions of the time-base and measuring-mode switches. For example, if the time-base output is 1 kHz, so the time between the clock pulses is 1 ms, the LSD (least significant digit, i.e. the one on the right) represents kHz, the second digit from the right represents tens of kHz and so on.

If the dimension indicator is also set to "kHz", everything is now all right (see fig. 2.2). However, if the time-base switch is moved one step back, the clock pulses follow each other every 10 ms which means that the LSD is now indicating steps of 100 Hz. If the dimension indicator is still set to "kHz" we have to move the decimal point one place to the left so that it now lies between the first and second digits (from the right), i.e. at DP1. Table 2.1. illustrates a possible relation between the time-base frequency and the position of the decimal point.

Any one of the time-base settings (ranging from 1 μs to 1 s in our example) can be used. Readings are given in Hz, kHz or MHz. The time-base setting is generally chosen to give the best resolution. If e.g. a frequency just above 2 MHz has to be measured, a 1 μs time base would give a reading of 2 MHz while a 1 ms measuring time might give a reading of 2345 kHz and a 1 s time base a reading of 2345678 Hz. The last of these settings offers the highest resolution (1 Hz), and is generally the one that will be chosen.

Time-base	DP 2	DP 1	DP 0	Dimension
1 μs			x	MHz
10 μs		x		MHz
100 μs	x			MHz
1 ms			x	kHz
10 ms		x		kHz
100 ms	x			kHz
1 s			x	Hz

Table 2.1. Decimal point settings in the frequency mode

In the above example we have been using the internal 1 MHz crystal oscillator as time reference. It is also possible (e.g. if one wants to have a higher precision of the time reference) to use an external frequency (time) standard. This external standard should preferably have the same frequency as the instrument's internal clock because decimal points and the setting of the dimension indicator are based on that. If the external and internal clock frequencies are not equal one must carry out some calculations to find the proper frequency. If the ratio is 10 (or powers of 10) one only has to shift the decimal point one or more places; however, other factors can make the calculations more difficult.

Frequency-ratio measurements

This measuring mode provides a simple means of comparing two frequencies. In fact, this mode is nothing but the FREQUENCY mode with the internal crystal oscillator switched off (as in the EXT. STANDARD setting) and with a second input channel provided to feed a signal of the appropriate shape to the time-base divider chain (fig. 2.4.).

When the time-base switch is in position 1 (corresponding to 1 μs in the frequency mode) the signal from input B is not divided at all and one measures the ratio between A and B directly. (Because the ratio of two frequencies is dimensionless, no dimension is indicated in the display.) This direct comparison method has however the disadvantage that when the two frequencies are very close to one another the accuracy of the measurement becomes rather low. For instance if we compare 1 MHz (F1) with 200 kHz (F2) the main gate is open for 5 μs and 5 pulses are counted; a 5 is thus displayed Since - as we shall see later - there is always an uncertainty of 1 digit in digital instruments, the real ratio could be either 4 or 6, giving a possible error of 20%. If we shift the time-base selector one place to the right, frequency F2 is divided by 10 and the main gate is opened 10 times longer resulting in a display of 50; with the same uncertainty of $\pm$ 1 digit, this already improves the accuracy by a factor of 10 (2% instead of 20%). We can improve the accuracy still further by switching in more time-base dividers. In order to ensure that the decimal point is in the right position in the display, the latter is often automatically shifted together with the time-base divider. The relation between the positions of the decimal point (DP) and the time-base divider in our

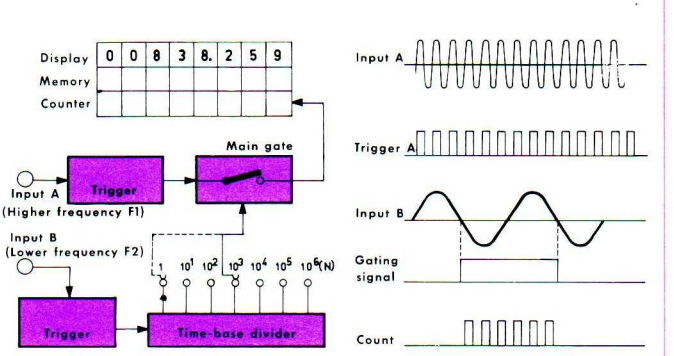


Fig. 2.4. Simplified block diagram and signal flow for the frequency-ratio mode

Time base	Factor	DP 6	DP 5	DP 4	DP 3	DP 2	DP 1	DP 0
1 μs	1							x
10 μs	10						x	
100 μs	10^2					x		
1 ms	10^3				x			
10 ms	10^4			x				
100 ms	10^5		x					
1 s	10^6	x						

Table 2.2. Decimal point settings in the frequency-ratio mode

Period measurements

a. *Measuring single periods*

As we have seen in the previous paragraph, if one wants to have a high resolution when measuring frequencies the gate time must be made as long as possible.

For example a resolution of 1 ppm with a frequency of the order of 1 MHz can be obtained with a gate time of 1 second (LSD is in Hz); at a frequency of the order of 1 kHz, the gate time required will be 1000 seconds (LSD is in mHz) which is already becoming unduly long. If a 1 Hz signal should have to be measured with this resolution (1 μHz) the gate time would have to be a million seconds or more than 10 full days, which is of course completely impractical for measuring purposes.

Fortunately we have another way of measuring these lower frequencies with high resolution in a relative short time: by PERIOD MODE measurements.

As the period of a signal (T) is the reciprocal of its frequency (F = 1/T), period measurements may thus be expected to bear a similar inverse relationship to frequency measurements. And as shown in fig. 2.5. the period mode is indeed essentially the inverse of the frequency mode, as a result of reversal of the main-gate inputs.

In the period mode the signal to be measured is fed to the input amplifier after the trigger level and polarity have been determined (see chapter 1). After being processed in this stage it passes to the main-gate control input where it determines how long the gate will be open. The first trigger pulse opens the main gate, the next one closes it. The time-base signal is fed to the signal input of the main-gate. The gate output therefore consists of timing pulses representing the measured signal's period time. If for instance the signal to be measured has a frequency of 20 kHz (period 50 μs) and the reference signal is 1 μs, the main-gate will be open for 50 μs and in this time 50 timing pulses will pass the main gate. These 50 pulses are then processed by the DCU to provide a display of 50 (μs).

If we now want to have - as in the above example - a resolution of 1 ppm for a frequency of 1 Hz we switch the time-base selector to 1 MHz thus giving 1 μs timing pulses.

Feeding the 1 Hz signal to the main gate opens this gate for 1 s, during which time $\frac{1}{10^{-6}} = 10^6$ pulses will pass and the display will show 1000000 (μs). In other words, we now have the desired resolution of 1 ppm with a measuring time of only 1 s. A disadvantage of this method is however that the reading is not in Hz but in seconds so one has to carry out a small calculation in order to find the frequency.

As in the other measuring modes, the position of the decimal point and the selected time-base frequency are also related, as shown for our example in the table 2.3:

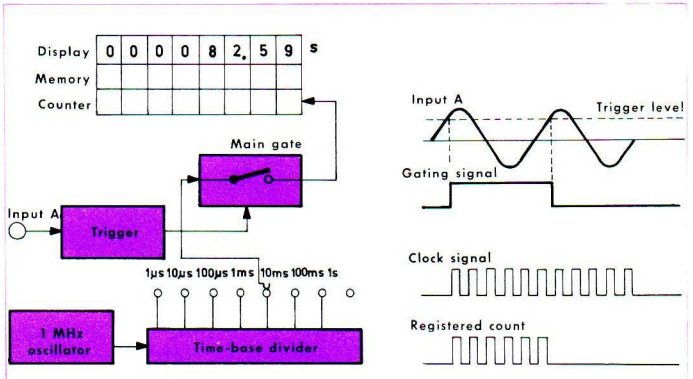


Fig. 2.5. Simplified bock diagram and signal flow for the single period mode

Time-base setting	DP_2	DP_1	DP_0	Dimension
1 μs			x	μs
10 μs	x			ms
100 μs		x		ms
1 ms			x	ms
10 ms	x			s
100 ms		x		s
1 s			x	s

Table 2.3. Decimal point settings in the period mode

There is of course also a limit to the increase in resolution in the PERIOD mode, since higher resolution demands a higher frequency of the timing signals, which is limited by the frequency range of the main-gate and first DCU decades. For example, a 1 MHz counter can never have a higher resolution than 1 μs; a 100 MHz counter never better than 10 ns.

b. *Multiple period measurements*

As we have seen, the single-period mode permits relatively fast measurements on low-frequency phenomena with high resolution. However, the disadvantage of this measuring mode is that the accuracy can be rather poor (chapter 4 will deal in more detail with accuracies in digital frequency and time measurements). It is therefore often desirable to average the reading over a number of periods in order to achieve a better accuracy and even better resolution as well. This is done in the multiple-period or period-averaging mode.

The simplified block diagram for this mode is given in fig. 2.6.: just as in the single-period mode,the input signal is processed and trigger pulses are derived in the input stage. However, the trigger pulses are no longer fed directly to the main-gate control circuit but are applied to the input of the time-base divider chain. The main gate is opened by the first trigger from the divider and remains open until the preset number of pulses (in our example 1000) have passed through the time-base divider and the closing pulse is delivered. The total count, which is 1000 times greater than in the single-period mode, is then displayed. But as we want to read the exact time of one single period we have to divide the reading by 1000 (in our example) which can be easily done by shifting the decimal point three places to the left. The relation between time-base setting and the position of the decimal point is given in the table 2.4.

It can be clearly seen from this table that e.g. in the 10^6 setting the resolution is also drastically improved and is coming into the picosecond range. There are of course limitations here too, as we shall see in the chapter on digital accuracies.

The larger the number of periods over which averaging is performed, the better the results of the measurement. However, we must take care not to exceed the display capacity. (E.g. an 8-digit counter has a maximum display of 99999999, in other words 10^9 counts give overflow.) We should realize that averaging over a large number of periods makes the measuring time long again, so one of the advantages of the (single-) period mode is lost (e.g. averaging a 100 Hz signal over 10^6 periods means a measuring time of 10^4 seconds).

As we can see from the block diagram the frequency counted is always 1 MHz because we are using the time-base divider for other purposes. In many counter-timers nowadays, the time-base divider is therefore split in two groups. For instance, in an 8-decade divider the first four decades are connected to the crystal oscillator and the last four are used for signal averaging. In this arrangement one can then select five clock frequencies and have five averaging modes (1-10^4 periods). The advantage of this arrangement is that when one wants to have a high averaging mode(for accuracy requirements) but the counter capacity is limited to e.g. 8 decades, one can select a clock frequency which eliminates the risk of overflow. The following example will clarify this:

Given a signal of 1 Hz, clock frequency 1 MHz, averaging periods 10^4, the total number of counts is $10^4 \cdot 10^6 = 10^{10}$ pulses, which exceeds the capacity of the 8-decade counter. However, changing the clock frequency to 10 kHz gives a total count of 10^8 which is well within the capacity of the 8-digit counter while the averaging is still performed over 10^4 periods.

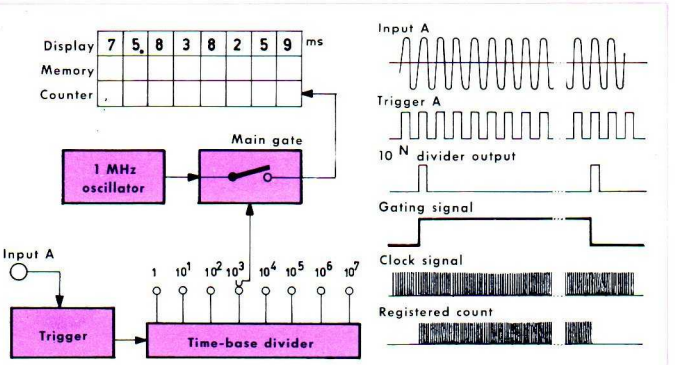


Fig. 2.6. Simplified block diagram and signal flow for the multiple-period mode

Time-base setting	Dividing factor	DP_6	DP_5	DP_4	Dimension
1 μs	1	x			s
10 μs	10			x	ms
100 μs	10^2		x		ms
1 ms	10^3	x			ms
10 ms	10^4			x	μs
100 ms	10^5		x		μs
1 s	10^6	x			μs

Table 2.4. Decimal point settings in the multiple-period mode

Time-interval measurements

a. *Single mode*

In the measuring modes we have just discussed, we measure the time between two identical points on a waveform. However, if we want to measure the time between two different points on a waveform or between two points on two different signals we need two separate input channels, each with its own circuits for trigger level, polarity etc.

The resulting measuring mode (time-interval mode) can be considered as a combination of the totalizing (START/STOP) and PERIOD modes. As in the totalizing mode, the main-gate is opened and closed with a START/STOP signal (however, no longer with a simple switch but by means of input amplifiers of the kind used in the PERIOD mode). The resemblance with the PERIOD mode is that the clock pulses counted are again derived from the crystal oscillator.

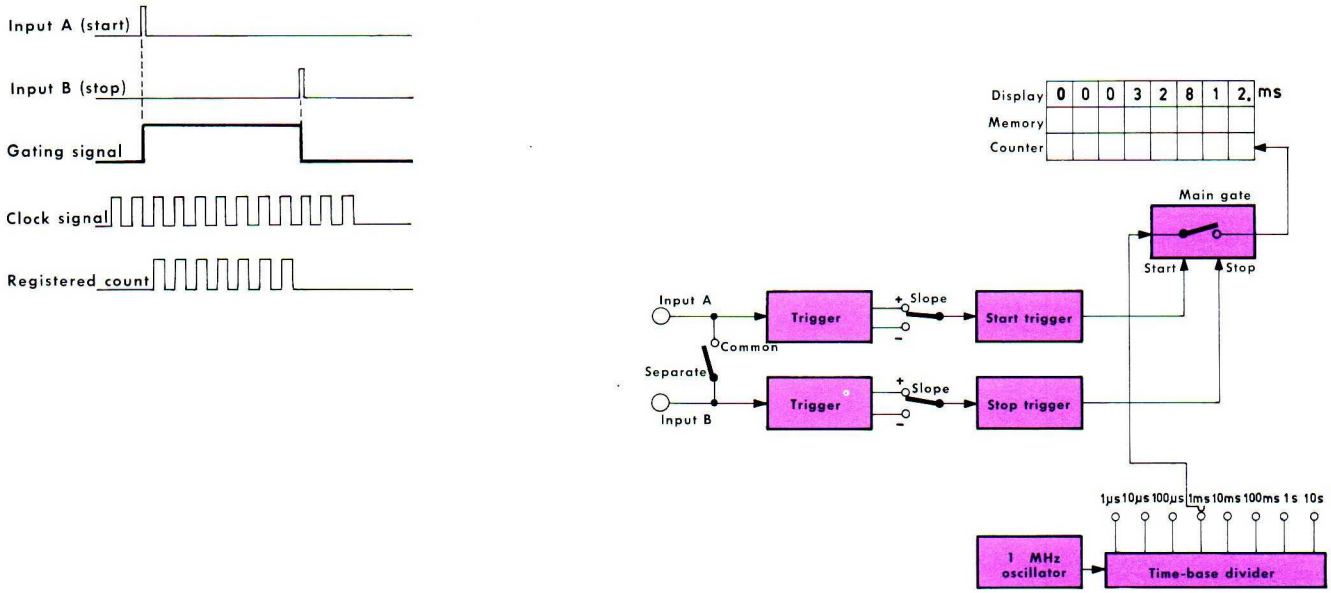


Fig. 2.7. Simplified block diagram and signal flow for the time-interval mode

A simplified block diagram is shown in fig. 15. Input A is the START channel, where the trigger level and the polarity are set and the signal is conditioned so that it can open the main gate. The STOP signal for the counter is derived from input B in the same way. The SEP/COM switch is a special feature of the TIME INTERVAL mode. In the separate (SEP) position the two channels are completely independent and the counter can handle signals from two different sources, while in the common (COM) position the inputs are in parallel so only one signal is fed to the counter but one can select different, independent parameters such as trigger level and polarity for the START and STOP functions. An application of this facility is illustrated in fig. 2.8.

As with the PERIOD mode, here too one can select various resolutions of the time-base; the relation between resolution and the position of the decimal point is in our example the same as in the SINGLE PERIOD mode (see the appropriate table 2.3).

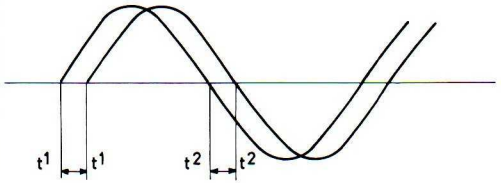


Fig. 2.8. Phase-difference measurement

The time-interval mode can be used for digital phase measurements. The measurement is made by determining the time interval between coresponding points on two identical waveforms.
As a sine wave has its steepest slope at the zero crossing it is better to measure the time interval between the points where the signals are 0 volt. The LEVEL potentiometer should thus be set to "0". This will minimize all errors due to differences in amplitude between the two signals.
To eliminate DC components, AC coupling should be used. Systematic errors can be eliminated by measuring the time interval with the SLOPE switch of both channels first in position "+" and then in position "—".
If the first result is t_1, and the second result t_2, the corrected value is:

$$t\varphi = \frac{t_1 + t_2}{2} \text{ and hence}$$

$$\text{the phase angle } t\varphi = \omega \frac{t_1 + t_2}{2}$$

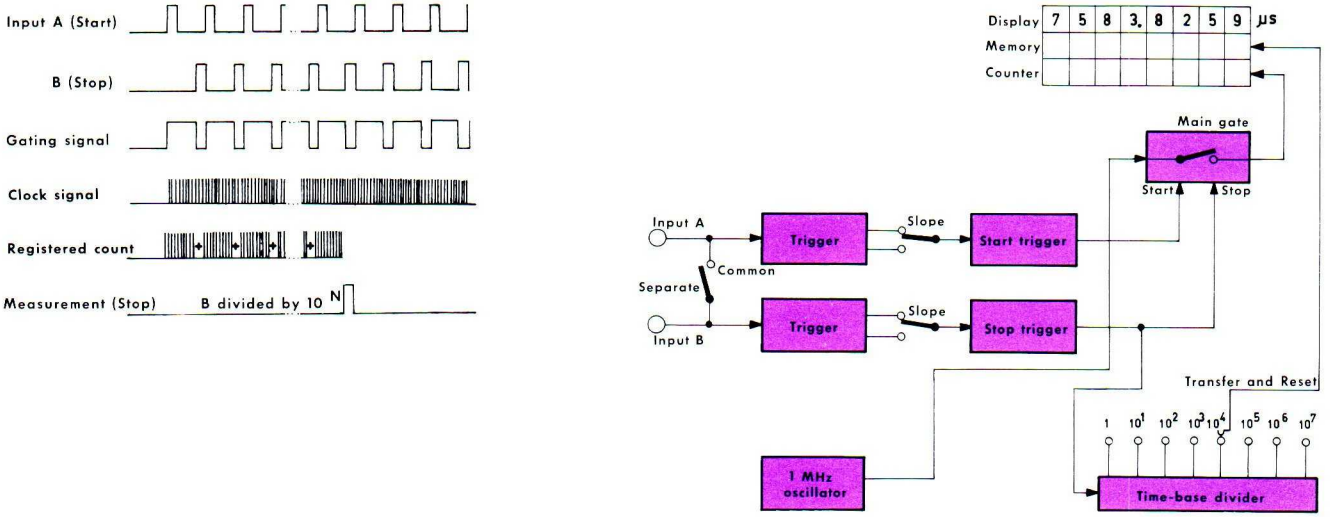


Fig. 2.9. Simplified block diagram and signal flow for the time interval average mode

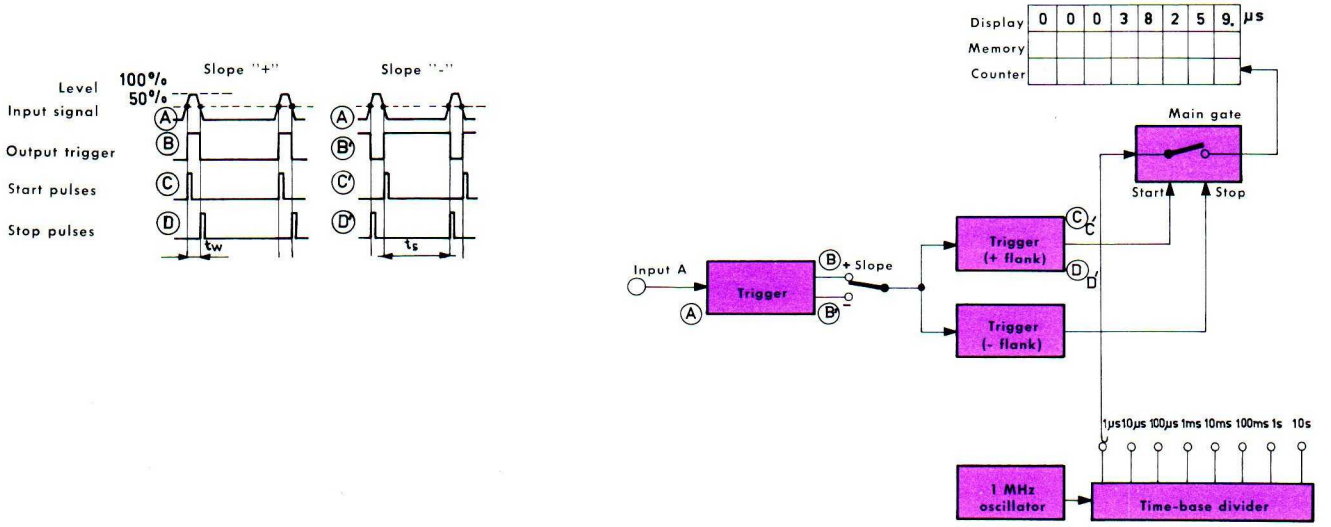


Fig. 2.10. Simplified block diagram and signal flow for the pulse-width or pulse spacing mode

b. *Time-interval averaging*
As with period measurements, here too an averaging mode is possible. The block diagram of this mode is given in fig. 2.9, which in view of the above is self-explanatory. There is one fundamental difference between the multiple-period and the multiple-time-interval mode: in the first case the main gate remains open until the very last of the averaged pulses has been counted by the time base chain, whereas in the T.I. averaging mode the main-gate closes at each stop pulse, but the DCU where all the counts are totalized is not reset until the last stop pulse has been counted. This STOP pulse is given when the time-base divider has totalized the selected number of intervals. This difference, as we will see in chapter 4, is the main reason for differences in accuracy and resolution between this two measuring modes. The relation between the position of the decimal point and the time-base dividing factor is in our example the same as for the multiple-period mode (see table 2.4.).

Pulse-width measurements
The PULSE WIDTH mode may be regarded as a special combination of the period and time-interval modes, based on a single channel measurement with an automatic dual-channel triggering facility. The block diagram is given in fig. 2.10. The difference between this mode and the single-period mode is that the trigger pulses are generated at both the positive- and negative-going edges. For positive pulse polarities, as shown in the figure, the main gate is opened at the positive edge of the pulse (C), and closed again at the negative edge (D). In this way the pulse width t_w is measured. If however the polarity (trigger slope) selector is set to negative slope the main gate is opened at (C'), and closed at (D'), so that the pulse spacing (t_s) is measured. As pulse width and pulse spacing are both defined at 50% pulse amplitude level the trigger level must be set exactly to this 50% level for accurate measurements (fig. 2.11./2.12.). The better counter types have either a calibrated level setting or even a level (check) output, which can be used for very accurate level setting with the help of e.g. a dual-trace oscilloscope. The reading is given in s, ms, μs and so on (as long as the counter's resolution permits this), and the decimal-point setting for our example is the same as for the single-period or T.I. mode.

Average pulse widths (or spacings) can be measured according to the same principle as for the T.I. average mode. Here too, the counter continues to totalize the pulse width until the time-base divider reaches the selected value, when the measurement is stopped and the result (divided by the correct factor) is displayed. As with the other averaging modes, accuracy and resolution can be improved, if certain conditions are fulfilled (see chapter 4).

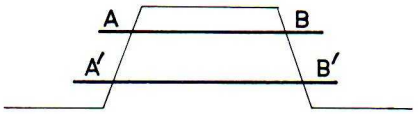


Fig. 2.11. Variation in pulse width with trigger level.

Fig. 2.12a. When the counter is set to WIDTH and "Triggering +" it will be triggered by the positive slope at "A" and again at "B". Note that the pulse width reading "AB" will vary with trigger level according to the pulse shape (see also next curve).

Fig. 2.12b. When the counter is set to WIDTH and "Triggering —" it triggers first at "B" on the negative slope and again at "C" on the positive. This then gives a direct reading of the pulse delay "BC".

Fig. 2.12c. When the counter is set to PERIOD and "Triggering +", it will trigger at "A" and "C" to record the repetition time "AC". The measured period can also be averaged over 10^n period by setting the counter to MULTIPLE PERIOD.

Scaling

In this mode an incoming frequency can be divided by various powers of 10. The simplified block diagram is given in fig. 2.13., which shows that in this mode a frequency is applied to the external standard input and routed through the time-base dividers to an output socket (usually situated at the rear of the instrument). The scaling factor is selected by the time-base multiplier switch.

Checking

In the CHECK mode (fig. 2.14.) the internal crystal frequency is counted for a time set by the time-base switch. The display must naturally always show the value of this crystal frequency:

$\frac{fc}{fc \times 10^{-n}} = 10^{n}$ (Hz, kHz or MHz, with the appropriate position of the decimal point).

This mode does not check the absolute accuracy of the counter or the crystal oscillator, since:

$\frac{fc + \triangle f}{(fc + \triangle f) \cdot 10^{-n}} = 10^{n}$ where fc is the specified frequency of the crystal oscillator and $\triangle f$ the frequency error of the crystal oscillator.

This check mode is the last of the measuring modes encountered in most universal counters.

There are many other measuring modes or small variations on the above-mentioned themes; but as they are mostly highly specific to a narrow range of applications, they are not included in this general survey.

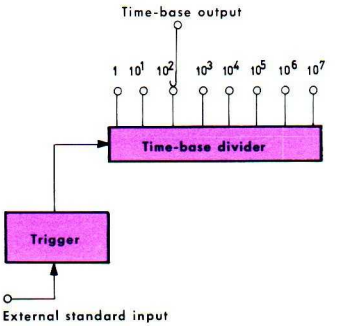


Fig. 2.13. Simplified block diagram for scaler operation

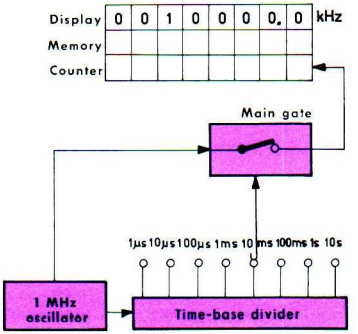


Fig. 2.14. Simplified block diagram for self-check operation

Questions

Q.2.1. A counter is operating in the frequency mode, with the time base set to 10 ms and the dimension indicator to MHz. The decimal point is then between digits:

A 6 and 7

B 7 and 8

C 4 and 5

A	
B	
C	

Q.2.2. A counter normally working with an internal clock frequency of 1 MHz is used with an external standard of 4 MHz. In order to get the correct result the reading in the frequency mode should be:

A Multiplied by 4

B Multiplied by 2

C Divided by 4

A	
B	
C	

Q.2.3. An 8-digit counter with a time-base accuracy of 10^{-8} and as usual a display accuracy of $\pm$ 1 digit is used to measure a 400 Hz signal in time-base setting 10 s. The measurement accuracy will then be:

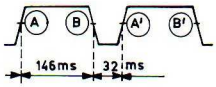
A 2.5×10^{-8}

B 1×10^{-8}

C 2.5×10^{-4}

A	
B	
C	

Q.2.4. The pulse below is applied to a counter set to the PULSE WIDTH mode. Slope selector is "pos".



Q.2.4a. The read-out will be

A 178 ms

B 32 ms

C 146 ms

A	
B	
C	

Q.2.4b. After inversion of the pulse the read out will be

A 178 ms

B 32 ms

C 146 ms

A	
B	
C	

Q.2.5. The number of digits in a counter is basically related to:

A The required frequency range

B The clock accuracy

C The clock frequency

A	
B	
C	

Q.2.6. A 1.5 kHz signal is applied to a counter set to MULTIPLE PERIOD 10^4. The time-base resolution is 1 μs. How many digits are needed for the display?

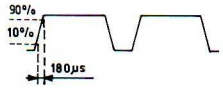
A 7

B 6

C 4

A	
B	
C	

Q.2.7. For measurement of the rise time of the pulse below the counter should be set to



A PERIOD mode

B PULSE WIDTH mode

C TIME INT. mode

A	
B	
C	

Q.2.8. In order to avoid overflow of the counter display in a MULTIPLE TIME mode one should

A Decrease the time-base frequency

B Increase the number of pulses over which the average is taken

C Increase the frequency range of the counter

A	
B	
C	

Q.2.9. Sometimes a digital printer is connected to the BCD output of a counter. As this type of printer is normally a mechanical device it is rather slow, so the normal display time is not long enough for the print-out of all the characters. In order to inhibit a new measurement during printing, the printer delivers an inhibit signal (logic "0"). To which point in the diagram of fig. 2.3. should this signal be connected?

A 7

B 9

C 11

A	
B	
C	

Q.2.10. The "check" function in a digital counter is checking:

A The operation of the instrument

B The accuracy of the crystal oscillator

C The input amplifier

A	
B	
C	


PM 6645 frequency counter 30 Hz - 512 MHz
PHILIPS
0 9 . 6 3 3 9 0 4 7
GO
GHz
DISPLAY TIME
MIN
GO
MAX
INPUT A
POWER ON
REMOTE
SUB-UNIT
RATIO
CHECK
FREQ
GATE TIME
10 ms
100 ms
1 s
10 s
RESET
PM 6634 frequency converter 1 - 12.6 GHz
FREQUENCY PRESET
0 9 . 4
GHz
PRESET
AUTO
OUTPUT
INPUT

Chapter 3
Plug-in units and special functions

In the early days of digital counters the instruments were rather limited in performance, especially where sensitivity and frequency range were concerned. Plug-in systems were developed in order to overcome these limitations. With these plug-in modules, it is possible e.g. to extend the frequency range of a fairly low frequency counter into the microwave region or to increase the input sensitivity by a factor of 50 or more.

Since the introduction of plug-in systems the variety of the available modules has increased and their capabilities have expanded to a point where a general-purpose plug-in counter can fulfil the function of a number of other instruments as well as performing quite a lot of measurements that were impossible up to now.

At the present time, there are at least ten distinct types of plug-in modules available for use with electronic counters. We shall describe each of the ten types briefly below and in detail in the rest of this chapter.

Prescalers are modules that scale the input down to a frequency range that can be accommodated by digital counters. Prescaler modules currently available are capable of operation at frequencies up to 1 GHz.

Frequency converters (working on the heterodyne principle) are used to extend the upper range of frequencies that can be measured with electronic counters. These modules typically cover frequency ranges from 50 MHz up to 21 GHz, and input sensitivities range from 50 mV_{rms} to 100 mV_{rms}.

Transfer oscillators constitute another group of plug-in modules that provide frequency measurement capabilities ranging from 50 MHz up to 40 GHz. Typical input sensitivities of these modules range from 50 mV_{rms} to 100 mV_{rms}.

Automatic dividers, which represent a special form of the transfer oscillator, generally divide the input frequency by a factor of 100 or 1000. Their frequency range goes up to the X-band.

Time-interval modules are used to convert a basic frequency counter (without time-interval mode) into an instrument for the acurate measurement of time intervals. Present state-of-the-art time-interval modules (TIM's) provide a measuring accuracy of 10 (or 1) nanoseconds (10 MHz clock x 10), and are capable of resolving pulse pairs that are separated in time by as little as 3 nanoseconds.

Pre-amplifier modules are available to facilitate the measurement of low-level signals. Typically, they are capable of amplifying 1 mV signals to the level required to drive a frequency counter, and they are available for operation at frequencies from 10 Hz to 500 MHz.

Preset modules are devices that provide a means of manipulating a counter's time-base, its input frequency or its DCU to provide a read-out bearing any arbitrarily selected relationship to a particular input. For example, a preset module can be used to enable a counter to display the output of a digital transducer in terms of gallons per minute, feet per second, pounds per hour, etc.

Digital voltmeter modules - as their name suggests - convert a frequency counter into a DVM. Since much of the circuitry in a DVM is duplicated in a frequency counter, the plug-in module needs to provide only the circuitry that is unique to the DVM.

The sine-wave oscillator is one of the more recent additions to the family of plug-in modules available for use with frequency counters. One unit of this type converts a frequency counter into a sine-wave source of accurately known frequency. Basically an LC or RC oscillator, the unit does not have a calibrated dial, the frequency being read directly from the counter.

Programme units are also available as plug-in modules for electronic counters that have provision for external programming. One of these units permits automatic selection of up to ten programmes, which are established by means of plug-in cards with 64-bit capacity for programme instructions.

Prescaler

The principle of the prescaler is quite simple, as can easily be seen from the block diagram of fig. 3.1.

The RF input frequency is conditioned in the trigger/shaper circuit and then fed to a chain of binary dividers (scalers). After being scaled down to a frequency well within the counting range of the given frequency counter the signal is fed to this counter, which will of course only register $1/2^N$ (N being the number of binary scaler steps) of the input pulses in the normal gate time. The gate time is therefore simultaneously extended by the same factor as the scaling factor, so the counter display will show the correct frequency (at the expense of a longer measuring time).

It would be much easier to work with a prescaling factor of 10 (or a power of 10) because then there is no longer any need for additional time base dividing: a simple shift of the decimal point by one or more places has the same result.

Although the block diagram looks simple, the real circuit is rather tricky and involves discrete HF transistors, tunnel diodes, ECL circuits or thin film hybrids.

It was therefore practical impossible to make decade dividers in the early days because the maximum counting speed was reduced drastically when the flip-flops were loaded with additional gates for making a decade divider out of 4 flip-flops.

Fortunately, modern HF components do now permit the construction of real decade dividers. They generally consist of a binary scaler followed by a quinary ("divide by 5") ring counter.

The circuit diagram of such a quinary ring counter made in thin-film technology for the Philips RF counters is depicted in fig. 3.2.

The prescaler is easy to use and can give direct readings. Just like the normal direct counter it can measure FM signals, averaging them during the gate time.

Prescaling has only one drawback: it is slow. For example, a frequency measurement with a divide by 10 prescaler with a 1 Hz resolution would take 10 seconds, and the corresponding measurement with a divide by 100 prescaler would even take 100 seconds of measuring time.

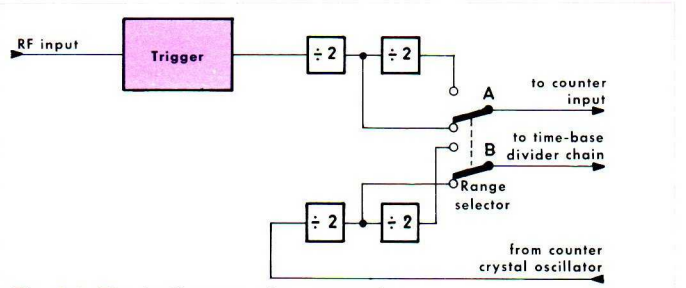


Fig. 3.1. Block diagram of a pre-scaler.

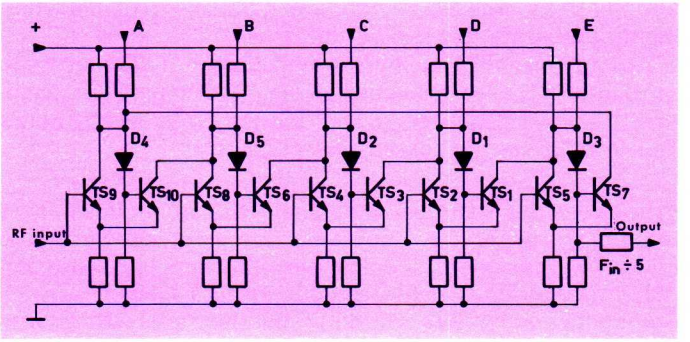


Fig. 3.2. Circuit diagram of a thin-film quinary ring counter. (The outputs A, B, C, D and E are used for decoding purposes if a numerical read-out is required.)

Heterodyne frequency converter

All frequency-extending plug-ins have one thing in common: in some way or another they bring the frequency to be measured down into a range which can be counted by a normal digital frequency meter. In the prescaler this end was achieved by dividing the input frequency by a con-

stant factor, while in the heterodyne converter the input is translated downwards in frequency by mixing it with signal of precisely known slightly different frequency. The resulting difference signal which is now within the frequency range of the counter is then counted and displayed.

The principle as applied in the heterodyne frequency converter (see block diagram fig. 3.3.) is as a matter of fact identical with that of the superheterodyne radio receiver.

The converter is made up basically of four parts:
a harmonic generator, a tunable filter (cavity), a mixer and an RF low pass amplifier ("video" amplifier).

In order to facilitate the explanation of the function of the circuit, let us assume that the digital frequency counter used has a frequency range of at least 200 MHz (e.g. Philips type PM 6645 or PM 6650).

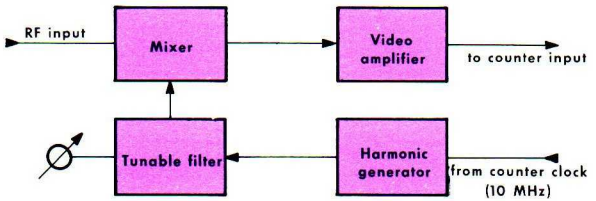


Fig. 3.3. Block diagram of a heterodyne converter.

The clock frequency of this counter (10 MHz) is applied to the converter and multiplied by 20, thus making it 200 MHz, and then amplified to a sufficient power level to drive a harmonic generator. This harmonic generator (usually a step recovery diode) then generates a comb of frequencies at 200 MHz intervals, covering e.g. the frequency range from 200 MHz to the X-band (12.4 GHz) with approx 60 discrete frequencies. This "picket fence" is then applied to the tunable cavity (tunable filter) which will select one only of the harmonics and apply it together with the input signal to the mixer, which is an untuned wideband device. When now an RF signal is applied to the input, the cavity is tuned upwards until a difference frequency is obtained which can pass through the lowpass amplifier (1-220 MHz in our example); a built-in level indicator then indicates that there is a measurable RF signal present at the output. The output signal is then applied to the frequency counter, which measures the difference signal. Because we started from the lower frequency, we know that the selected harmonic is somewhat lower than the RF input. The frequency indicated by the counter therefore has to be added to the frequency selected by the cavity. This frequency is always indicated in some way or another on the panel of the converter.

A numerical example will illustrate this more clearly: Suppose an input frequency of 2.35 GHz is to be measured. Initially the tunable filter is set to the lowest harmonic value. The cavity is then tuned and the frequency of the harmonics is increased in steps of 200 MHz until a reading is observed on the level meter. This will happen when the 11th harmonic is selected, i.e. when the cavity is tuned to 2.2 GHz. In this case there will be a difference frequency of 2.35 - 2.2 GHz = 150 MHz. This signal is amplified by the low pass amplifier and then fed to the counter which will register 150 MHz. The input frequency is thus 2.2 GHz + 0.15 GHz = 2.35 GHz. The input frequency is thus found by adding the reading of the converter dial and the value displayed on the counter.

If now the cavity is tuned upwards to another beat, a reading of 50 MHz would be obtained with the 12th harmonic (2.4 GHz): in this case, however, the counter reading should be subtracted from the frequency selected (2.4 GHz — 0.05 GHz = 2.35 GHz) giving the same final result as above.

Of course there are many more beats than the above two, but in most cases the beat frequency lies outside the pass-band of the video amplifier and is thus not registered. In particular cases, however, input signals can produce three beats within the pass-band of the video amplifier which thus give legitimate answers. An example will illustrate this: Assume an input signal of 8.215 GHz:

	A	B	C
Input signal (GHz)	8.215	8.215	8.215
Harmonic frequency (GHz)	8.000	8.200	8.400
Difference frequency (GHz)	215	15	185

All difference frequencies lie in the pass-band of the video amplifier (220 MHz) and give correct answers, provided the counter reading is subtracted in case C.

The above heterodyne converter which is manually tuned, was one of the first means used to extend digital frequency measurements into the microwave frequency range.

A disadvantage of this method is that one must always add (or subtract) the counter's digital read-out to (from) the converter reading. In order to overcome this disadvantage the manually tuned heterodyne converter has been automated by replacing the cavities by electronically tuned Yttrium - Iron - Garnet (YIG) filters (see p. 33). While the technical performance is equivalent to that of the ma-

nually tuned converters, the operation is fully automatic and provides a direct digital read-out.

In fig. 3.4. a simplified block diagram of the automatic converter as is used in the Philips PM 6634 is given. This circuit functions as follows:

The 10 MHz reference frequency derived from the counter is applied to a phase-lock circuit in which the fifth harmonic of the reference is phase-locked to the 50 MHz oscillator frequency. The converter thus maintains the accuracy and stability of the counter's time base.

The 50 MHz frequency is multiplied four times to 200 MHz and applied to a power amplifier. This stage drives the comb generator that produces a comb of harmonics from 0.8 GHz to 12.6 GHz with a 200 MHz interval between each frequency. These comb lines are continuously applied to the yttrium-iron-garnet (YIG) filter (a magnetically tuned high-Q resonator device).

The mixer produces two signals: first, a DC signal with a level proportional to the power of the input RF signal, and secondly a heterodyned signal whose frequency is the difference between the input RF frequency and the comb line frequency to which the YIG filter is tuned.

The DC signal is picked off at the input of the pre-amplifier as a logic "1" and coupled to the YIG control circuits via the video control circuits. This starts a BCD counter whose output is converted into a staircase voltage by the digital-to-analogue converter. The YIG driver, in turn, produces a current proportional to the staircase voltage. This current continuously tunes the YIG filter until the frequency of the heterodyned output signal of the mixer falls within the range from 10 MHz to 220 MHz, corresponding to the passband of the tuned pre-amplifier. The video control circuits then provide a stop signal for the BCD counter in the YIG control circuit. The YIG filter will now be tuned to the comb line frequency just below the input frequency. The decade counters coupled to the D/A converter will now be locked and will feed their instantaneous states as signals presetting the three most significant digits of the basic counter. The YIG control circuits feed a gating signal to the video amplifier, which opens. The heterodyned signal from the mixer can now pass through the pre-amplifier and the video amplifier to the counter, where the frequency of the heterodyned signal is added to the preset frequency so that the **complete** result is presented on the counter's display.

Inspection of the block diagram of fig. 3.4. will show that the automatic heterodyne converter incorporates a special feature: the PRESET/AUTO mode. In many applications more than one frequency with sufficient amplitude may be present in the range 0.8 to 12.6 GHz. If in that case the converter is used in the AUTO mode, the filter scan will stop at the first (lowest) frequency and the other frequencies are not measured. The PRESET/AUTO mode is therefore built in so that the initial frequency of the YIG filter can be preset. Frequencies lower than the preset value are not measured. In the PRESET (manual) mode, the decade counters in the D/A converter will be locked to a state dictated by the setting of the thumbwheel switch FREQUENCY PRESET. The preset frequency should be lower than the RF input signal frequency but so high that the difference frequency (f_{RF}-f_{comb}) of the mixer output is within the frequency range of the preamplifier (10 - 220 MHz).

When the converter is switched over from PRESET to AUTO, the YIG filter is again continuously tuned, but starts from the preset frequency.

The following example (fig. 3.5.) should help to explain this.

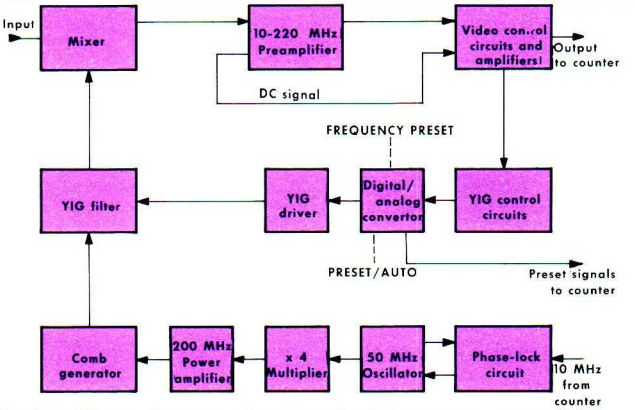


Fig. 3.4. Block diagram of automatic heterodyne converter.

An RF signal containing the frequencies A, B and C is fed to the converter. If one wishes to measure frequency C, the converter should be preset to such a frequency that the difference f_{PRESET}-f_B is greater than the passband of the preamplifier (220 MHz). In the present example the converter should be preset to 12 GHz, giving a difference frequency of 320 MHz. When the converter is switched over to AUTO, the scaning goes on and stops at the 12.2 GHz combline and the counter displays frequency C, i.e. 12.3 GHz. If the converter were preset to 11.8 GHz, an erronuous display would be obtained because the difference frequency (f_{PRESET}-f_B) would amount to 120 MHz, which is then within the passband of the preamplifier.

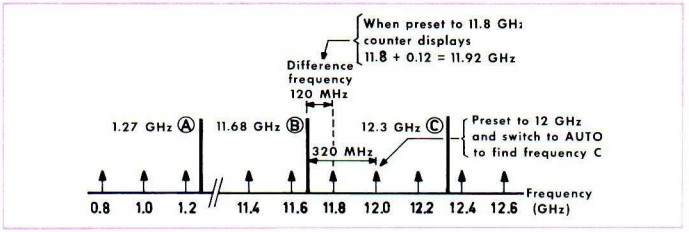


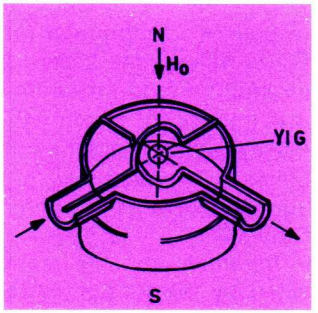
Fig. 3.5. Presetting the comb line frequency in the PRESET/AUTO mode. In the AUTO mode the YIG filter scan stops at 1.2 GHz and signal A is detected. For automatic tracing of a signal having a frequency higher than signal B, the comb line should be preset to 12 GHz. In this example only signal C will thus be detected.

This difference frequency would be added to the preset value in the counter, thus giving a display of 11.8 + 0.12 = 11.92 GHz. The distance between frequencies A (1.27 GHz) and C (12.3 GHz) in this example is so large that harmonics of frequency A will hardly be strong enough to interfere, but one should always reckon with this possibility.

YIG Filters

Of recent years, single-crystal Yttrium Iron Garnet (YIG) has become a very interesting and important material for applications in magnetically tunable microwave devices such as filters, limiters, circulators and delay lines. Most of these devices can basically be described as filters. YIG spheres or discs, highly polished, are used as high-Q resonators. The resonant frequency is solely determined by an external static magnetic field and not by the volume of the YIG sample. The tuning characteristic for spheres is given by the simple relation $f_r = \gamma H$, where f_r is the resonant frequency in MHz, H the applied magnetic field in oersted, and γ the gyromagnetic ratio in MHz/Oe.

Pure YIG has a gyromagnetic ratio of $\gamma = 2.8$. This offers linear tuning ranges over more than a frequency decade, using YIG spheres with a typical diameter between 0.5 and 1 mm. A simple YIG band-pass filter structure is shown here. Only signals at the resonant frequency are coupled by the YIG sphere from the input line to the output line; signals at other frequencies are highly decoupled because of the orthogonal position of the coupling loops. A multi-stage YIG band-pass filter is applied in the Philips automatic heterodyne converter PM 6634.



Coupling structure of a single-stage YIG band-pass filter.

Heterodyne converters with manual or automatic tuning are available nowadays in many frequency ranges up to 21 GHz.

Their main features are:

—1 They are simple both in principle and operation.

—2 They can measure the frequency of CW signals with a considerable amount of FM.

—3 They give a much higher resolution for a given gate time, because the ambiguity of the main counter of ± 1 count is not multiplied by the harmonic number as in other techniques.

The transfer oscillator

Just like the heterodyne converter, the transfer oscillator (TO) mixes the incoming (unknown) frequency with an internally generated signal. The main difference between the two methods is that in the heterodyne converter the internal signal is a standard signal and the mixing product is measured by the digital counter, while in the TO the internal signal is variable and it is **this** signal which is measured by the counter.

Basically, the principle is the same as that used for dial calibration of signal generators or transceivers (see fig. 3.6.). The TO consists of a variable-frequency oscillator (VFO) with a very accurately calibrated dial, a mixer, a video amplifier and a zero beat detector (viz. a pair of headphones, oscilloscope screen etc). When the output of the VFO and the unknown frequency are applied to the mixer, the difference frequency or zero beat can be heard with the pair of headphones (or seen on the screen etc). The VFO is tuned until a zero beat is obtained; the frequency can then be read off on the VFO dial. When now the counter is connected to this VFO, a direct digital display of the VFO frequency (and hence of the unknown frequency) is obtained. The accuracy of this reading naturally depends strongly on the accuracy of the zero beat and the stability of the VFO.

Furthermore, in the method described above we are limited by the frequency range of the counter, since both the VFO and the unknown frequency must be within this range.

Plug-in TO's therefore incorporate a harmonic generator (fig. 3.7.). One output of the VFO goes to the digital frequency meter and the other to a harmonic generator which can deliver strong harmonics up to at least the 100th harmonic.

If the VFO has e.g. a tunable range of 100 - 200 MHz, microwave frequencies up to 20 GHz can be measured in this way. After mixing, the input signal and one of the harmonics will produce a difference frequency which is no longer fed to a pair of headphones but displayed on an oscilloscope where the zero beat can be determined much more accurately.

As we mentioned above, one of the limitations on the accuracy of the transfer oscillator is due to the inherent instability of a VFO. A very good VFO has a stability of the order of 10 ppm, which is low compared with the accuracy and resolution of an average frequency counter.

The accuracy of the circuit can be improved by incorporation of a "phase-locked loop" (see fig. 3.8.). In this method the output of the video detector is applied not only to the oscilloscope (or headphones) but also to a phase detector where its phase is compared with that of a

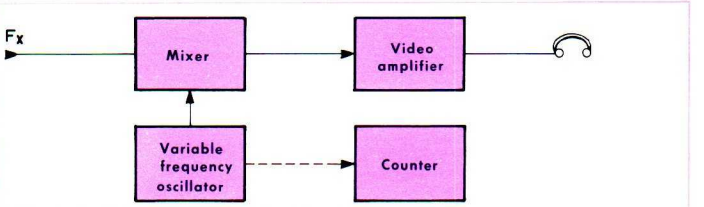


Fig. 3.6. Basic principle of transfer oscillator

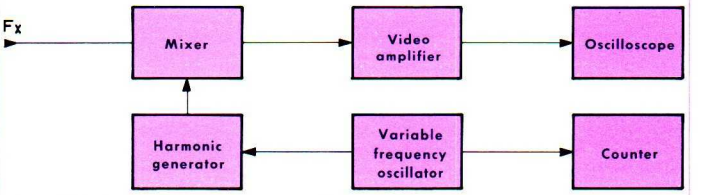


Fig. 3.7. Block diagram of a TO plug-in

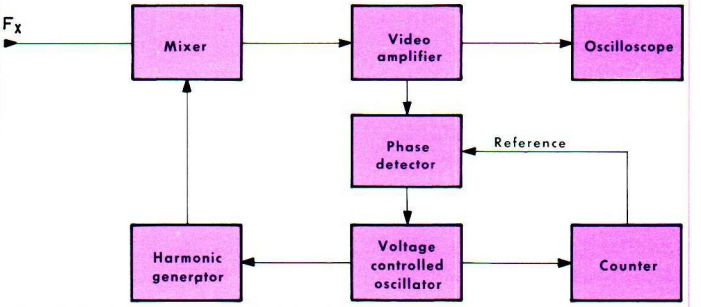


Fig. 3.8. Transfer oscillator with phase-locked loop

standard reference frequency (generally derived from the main counter). As the oscillator is tuned across its range, one of its harmonics will produce a beat frequency with the frequency to be measured. This beat frequency (IF) is then amplified and applied to the phase detector. Any difference in frequency between the two inputs is detected and produces a corresponding change in the output of the phase detector. This resultant output then adjusts the voltage-controlled oscillator (VCO) over a narrow range. The VCO frequency is then measured by the main counter as described above. Under these conditions the VCO will be phase-locked, the zero beat will be more stable and the reading will be correct within the limits of the stability of the counter.

However, as it is impossible to obtain a phase lock with a zero IF frequency (video amplifier output), the VCO will be offset in frequency by the same amount as the applied reference frequency (e.g. 1 MHz). In this case the counter will always give a reading which is 1 MHz wrong and as there are two possible 1 MHz beats one reading will be

1 MHz too low and the other (the image) will be 1 MHz too high. In modern TO's one of these sidebands is selected in such a way that one always has to add 1 MHz to the reading.

So far, we have been discussing methods of improving the basic oscillator. However, the counter still indicates the fundamental frequency of this oscillator and as long as we do not know which harmonic is beating with the input signal we do not know what the input frequency really is. If e.g. the VFO has a range of 100 - 200 MHz and the input frequency is 960 MHz, the TO will beat with the 6th harmonic of 160 MHz and the counter will indicate 160 MHz. If we know which harmonic is causing the beat we can simply multiply the counter reading by the harmonic number to get the correct frequency. However, an even better method is to extend the gate time of the counter by the harmonic number (N). (In our example we make the gate time 6 times longer, so that the counter will display 6 x 160 = 960 MHz.) All transfer oscillators therefore have a built-in time-base extender, mostly in the form of thumb-wheel switches, which can be set to the harmonic number causing the beat. In other words, if the RF input beats with the 36th harmonic of the VFO, the gate time is increased by a factor of 36. For this purpose the counter clock frequency is passed via the preset switches in the TO before it is connected to the normal time-base dividing chain.

When now one wants to measure an unknown input frequency one must determine which harmonic of the VFO is mixing with the input frequency to produce a zero beat. If the input frequency is already known to a reasonable accuracy the procedure is quite simple: First set the harmonic selector switches to 01 (no gate time extension, i.e. the counter is displaying the VFO frequency directly).
Now tune across the range until a zero beat (no phase-lock!) is obtained. Divide the RF input frequency by the VFO frequency to get the harmonic number:

$$\text{Harmonic number (N)} = \frac{\text{RF input frequency}}{\text{VFO frequency}}$$

then set the harmonic switches to N and the counter will display the correct answer directly. If there is any doubt about this reading, simply tune the VFO downwards (or upwards) until the next zero beat is obtained and set the harmonic switches one number higher (or lower). This should produce the same frequency indication.

When the input frequency is completely unknown, the harmonic number N can be found by applying a simple relationship. At a zero beat the input frequency is the VFO frequency times N ($F_x = NF_1$). When the oscillator frequency is increased so that another frequency causes a zero beat, the harmonic producing the second zero beat will have a harmonic number one less than the first, so $F_x = F_2(N-1)$. By equating the terms on the right-hand sides of these two equations we find:

$$NF_1 = (N-1)F_2 \rightarrow N = \frac{F_2}{F_2 - F_1}$$

For example, if the input frequency to be measured is exactly 4 760 MHz a zero beat will occur e.g. at an oscillator frequency of 136 MHz (F_1) when the 35th harmonic of F_1 beats with the input frequency. When the oscillator is tuned upwards to 140 MHz (F_2) the 34th harmonic produces a zero beat. The harmonic number is thus found to be:

$$N = \frac{140}{140 - 136} = 35$$

so the input frequency is 35 x 136 = 4 760 MHz.
Of course, when the TO is used in the phase-lock mode the IF frequency must be taken into account. However, in modern TO plug-ins this offset frequency is preset in the counter registers directly (as in the automatic heterodyne converter) so that the counter displays the correct frequency independent of the operating mode (zero-beat or phase-lock).

The manually tuned TO requires considerable operating skill and sometimes rather complex computations to determine the right harmonic. In order to get round this difficulty, automatic transfer oscillators, which require hardly any skill to operate, have been built. One simply applies a signal to the input and turns the sensitivity control up until a steady reading is observed on the counter. Fig. 3.9. shows the basic block diagram of such an automatic TO. The input signal is fed to the phase-lock circuit as usual. In the absence of an RF signal, there is no signal at the output of the IF amplifier. The sweep oscillator (saw-tooth generator) is free-running, sweeping the oscillator over the entire VCO range. All the harmonics of this VCO are capable of mixing with the input signal. If now an input signal is present one of these harmonics will beat with the input frequency and produce an IF signal which is then compared in phase with the reference frequency until phase lock is achieved. The

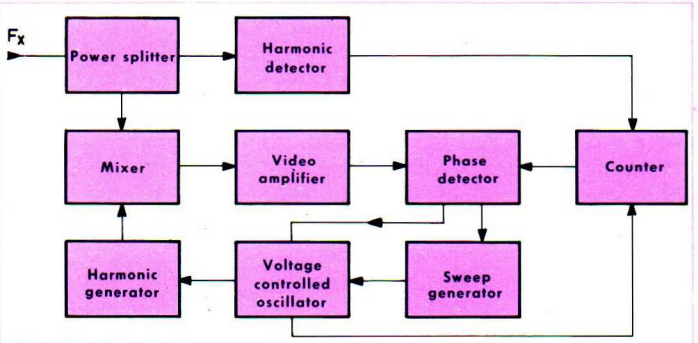


Fig. 3.9. Block diagram of automatic transfer oscillator

comparator then generates a signal inhibiting further sweeping of the VCO.
The VCO is now automatically tuned to a frequency which is an exact sub-multiple of the input frequency (plus the IF offset), and the VCO output is routed to the frequency counter. In order to find the harmonic number, the input signal is also fed to the harmonic detector. The selected gate time of the basic counter is then multiplied by this number to give a direct reading of the input frequency. The automatic TO is very sensitive to unwanted FM. Furthermore, both the automatic and the manual TO have relatively long acquisition and gate times.

The automatic divider

The automatic divider is basically a special version of the phase-locked transfer oscillator, in which the input frequency is divided by a constant factor e.g. 100 or 1000.
Such a divider consists basically of two VFO's, two harmonic generators, a digital divider, three mixers and two phase detectors, and works as follows (see fig. 3.9.).

The first VFO (F_1) is phase-locked to the input frequency (F_x), in the same way as the normal transfer oscillator. The second VFO (F_2) is phase-locked to a frequency which differs from F_1 by e.g. 1%.

The input frequency F_x is applied together with the harmonics of F_2 to mixer I. The output frequency of this mixer is now equal to F_x divided by 100 in our example, and can be measured by a normal RF counter.

The phase-locking occurs as follows:
The VFO's F_1 and F_2 are mixed in mixer II to give a difference frequency F_m. Furthermore, the frequency F_1 is digitally divided by 100. The output of this divider, $F_1/100$, is compared in phase with the output of mixer II (F_m). The phase detector controls the frequency of VFO 2 (F_2) in such a way that $F_m = F_1 - F_2 = F_1/100$ or $F_2 = 0.99\ F_1$. In other words, F_2 differs by 1% from F_1 as required. Furthermore we know that $F_x = NF_1$ (the same relation as in the normal TO), and $0.99\ F_x = NF_2$.
$F_x - 0.99\ F_x = 0.01\ F_x$, and since $0.99\ F_x = NF_2$
$F_x - NF_2 = 0.01\ F_x = F_0$.

As F_x and NF_2 are the two signals applied to mixer I, the output frequency (F_0) of this mixer is exactly 1% of the input signal F_x. As can be seen from the calculation the harmonic number N (the factor that is difficult to find in the normal TO) disappears completely.

If we had used a 1000 divider instead of a 100 divider in our example the output frequency would of course have been 1000 times lower than the input frequency. Any other dividing factor could have been chosen, but dividing factors which are powers of 10 have the advantage that we can simply shift the decimal point the appropriate number of places to give a direct reading of the input frequency. With any other dividing factor, we would have to manipulate the gate time.

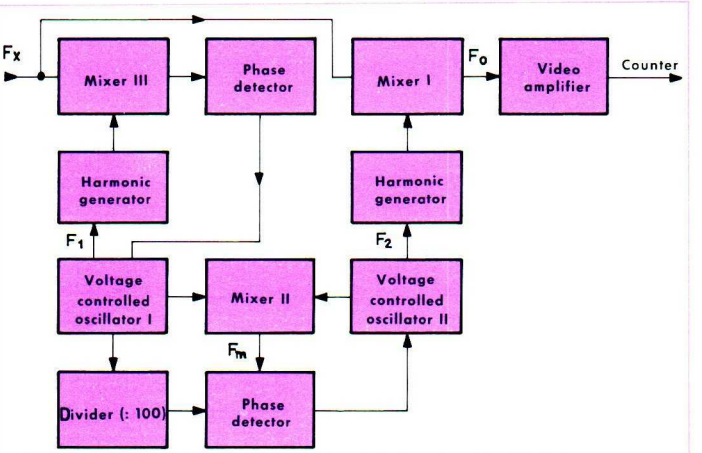


Fig. 3.10. Block diagram of automatic frequency divider

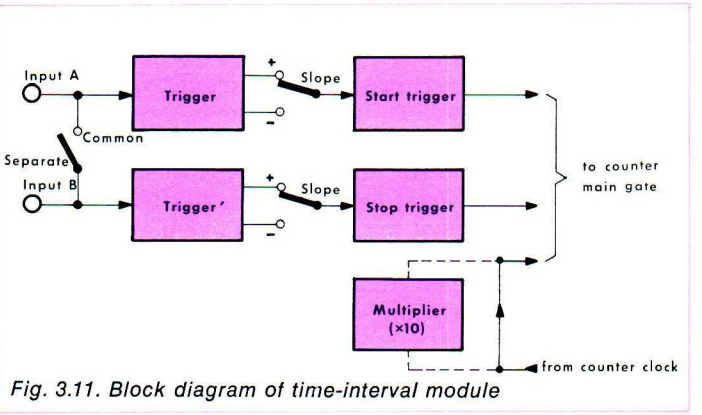


Fig. 3.11. Block diagram of time-interval module

Time-interval modules

Time interval modules (TIM) are used to make a time-interval measuring device out of a typical frequency counter. In general, they include a sensitive high-performance amplifier and shaping circuitry to produce standardized waveforms. Two independent channels are usually employed, one to control the start of the counter's main gate, and the other to control the stop of this gate. The counter then counts its internal clock pulses and indicates the time interval between the start and stop pulses.

Most TIM modules also provide slope selection (see fig. 3.11.), so that a time-interval measurement can be triggered by either a positive-going or a negative-going input

waveform, to generate a start or a stop command respectively. Provision is usually made for input DC offset and input attenuation as well.

TIM plug-in modules that accept the crystal frequency (10 MHz) from a counter, multiply it too 100 MHz and then use this frequency as the input to be measured by the counter between the start and stop pulses are also available.

By keeping all of the high-speed circuitry within the plug-in module, it is possible to obtain time resolutions down to 10 nanoseconds, and to resolve pulse pairs that are separated in time by as little as 30 nanoseconds. High-speed units of this type generally have a nominal input impedance of 50 ohm, and require a minimum input amplitude of 1 volt peak with a rise time of at least 0.5 volt per nanosecond.

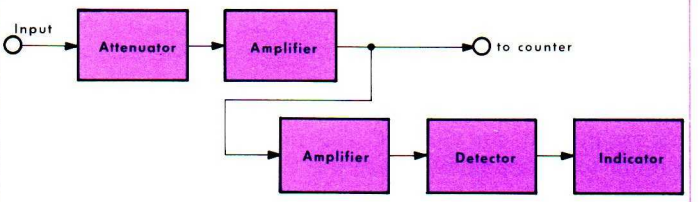


Fig. 3.12. Block diagram of pre-amplifier

Pre-amplifier modules

Pre-amplifier (PRE) plug-in modules are used to provide a signal level that is adequate for reliable operation of a frequency counter from a low-level source. The typical frequency response of modules that are currently available is from 10 Hz to 500 MHz, and input sensitivities are of the order of 1 millivolt. Input impedance is typically 1 megohm with very low input capacitance. Most provide some kind of input attenuator, as well as a meter to indicate that the signal level is sufficient to ensure proper driving of the counter. Most also provide an auxiliary 50 ohm output.

The input signal (see the block diagram of fig. 3.12.) is applied to the amplifier via an attenuator network, which is used to select the proper input level for the amplifier so that overloading (and hence an increase in signal-to-noise ratio) will be avoided.

The output signal is amplified again to obtain a sufficiently high signal to drive the level indicator, and then rectified. The level indicator shows whether the plug-in output is satisfactory for triggering the counter.

Comparison of various RF frequency measuring techniques

	Frequency Counter (direct)	Prescaler	Heterodyne Converter	Transfer Oscillator	Automatic Divider
Sensitivity	Good	Good	Fair	Good	Fair
Input impedance	High/50 ohm	50 ohm	50 ohm	50 ohm	50 ohm
Frequency range	500 MHz	1000 MHz	100 MHz-21 GHz 3-4 ranges	100 MHz-40 GHz 1-2 ranges	300 MHz-18 GHz 1 range
Measuring time[1])	Good	Poor[2])	Good	Poor[2])	Poor[2])
FM tolerance	Good	Good	Good	Fair (poor-Auto)	Poor
Pulsed RF	Poor[4])	Poor	Poor	Good (poor-Auto)	Poor
Ease of operation	Good	Good	Fair[3])	Difficult[3])	Good

[1]) For the same resolution.

[2]) Depending on the prescaling factor, the harmonic number or the dividing factor.

[3]) With automatic versions, good.

[4]) In special BURST-mode version: good.

Preset modules

"Preset" plug-ins are versatile modules that extend the application of counter/timers quite considerably. The "preset" function has developed into two quite different circuitries, each with its own application.

The first one is the so-called "register preset" (sometimes called "arithmetic preset"). In this case a BCD number set e.g. by means of thumbwheel switches is forced (via the preset inputs) into the counter chain (see fig. 3.13.), so that the counter starts counting from this value. One could use this facility e.g. for GO/ NO GO testing, by presetting the counter to the complement of the GO level (full scale reading minus GO level). As soon as the count reaches the GO level, overflow occurs and a carry is produced which can be used to initiate some desired action.

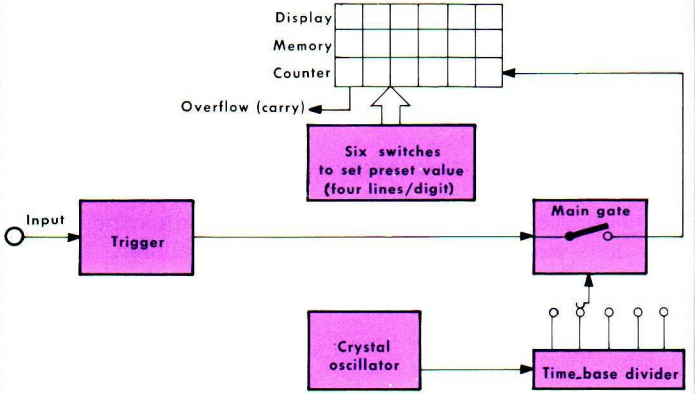


Fig. 3.13. Block diagram of preset counter with register preset

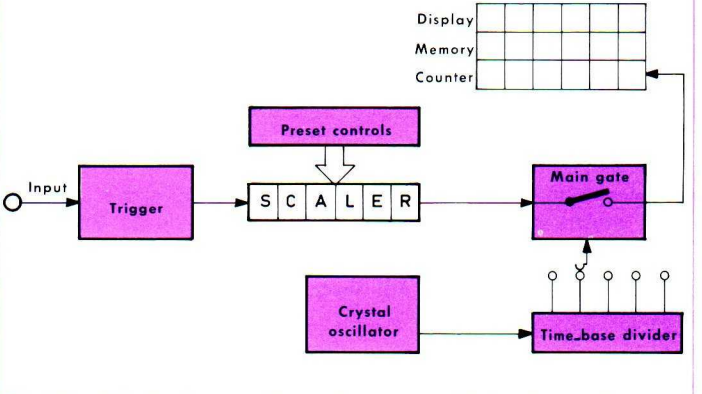


Fig. 3.14. Block diagram of preset counter with input preset (scaler)

For example, if one wants to use a 6-digit counter for limit detection in batch counting, with a batch size of 4600, the counter is preset to 1 000 000 - 4600 = 995 400. As soon as a full batch has been counted, the counter will read 000 000, with a "1" overflow.

Another example may be taken from the testing of RF receivers. If the IF frequency is preset and the local oscillator frequency is measured, the counter actually displays IF frequency + LO frequency = carrier frequency. If the LO frequency is above the carrier frequency the counter is preset to the complement of the IF frequency. The counter starts from this IF complement goes through 00 . . . 0 until it displays the carrier frequency (LO — IF = carrier). This illustrates the arithmetic function of this preset mode: in the first example two frequencies were added, in the last example subtracted.

The other preset mode is the "input" or "time-base" preset mode (fig. 3.14. and 3.15.). Here the input signal or the time-base signal is prescaled (divided) in a multiple decade counter the scaling factor of which is adjustable to any integral value between 1 and 10^K - 1 (where K is the number of decades). A numerical example will clarify this. If one has e.g. a 3 decade counter, and one wants to set the dividing factor to 123, the decades are preset to the 1000's complement of 123, i.e. 877. The counter thus starts at 877.

After counting 123 pulses the counter overflows and produces a carry; in other words each 123 pulses produces 1 carry, which is equivalent to dividing by 123. Of course as soon as the count reaches zero the preset value has to be fed into the registers again; this could be done automatically by making the carry enable the preset gates. So in general a presettable counter or counter chain can be

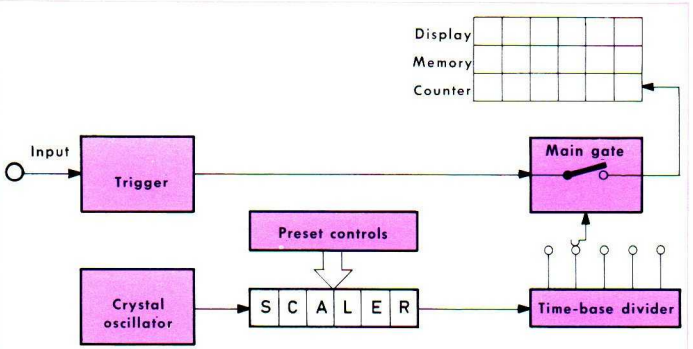


Fig. 3.15. Block diagram of preset counter with time-base preset

used as a modulo N divider by simply modifying the count length with the preset inputs.

The functions provided by such plug-ins are mostly F_{in}xN; F_{in}/N, PxN and ratio N. Typical modules contain 5-digit or 6-digit thumbwheel selectors, thus providing scaling factors up to 10^5 or 10^6.

In the F_{in} x N mode, the normal time base of the counter is extended by a factor of N. For example, if the selected time base is one microsecond and the value of N is set to 123, the time base would become 123 microseconds and the input frequency would be counted for this period of time.

The "F_{in}/N" mode causes the input frequency to be divided by the factor N before it is counted. Similarly, the "P x N" mode produces a reading representing the average period of an input signal based on N period measurements.

These facilities are mostly applied in the industrial field where one wants to convert a reading in arbitrary electrical units to mechanical units such as feet/square inch, r.p.m., radians/sec., etc.

DVM modules

Several DVM (digital voltmeter) plug-in modules are available for use with high-performance frequency counters. A typical integrating DVM module has a rated accuracy of ± 0.025% of full scale, with linearity of 0.025% of reading for 150% over range, and 0.1% of reading for 300% over range. Full-scale voltage ranges are 1, 10, 100 and 1000 volt and automatic indication of polarity is also provided. Another DVM plug-in module is basically a voltage/time-interval converter, using a linear voltage ramp and coincidence circuits to generate a time interval that is proportional to the voltage in question. The time interval is subsequently measured and displayed by counting a 10 MHz signal from the counter's time base. This module produces a 6-digit readout in the 10, 100 and 1000 volt ranges.

Special-function counters, compact counters

The introduction of the digital counter put on the market a new measuring tool with a whole range of applications which were not initially envisaged. This resulted in the introduction of the plug-ins described above, each of which covered a new application area. This approach had however one big disadvantage: it was expensive.

The main reason for this is that a counter main frame which can accept plug-ins for all kind of applications must be very versatile and hence very expensive. For instance, a typical time-interval counter does not need the very accurate (expensive) time-base oscillator; and a typical RF frequency counter does not need the high-performance DC-coupled input amplifier(s) required for period and time measurements (a simpler AC coupled amplifier would do), and so on.

This resulted in the introduction on the market of relatively much cheaper special-function counters designed for one (or a few) typical application(s), such as microwave counters, timers, presettable counters etc. They all have one or more of the functions described above in compact form, so there is no need for further explanation except for the most recent addition to the counter family, a special-function counter which has never been available as a plug-in. We will therefore give a brief description of this "reciprocal" counter here.

The reciprocal counter (computing or calculating counter) As we saw in chapter 2, if we want to measure rather

low frequencies with high resolution we have to set rather unpractical gate times (e.g. a gate time of 1000 seconds is needed to measure 10 Hz with a resolution of 10^{-4}; which is unduly long). We also know that this problem can be overcome by measuring the period instead of the frequency. If the proper time-base frequency is selected (10 μs in the above example), we get the result in one period (0.1 second). The disadvantage of this method however is that one then has to carry out some calculations (taking the reciprocal) in order to find the proper frequency, which wipes out some of the time savings achieved in the period mode. Especially when one wants to carry out frequency adjustments, this can be very annoying.

Fortunately, digital circuits lend themselves very well to arithmetic operations, as we have seen. The solution to the above-mentioned problem is thus to build a small calculating facility into the counter to take care of this simple calculation: $1/T_x = F_x$. In practice the instrument first measures the period, then automatically computes and displays the corresponding frequency in 5 or more digits. There are several ways in which this can be done. We will briefly describe one of them here, which is as a matter of fact nothing more than a special version of a presettable counter in which we convert one unit (second) into another (Hz). The simplified block diagram of fig. 3.16. illustrates the operation of the reciprocal counter.

The input frequency is shaped etc., in the input stage and then measured in the period mode. The value N in the register of the period-mode counter is equal to T_x/T_c (where is T_x the period of the unknown frequency and T_c the period of the clock frequency). This value N is then used to preset the scaler to 10^n-N; as we have seen above, this in fact causes the scaler to divide by N.

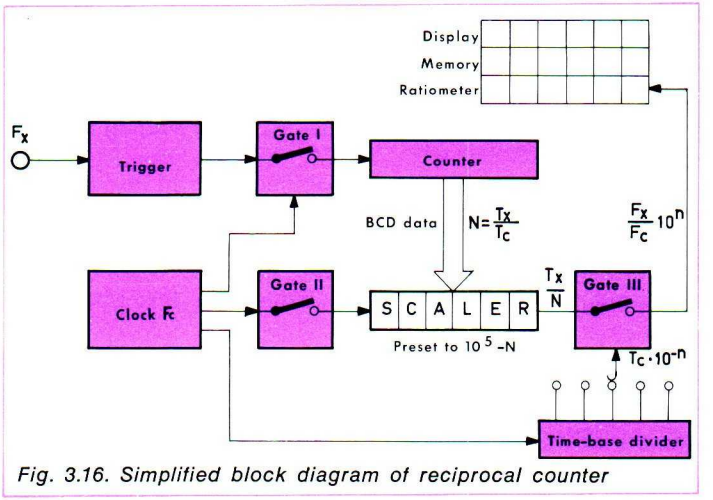


Fig. 3.16. Simplified block diagram of reciprocal counter

As the input frequency of the scaler is also the clock frequency, the output will be the clock frequency divided by N: $T_c/N = T_c(T_c/T_x)$. This signal is then applied to the (multiple) ratiometer together with the clock signal (divided by 10^n), giving the count:

$N_f = (T_c^2/T_x) : (T_c/10^n) = (T_c^2/T_x) \cdot (10^n/T_c) =$
$= (T_c/T_x) \cdot 10^n = (F_x/F_c) \cdot 10^n$

The output of the ratiometer is thus the unknown frequency, the number of digits displayed depending e.g. on the dividing factor (gate time) of the time-base divider.

Of course, the circuit should be designed so that the various gates open and close at the proper times.

It should be noted however that the accuracy of this measurement is the same as that of a period measurement, not that of a frequency measurement, as we shall learn in the next chapter.

Questions

Q.3.1. With a 10 times prescaling plug-in the decimal point in the display should be shifted:

A. One place to the left

B. One place to the right

C. Shifting does not help, the time base should be changed.

A	
B	
C	

Q.3.2. In a measurement with a heterodyne plug-in only two beats F_1 and F_2 ($F_1 < F_2$) are found. The unknown frequency now lies:

A. Below F_1

B. Above F_2

C. Between F_1 and F_2

A	
B	
C	

Q.3.3. Two microwave frequencies (a sufficient distance apart) are applied simultaneously to a manually tuned heterodyne converter. The measurement of both frequencies is:

A. Possible

B. Impossible

C. Possible if the lower one is accurately known

A	
B	
C	

Q.3.4. Two frequencies of 1.95 GHz and 8.65 GHz are applied to an automatic heterodyne converter with a comb frequency distance of 200 MHz. The converter is in the PRESET-AUTO mode, and is preset to 2.00 GHz. The reading of the counter will be:

A. 8.60 GHz

B. 1.95 GHz

C. 2.05 GHz

A	
B	
C	

Q.3.5. During the determination of the harmonic number of an unknown frequency with a transfer oscillator plug-in, two zero beats were observed, one at 168 MHz and the other at 174 MHz. The harmonic number N is now:

A. 28

B. 29

C. 30

A	
B	
C	

Q.3.6. The unknown frequency in the question 3.5 is:

A. 4.872 GHz

B. 4.704 GHz

C. 5.046 GHz

A	
B	
C	

Q.3.7. In a measurement with a transfer oscillator, using a phase-lock mode with 1 MHz offset, the harmonic number N was found to be 4. The time-base extension was set to 4 x, the frequency range of the TO local oscillator was 100-200 MHz and the input frequency was 790 MHz. The display of the counter now shows:

A. 790 MHz

B. 789 MHz

C. 786 MHz

A	
B	
C	

Q.3.8. The measuring time of an automatic heterodyne converter is:

A. Shorter than

B. Longer than

C. The same as that of an automatic transfer oscillator for the same resolution.

A	
B	
C	

Q.3.9. The frequency measured by an automatic divider plug-in is:

A. The local oscillator frequency (times N)

B. The mixed product

C. The unknown frequency divided by the scaling factor

A	
B	
C	

Q.3.10. It is desired to do without the preset facility in a presettable counter with a 5-decade time base preset (see fig. 3.15). Instead of switching off the complete scaler chain, one could achieve the same result by presetting the scaler to:

A. 99999

B. 00000

C. 00001

A	
B	
C	

Q.3.11. The BCD output of a reciprocal counter always gives the:

A. Period

B. 10^n - 1 complement of the period

C. Frequency

A	
B	
C	


TAXI

Chapter 4
Accuracy

In the previous chapters of this book we have discussed the design of the digital counter and the various types of measurements that can be performed with it. As we have already mentioned, one of the very great advantages of this type of instrument is the possibility of very high accuracy. We say "possibility" because there are quite a number of cases where the instrument can produce wrong answers. Recognition and understanding of the sources of the errors will help the user to find ways of reducing their effects, thus increasing the utility of measurements with digital counters.

Although counters often have quite a large number of digits (8 or even more) this does not give any guarantee of accuracy but merely the possibility of a rather high resolution. The accuracy depends on other factors.

The errors to which digital counters are liable may be divided into two main categories:

a) errors inherent in the digital system itself and
b) errors specific to the measuring mode involved.

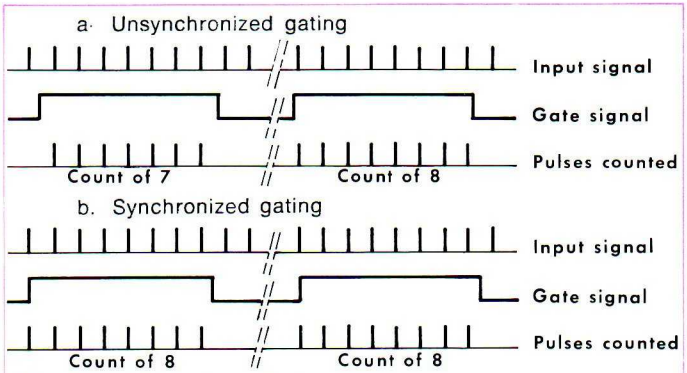


Fig. 4.1. ± 1 count ambiguity.

Inherent errors

The ± one count error

The basic error for all digital instruments is the ± 1 count error, which is due to the fact that the two signals applied to the main gate are not usually synchronized. As may be clearly seen from fig. 4.1., if gating is unsynchronized the numbers of pulses passed by two successive gating pulses, and hence the counts, may differ by 1. This ± one count error naturally applies only to a single measurement: in a series of measurements, the final answer can be averaged and the error may be very greatly reduced.

The relative error caused by this ± 1 count ambiguity is of course a function of the number of counts, as may be seen from the following equation:

$$\text{Relative error} = \frac{1}{\text{number of counts}} 100\%$$

This relation is given in graphic form in fig. 4.2.

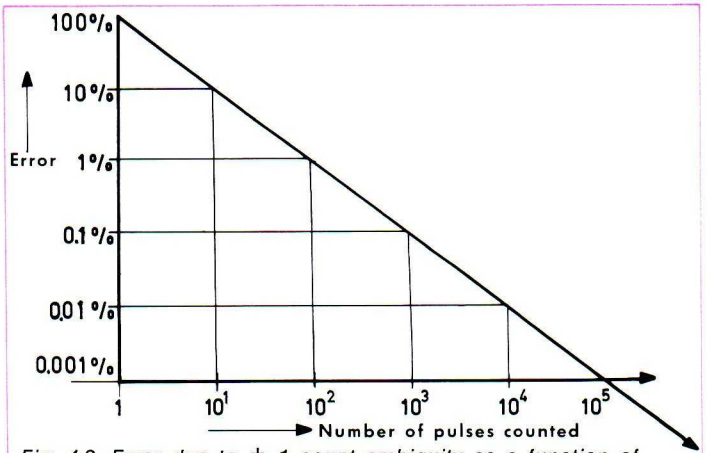


Fig. 4.2. Error due to ± 1 count ambiguity as a function of number of pulses counted.

Time-base error

The other major factor determining the accuracy of the counter system as such is the stability of the time base. As most counters use a crystal oscillator to produce the clock pulse, the main factors which could affect the accuracy of the clock frequency are temperature, long-term and short-term stability and supply voltage variations.

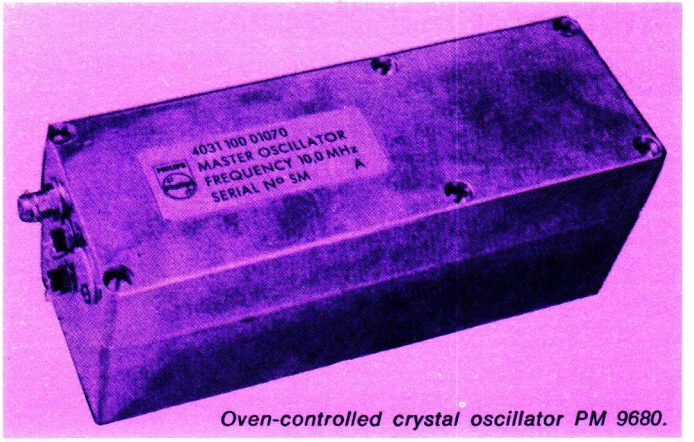
The *temperature* dependence can be minimized by choosing a crystal cut with a low temperature coefficient, or by operating the crystal at a fixed temperature at which the temperature coefficient is zero (the turning point; see fig. 4.3.). A typical temperature coefficient in a range of ± 1 °C around the turning point is about 5×10^{-9}/°C. When better performance is required, the quartz oscillator must be operated in a thermostatically controlled oven, accurately set to the turning point of the crystal. Even better performance can be obtained by making the oven proportionally controlled. The Philips type PM 9680 oven-enclosed crystal oscillator has proportional control and its temperature coefficient is of the order of 5×10^{-10}/°C.

The *long-term drift* (aging) of the crystal oscillator is due to migration of small particles between the quartz slice and its vapour-deposited electrodes. Aging rates depend strongly on the quality of the quartz crystal but are highest during the first month of operation. Better types of crystal oscillators have an aging rate of less than 2.10^{-8} per year (see fig. 4.4. and 4.5.).

The short-term *stability* is mainly affected by defects in the crystal grid and instability of the oscillator circuit. It is by nature non-systematic, i.e. it causes the frequency to fluctuate about the (long-term) mean value. It is therefore very difficult to define the short-term drift exactly. It is generally specified as the root mean square (RMS) of the frequency deviation over a certain averaging time. The better types of crystal oscillators give values of a few parts in 10^{10} per second of averaging time (under constant environmental and supply-voltage conditons) and a few parts in 10^{9} in 24 hours averaging time (see fig. 4.4.).

The last important factor influencing the accuracy of the crystal oscillator accuracy is the *stability of the power supply*. Good stabilized power supplies give clock frequency variations of a few parts in 10^{10} per 10% line-voltage variation.

It will be clear from the above that all these factors should be taken into account when determining the accuracy of digital measurements.



Oven-controlled crystal oscillator PM 9680.

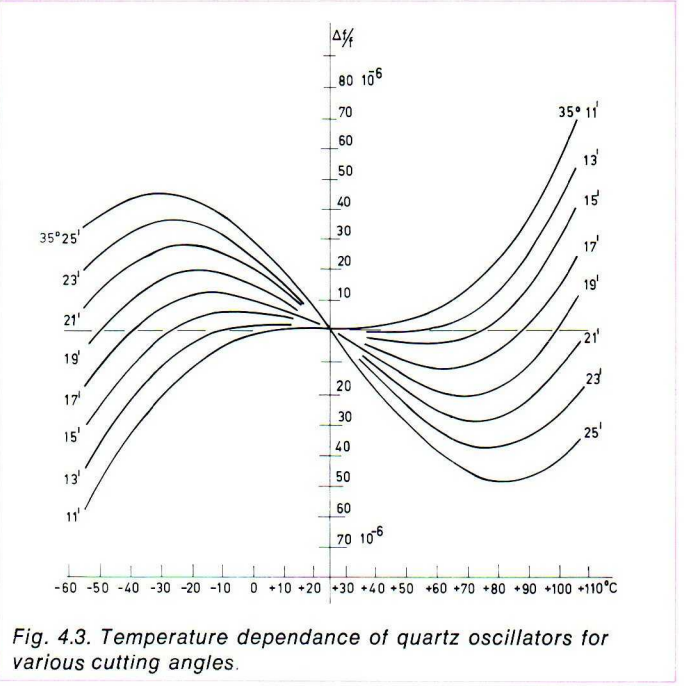


Fig. 4.3. Temperature dependance of quartz oscillators for various cutting angles.

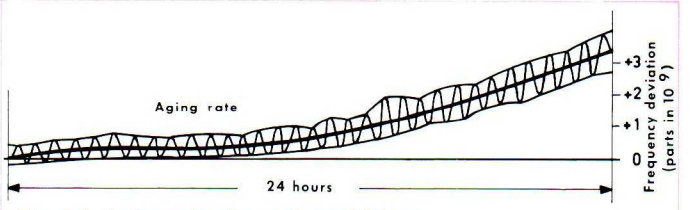


Fig. 4.4. Aging rate of quartz oscillators.

Furthermore, when a crystal oscillator is used for a considerable period of time, the cumulative effect of the above-mentioned factors may cause its frequency to drift beyond the permissible limits. It will therefore be necessary to recalibrate the oscillator from time to time. It is common practice to do this with a reference source whose accuracy is at least one order of magnitude better than that of the unit to be calibrated.

The best standard is an atomic frequency standard; this is available from three different classes of devices ("atomic clocks"):

a) masers (hydrogen or ammonia type)
b) atomic-beam resonators (cesium type)
c) gas cells (rubidium type).

The atomic clock is based on the use of a periodic phenomenon, viz atomic or molecular oscillations. It uses the frequency of a spectral line emitted by an atom on passing from a higher to a lower energy level which is very accurately defined and unaffected by temperature, aging etc. Typical stabilities of atomic frequency standards are about $1x10^{-12}$ for the maser throughout its life, a few parts in 10^{-12} for the cesium-beam resonator throughout its life, and about $2x10^{-11}$ per month for the rubidium gas cell.

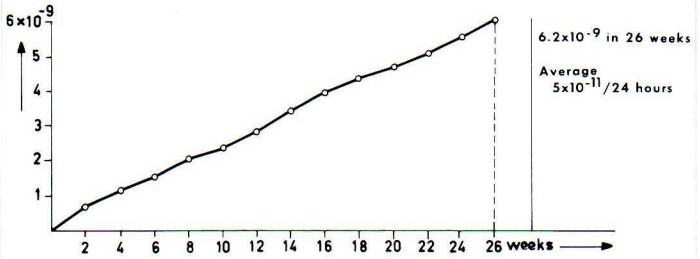


Fig. 4.5. Aging characteristic of Philips PM 9680 crystal oscillator in proportional controlled oven.

Unfortunately, atomic frequency standards are too expensive for most users of digital counters. However, there is generally a possibility of using these standards indirectly for calibration, since most governments or broadcasting authorities broadcast radio signals at standards frequencies, which are controlled by atomic standards. The stability of these frequencies is of the order of a few parts in 10^{11}. When using such a type of frequency standard one should remember that radio transmissions are subject to a variable propagation delay, especially in the higher frequency region when the propagation involves reflection from the ionosphere. As the ionosphere moves up and down, the carrier frequency will be phase modulated. This results in a frequency error which increases with the distance between transmitter and receiver for the higher carrier frequencies. Errors of the order of a few parts in 10^7 can easily occur here. It is therefore much better to use VLF carriers (10-100 kHz) for calibration purposes because here the errors are much smaller (propagation occurs mainly via the ground wave). Most standard frequency carriers contain some kind of modulation for timing purposes and cannot therefore be used directly for calibration. Special receivers has been built for this purpose; they generally compare a local standard frequency with the carrier frequency received, and display the difference.

	PM 9680	PM 9681
Frequency	10 MHz	10 MHz
Aging	$1.5x10^{-9}$/24 h*)	$5x10^{-10}$/24 h*)
Temperature	$\pm 5x10^{-10}$/°C**)	$\pm 5x10^{-10}$/°C**)
Line voltage ($\pm$ 10%)	$1x10^{-10}$	$1x10^{-10}$

*) Average after 72 hours of continuous operation **) Average

Table 4.1. Characteristics of Philips oven-controlled crystal oscillators.

Errors dependent on the functional mode

Frequency-mode errors

In the first place, the accuracy of a frequency measurement by a counter is influenced by the ± 1 count ambiguity and the clock accuracy. The effects of these two factors can be combined in one diagram (fig. 4.6.).

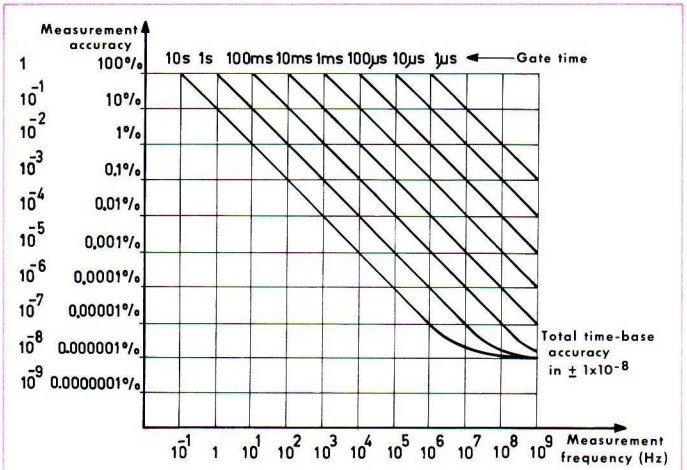


Fig. 4.6. Frequency error as function of gate time, ± 1 count ambiguity and clock accuracy.

A numerical example:

Frequency 10^8 Hz
Gate time 1 s
Number of pulses 10^8
Display accuracy ± 1 digit
Time base accuracy ± 1 digit
Total accuracy ± 2 digits = 2×10^{-8}.

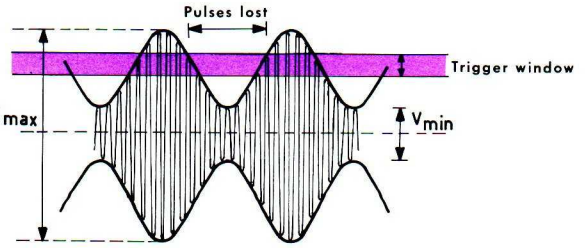


Fig. 4.7. Error caused by amplitude modulation.

Other errors in frequency measurements can be due to amplitude modulation, frequency modulation, noise and other interfering signals.

When an amplitude-modulated signal is to be measured an error can occur when the trigger level is set incorrectly; this can be seen clearly from fig. 4.7.

When however the trigger level is set correctly, e.g. symmetrically around the zero line, the measured value will be correct as long as V_{min} is larger than the trigger window.

A special case of amplitude modulation (pulse modulation or RF burst signals) requires special attention: when the selected gate time is of the same order as or greater than the burst time, enormous errors can occur. It is characteristic of RF burst signals that the "burst on" time is small compared with the "burst off" time. (See fig. 4.8.). A typical example of such a signal is the colour burst in video signals. If for instance the burst time is 200 μs and the "burst off" time is 10 ms, the chance that the gate time (which should be 100 μs or smaller) falls exactly within the 200 μs burst time is extremely small; in practise the burst signal will be "sliced" by two successive gates giving an erroneous, unstable reading. The solution to this problem is clearly synchronized gating. This is achieved as follows. At the start of the measurement the time-base divider is set as usual to 99...9, but does not start counting until it receives a command. (The time-base divider is than said to be "armed".) In the absence of a signal nothing happens, but as soon as the first pulse of the burst arrives the time-base divider starts counting (an additional gate is required for this purpose; see fig. 4.9.). The gate time is then synchronous with the burst period, and as long as this gate time is smaller than the burst period the counter will display the correct frequency. The best method of measurement in the "armed" burst mode is to start with the smallest possible gate time and increase this until an unstable reading is observed. The time-base selector is then set back one step, to give the correct answer with the highest possible resolution. An automatic "burst" mode is build into the Philips PM 6650 counter/timer.

In case of frequency-modulated signals one cannot of course speak of one specific frequency because the frequency is changing all the time. The frequency displayed by a counter will then be an average over the gate time chosen. In practise however the displayed value will be very close to the actual value, especially when the gate time is a multiple of the modulation period. Care should of course be taken to ensure that the frequency excursion of the FM signal remains within the pass band of the counter. If the input signal is mixed with another signal, as is usually done with heterodyne converters, care must be taken to

ensure that the FM signal does not drive the mixer output via a zero beat, as this would lead to an appreciable error.

Noise is another factor which can greatly affect the accuracy of the measurement, when the peak-to-peak value of the superimposed noise signal is large enough to cause extra "triggers" as depicted in fig. 4.10a. In this case extra counts will be registered. This error will be greatest when the trigger window is around the part of the signal with a rather low slope (fig. 4.10b.). There are quite a number of methods of avoiding the errors due to noise. One point which should be remembered is that in this case it is the absolute value of the noise that is important, and not the signal-to-noise ratio. One useful method of combatting this error is thus to adjust the signal level to such a value that the **noise** amplitude is smaller than the trigger window (fig. 4.10c.). A numerical example will illustrate this. Suppose that a RF frequency meter (e.g. Philips PM 6645) with 5 mV sensitivity, (i.e. 15 mV trigger window) has to measure a 1 V RF signal with a 100 mV_{pp} noise signal superimposed. In this case the measurement will not be correct because the noise is triggering the pulse shaper, so too many pulses are counted. If the input signal is attenuated e.g. 100x, however, the noise signal is well within the trigger window and the signal is still 10 mV_{rms} (more than enough for accurate counting): the reading will thus be correct.

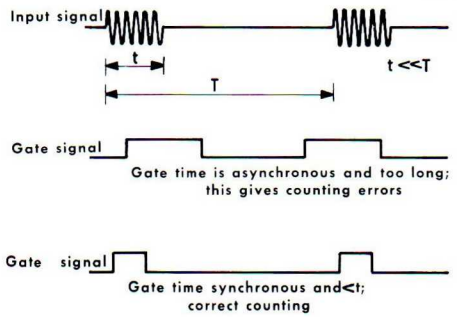


Fig. 4.8. Burst frequency measurement.

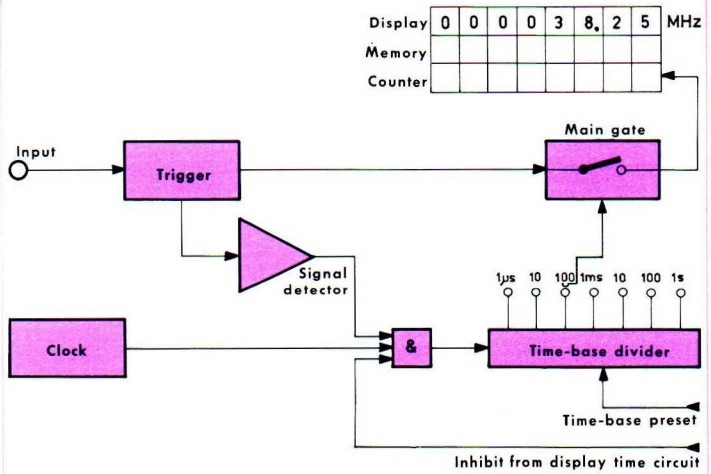


Fig. 4.9. Simplified block diagram of burst frequency mode.

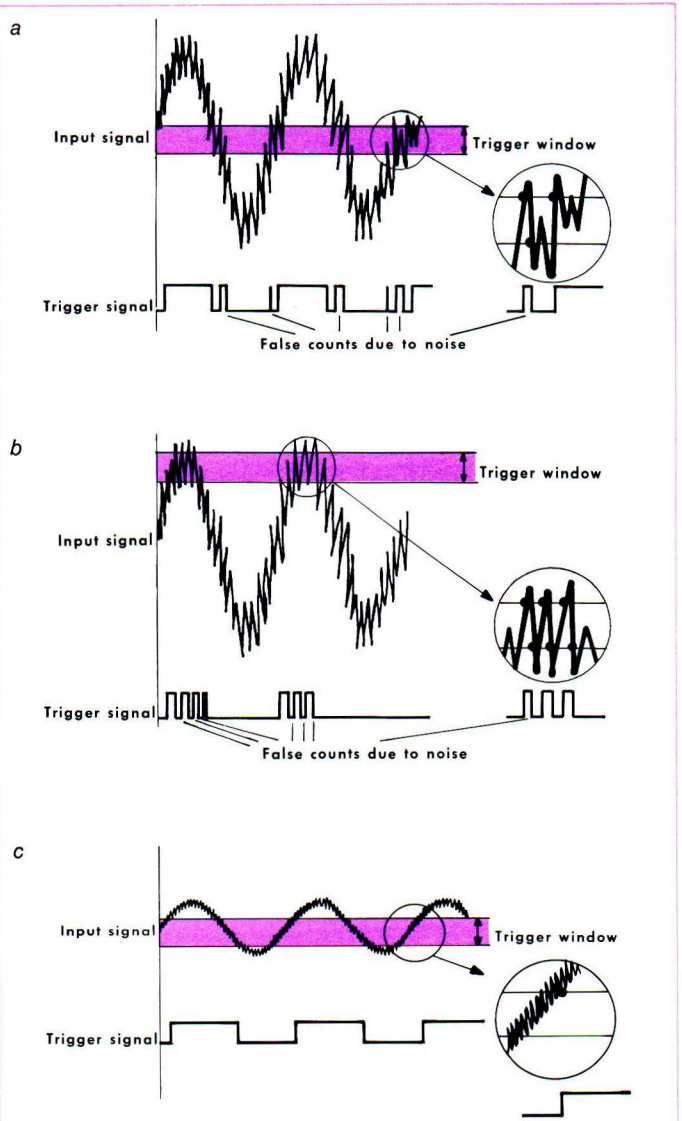


Fig. 4.10. The influence of noise.

Since the amplitude of the noise is not generally known in practice the measurement should be started with maximum sensitivity (minimum attenuation) and the attenuation increased until a stable frequency reading is obtained. An even simpler solution of course is to build into the counter an automatic gain control (ACG) which regulates the signal to a value that is just sufficiently larger than the trigger window to ensure a correct reading. (Such an AGC is incorporated in the Philips counters PM 6645 and PM 6650).

The above method works very well for RF measurements where the amplitude of the noise is smaller than the actual signal. Interference signals from power switches, welding machines, electric motors, thyristor control stages, etc., which are of the same amplitude as the RF signal (or larger), do of course cause false trigger pulses, but as their repetition frequency is so much lower than that of the RF signal to be measured they have hardly any influence on the accuracy of the RF measurement.

In low-frequency measurements, on the other hand, these interference spikes can seriously influence the accuracy of the measurement. The best method of avoiding this kind of error is to switch a filter in front of the counter to reduce the effect of the interference signals. The disadvantage of such filters is that in order to be effective they must have the lowest possible lower cut-off frequency, which can give difficulties if one has to measure frequencies close to this lower cut-off frequency. Special LF counters have overcome this problem with the aid of an ingenious automatic

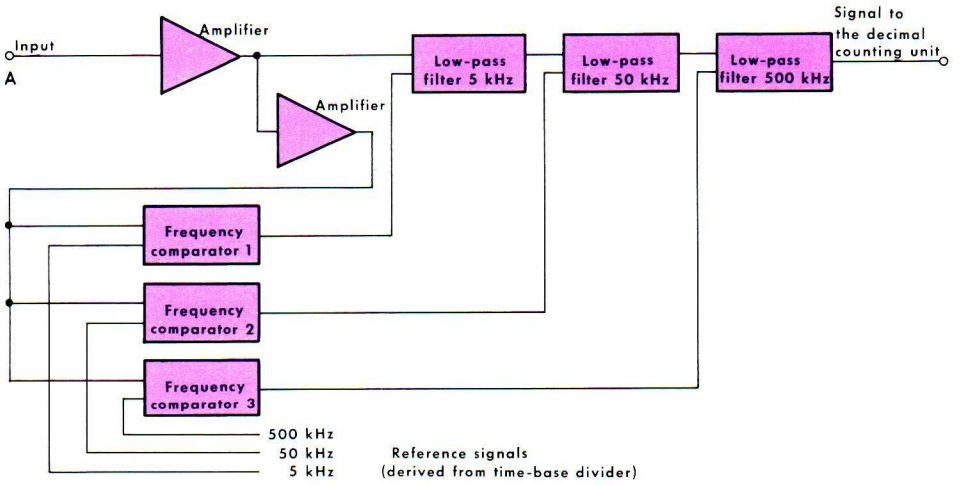


Fig. 4.11. Simplified block diagram of automatic noise filter.

Principle of operation of the automatic noise filter

The noise-rejection performance of these instruments is based on a 3-stage filter (cut-off frequencies at 5, 50 and 500 kHz. These three stages are automatically selected as a function of the frequency of the signal under test.

The signal frequency is simultaneously compared with 3 difference frequencies in 3 different comparators.

If the signal under test has a frequency lower than 500 kHz, frequency comparator III activates the 500 kHz low-pass filter (via an electronic switch). If the signal under test has an even lower frequency (below 50 or 5 kHz), the other filters are also switched in as appropriate.

noise filter which rejects **all** signals with a frequency higher than that of the signal under test (see fig. 4.11.), which is self-explanatory).
It will be clear from the above that the position of the trigger window with respect to the signal to be measured (the trigger offset) can be of great importance in determining the accuracy of the measurement. Good counters should be provided with controls for varying the offset of the trigger window, and with means of monitoring the trigger level. Philips counters PM 6630 and PM 6650 have for this purpose a special trigger-level output socket to which a DVM or oscilloscope can be connected. Fig. 4.12. shows some more examples of correct and incorrect trigger-level settings.

Another possible source of errors is a spurious signal of about the same amplitude as the signal to be measured. If the frequency of the undesired signal is much higher than the frequency to be measured, it can be handled in the same way as a noise signal. It will be present as a band along the lower-frequency signal and as long as the peak-to-peak amplitude of the higher-frequency signal is smaller than the hysteresis the lower frequency will be measured correctly. The same applies to spurious signals below the frequency to be measured. If however the amplitude of the spurious signal is greater than the hysteresis, errors may be produced - depending on the frequency ratio and the two amplitudes. When the undesired frequency aproaches the frequency to be measured the error becomes smaller. A useful guide to what to expect is given by the parameter K, defined by:

$$K = \frac{V_H}{\frac{F_L}{F_M}V_L + \triangle}$$

where:
V_H is the peak-to-peak amplitude of the higher frequency signal, and
V_L that of the lower-frequency signal,
F_H the higher frequency,
F_L the lower frequency,
$\triangle$ the hysterisis or trigger window.
When $K >> 1$ the higher frequency will be measured, whereas when $K << 1$ the lower frequency will be measured. The closer K is to 1, the greater the chance of counting errors.

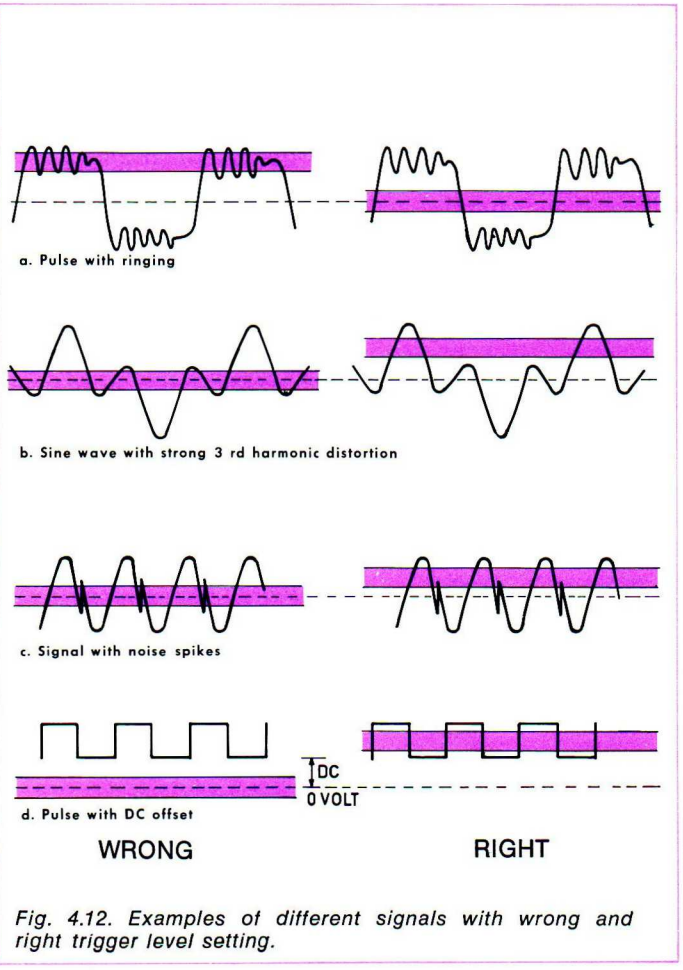


Fig. 4.12. Examples of different signals with wrong and right trigger level setting.

Period-mode errors

As in the frequency mode, the clock accuracy and the ± 1 count ambiguity are the primary sources of error here too. A typical period-mode error is the trigger error, i.e. the error in the time at which the main gate is opened and closed. In the frequency mode the main gate is opened and closed by the fairly clear-cut time-base signal. In the period mode, however, the main gate is operated by the signal to be measured which may contain hum, noise or interference spikes - all of which could offset the triggering point. Drift of the trigger level could cause error too.

All these possible sources of error could cause the main-gate time to be too long or too short, or could even cause the main gate to open too often.

This can be explained as follows (fig. 4.13.).

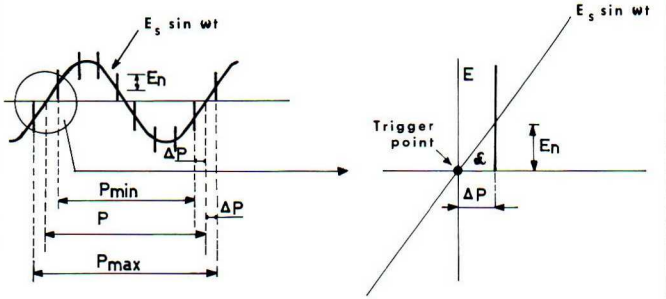


Fig. 4.13. Influence of noise in period-mode measurements

If the slope (assumed constant) of the signal at the trigger point is $S = \tan \alpha$ (V/s) and the noise amplitude is E_n, we may write: $S = \tan \alpha = \frac{E_n}{\triangle p}$ (volt/s) (1)

If we assume the signal to be sinusoidal and given by $E_s \sin \omega t$, we can calculate the slope of this signal at the trigger point as follows.

$\frac{dV}{dt} = E_s \omega \cos \omega t$ and at $t = 0$:

$$\frac{dV}{dt} = E_s \omega = E_s\, 2\pi f = E_s \frac{2\pi}{p} \qquad (2)$$

At the trigger crossing (1) = (2), so

$$\frac{E_n}{\triangle p} = \frac{E_s 2\pi}{p} \quad \text{and} \quad \frac{\triangle p}{p} = \frac{E_n}{2\pi E_s} \qquad (3)$$

and as this error can be producted twice (at opening and closing), the total error is given by $\frac{2\triangle p}{p} = \frac{1}{\pi} \frac{E_n}{E_s} \cdot 100\%$

For a S/N of 40 dB this gives $\frac{1}{\pi} \cdot \frac{1}{100} \cdot 100\% \approx 0.3\%$ so a 1% noise can give a 0.3% time error for sinusoidal signals.

This calculation shows clearly that the trigger error depends not only on the noise voltage (ratio) but also on the slope of the signal to be measured.

For instance if we want to measure the period of a square-wave signal with a rise time which is e.g. 1% of the period of the signal the slope $\frac{dV}{dt}$ at the trigger point would be:

$\frac{dV}{dt} \approx \frac{E_s}{0.01p}$ and

$\frac{E_s}{0.01} = \frac{E_n}{\triangle p}$ so that

$\frac{2\triangle p}{p} = 2\frac{E_n}{E_s} \cdot \frac{1}{100} \cdot 100\%$

which is $\frac{50}{\pi}$ times better than for a sinusoidal signal.

On the other hand, if the trigger level were shifted to the flat top of the sine wave, the error could be enormous.

It will be clear from the above that the high accuracy of the clock frequency and the ± 1 count ambiguity hardly count when it comes to the over-all accuracy of single-period measurements on sinusoidal signals.

Fortunately, as we have explained in chapter 2 there is a way of improving the accuracy. Since the error is only made at the moment of opening and closing the gate the multiple-period mode provides the solution. If we measure e.g. 10 consecutive periods the relative error is reduced by a factor of 10: the absolute error is still $2\triangle p$, but the denominator in the formula (3) is now 10 times larger:

$$2\frac{\triangle p}{10p} = \frac{1}{\pi} \frac{E_n}{E_s} 100\% \text{ (for a sinusoidal signal)} \qquad (4)$$

So the more periods we count the better the accuracy, until the total error is practically reduced to the standard ± 1 count ± clock accuracy. The combined result of the various sources of error is given in the graphs of fig. 4.14.

Summarizing, we may list the basic conditions for good measurements as follows: the trigger window should be set at a clean part of the signal, where the signal slope is maximum, the count should be made over as many periods as possible (this involves use of the multiple mode), the signal-to-noise ratio should be high.

Errors in the time-interval mode.

In this mode, we find the same main sources of error as in the period mode, viz. clock accuracy, ± 1 count ambiguity and trigger errors. As time-interval measurements are nearly always performed on pulse-shaped signals (mea-

surement of rise and fall times, pulse width etc.) the trigger error is generally specified as:

$$\triangle t = \pm \frac{E_n}{S},$$

where:
$\triangle t$ = error in seconds,
E_n = peak noise voltage,
S = (tan α) = signal slope (V/s).

It follows from the above formula that the better the signal slope at the triggering point, the smaller the measurement error; this is illustrated in fig. 4.15. The over-all error naturally decreases as the time interval to be measured increases. Fig. 4.16. shows this total error due to clock accuracy, ± 1 count ambiguity and trigger error at constant noise amplitude as a function of the total time interval (T) measured, for a number of different signal slopes:
Total error:

$$\frac{2\triangle t}{T} = \frac{2E_n}{ST}\ 100\% \pm 1 \text{ count} \pm \text{clock accuracy}.$$

So far the errors in the time-interval mode followed the

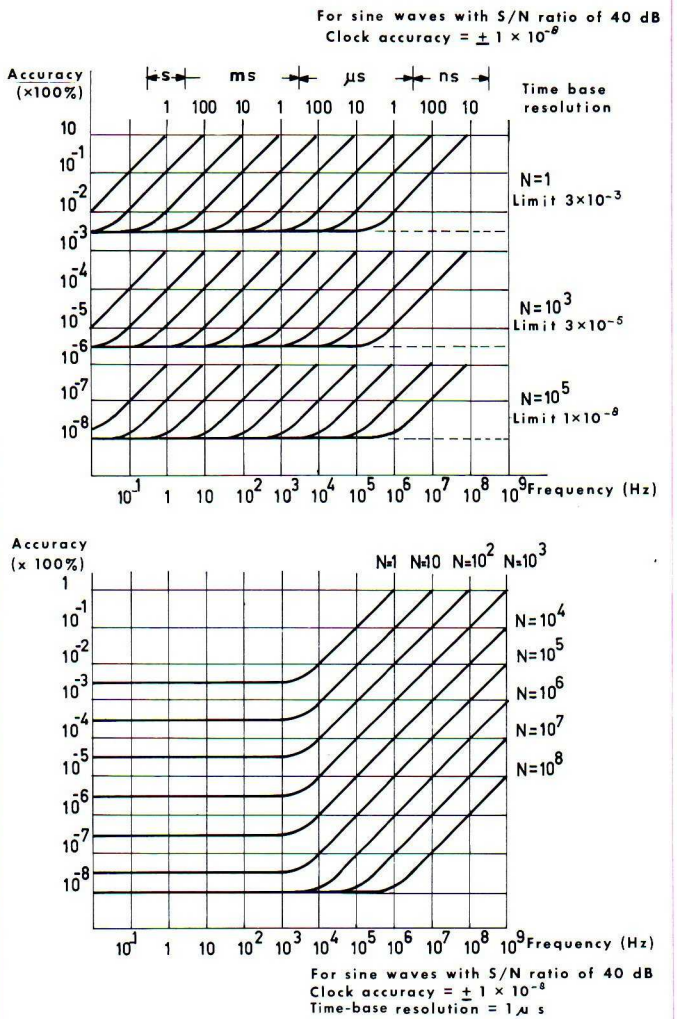


Fig. 4.14. Accuracy as factor of time-base resolution, clock accuracy, ± 1 count ambiguity and multiplier factor (N) for period mode

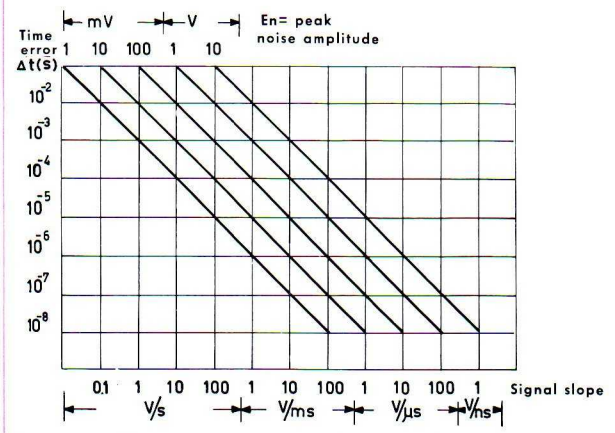


Fig. 4.15. Time error (Δt) as function of peak noise voltage (E_n) and signal slope

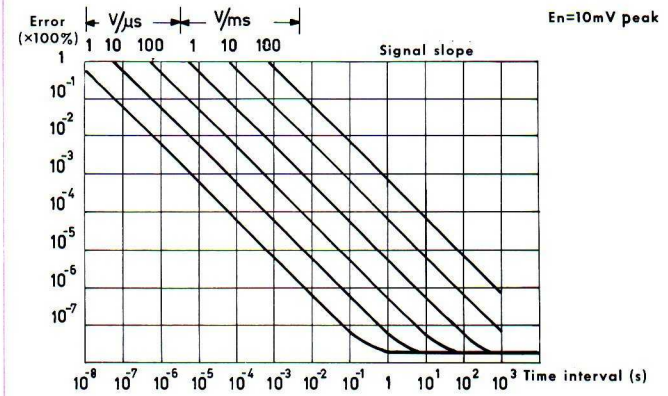


Fig. 4.16. Total error in time-interval measurements as function of total time interval and signal slope

rules discussed above. There are however some additional error sources here which are not found in the frequency and period modes. One of these sources is the trigger window itself.

Fig. 4.17a. shows how triggering occurs normally in measurement of e.g. pulse width, where the trigger level is set to 50% of pulse amplitude. Owing to the hysteresis of the trigger circuits, triggering will not occur at the trigger level set (points A and B (t_1)) but somewhat later: at a higher voltage when the trigger slope selected is positive (point A') and at a lower voltage (point B') when the slope selected is negative.

As a result, the time measured in the above example (t_2) will be longer than it should be. The error due to trigger hysteresis can be calculated in the same way as that due to the influence of noise signals:

$$\triangle t = \pm \frac{E_n}{2S_1} \pm \frac{E_n}{2S_2}$$

where:

$\triangle t$ = error in seconds;
E_n = trigger window (in V);
S_1 = slope (in V/s) of the first trigger pulse (start);
S_2 = slope (in V/s) of the second trigger pulse (stop).

However, modern time-interval counters (such as the Philips PM 6650) have a built-in compensation network that automatically eliminates this error by shifting the trigger window down by half the hysteresis band for positive slopes and upwards for negative slopes, so that triggering really does occur at points A and B, see fig. 4.17b.

Another source of error is the setting of the trigger level. For example, if we want to measure pulse widths we set the trigger level to 50% while for rise-time or fall-time measurements we need two trigger levels at 10% and 90%. Errors in these settings are not corrected by trigger hysteresis compensation; e.g. a 5% setting error in a trigger range of 1 V gives a 50 mV level error, the full weight of which is felt in the over-all error equation. The same applies to drift of the set trigger level. Care must therefore be taken to ensure very stable trigger-level circuitry. The result of these setting errors can be expressed in the equation below.

$$\triangle t = \pm \frac{E_1}{S_1} \pm \frac{E_2}{S_2} \text{ seconds}$$

where:

$\triangle t$ = error in seconds;
E_1 = level setting error or level drift (in V) in the start channel;
E_2 = level setting error or level drift (in V) in the stop channel;
S_1 = signal slope (V/s) in the start channel;
S_2 = signal slope (V/s) in the stop channel.

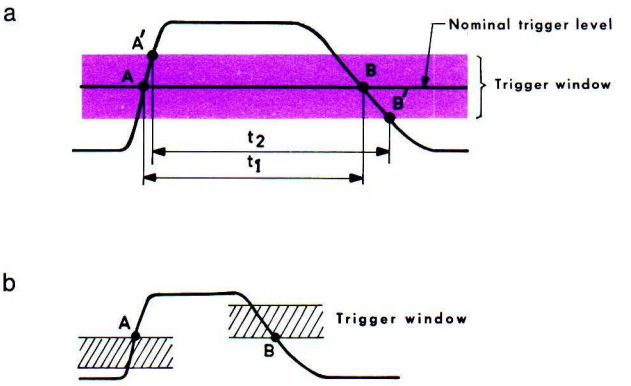


Fig. 4.17a. Trigger hysteresis error
Fig. 4.17b. Compensation of error due to trigger hysteresis

These errors can be corrected if we have a facility for measuring the set level. The Philips counters PM 6630 and PM 6650 have two analog outputs for this purpose; e.g. a digital voltmeter connected to one of these outputs can be used to monitor high-accuracy setting of the required levels.

However, this method can only be used if the signal amplitude is known exactly. Since e.g. for a rise-time measurement we need to set the trigger levels at exactly 10% and 90% of the signal amplitude, when the signal level is not known one has to use other methods to improve the accuracy.

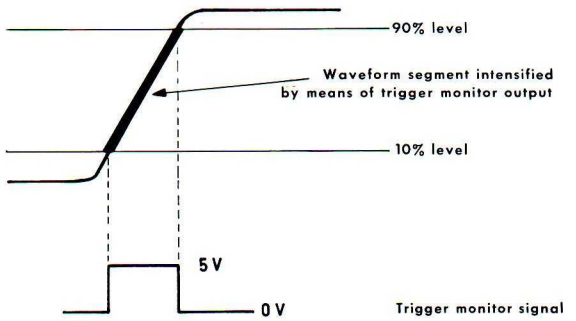


Fig. 4.18. Segment intensified by means of gate output

One possible method, used in the PM 6650, is to monitor the time interval to be measured on an oscilloscope screen. The gate signal (representing the time between opening and closing of the main gate) is available at an additional output and may be used for intensifying (Z-axis modulation) the waveform segment over which the time interval is measured (see fig. 4.18.).

So far we have been discussing errors caused by imperfections in the trigger circuit. There are of course many other possible errors. A difficult one to cope with in conventional counters is a sudden noise peak in the "stop" channel due e.g. to contact bounce in time measurements on mechanical relays. This spurious "stop" signal leads to too low a result in a count-up counter. Special trigger-hold-off (trigger masking) circuits have been developed to solve this problem.

The operation of a trigger masking circuit is illustrated in fig. 4.19. The masking time - which is controlled by a control knob on the front panel - begins at the instant the start channel is triggered. During this masking time the stop channel ignores all trigger pulses. As soon as the masking (trigger hold-off) time is over, the stop channel is in normal working condition again. The precision of this delay setting is not very important, though of course the delay must not be so long as to mask the real stop pulse. In practice, there is generally a special mask-check position on the function switch by means of which the masking time is accurately measured by the counter.

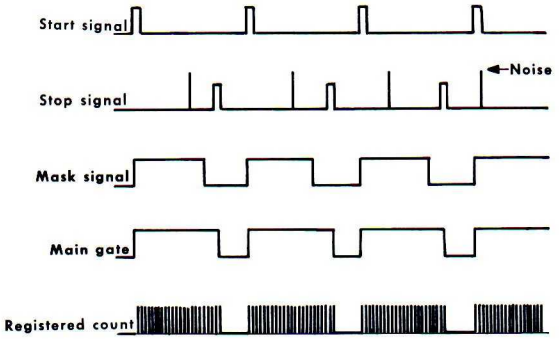


Fig. 4.19. Masking in time-interval measurements

This masking facility is particular useful for measurement of the closing time of a relay, where contact bounce generally gives problems: instead of measuring the correct closing time, most timers will measure only the duration of the first bounce. With the masking circuit, the effect of the bounce time can be eliminated by adjusting the delay to be longer than the bounce period (fig. 4.20).

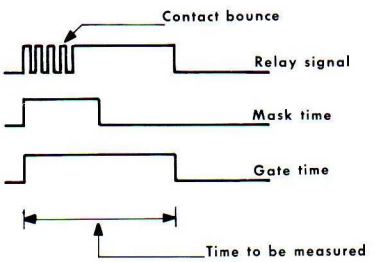


Fig. 4.20. Time measurements on relays with contact bounce

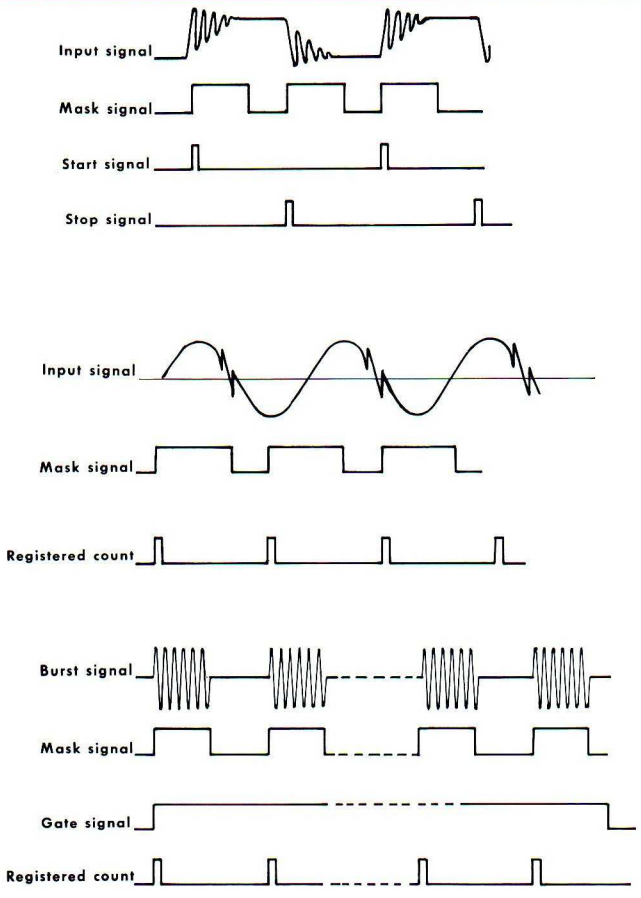


Fig. 4.21a. Pulse-width measurement on a signal with considerable "ringing"
Fig. 4.21b. Frequency measurement on signals with noise
Fig. 4.21c. Burst measurements

Other examples of the application of masking are given in fig. 4.21.

Finally, one error frequently overlooked is that caused by non-identical start and stop channels. Especially in the sub-nanosecond range, we need very fast, identical channels. Differences in propagation delay between the two channels cause systematic errors which cannot be eliminated. The same applies to connection cables of different lengths (a 20 cm difference in cable length gives a systematic error of 1 ns!). High-performance time-interval counters (like the PM 6650) therefore have carefully equalized start/stop channels, and the user should take care to ensure that the two connecting cables are identical in all respects.

As we have seen above, there are quite a number of factors which can drastically reduce the accuracy of measurements in the time-interval mode. In the period mode we learned that we could considerably improve the accuracy by switching to the multiple-period mode, since the errors only occur at the opening and closing of the main gate in this mode. This advantage does not apply to the time interval average mode, however, because here the gate is opened and closed at the start and finish of each time interval; so instead of being averaged out, the trigger error and $\pm$ 1 count ambiguity actually can accumulate.

However, the "average" mode does improve this situation too. Provided the signal is periodic (T is constant, fig. 4.22.) and the frequency (1/T) is not synchronous with the clock frequency, (criterion of randomness), the time interval $\triangle t$ can be measured with fairly high resolution and accuracy by averaging over say 10^N periods: this gives N more digits' resolution, and since this is a statistical measurement the error is reduced by a factor of $\sqrt{10^N} = 10^{N/2}$.

In principle the number registered in the digital counting unit (DCU) will always be a multiple of the clock period, but there are ways of measuring fractions of the clock period. A numerical example will clarify this (fig. 4.22.).

The time interval to be measured here is 14 ns and the clock-pulse duration is 10 ns. Now it can be proved that in this case the DCU will register 1 count in 60% of the time intervals, and 2 counts in 40%.

This means that after 1000 consecutive time-intervals 1 count will have been registered in 600 intervals (600x10 ns = 6000 ns) and 2 counts each in 400 intervals (400 x 20 ns = 8000 ns). The total count will then be 14000 ns over 1000 intervals, giving an average of 14 ns/interval.

This rule is also valid for time intervals smaller than the clock frequency. For example, with an 8-ns time interval we get: 20% no count; 80% 1 count:

200 x 0 ns = 0
800 x 10 ns = 8000
total count 8000 ns per 1000 intervals = 8 ns/interval.

However, this calculation is only valid if we have transformed the consecutive time intervals into multiples of the clock period, in other words if we have removed the $\pm$ 1 count ambiguity. This is done by the coincidence circuit shown in fig. 4.23., which works as follows. First, the start pulse is stored in flip-flop A (Q_A is HIGH) at time 1; the D input of flip-flop C will then become HIGH too, and the next clock pulse (at time 2) will toggle flip-flop C so that $\overline{Q}_C$ goes LOW.

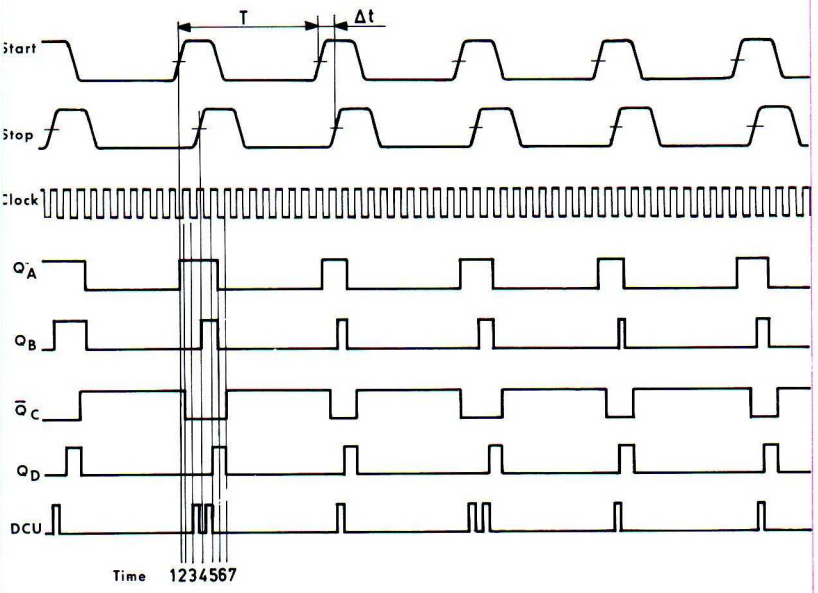


Fig. 4.22. Counting fractions of a time interval in the time-interval average mode

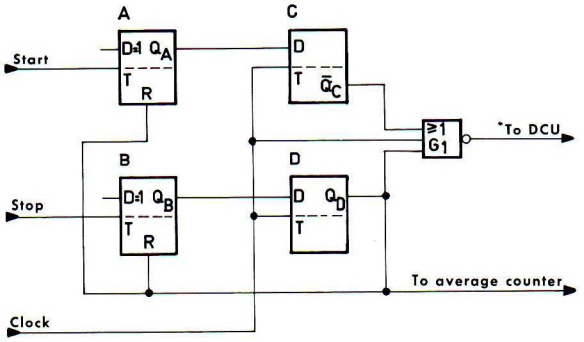


Fig. 4.23. Synchronous gating in the time-interval average mode

When the clock pulse disappears (time 3) all inputs to the coincidence gate are LOW so the output of gate 1 goes HIGH and delivers the first pulse to the DCU (start sequence). The stop sequence goes as follows: At time 4 flip-flop B is set; at the next clock pulse (time 5) Q_D goes HIGH, blocking gate 1. The output of flip-flop D is also used for resetting flip-flops A and B, which occurs after some delay (time 6). Finally, since Q_A and Q_B are LOW again, the next clock pulse will reset flip-flops C and D (time 7) and a new sequence can start. In the above example we have worked with a very small time interval (1 or 2 counts) but the circuit will of course also work with any number of counts in a given interval. The circuit described above is incorporated in the Philips PM 6650 counter/timer.

Errors in the pulse-width mode

As the pulse-width mode is basically a special version of the time-interval mode, the errors will be governed by the considerations discussed above.

Errors in the ratio mode.

Just as in the period mode, the trigger error and the ± 1 count ambiguity have to be taken into account here.
Use of the multiple-ratio mode improves the accuracy, just as use of the multiple-period mode makes period measurements more accurate.

Conclusion

Summing up, we may state that the digital counter/timer can be a very accurate measuring instrument provided one understands and recognizes the possible sources of error and takes the appropriate measures to minimize their effect. In general:

— A steady reading is usually correct
— An unstable reading is definitely wrong
— When in doubt, monitor the signal to be measured with an oscilloscope, and if possible display the trigger levels or gate pulse on the screen at the same time.

Questions

Q.4.1. For a given resolution, the measuring accuracy when using a 10-times prescaler is
A. The same as,
B. Better than,
C. Worse than for the same measurement without prescaling.

A	
B	
C	

Q.4.2. A heterodyne converter is connected to a 500 MHz frequency meter. The converter can operate in 100 or 200 MHz frequency steps; which gives the best accuracy?
A. 100 MHz steps
B. 200 MHz steps
C. Does not matter.

A	
B	
C	

Q.4.3. In order to reduce the $\pm$ one count ambiguity in time-interval measurement, one should
A. Increase the clock frequency
B. Decrease the clock frequency
C. Improve the clock stability.

A	
B	
C	

Q.4.4. Measurement on a 100% amplitude-modulated signal can be performed
A. Using any counter
B. Only with aid of a counter with special facilities
C. Is never possible.

A	
B	
C	

Q.4.5. A frequency of 10 kHz with a signal/noise ratio of 40 dB is measured in
A. The frequency mode with a gate time of 1 s
B. The period mode with a resolution of 100 μs
C. The multiple-period mode with N = 1000.
The clock accuracy is 10^{-8}

a. Which of the three measuring modes gives the highest accuracy?
A. Frequency mode
B. Period mode
C. Multiple-period mode

A	
B	
C	

b. Which of the three modes gives the shortest measuring time for a given accuracy?
A. Frequency mode
B. Period mode
C. Multiple-period mode

A	
B	
C	

Q.4.6. An RF burst signal with a burst repetition rate of 10 ms and a burst time of 1 ms is measured with the frequency meter in the burst mode. The gate time should be
A. $\leqslant$ 1 ms
B. $\geqslant$ 1 ms
C. $<$ 1 ms

A	
B	
C	

Q.4.7. A microwave signal can be measured e.g. with the aid of an automatic heterodyne converter or an automatic transfer oscillator. For a given measuring time, the highest accuracy is achieved with
A. The automatic transfer oscillator
B. The automatic heterodyne converter
C. Doesn't matter which

A	
B	
C	

Q.4.8. A low frequency signal of 1 kHz with a signal/noise ratio of 50 dB is measured in the single-period mode with a clock period of 10 ns. How many of the digits displayed are not significant?
A. = 1
B. = 2
C. = 3

A	
B	
C	

Q.4.9. A 10 MHz crystal oscillator is to be calibrated to an accuracy of 10^{-7} with the aid of a 9-digit 500 MHz counter. The counter gate time needed to achieve this accuracy is
A. 10 ms
B. 100 ms
C. 1 s

A	
B	
C	

Glossary of terms

AGEING (aging) - The non-reversible, generally gradual change of resonance frequency with time in crystal oscillators.

BCD (Binary coded decimal) - Four bits of binary informations can be used to encode one decimal digit. When the successive digits of a decimal number are coded in this way, the number is said to be in the BCD (binary coded decimal) code.

BCD output - If a counter has a BCD output, the measuring result is available at this output in BCD code. This output can be in the parallel mode when all BCD digits are available at the same time (9 decimal digits thus require 9 x 4 output lines) or in the serial mode when the decimal digits are presented at the output sequentially.

CLOCK - In digital systems in general the clock is a timing device which produces pulses at a steady rate. In counter/timers the clock is the heart of the time-base circuitry producing the time reference for frequency and time measurements.

COINCIDENCE GATE - A gate circuit whose output depends on the presence or absence of a specific coincidence of input signals.

CONVERTERS - A device which converts information presented into a form compatible with the instruments circuitry. In digital counters a converter is mostly used to extend the frequency range of a digital frequency meter. It converts the input frequency down to a frequency which can be handled by the counter.

COUNTER - 1. A device which records the number of pulses it has received at its input. Depending on the circuitry it can count and store in binary or another code form.
2. Abbreviation for digital counter/timer.

DATA - A general term used to devote any or all facts, numbers, letters and symbols used for processing by digital equipment. In counter/timers it generally refers to output (being the measuring result, often in BCD code) or input data (the information for remote programming of the instrument).

DCU - Decimal counting unit, the heart of a digital counter, consisting of a number of decade assemblies in cascade. There are as many decade assemblies as there are digits in the display.

DECADE - A group of ten units, in digital techniques generally a counter which counts and stores up to ten (see "counter").

DECADE ASSEMBLY - The basic unit of a DCU. Each decade assembly generally consists of 5 units: a decade counter, a memory, a BCD-to-decimal decoder, a numerical indicator and an indicator driver.

DECODER - A decoder is a device used to convert information from one coded form into a more useful form (e.g. a BCD to decimal decoder).

DISPLAY - A device which converts the electrical (decimal) data (e.g. the measuring results) into a visible form. Typical display devices are the NIT, LED or cathode-ray tube.

DISPLAY TIME - The time during which the data are presented on the display(s). This time can generally be set within the range 0.05 - 5 s. A special (HOLD) switch also makes it possible to set the display time to infinity. When the display time is over, a new measurement starts (see also SAMPLING RATE).

DIVIDER (or scaler) - A device that divides an input frequency by a certain factor e.g. a decade scaler divides the input frequency by a factor of ten (see also PRESCALER).

DRIFT - The deviation of the operating frequency of a crystal oscillator from its nominal value generally owing to temperature variations.

DYNAMIC DISPLAY - A display where the presentation of each decimal digit takes place in sequential form (see BCD output, serial mode).

ENCODER - A device which takes information in one code and transforms it into another (e.g. decimal-to-binary encoder).

ERROR - The general term expressing the deviation of a measured value from the theoretically correct or true value or the part of the error due to a particular cause (e.g. trigger error, time-base error etc.).

FREQUENCY CONVERTER - A part of a frequency counter (often made as a plug-in) which converts the frequency to be measured down to a value measurable by the counter.

FREQUENCY MODE - The selected function of the counter/timer when the instrument functions as a digital frequency meter.

FREQUENCY-RATIO (MODE) - The selected function of the counter/timer where it measures the ratio between two input frequencies.

HETERODYNE CONVERTER - A frequency converter working on the heterodyne principle.

HYBRID CIRCUIT - A circuit made by a combination of different integration techniques.

HYSTERESIS (TRIGGER WINDOW) - The lag in response of a circuit after an increase or decrease in the signal amplitude.

INTERFACE - The boundary between two electronics systems.

LED - Light-emitting diode. When the minority carriers recombine in a forward biased junction diode they can give up their energy in form of quanta of light (photons). A number of these diodes can be placed in an array to form an (alpha-) numerical indicator.

MAIN GATE - The input gate to the DCU, controlled by the input signal and by the time-base generator.

MASKING - A method used for rejecting noise in the input signal. The input signal is masked during a certain time so that no miscounting due to noise can occur.

MEMORY - An (electronic) device in which data can be stored and from which data can be obtained when necessary. (Also called storage).

MODE - The selected operational function of a counter/timer.

MULTIPLEXING - The transmission of different data simultaneously or sequentially over a single line or a group of lines.

MULTIPLE-PERIOD MODE - The function where the counter/timer measures a selected number of successive periods.

NIT - Numerical indicator tube: a gas-filled, cold-cathode display tube with a common anode and 10 individual cathodes, formed in the shapes of the numerals 0 to 9.

NIT DRIVER - generally a combined circuit consisting of a BCD to decimal decoder and a low-to-high-level interface.

PANDICON - A multidigit planar 7-segment numerical indicator tube. All cathodes of the same |kind| are interconnected, and the digit position is selected by driving the appropiate anode with a positive voltage.

PERIOD MODE - The selected function of the counter/timer where it measures the time of one single period.

PRESCALER - (Plug-in) frequency converter functioning on the divider principle.

PRESET - When preset, the memory or input divider of a digital instrument is set to a specific value.

PULSE-PAIR RESOLUTION - The pulse-pair resolution of a counter is the minimum time between the two pulses of a pulse pair which the counter recognizes as seperate pulses.

PULSE REPETITION RATE - The number of electric pulses per unit time.

PULSE-WIDTH MODE - The selected function of the counter/timer where it measures the pulse width or pulse duration.

RECIPROCAL COUNTER - Special-purpose counter which measures the period of a periodic signal and converts the result of the measurement with an internal arithmetic unit into frequency, which is displayed.

RESET - When reset, a device or an instrument is returned to zero or to another specified condition.

RESOLUTION - In practice, the value of the least significant digit (LSD).

RING COUNTER - See "shift register".

RISE TIME - The time required for the leading edge of a pulse to rise from one tenth of its final value to nine-tenths of its final value.

SAMPLING RATE - The rate at which measurements are made. In e.g. the frequency mode, the samping rate is the inverse of the sum of gate time and display time.

SCALING - 1. The same as dividing.
2. The scaling mode of a counter is the special function where the frequency of an input signal is divided by the time base chain by a specified power of 10.

SHIFT REGISTER - A storage device consisting of a chain of flip-flops in which the contents can be shifted one or more positions. In a shift to the right the right most bits on the far right of the number stored are lost, in a shift to the left the bits on the far left. In a circulating shift register no data are lost because the data leaving the register at one end are reinserted at the other.

S/N RATIO - The signal-noise ratio is the ratio of the amount of signal carrying information to the amount of signal not carrying information. The S/N ratio is mostly expressed in dB.

STATIC DISPLAY - Display circuitry where the presentation of each decimal digit takes place simultaneously (see BCD output, parallel mode).

TCXO - Temperature-compensated crystal (X-tal) oscillator. A TCXO comprises a crystal oscillator and a thermally controlled circuit that compensates for frequency changes over the specified temperature range.

TIME BASE - Generally a chain of decade dividers, which together with the crystal oscillator forms the time reference for the counter/timer.

TIME-INTERVAL AVERAGE MODE - The function where the counter/timer measures a selected number of successive time intervals.

TIME INTERVAL MODE - The function where the counter/timer measures the time interval between e.g. two levels of the same signal (rise time) or between two pulses on different lines (delay).

TRANSFER PULSE - The pulse enables data counted in the counter decades to be transferred to the memory.

TRANSFER OSCILLATOR - Another type of frequency converter, in which the input signal is mixed with a harmonic of a VFO, the fundamental of which is measured by the counter.

TRIGGER WINDOW (see hysteresis).

TOTALIZING MODE - The function where the counter counts incoming pulses until a manual stop signal is given.

VCO - Voltage-controlled oscillator. Basically a VFO tuned by the setting of a DC voltage.

VFO - Variable-frequency oscillator: an oscillator whose frequency can be varied (manually or electrically) within a certain range.

YIG filter - An (Yttrium-iron-Garnet) microwave filter based on the properties of small YIG spheres.

Answers to questions

Questions	1.1	1.2	1.3	1.4	1.5	1.6	1.7	1.8	1.9	1.10
Answers	A	C	A	B	A	A	B	B	B	C

A.1.1. As we have seen the width of the trigger window (or the hysteresis) determines the sensitivity. The larger the window the larger the signal required to switch the Schmidt trigger. Decreasing the window by a factor of 4 thus means that the trigger-signal amplitude can be reduced by the same factor, so the sensitivity is increased 4-fold. (Answer A)

A.1.2. As we have learned, whether a logic gate will function as an AND or OR gate depends on the definition of the logic levels. This is of course also true for the main gate of a counter; in other words, depending on the circuitry this may be either an AND gate or an OR gate. (Answer C)

A.1.3. The PANDICON® is a multi-digit numerical display tube; because of the limited pin connections available is one single envelope, dynamic display is the only possible method, see fig. 1.6. (Answer A)

A.1.4. The advantage of the use of a memory in a counter is that it gives a steady display without continuous changing of digits during the measurement. In other words, it is used for convenience of operation. (Answer B) (Although the BCD output is connected to the memory output in most counters, this does not mean that the memory is necessary for the BCD output. The printer can equally well be connected directly to the counting decades).

A.1.5. The first decade of a counter chain divides the input frequency by a factor of 10, so does the second, etc. This means that the second decade can be 10 times slower than the first, the third 100 times slower and so on. The first decade thus determines the counting speed of the C.D.U. Of course the main gate must have at least the same speed as the first decade, but the main gate is not part of the D.C.U. so answer A is correct.

A.1.6. When the counting is finished the contents of the decades have to be transferred to the memory. Only when the memory has taken over these data can the decade counter be reset. Thus first the transfer pulse is given and then the reset pulse. (Answer A, see fig. 2.3.).

A.1.7. As the signal flow is from left to right in the diagram the LSD is given by the decade on the far left. The diagram is easy to read if we turn it back to front.

So answer B is correct.

A.1.8. As we know, each decade output in the time base divider chain has a 10 times lower frequency than the foregoing output. The frequencies of the successive outputs are thus:

* T1 = (100 kHz) = 10 μs (clock frequency)
T2 (10 kHz) = 100 μs
T3 (1 kHz) = 1 ms
T4 (100 Hz) = 10 ms
* T5 (10 Hz) = 100 ms
T6 (1 Hz) = 1 s
T7 (0,1 Hz) = 10 s
* T8 (0,01 Hz) = 100 s

The correct answer is thus: T1 = 10 μs; T5 = 100 ms and T8 = 100 s; (Answer B).

A.1.9. An aging rate of 3×10^{-9}/day means that the crystal oscillator could drift from the nominal frequency by this amount at most. The maximum drift in 30 days is thus $30 \times 3 \times 10^{-9} \approx 10^{-7}$. Since this value equals the required accuracy, the crystal oscillator should be recalibrated once a month. (Answer B)

A.1.10. When the transfer line is kept HIGH continuously during counting the D flip-flops in the memory are directly connected to the outputs of the decade counters and thus follow the states of the various flip-flops in the decade counter immediately; the display will thus also follow the counting continuously, so answer C is correct.

Questions	2.1	2.2	2.3	2.4a	2.4b	2.5	2.6	2.7	2.8	2.9	2.10
Answers	C	A	C	C	B	B	A	C	A	C	A

A.2.1. With a gate time of 10 ms the LSD (frequency resolution) is 100 Hz. Expressing this value in MHz means multiplying by 10^{-4}, or shifting the decimal point four places to the left; the DP is thus situated between digit 4 and 5 (answer C).

A.2.2. As the clock frequency is 4 times higher than normal, times derived from it will be 4 times smaller. Thus the main gate also remains open for a quarter of the normal time, so $^1/_4$ of the normal number of pulses are counted i.e. the reading should be multiplied by 4. (Answer A). Note: If the counter is in the PERIOD mode, 4x too much pulses are generated so in this case the reading should be divided by 4.

A.2.3. The reading of this counter will be 400.0 Hz $\pm$ 1 LSD (= 0.1 Hz). The accuracy is thus 1 part in 4000 which is equivalent to 2.5×10^{-4} (answer C). Note: The accuracy of the time base, which is 1 part in 10^8, does not of course influence the accuracy in this case at all.

A.2.4a. With the slope selector set to "pos" the counter starts at the first positive-going edge (A) and stops at the first negative-going slope (B), which gives a time of 146 ms (answer C).

A.2.4b. When the pulse is inverted, the first positive-going edge is at (B), the negative-going one at (A'), so the time measured here is 32 ms (answer B).

A.2.5. A clock accuracy of e.g. 10^{-4} means that the LSD of a 4-digit reading is liable to uncertainty. Increasing the number of digits in the display beyond 4 does not add anything at all to the accuracy. In an 8 digit counter with this clock, only the first 4 digits of a full display would be reliable; the last 4 would not mean anything. There is thus no point in having more digits than the clock accuracy allows for (answer B).

A.2.6. The period time of this signal is $\frac{1}{1.5}$ = 0.66 ms. The total averaging time over 10^4 period will be 0.66×10^4 = 6.66 sec. = 6.666 666 μs, which is the value displayed. So 7 digits are used (answer A).

A.2.7. As the rise time is defined as the time between the 10% and 90% points of the rising edge, one needs two independent level settings for the trigger circuit. This of course is not possible in the PERIOD and WIDTH modes but only in the TIME INTERVAL mode, which has two independent input channels (answer C). Note: The polarity setting should be the same for both channels ("Pos" for rise time and "neg" for fall time with positive-going pulses).

A.2.8. MULTIPLE modes mean relatively long measuring times. The longer the measuring time the more pulses are counted. So when one wants to decrease the total number of counts one must decrease the time-base frequency (answer A).

A.2.9. A new measuring cycle is initiated by the time-base generator switching over the main-gate flip-flop. One can prevent this by keeping this flip-flop in the RESET condition, so the inhibit signal has to be applied to the reset input of this flip-flop ⑪, answer C.

A.2.10. The accuracy of the counter (or crystal oscillator) can never be checked in the CHECK mode, because as the signal is compared with itself the reading will always be 100.000 ... ($\pm$ 1 digit). The input circuit cannot be checked either in most counters, because the clock signal is already conditioned to the right logic levels so that it will be fed directly to the main gate. The check function is in fact intended for checking the overall functioning of the counter (displays, memory, reset, BCD output, time-base ranges etc.); answer A.

Questions	3.1	3.2	3.3	3.4	3.5	3.6	3.7	3.8	3.9	3.10	3.11
Answers	B	C	A	C	B	A	B	A	C	A	C

A.3.1. Prescaling by a factor of ten means that 10 times fewer pulses are counted, so the display will be 10 times too low; the decimal point should therefore be shifted to the right (answer B).

A.3.2. The unknown frequency must of course be between F_1 and F_2, because if the frequency was below F_1 the beat product F_2-F_x could not pass the low-pass amplifier, and the same applies to frequencies above F_2. Only if F_x is between F_1 and F_2 can the mixed product pass the video amplifier (answer C).

A.3.3. Of course this is possible. Going from the bottom end of the scale one first measures the lower frequency, and then goes on to the next beat (not counting the extra 1 or 2 beats of the lower frequency) (answer A).

A.3.4. A comb frequency distance of 200 MHz means that the low-pass amplifier of the plug-in also has at least a bandwidth of 200 MHz. So a preset frequency of 2.00 GHz will beat with the lower frequency and causes the scanning to stop. The beat frequency of 0.05 GHz will then be measured by the counter and added to the preset value, giving the result: 2.00 + 0.05 = 2.05 GHz (answer C).

A.3.5. Application of the standard formula gives:

$$N = \frac{F_2}{F_2 - F_1} = \frac{174}{174 - 168} = \frac{174}{6} = 29 \text{ (answer B)}$$

The frequency is:

A.3.6. $N.F_1 = 29 \times 168$ MHz $= 4{,}872$ GHz (answer A).

A.3.7. We know that in the phase-lock mode the difference between the input signal and the n^{th} harmonic of the VFO should be 1 MHz. In our example:
$790 - N.f_0 = 1 \rightarrow N.f_0 = 789$; therefore $f_0 = 789{:}4 = 197.25$ MHz, and as the main gate is extended 4 times the reading will be $4 \times 197.25 = 789$ MHz again (answer B).

A.3.8. Assuming that the searching time till the first beat is found is the same for both instruments, we know that the heterodyne convertor then displays the mixed product plus the preset frequency of the comb generator directly, while in the case of the TO the time base has to be multiplied by the harmonic number N, which makes the measuring time of the latter N times longer (answer A).

A.3.9. The transfer oscillator measures the local oscillator frequency, the mixed-product measurement is typical for the heterodyne convertor, and for the automatic divider - as the name already indicates - the signal to be measured by the counter is the input frequency divided by the scaling factor (answer C).

A.3.10. No scaling factor means in fact dividing by 1, and as the 100 000's complement of 1 is 99999 one should set the scaler to 99999 (answer A). In case B the scaler has to count the full range (00000 is the complement of 100 000) so the dividing factor is 100 000, while in case C the dividing factor is 99 999.

A.3.11. As the BCD output is always connected to the display section of a counter, the information contained in the BCD output is of course the frequency (answer C).

Questions	4.1	4.2	4.3	4.4	4.5a	4.5b	4.6	4.7	4.8	4.9
Answers	A	B	A	B	C	C	C	B	B	C

A.4.1. The greater the gate time in frequency measurements, the greater the accuracy. When a 10 times prescaler is used the gate time has to be 10 times longer; however, 10 times fewer pulses are counted so the error caused by the $\pm$ 1 count ambiguity remains the same. (Answer A).

A.4.2. Assuming the clock accuracy is good enough, the only other source of error is the $\pm$ 1 count ambiguity which is relatively twice as small with the 200 MHz steps as with the 100 MHz steps (answer B).

A.4.3. As can be seen from fig. 4.2, the influence of the $\pm$ 1 count ambiguity becomes relatively less when more pulses are counted. The number of pulses counted can be raised by increasing the clock frequency (answer A).

A.4.4. A 100% amplitude-modulated signal has to be handled in the same way as a burst signal, so only a counter with a burst-mode facility can be used for this purpose (answer B). The gate time selected should be smaller than the period time of the modulation frequency.

A.4.5. This problem can be solved by inspection of the table given below.

Measurement mode	Display	Accuracy	Measuring time
Frequency	10 000	$10^{-8} \pm 1$ digit $= 10^{-4}$	1 s
Period	1 000	$10^{-8} \pm 1$ digit $\pm 0.3\% = 4.10^{-3}$	100 µs
Multiple per.	1 000 000	$10^{-8} \pm 1$ digit $\pm 0.3\ 10^{-3}\% = \pm 4.10^{-6}$	100 ms

The multiple-period mode is thus superior as regards both criteria mentioned (answers 4.5a/C and 4.5b/C).

A.4.6. The gate time in a burst-mode measurement must always be smaller than the burst time. In the case in question, the gate time should thus be less than 1 ms (answer C).
Note: A gate time which is exactly equal to the burst time (answer A) is wrong because a number of pulses are lost owing to the delay which is needed for starting the counter.

A.4.7. Assuming that the clock accuracy is high enough for the application, the only other source of error that matters is the $\pm$ 1 count ambiguity again. As the frequency measured in the transfer oscillator is basically lower than in the heterodyne converter, the influence of the $\pm$ 1 count ambiguity is larger with the transfer oscillator than with the heterodyne converter for the same measuring time; answer B is thus correct. Of course when the gate time is multiplied by N as is normally done with the transfer oscillator, the accuracy is the same but the measuring time is N times longer.

A.4.8. With a signal of 1 kHz and a resolution of 10 ns in the period mode the counter will display 100 000. With a signal/noise ratio of 50 dB the trigger error is $\approx 0.1\%$, so the last two digits are not significant (answer B).

A.4.9. To measure a 10 MHz signal with an accuracy of 10^7 we need a resolution of at least 1 Hz, which is achieved with gate times of 1 s or more (answer C).

PM 6610 SERIES RF COUNTERS

PERFORMANCE SURVEY OF PM 6610 SERIES OF UNIVERSAL COUNTERS

Type number \ Function	Frequency MHz				Period and period average	Multiple ratio	Totalizing of counts	Time interval
	80	250	520	1 GHz				
PM 6611	■				■	■	■	
PM 6612	■				■	■	■	■
PM 6613	■	■			■	■	■	
PM 6614	■	■	■		■	■	■	
PM 6615	■	■	■	■	■	■	■	

This new series of portable counters offer a tailor-made specification. This is achieved by providing a choice of frequency ranges, see table, that match market requirements plus a wide choice of options such as time-base stability and BCD output.
A competitive price is achieved by taking maximum advantage of Philips custommade MOS-LSI and thin-film circuitry and other components.

Two input channels
The PM 6610 series are primarily designed for high-frequency measurements. The PM 6613, PM 6614 and PM 6615 feature a special RF input channel.
The 80 MHz input is also employed to perform the universal measuring functions like PERIOD, PERIOD-AVERAGE, MULTIPLE-RATIO, TOTALIZING of COUNTS and SELF-CHECK.

RF measuring inputs
In addition to the general-purpose 80 MHz channel the VHF/UHF models PM 6613, PM 6614 and PM 6615 offer a secound RF input.

Ease of operation
The operator needs not concern himself with setting the amplitude for optimum triggering. The AUTOMATIC PIN-diode circuit attenuates the input signal to a level just slightly above the value of the trigger window.
For the construction of the PIN-diode attenuator, a multi-stage type has been selected to bridge a very wide 62 dB dynamic input voltage range. The attenuator ensures optimum triggering at any input level between —27 dBm and +35 dBm
(10 mV_{rms} . . . 12 V_{rms}).

RF input protection
Unlike conventional AGC-circuits, the multi-stage PIN-diode circuit really ATTENUATES the input signal, thus strongly reduces the signal level at the input of the sensitive amplifier.

Noise suppression
The automatic attenuator also eliminates false counts due to noise in the RF input signal. The noise is attenuated so much that it cannot span the trigger window.

Digital and analog interface facilities
For easy handling of the measuring digital the BCD output unit PM 9674 is as an optional extra.
The digital-to-analog converter PM 9675 provides high-resolution analog output for recording.

Technical Data

Measuring modes: see table
Frequency range : see table

Period
Range : 100 ns - 100 s

Period average
Range 1 Hz - 10 MHz
Periods averaged 10^2 & 10^4

Time Interval (PM 6612 only)

Ratio $\frac{10\ \text{Hz} \ldots \text{f max}}{1\ \text{kHz} \ldots 10\ \text{MHz}}$ N.

Input A (all models)
10 Hz - 80 MHz
10 mV (20 Hz - 80 MHz)

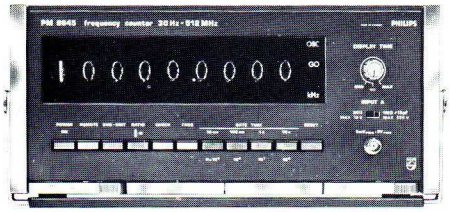
Input B
PM 6612 stop channel = input A
PM 6613 5 MHz - 250 MHz, 10 mV
PM 6614 50 MHz - 520 MHz, 10 mV
PM 6615 50 MHz - 1 GHz, 10 mV

Input C (rear, all models)
1 kHz - 10 MHz, 500 mV

Time-base oscillator
Choice of 4 options:
up to: ± 1.5 x 10^{-9}/24h
and ± 5 x 15^{-10}/°C

Power: 110/220 V AC
Optional: Power pack

512 MHz FREQUENCY COUNTER PM 6645



The PM 6645 is a 'frequency only' instrument and as such gives more economic high-performance measurements of frequency than a general-purpose counter/timer. It is ideal for R and D laboratories and for automated testing of telecommunications equipment due to its high sensitivity, combined with a high 1 Hz resolution which is reached in only 1 second due to the direct gating. These features make the PM 6645 the most powerful frequency counter on the market today. The basic frequency range is 512 MHz, which can be extended to 1 GHz or 12.6 GHz, while another sub-unit increases the basic 5 mV sensitivity tot 500 μV over the range 10 kHz to 200 MHz.
A significant benefit of making RF measurements on this instrument is the automatic attenuation circuit that enables a wide dynamic range of 60 dB to be handled and at the same time reduces noise to a level below the trigger window.

Technical Data

Frequency range 30 Hz - 512 MHz

Input:
Impedance 1 MΩ// 15 pF or 50 Ω
Sensitivity: 5 mV_{rms}

Attenuator: automatic
Input range: 5 mV - 5 V_{rms}

Read-out:
9 digits
Display time
2-50 ms, 0.02 - 5 s or HOLD

Time base
3 options available
up to 1.5 x 10^{-9}/24h
and 5 x 10^{-10}/°C

Options:
PM 9688 Analog output
(BCD-to-analog converter)
PM 9682 BCD output
(HNIL and TTL compatible)
PM 9683 Remote program input
(HNIL and TTL compatible

PLUG - INS

PM 6633 Preamplifier plug-in
The PM 6633 is a low-noise plug-in preamplifier unit which increases the input sensitivity of the PM 6645 counter.
Frequency range 10 kHz - 200 MHz
Gain x 0.5 ..... x 50 (5 steps)

12.6 GHz Automatic microwave converter PM 6634
When the PM 6645 is combined with the 12.6 GHz microwave converter PM 6634, the result is an automatic μ-wave counter with unique and significant advantages.
Frequency range 1 - 12.6 GHz
Sensitivity: - 7 dBm

PM 6636 Automatic prescaler plug-in
The PM 6636 is used to extend the direct counting capability to over 1 GHz. This is achieved by pre-scaling (dividing) the input frequency.
Frequency range 0.1 ... 1 GHz
Sensitivity: 10 mV

512 MHz COUNTER/TIMER PM 6650

The PM 6650 is a powerful and versatile instrument that allows accurate time and frequency measurements to be made in a convenient manner. For example, the RF channel incorporates an automatic PIN-diode attenuation circuit that enables a wide 62 dB dynamic range to be handled and at the same time reduces noise to a level below the 'trigger window'. Similarly time measurements are facilitated and accuracy improved by a combination of features including LED indicators for quick setting of trigger levels, trigger level monitoring, automatic hysteresis compensation and the time interval averaging technique. Together with the 100 MHz clock rate and very fast, equalised start/stop channels, this allows resolutions of up to 1 ps to be achieved. This figure is some 10,000 times beter than that reached with conventional methods.

The basic 512 MHz specification of the PM 6650 can be extended still further by sub-units, which increase the frequency range to 1 GHz or 12.6 GHz, while another unit increases the basic sensitivity by a factor of 50.

Options are also available in the specification. There is a choice of three crystal oscillators in order to meet individual stability requirements and at any time the user can add printed circuit boards in order te provide the facilities of remote programming, a BCD output and an analog output. The PM 6650 is thus one of the most powerful and versatile time and frequency measurement tools on the market today.

Technical Data

Frequency
Range: DC - 512 MHz
Mode: Normal or burst
Gate times: 100 ns - 100 s
Inputs: A or C

Period
Range: DC - 10 MHz
Resolution: 10 ns - 1 s
Input: A

Period Average
Range: DC - 10 MHz
Periods averaged (N): 1 - 10^6
Resolution: 10 ns/N
Input: A

Time Interval
Range: 40 ns .... 10^9 s
Resolution: 10 ns - 1 s
Inputs A&B

Time Interval Average
Range: 100 ps ... 10 s
Intervals Averaged (N): 1 ... 10^8
Resolution: 10 ns/$\sqrt{N}$
Inputs A&B

Multiple Ratio

$\frac{A}{B}$ N

Range DC ... 160 MHz (A)
DC ... 10 MHz (B)
Multiplier (N): 1 ... 10^7
Inputs: A&B

Inputs

A&B
Frequency range DC ... 160 MHz
Sensitivity: 50 mV_{rms}
Impedance: 1 MΩ//25 pF of 50 Ω
Trigger slope: + or − level, preset 0 or − 3V .... + 3V

C
Frequency range: 5 MHz ... 512 MHz
Sensitivity: 10 mV_{rms}
Impedance: 50 Ω

General
Display 9 digits
time 0.05 ... 5 s, HOLD

Time base
Choice of three options
up to 1,5 x 10^{-9}/24h
and 5 x 10^{-10}/°C

Options
PM 9684 BCD output TTL/HNIL
PM 9685 Remote control TTL/HNIL
PM 9686 I.E.C. bus interface
PM 9687 Analog output
For plug-in options see PM 6645, page 63

Acknowledgement
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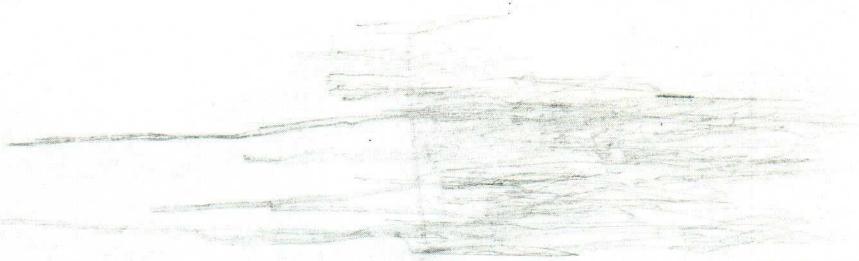
Part 1 Basic binary theory and logic circuits
The first part of the digital instrument course deals with the fundamentals of binary theory and logic circuitry.
The chapter headings are:



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