PHILIPS

Electronic components and materials

Technical note 084

Using seven-segment LED displays with the 2650 microprocessor

Seven-segment displays can provide a cheap and simple information display for use with microcomputers. They are of particular use in displaying information such as error codes, status etc. to the operator. Of the various types of seven-segment display available, the light emitting diode (LED) is the most common and suitable for the present purpose.

LED display drive by a microprocessor

Most seven-segment LED displays can be driven directly from an integrated circuit. The choice of common anode or common cathode devices depends on the type of driver IC used. The decoding from the microprocessor's internal BCD or hexadecimal code to that for the seven-segment display can be performed either by hardware or by software.

Static or dynamic drive?

Static drive to a display requires a separate latch/driver for each segment of each digit. This provides a continuous drive for each digit while placing the minimum load on the microprocessor: the microprocessor only has to update digits as they change. Any number of digits can be driven in this system.

Dynamic drive to two or more displays involves the time-sharing of one driver/decoder device by all the digits. The corresponding segments of the separate digits are interconnected via common segment lines to the decoder/driver. Digit scanning is then performed by successive activation of each digit's common anode at the same time as that digit's segment information is presented by the decoder/driver. If this procedure is repeated fast enough (more than 70 times per second) the display will appear flicker-free to the human eye.

When a number of digits (n) are driven dynamically, each digit is activated 100/n per cent of the time. The maximum number of digits that still provides an acceptable read-out depends on the allowable peak segment current and the average current to adequately light a segment. For the CQY81 device, this number is about eight.

The dynamic drive method results in a system with considerably less hardware than the static drive method, but places a far greater load on the microprocessor, even if the digit scanning is performed by hardware.

I/O device addressing

The 2650 microprocessor can address data output devices in three ways: non-extended I/O, extended I/O and memory-mapped I/O.

signetics

Non-extended I/O

The two non-extended output ports are addressed when the microprocessor executes WTRD and WTRC instructions. The signal ADR14-D/C provides selection of one of the ports, C or D. Figure 1(a) shows the generation of a suitable $\overline{LE}$ (Latch Enable) signal.

Extended I/O

The two-byte instruction WRTE provides addressing for up to 256 external devices. The second byte of the instruction is an eight-bit address that is output on the address bus (ADR0 to ADR7). Figure 1(b) shows the generation of a suitable $\overline{LE}$ signal.

Memory-mapped I/O

The external device is addressed as if it were a memory location. Obviously, the device address must be outside the range used for memory addressing. Figure 1(c) shows the generation of a $\overline{LE}$ signal.

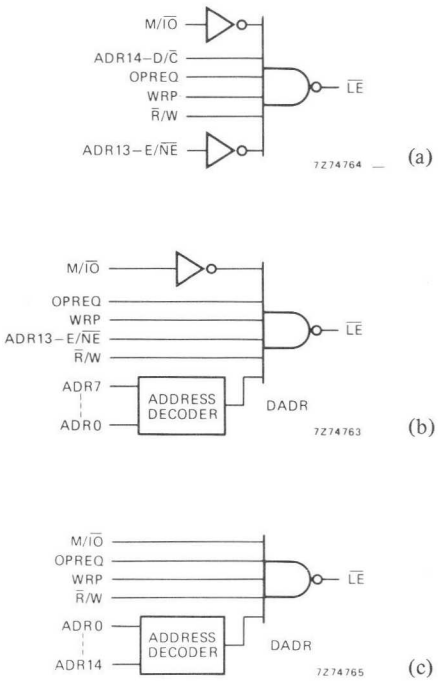

Fig. 1 Generation of $\overline{LE}$ (Latch Enable) signal. (a) With non-extended I/O. (b) With extended I/O. (c) With memory-mapped I/O.

One-digit display with software decoding

A single seven-segment display is driven via two quadruple D-type flip-flop ICs from the microprocessor data bus. The circuit diagram is shown in Fig. 2. A software routine, see Fig. 3, in the microprocessor's memory converts BCD or hexadecimal code into the seven-segment code. The code to be converted is in the four least significant bits of R3. Because the four most significant bits of R3 are zero, R3 can be used as an index for the conversion table. Table 1 shows the conversion from hexadecimal to seven-segment code. The LED display is addressed as non-extended output port D, using the $\overline{LE}$ signal of Fig. 1(a).

TABLE 1 Hexadecimal and seven-segment codes

segment	a	b	c	d	e	f	g	dp	7 segment
data bit	B7	B6	B5	B4	B3	B2	B1	B0	code
Hex code									in hex
0	0	0	0	0	0	0	1	1	03
1	1	0	0	1	1	1	1	1	9F
2	0	0	1	0	0	1	0	1	25
3	0	0	0	0	1	1	0	1	0D
4	1	0	0	1	1	0	0	1	99
5	0	1	0	0	1	0	0	1	49
6	0	1	0	0	0	0	0	1	41
7	0	0	0	1	1	1	1	1	1F
8	0	0	0	0	0	0	0	1	01
9	0	0	0	0	1	0	0	1	09
A	0	0	0	1	0	0	0	0	10
B	1	1	0	0	0	0	0	0	C0
C	0	1	1	0	0	0	1	0	62
D	1	0	0	0	0	1	0	0	84
E	0	1	1	0	0	0	0	0	60
F	0	1	1	1	0	0	0	0	70

0 means segment switched on.
1 means segment switched off.

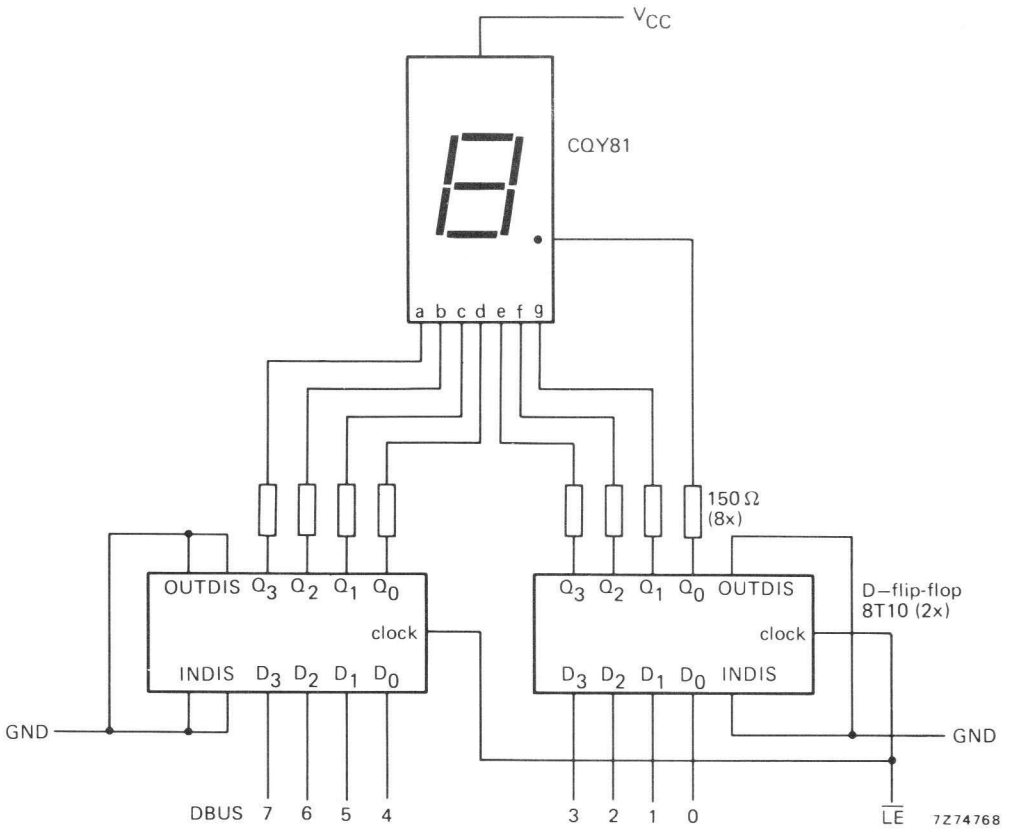

Fig. 2 Circuit diagram of a one-digit display with software decoding.

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TWIN ASSEMBLER VER 2.0                                  PAGE 0001

LINE ADDR  OBJECT  E SOURCE

0001                * DISPLAY DRIVE ROUTINE
0002                * THIS ROUTINE CONVERTS A HEX CODE TO A
0003                * 7 SEGMENT CODE AND OUTPUTS THIS 7 SEGMENT
0004                * CODE.  THE 4 LOWER BITS OF REGISTER R3 MUST
0005                * CONTAIN THE HEX CODE AND THE 4 UPPER BITS
0006                * MUST BE ZERO.
0007                *
0008                * DEFINITIONS OF SYMBOLS:
0009 0000           R0      EQU     0       PROCESSOR REGISTERS
0010 0003           R3      EQU     3
0011                *
0012                ************************************************
0013                *
0014                * PROGRAM MEMORY
0015                * CONVERSION ROUTINE
0016 0000                   ORG     H'500'
0017 0500 0F6510    ROUT    LODA,R0 DEC,R3  FETCH EQUIVALENT 7
0018                *                   SEGMENT CODE OUT OF
0019                *                   CONVERTION TABLE
0020 0503 F0                WRTD,R0         OUTPUT THIS CODE
0021                *                    TO PORT D
0022                *
0023                * CONVERSION TABLE DEC CONTAINS THE 7 SEGMENT
0024                * CODE WHICH ARE EQUIVALENT WITH THE HEX
0025                * CODES 0 THROUGH F.
0026 0504                   ORG     H'510'
0027 0510 03        DEC     DATA    H'03'   DIGIT 0
0028 0511 9F                DATA    H'9F'   1
0029 0512 25                DATA    H'25'   2
0030 0513 0D                DATA    H'0D'   3
0031 0514 99                DATA    H'99'   4
0032 0515 49                DATA    H'49'   5
0033 0516 41                DATA    H'41'   6
0034 0517 1F                DATA    H'1F'   7
0035 0518 01                DATA    H'01'   8
0036 0519 09                DATA    H'09'   9
0037 051A 10                DATA    H'10'   A
0038 051B C0                DATA    H'C0'   B
0039 051C 62                DATA    H'62'   C
0040 051D 84                DATA    H'84'   D
0041 051E 60                DATA    H'60'   E
0042 051F 70                DATA    H'70'   DIGIT F
0043 0500                   END     ROUT

 TOTAL ASSEMBLY ERRORS = 0000
```

Fig. 3 Display drive routine for the circuit of Fig. 2.

One digit display with hardware decoding

The hardware decoding can be performed either by a PROM or by a specially designed BCD-to-seven-segment decoder.

Display drive using a decoder device

Figure 4 shows an example of hardware decoding of the microcomputer output using a decoder/driver and a separate latch, and Fig. 5 an example using a combined latch/decoder/driver. Current limiting resistors are required when using the N7446A and N7447A, whereas the N9734 has constant current outputs, thus avoiding the need for limiting resistors.

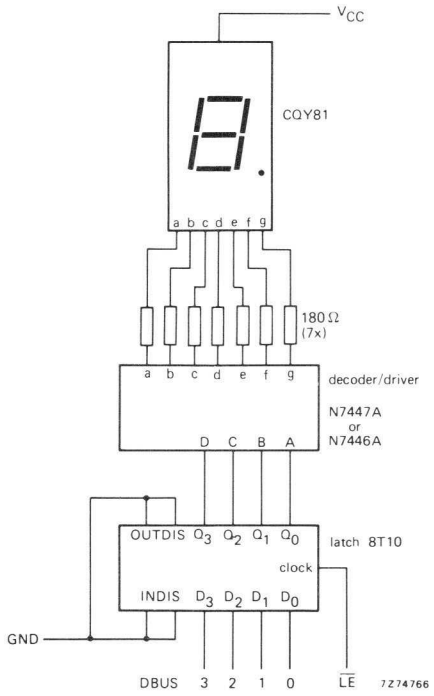

Fig. 4 Hardware decoding using a decoder/driver and separate latch.

Display drive using a PROM

A PROM such as the 82S23 or 82S123 can be used in place of the decoder/driver in Fig. 4. Whereas most decoder/drivers provide only BCD-to-seven-segment code conversion, the PROM can be programmed to display hexadecimal digits (0 to 9 and the letters A to F) and the decimal point. These devices can sink a current of 16 mA, allowing direct drive of the display via current limiting resistors.

Locations 0 to 15 of the PROM are used to store the conversion code. Table 2 defines the functions of the PROM as a decoder. A zero bit value causes the corresponding segment to be illuminated. If locations 16 to 31 are left unprogrammed (all zeros) the most significant address line performs a lamp-test function. When a word in the range 16 to 31 is addressed, all the segments will light. When the $\overline{CE}$ input is high, all outputs will be high and the display will be dark.

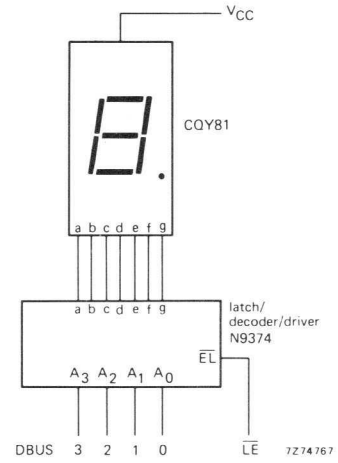

Fig. 5 Hardware decoding using a combined latch/decoder/driver.

TABLE 2 Programming of PROM decoder

display	inputs						program in memory								
							segment	a	b	c	d	e	f	g	dp
	CE	A4	A3	A2	A1	A0	bit	B0	B1	B2	B3	B4	B5	B6	B7
0	0	0	0	0	0	0		0	0	0	0	0	0	1	1
1	0	0	0	0	0	1		1	0	0	1	1	1	1	1
2	0	0	0	0	1	0		0	0	1	0	0	1	0	1
3	0	0	0	0	1	1		0	0	0	0	1	1	0	1
4	0	0	0	1	0	0		1	0	0	1	1	0	0	1
5	0	0	0	1	0	1		0	1	0	0	1	0	0	1
6	0	0	0	1	1	0		0	1	0	0	0	0	0	1
7	0	0	0	1	1	1		0	0	0	1	1	1	1	1
8	0	0	1	0	0	0		0	0	0	0	0	0	0	1
9	0	0	1	0	0	1		0	0	0	0	1	0	0	1
A	0	0	1	0	1	0		0	0	0	1	0	0	0	0
B	0	0	1	0	1	1		1	1	0	0	0	0	0	0
C	0	0	1	1	0	0		0	1	1	0	0	0	1	0
D	0	0	1	1	0	1		1	0	0	0	0	1	0	0
E	0	0	1	1	1	0		0	1	1	0	0	0	0	0
F	0	0	1	1	1	1		0	1	1	1	0	0	0	0
LT	0	1	X	X	X	X		0	0	0	0	0	0	0	0
OFF	1	X	X	X	X	X		1	1	1	1	1	1	1	1

Static multi-digit display

This is the most straightforward approach to driving a multi-digit display: each digit is driven by an independent latch. The decoding can be performed either by hardware or by software; the software method will, however, require twice as many output instructions as the hardware method. Figure 6 shows an eight-digit static drive with hardware decoding. Memory-mapped I/O is employed, assuming that the memory size is less than 16 kbytes so that ADR14 can be used to select the output port. The system can display both BCD and hexadecimal symbols, depending on the type of decoder used. Figure 7 shows a listing of the program to drive this display.

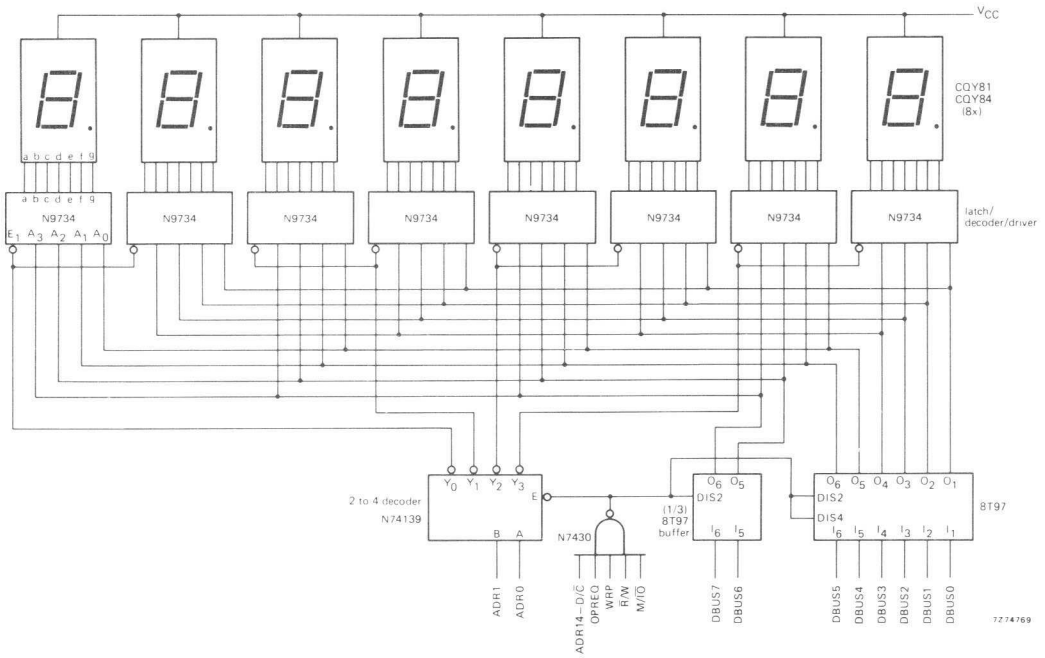

Fig. 6 Eight-digit static drive using hardware decoding.

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TWIN ASSEMBLER VER 2.0                                    PAGE 0001

LINE ADDR  OBJECT  E SOURCE

0001                * DISPLAY DRIVE ROUTINE.
0002                * THIS ROUTINE DRIVES A STATIC 8 DIGIT 7 SEGMENT
0003                * LED DISPLAY.  THE LED DISPLAYS ARE ADDRESSED AS
0004                * MEMORY ( MEMORY MAPPED I/O ).  THE TWO LEAST
0005                * SIGNIFICANT ADDRESSBITS SELECT THE FOUR PAIRS
0006                * OF LED DISPLAYS.  THE MOST SIGNIFICANT ADDRESS
0007                * BIT SELECTS MEMORY OR MEMORY MAPPED I/O
0008                *   ADR 14 = 0 --> MEMORY
0009                *   ADR 14 = 1 --> I/O
0010                *
0011                * DEFINITIONS OF SYMBOLS:
0012 0000           R0      EQU     0       PROCESSOR REGISTERS
0013 0003           R3      EQU     3
0014                *
0015                ********************************************************
0016                *
0017                * PROGRAM MEMORY
0018 0000                   ORG     H'500'
0019 0500 4000      IADR    DATA    H'40,00' INDIRECT ADDRESS
0020                *                       LED DEVICES
0021                *
0022 0502 0704      ROUT    LODI,R3 4       SET INDEX
0023 0504 0F4600    LOOP    LODA,R0 TBL,R3,-  FETCH TWO BCD CODES
0024 0507 CFE500            STRA,R0 *IADR,R3  OUTPUT THIS CODES
0025 050A 5B78              BRNR,R3 LOOP    TEST AND BRANCH IF NOT
0026                *                        ALL DIGITS WRITTEN
0027 050C 40                HALT
0028                *
0029                ********************************************************
0030                *
0031                * RAM MEMORY
0032                * TBL CONTAINS THE INFORMATION WHICH HAS TO
0033                * BE DISPLAYED.
0034 050D                   ORG     H'600'
0035 0600           TBL     RES     1       TWO MOST SIGNIFICANT DIGITS
0036 0601           TBL1    RES     1
0037 0602           TBL2    RES     1
0038 0603           TBL3    RES     1       LEAST SIGNIFICANT DIGITS
0039 0500                   END     IADR

 TOTAL ASSEMBLY ERRORS = 0000
```

Fig. 7 Listing of the program to drive the display of Fig. 5.

Dynamic multi-digit display

This approach uses only one decoder/driver which is time-shared by all the digits. The digit scanning can be performed either by software or by hardware. The software scanning method, however, requires 100% of the CPU's time while the display is activated. Thus, the choice of scanning method will depend upon the particular application.

Sixteen-digit display with software scanning

Figure 9 shows the circuit diagram of a dynamically driven 16-digit display, scanned in a loop of eight pairs of digits by the software. The digits are divided into two groups of eight, each group being driven via a BCD-to-decimal decoder from four bits of the data bus. The microprocessor can thus drive one digit from each group simultaneously by a single write instruction. Digit scanning is performed by a three-bit counter and BCD-to-decimal decoder/driver, providing eight chip enable signals. The counter is incremented each time a pair of digit codes are clocked into the flip-flops. The counter is reset by the RESET signal of the 2650. The digit codes must be output by the software in the correct sequence to remain synchronized with the counter. The listing of the software is given in Fig. 8.

```
TWIN ASSEMBLER VER 2.0                                          PAGE 0001

LINE ADDR  OBJECT  E SOURCE

0001               * DISPLAY DRIVE ROUTINE.
0002               * THIS ROUTINE DRIVES A DYNAMIC 16 DIGIT 7 SEGMENT
0003               * LED DISPLAY, OF WHICH THE TIMING IS DONE BY
0004               * SOFTWARE. THE DISPLAY IS ADDRESSED WITH NON
0005               * EXTENDED OUTPUTPORT D. THE PROCESSOR SCANS
0006               * CONTINEOUSLY THE DISPLAY. IT CAN BE STOPPED BY
0007               * AN INTERRUPT OR BY INSEPTING A TEST AND A BRANCH
0008               * IN THE SCANNING LOOP.
0009               * IN BOTH CASES THE CONTENTS OF INDEX REGISTER R3
0010               * HAS TO BE SAVED. WITH A INTERRUPT ALSO R0 HAS TO
0011               * BE SAVED.
0012               * THE INITIALIZATION OF REGISTER R3 HAS TO BE
0013               * DONE AFTER A RESET.
0014               * LABEL 'ENTRY' IS THE START OF THE ROUTINE WHEN
0015               * THE INITIALIZATION IS DONE.
0016               *
0017               * DEFINITIONS OF SYMBOLS:
0018 0000          R0      EQU     0       PROCESSOR REGISTERS
0019 0003          R3      EQU     3
0020 0003          UN      EQU     3       BRANCH COND. : UNCONDITIONAL
0021               *
0022               ************************************************
0023               * PROGRAM MEMORY
0024 0000                  ORG     H'500'
0025 0500 0708     INIT    LODI,R3 8       INITIALIZE AFTER RESET
0026               *                          OR RESET INDEX
0027               *
0028 0502 0464     LOOP    LODI,R0 100     RESET DELAY COUNTER
0029 0504 F87E     DELAY   BDRR,R0 DELAY   DELAY OF 300 CYCLES
0030               *
0031 0506 0F4600   ENTRY   LODA,R0 TBL,R3,- FETCH TWO BCD CODES
0032               *                          OUT OF THE DATA TABLE
0033 0509 F0               WRTD,R0         OUTPUT THIS CODES
0034 050A 5B76             BRNR,R3 LOOP    BRANCH IF SCAN LOOP
0035               *                          IS NOT READY
0036 050C 1B72             BCTR,UN INIT    CONTINUE WITH RESET INDEX
0037               *
0038               ************************************************
0039               * RAM MEMORY.
0040               * TBL CONTAINS THE INFORMATION WHICH HAS TO
0041               * BE DISPLAYED.
0042 050E                  ORG     H'600'
0043 0600          TBL     RES     1       TWO MOST SIGNIFICANT DIGITS
0044 0601                  RES     6
0045 0607                  RES     1       LEAST SIGNIFICANT DIGITS
0046 0502                  END     LOOP

 TOTAL ASSEMBLY ERRORS = 0000
```

Fig. 8 Listing of the program to drive the display of Fig. 9.

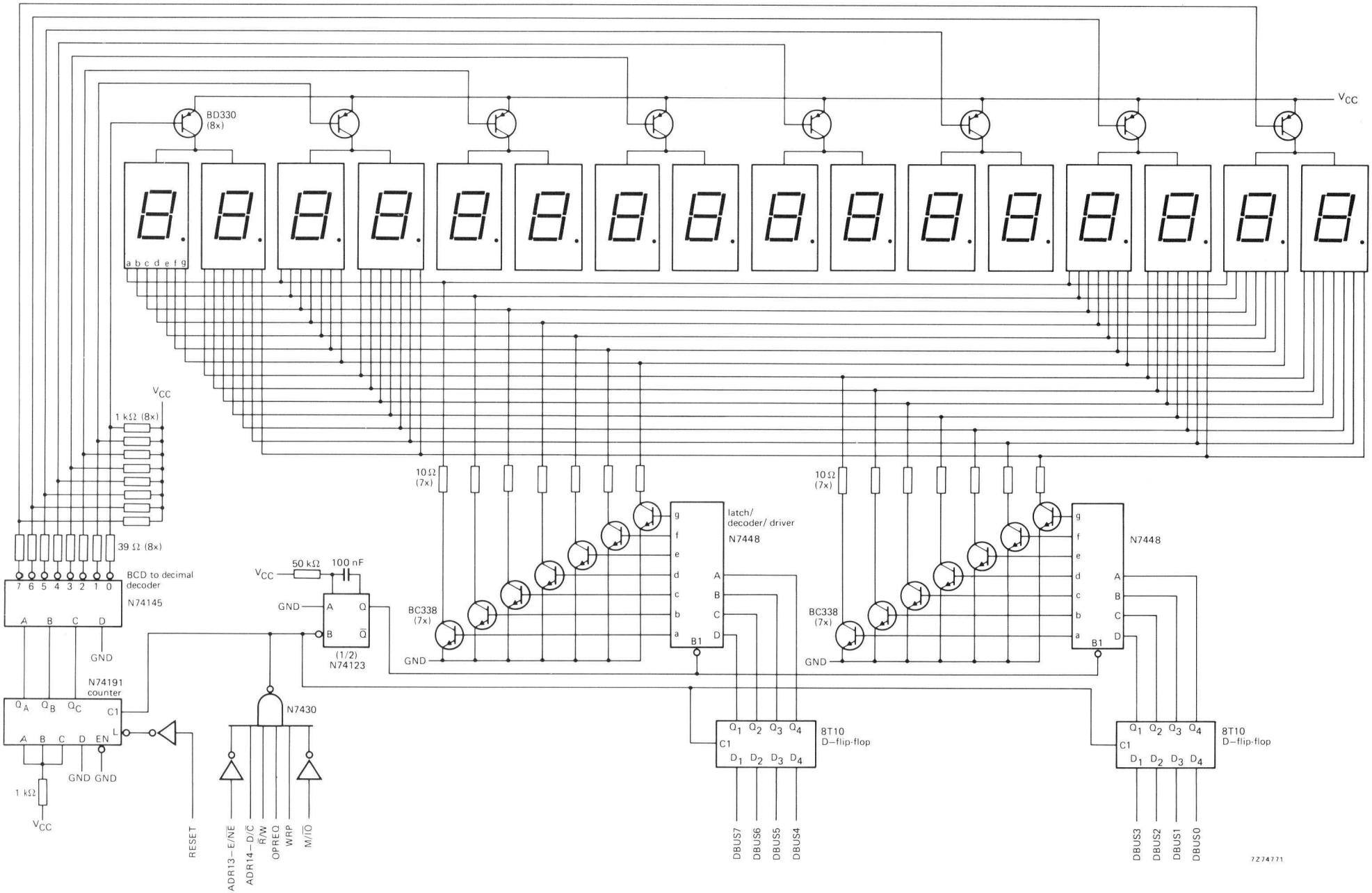

Fig. 9 Dynamic sixteen-digit display with software scanning.

Sixteen-digit display with hardware scanning

In the circuit of Fig. 11, as in the previous example, the digits are driven two at a time in two groups of eight. A hardware clock is used to generate program interrupts, causing entry to the display service routine every 1,8 ms. The chip enable signals are decoded from the three least significant address lines from the 2650.

The execution time of the interrupt routine listed in Fig. 10 is approximately 100 μs (2650 clock frequency = 1,25 MHz). This represents 5,5% of the microprocessor's time, while providing a continuous display. The peak current in the LEDs in the circuits of Figs 9 and 11 is 160 mA. With the duty ratio of 1 : 8, the average segment current is 20 mA, resulting in an easily read display.

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TWIN ASSEMBLER VER 2.0                                          PAGE 0001

LINE ADDR  OBJECT  E SOURCE

0001               * DISPLAY DRIVE ROUTINE.
0002               * THIS ROUTINE DRIVES A DYNAMIC 16 DIGIT 7 SEGMENT
0003               * DISPLAY SYSTEM OF WHICH  THE TIMING IS DONE WITH
0004               * A REAL TIME INTERRUPT CLOCK.
0005               * THE CONTENTS OF INDEX REGISTER R2(REG. BANK1)
0006               * HAS TO BE SAVED BETWEEN TWO INTERRUPTS.
0007               * REGISTER R3(BANK1) IS SUPPOSED TO BE FREE FOR
0008               * SAVING PSL.  THE LED DISPLAYS ARE ADDRESSED AS
0009               * MEMORY (MEMORY MAPPED I/O).  THE THREE LEAST
0010               * SIGNIFICANT ADDRESSBITS SELECT THE EIGTH PAIRS
0011               * OF LED DISPLAYS.  THE MOST SINIFICANT ADDRESS
0012               * BIT SELECTS MEMORY OR I/O.
0013               *
0014               * DEFINITION OF SYMBOLS:
0015 0000          R0     EQU    0        PROCESSOR REGISTERS
0016 0002          R2     EQU    2
0017 0003          R3     EQU    3
0018 0003          UN     EQU    3        BRANCH COND. UNCONDITIONAL
0019 0010          RS     EQU    H'10'    REGISTER BANK SELECT
0020               * RAM MEMORY
0021 0000                 ORG    H'600'
0022 0600          SAVE   RES    1        MEM. LOCATION TO SAVE R0
0023 0601          TBL    RES    1        TWO MOST SIGNIFICANT DIGITS
0024 0602                 RES    6
0025 0608                 RES    1        TWO LEAST SIGN. DIGITS
0026               ********************************************************
0027               * INTERRUPT SERVICE ROUTINE
0028 0609                 ORG    H'500'
0029 0500 7710     INTA   PPSL   RS       REG BANK 1
0030 0502 CC0600          STRA,R0 SAVE    SAVE R0
0031 0505 13              SPSL            SAVE PSL IN R3
0032 0506 C3              STRZ   R3
0033               *
0034 0507 0E4601          LODA,R0 TBL,R2,- FETCH CODES OUT OF
0035 050A CEE51B          STRA,R0 *IADR,R2 TABLE AND OUTPUT THEM
0036 050D 5A02            BRNR,R2 INTB    TEST INDEX
0037 050F 0E08            LODI,R2 8       SET INDEX
0038               *
0039 0511 03       INTB   LODZ   R3       RESTORE PSL
0040 0512 93              LPSL
0041 0513 0C0600          LODA,R0 SAVE    RESTORE  R0
0042 0516 4700            ANDI,R3 H'C0'   RECONSTRUCT COND. CODE
0043 0518 7510            CPSL   RS       REG. BANK 0
0044 051A 37              RETE,UN         RETURN,ENABLE INTERRUPS
0045               *
0046 051B 4000     IADR   ACON   H'4000' INDIRECT ADDRESS OF DISPLAY
0047               * INITIALIZATION
0048 051D 7710     INIT   PPSL   RS       REG. BANK 1
0049 051F 0608            LODI,R2 8       SET INDEX R2
0050 0521 7510            CPSL   RS       REG. BANK 0
0051 0500                 END    INTA

TOTAL ASSEMBLY ERRORS = 0000
```

Fig. 10 Interrupt routine for the circuit of Fig. 11.

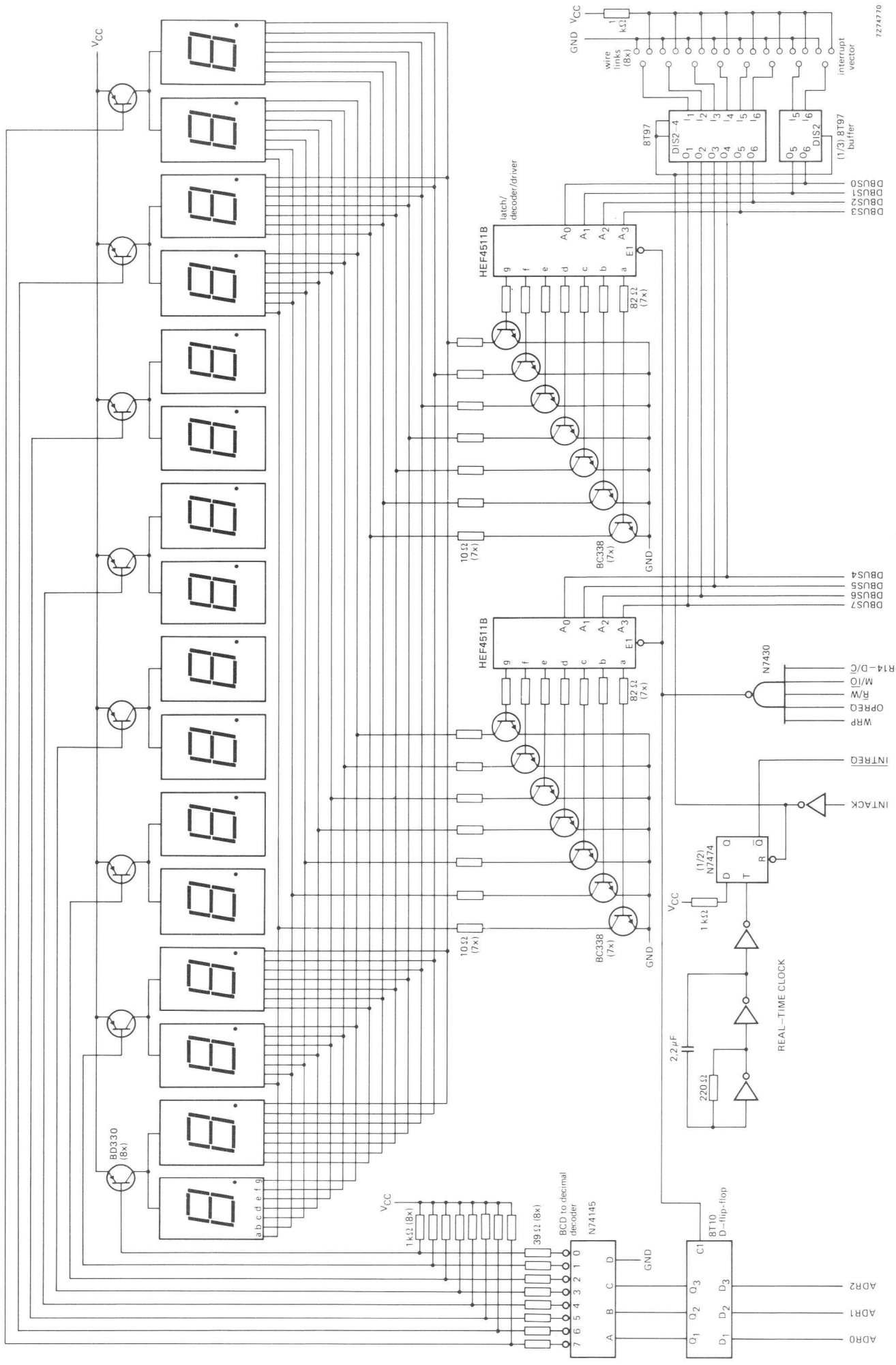

Fig. 11 Dynamic sixteen-digit display with hardware scanning.

Related 2650 publications

no.	title	summary
AS50	Serial Input/Output	Using the Sense/Flag capability of the 2650 for serial I/O interfaces.
AS51	Bit & Byte Testing Procedures	Several methods of testing the contents of the internal registers in the 2650.
AS52	General Delay Routines	Several time delay routines for the 2650, including formulas for calculating the delay time.
AS52	Binary Arithmetic Routines	Examples for processing binary arithmetic addition, subtraction, multiplication, and division with the 2650.
AS54	Conversion Routines	• Eight-bit unsigned binary to BCD • Sixteen-bit signed binary to BCD • Signed BCD to binary • Signed BCD to ASCH • ASCII to BCD • Hexadecimal to ASCII • ASCII to Hexadecimal
AS55	Fixed Point Decimal Arithmetic	Methods of performing addition, subtraction, multiplication and division of BCD numbers with the 2650.
SP50	2650 Evaluation Printed Circuit Board (PC1001)	Detailed description of the PC1001, an evaluation and design tool for the 2650.
SP51	2650 Demo System	Detailed description of the Demo System, a hardware base for use with the 2650 CPU prototyping board (PC1001 or PC1500).
SP52	Support Software for use with the NCSS Timesharing System	Step-by-step procedures for generating, editing, assembling, punching, and simulating Signetics 2650 programs using the NCSS timesharing service.
SP53	Simulator, Version 1.2	Features and characteristics of version 1.2 of the 2650 simulator.
SP54	Support Software for use with the General Electric Mark III Timesharing System	Step-by-step procedures for generating, editing, assembling, simulating, and punching Signetics 2650 programs using General Electric's Mark III timesharing system.
SP55	The ABC 1500 Adaptable Board Computer	Describes the components and applications of the ABC 1500 system development card.
SS50	PIPBUG	Detailed description of PIPBUG, a monitor program designed for use with the 2650.
SS51	Absolute Object Format	Describes the absolute object code format for the 2650.
MP51	Initialization	Procedures for initializing the 2650 microprocessor, memory, and I/O devices to their required initial states.
MP52	Low-Cost Clock Generator Circuits	Several clock generator circuits, based on 7400 series TTL, that may be used with the 2650. They include RC, LC and crystal oscillator types.
MP53	Address and Data Bus Interfacing Techniques	Examples of interfacing the 2650 address and data busses with ROMs and RAMs, such as the 2608, 2606 and 2602.
MP54	2650 Input/Output Structures and Interfaces	Examines the use of the 2650's versatile set of I/O instructions and the interface between the 2650 and I/O ports. A number of application examples for both serial and parallel I/O are given.
TN 064	Digital cassette interface for a 2650 microprocessor system	Interface hardware and software for the Philips DCR digital cassette drive.
TN 069	2650 Microprocessor keyboard interfaces	Simple interfaces for low-cost keyboard systems.
TN 072	Introducing the Signetics 2651 PCI Terminology and operation modes	Description of the 2651 Programmable Communications Interface IC.
TN 083	Using the Signetics 2651 PCI with popular microprocessors	Simple hardware interfaces to use the 2651 Programmable Communications Interface with various microprocessors.

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