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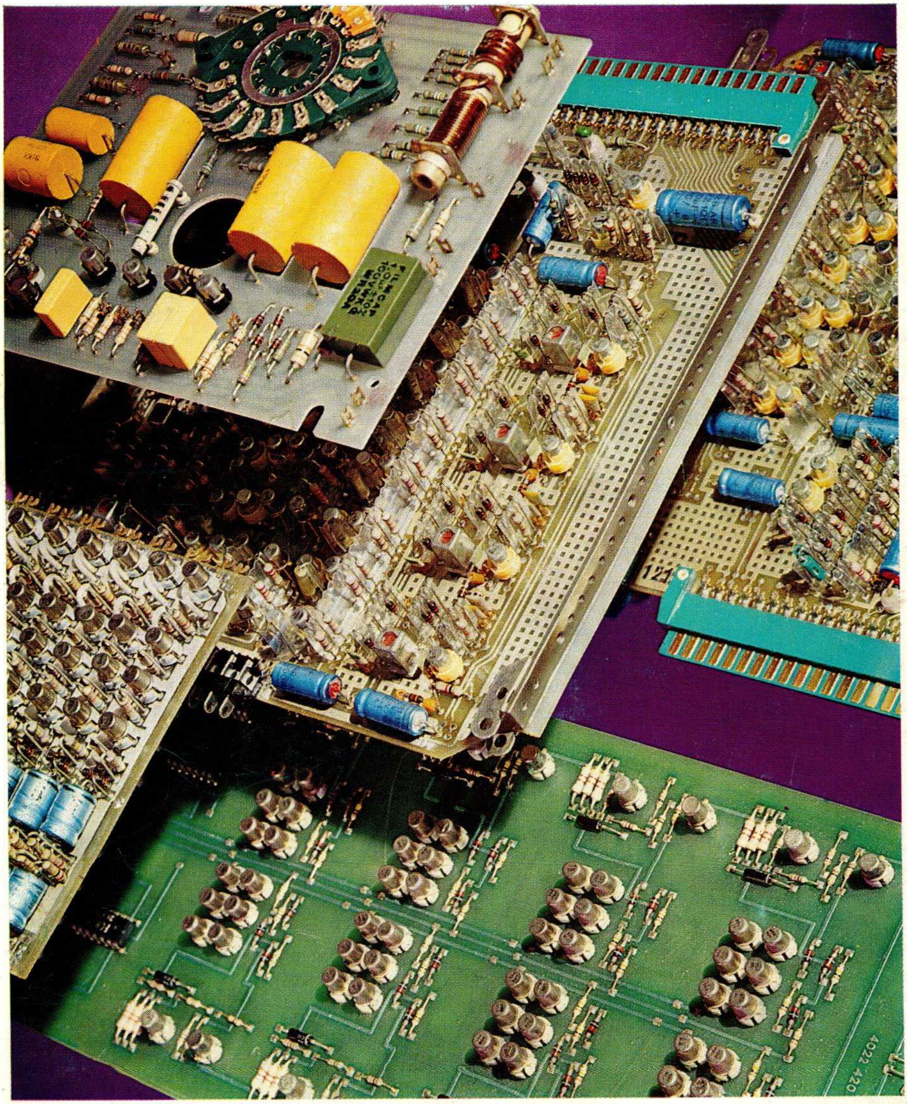
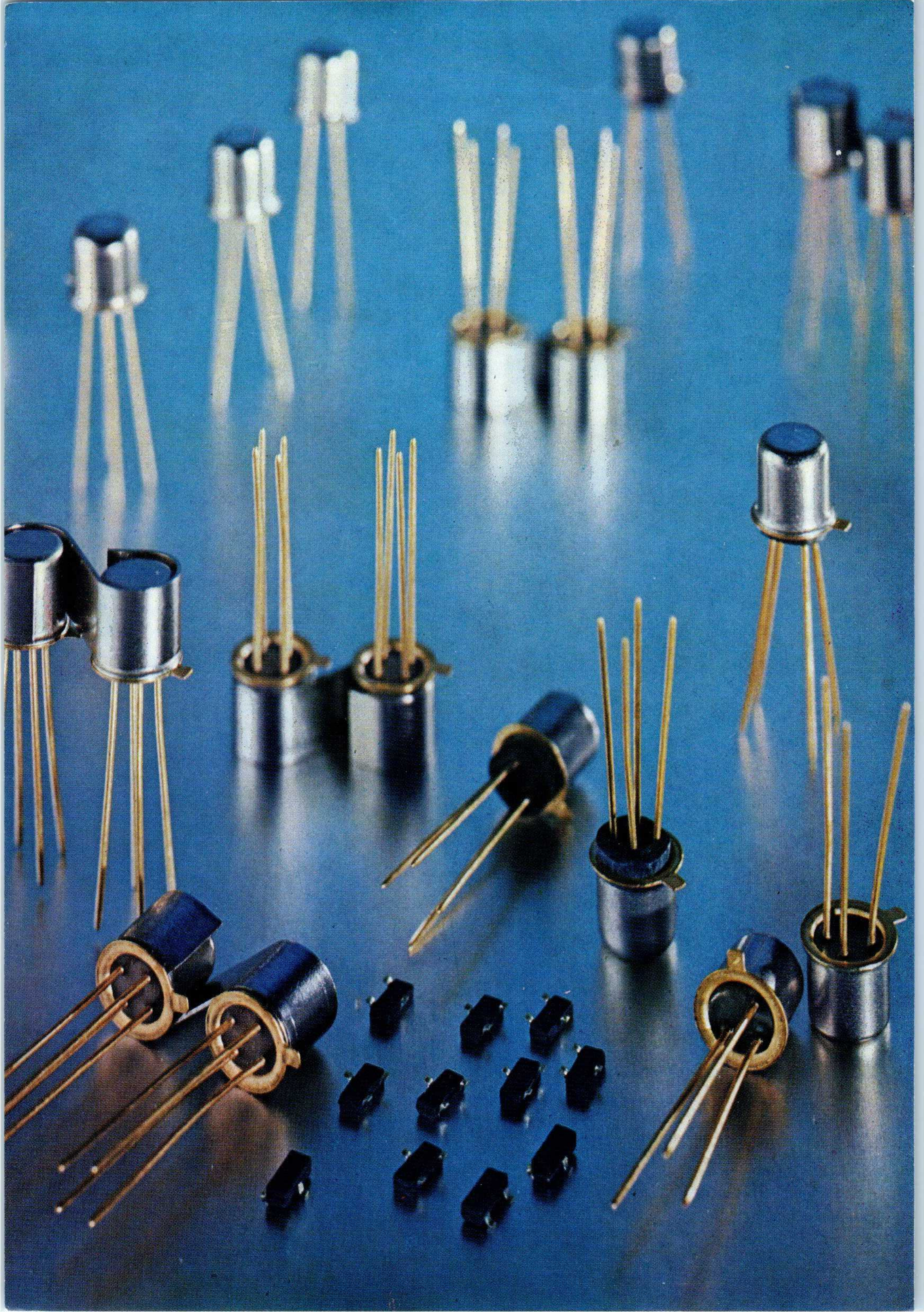
Application book

Electronic components and materials

Field effect transistors



Field-Effect Transistors



Field-Effect Transistors

PUBLICATIONS DEPARTMENT
ELECTRONIC COMPONENTS AND MATERIALS DIVISION

Contents

This book is based in part on Feldeffect-Transistoren by J. Wüstehube, Valvo GmbH, Germany, 1968; and in part on more recent material supplied by J. J. Hanse and B. J. M. Overgoor of Philips' Elcoma Division, The Netherlands, and J. J. Barham and J. A. Garters of Mullard Ltd., England. It has been edited by N. R. Bijlsma and P. Burwell of Elcoma Publications in cooperation with E. G. Evans of Central Technical Services, Mullard Ltd.

Foreword

The field-effect transistor operates on an entirely different principle from the bipolar transistor and, consequently, shows different characteristics. Having at his disposal integrated circuits and bipolar transistors as well as field-effect transistors can be of great value to the circuit designer provided he is acquainted with the specific characteristics of all three of these components. He must, of course, also be keen to recognize how these characteristics can be turned to optimum use. This book is intended to acquaint the designer with the characteristics of both junction-gate and insulated-gate field-effect transistors. Although it is primarily an Application Book, we thought that it might be useful first to discuss structure and functioning of both types of field-effect transistor and their respective characteristics that are most important to the customer. However, to fit in the framework of this book, the general part of this book could not be much more than a simple guidance for the circuit engineer. Those who wish to study the subject matter in further detail, have a wealth of literature at their disposal.

The application part contains numerous examples of applications based on the characteristics of field-effect transistors. Although these examples are related to highly concrete and actual applications, they serve primarily to illustrate the possibilities that FETs offer for similar applications.

The possibilities offered by applying FETs in specific application fields such as differential amplifiers, switching applications and communication equipment, are discussed in greater detail.

1 Introductory Survey

A field-effect transistor (FET) consists basically of a semiconducting current channel, the resistance of which is controlled by an electric field applied at right angles to the direction of current flow. The main difference between field-effect transistors and normal junction transistors is that in FETs the current is only carried by the majority charge carriers. Field-effect transistors are thus "unipolar" transistors, i.e. only one type of charge carrier is responsible for their action, unlike normal transistors, which are "bipolar".

Although field-effect transistors were originally described in detail and analysed in 1952 by Shockley, they remained in the laboratory stage for a long time. The evolution of the bipolar transistor had to take place to make possible today's practical FETs. A deeper knowledge of material properties was necessary, and the technologies of diffusion, photo-etching, masking, and planar and epitaxial construction were yet to be found and mastered.

Two main types may be distinguished at present:

a. Junction field-effect transistors.
   These are p-n junction field-effect transistors, also referred to as PN-FETs or simply FETs.
b. Insulated-gate field-effect transistors.
   The commonest type of IG-FET is the MOS-FET, characterised by the presence of metal, oxide and semiconductor layers in that order.

1.1 Terminology, characteristics, symbols

A field-effect transistor generally has three electrodes, called the source (s), the drain (d) and the gate (g); these names have been used exclusively in the Anglo-Saxon literature since 1952.

Fig. 1 shows a typical family of characteristics for a junction field-effect transistor. Comparison of these curves with those of a pentode tube shows that the source, drain and gate correspond to the tube cathode, anode and grid.

Fig. 1 also gives the symbol normally used for a junction field-effect transistor in circuit diagrams. In addition, the gate lead is normally indicated by an arrow (cf. Fig. 7). This arrow also indicates (as with bipolar transistors) the current direction or the polarity of the drain-source voltage for which the field-effect transistor has been designed. However, the functions of drain and source can in principle be interchanged (as with bipolar transistors, but unlike tubes); in accordance with this, the characteristics of Fig. 1 are continued into the third quadrant.

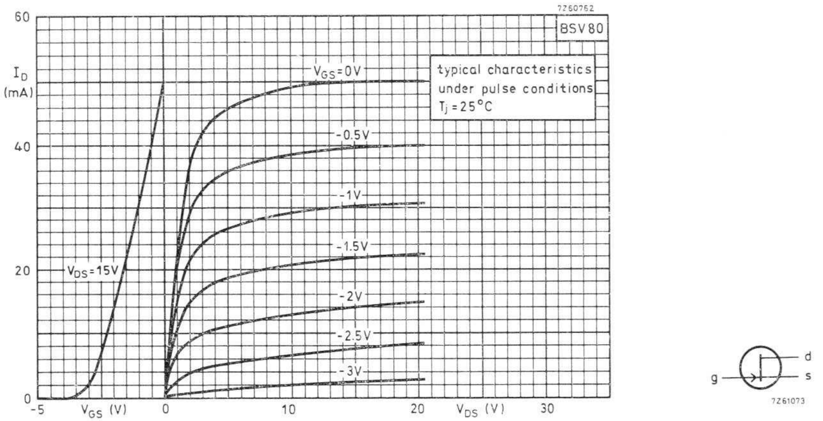


Fig.1 Symbol for a junction field-effect transistor, with an example of a family of output characteristics.

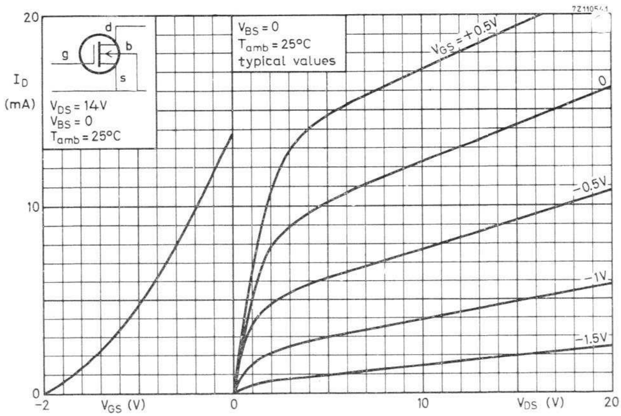


Fig.2 Symbol for a MOS field-effect transistor, with an example of a family of output characteristics and an input characteristic. The gate voltage of a MOS-FET can change sign.

Fig. 2 shows the characteristics of a MOS field-effect transistor. These also resemble pentode tube characteristics; the main difference between the PN-FET and the MOS-FET is that because the control electrode in the latter is insulated, the polarity of the gate-source voltage can be reversed. An arrow is used to indicate the substrate lead and shows the direction of the current-flow for the MOS as well as for the PN-FET in the forward-biased condition of the p-n junction (see also section 3.3).

1.2 Special properties of field-effect transistors and their practical significance

Field-effect transistors combine most of the good points of tubes and bipolar transistors. They require no heating, and are small. Like bipolar transistors, they can form part of integrated circuits (with MOS-FETS, this is particularly simple, as no extra insulation is required); and if necessary, they can be combined with bipolar transistors in such circuits.

Their input resistance is as high as that of electron tubes, while the MOS type has the additional advantage that the high input resistance is independent of the polarity of the control-electrode voltage (gate voltage), unlike the case with tubes. Direct connections can thus be made without the need for additional circuitry.

Fig. 3 shows an inverter stage constructed with the aid of a "normally-off" MOS-FET. (A normally-off or enhancement-type MOS-FET passes no current when the gate-source voltage is zero; this voltage must rise above a certain threshold value before drain current starts to flow; the current then increases with increasing voltage). If the threshold value of the gate source voltage is 3 V, then the inverter will be cut off at an input voltage of +2 V (Fig. 3 left), and

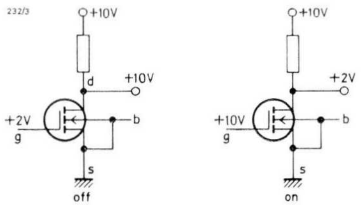


Fig.3 An inverter based on a MOS field-effect transistor ("normally-off" n-channel type; see section 3.2).

will pass current at a voltage of +10 V, Fig. 3 right. If the circuit is suitably dimensioned, the inverted signals at the output can share the same voltage levels, so that a number of these stages can be coupled directly. When bipolar transistors are used for such an application, additional circuitry is generally needed to deal with the potential differences between stages.

Complementary field-effect transistors (p-channel and n-channel types) can be made, and combined with advantage, as is the case with bipolar p-n-p and n-p-n transistors. For example, Fig. 4 shows a complementary inverter. This circuit acts as a commutator, connecting the output via a relatively low resistance either to earth or to the point +V.

Apart from small leakage currents (represented by the current generators in Fig. 4, right), no current flows during either of the two switching states, as long as the stages connected to the output are also MOS-FET stages, and if the output is unloaded. Power losses thus occur only during the actual switching process, as a result of transitory capacitive charge-transfer currents. In neither of its static states does the circuit consume any power.

As already stated, the current through field-effect transistors can be reversed, as with bipolar transistors; if use is made of this property, field effect transistors may be made symmetrical.

With small signals (near the origin of Fig. 1 or 2), a FET behaves like a linear resistor, which can be switched from a few hundred ohms to several hundred megohms by means of the gate voltage. This can be useful in low-drift chopper

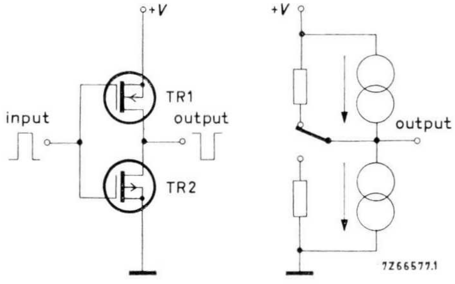


Fig.4 Complementary inverter with MOS field-effect transistors. The leakage currents, represented as current generators in the equivalent circuit, are very small (of the order 1 pA to 1 μA); the on-resistances are a few hundred ohms.

circuits, because unlike bipolar transistors, there is no e.m.f. in series with this resistor, and hence no error (offset) voltage. With higher drain-source voltages the resistance of a FET becomes highly non-linear; this can be used to good advantage in (integrated) digital circuits or in limiters.

The storage of minority charge carriers in bipolar transistors and the associated storage times lead to difficulties in high-frequency switching applications. Such storage effects are not found with majority charge carriers, which are operative in field-effect transistors, and hence lower switching times can be achieved.

Compared with bipolar transistors and tubes, field-effect transistors in (a.g.c.) controlled h.f. input stages give low noise and low cross-modulation (square-law input characteristic). Further, their operation is not much affected by radioactive radiation, because the life of the charge carriers does not play such an important role as in the diffusion of minority charge carriers in the base zone of bipolar transistors. Field-effect transistors are inherently less temperature sensitive than bipolar transistors, and are not prone to thermal run-away, because their current falls with increasing temperature, whereas it rises in bipolar transistors.

Finally, the operating point of depletion type field-effect transistors, like that of tubes, can be adjusted without the consumption of any power by "automatic grid bias"; this gives simpler circuits than with bipolar transistors.

2 The junction field-effect transistor

2.1 Mode of operation

2.1.1. Structure and characteristics

Fig. 5 sketches the structure of a junction field-effect transistor.[1] The source lead s and the drain lead d are connected by an n-type region, the "channel". A device of this kind is called an n-channel FET. With a positive voltage between drain and source, electrons (the majority charge carriers) move from the source to the drain, i.e. a current flows through the channel from d to s.

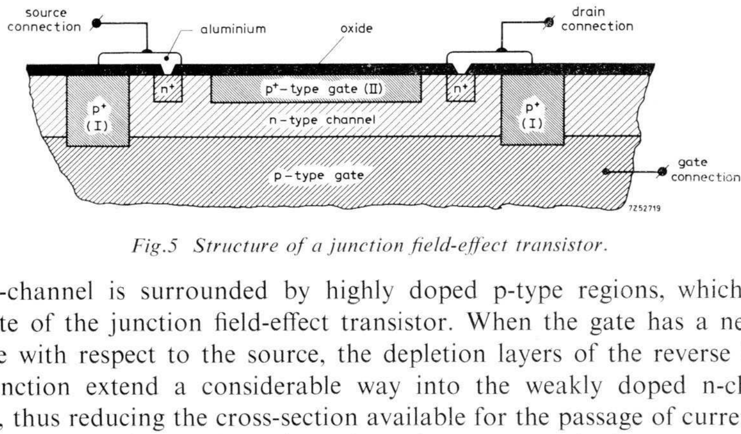


Fig.5 Structure of a junction field-effect transistor.

The n-channel is surrounded by highly doped p-type regions, which form the gate of the junction field-effect transistor. When the gate has a negative voltage with respect to the source, the depletion layers of the reverse biased p-n junction extend a considerable way into the weakly doped n-channel region, thus reducing the cross-section available for the passage of current (see Fig. 6). Because of the voltage drop along the current path, the reverse voltage at the p-n junctions increases from s to d, and with it the width of the depletion layers (see Fig. 6). On this basis, we can give a qualitative explanation of the output characteristics shown in Fig. 7 (right).

When the voltage V_{DS} is increased from zero at constant V_{GS}, the current I_D initially increases linearly with the voltage, the channel resistance remaining more or less constant (ohmic range). As the current increases more, the channel starts to become appreciably narrower, the channel resistance increases, and the rate of increase of I_D with V_{DS} becomes progressively lower, until the two depletion layers nearly touch one another at the drain end of the channel. The channel is now said to be "pinched off".

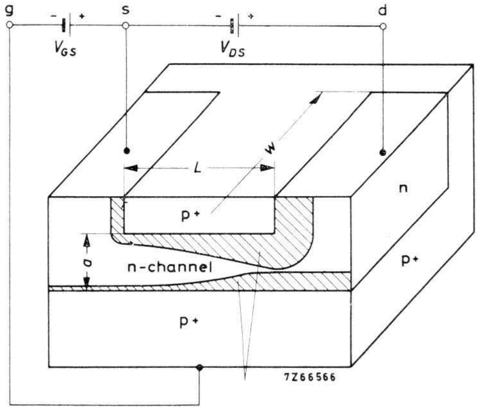


Fig.6 Schematic sectional view of a junction field-effect transistor (PN-FET), n-channel type. (The two p^+ regions – upper and lower gate – should also be imagined to be connected in front of the plane of the paper, so that the n-channel is in fact surrounded by an annular gate region).

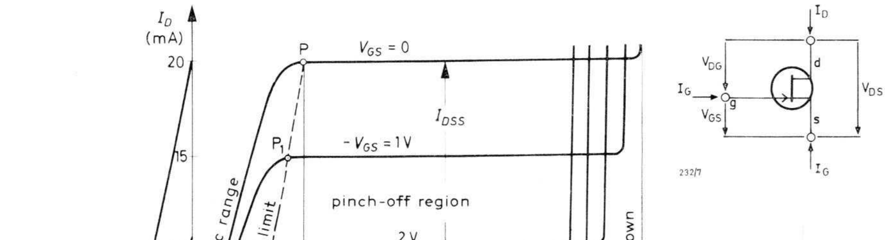


Fig.7 Characteristics of an n-channel junction field-effect transistor. Pinch-off voltage, $V_P = -6$ V.

The line joining the various drain-source voltages $V_{DS(P)}$ at which this pinch-off occurs (the pinch-off limit) is shown as a broken line in Fig. 7. $V_{DS(P)}$ is often also called the knee voltage. To the right of the pinch-off limit – in the pinch-off region* – the drain current only increases very slightly (see section 2.1.4).

As the reverse voltage V_{GS} between the gate and the source increases, the depletion layers on both sides of the channel become wider and the channel itself becomes narrower at a given channel current. The cut-off limit is thus reached earlier, i.e. at a lower current and a lower value of $V_{DS(P)}$. The $I_D - V_{DS}$ characteristic thus shifts towards lower drain currents with increasing gate-source voltage.

In order to prevent a rapid decrease of the gate input resistance, the gate-to-channel diode should not be allowed to become forward biased. In practice no appreciable gate current will flow at forward voltages below about 0.5 V, whereas at higher voltages the p-n junction becomes forward biased and gate current increases exponentially. This corresponds to the grid current in tubes.

If the dopings shown in Fig. 5 are reversed, we get a p-channel field-effect transistor. If the supply voltages are also reversed, this behaves in a complementary way to the n-channel FET. Under normal operating conditions the current in a p-channel FET flows from the source to the drain. In our following considerations we shall restrict ourselves mainly to n-channel transistors.

2.1.2 The pinch-off voltage

A fundamental quantity of the field-effect transistor is the pinch-off or threshold voltage V_P, which is defined as the reverse voltage between the gate zone and the channel zone at which the two depletion layers meet – i.e. at which the channel is pinched off.

The pinch-off voltage increases with the doping level in the channel zone, and with the distance a between the two gate zones. This voltage appears at two points in the characteristics shown in Fig. 7. In the first place the channel can be pinched off by applying the pinch-off voltage between gate and source in the reverse direction. Under these conditions the two depletion layers meet

*) *In the American literature, this region is generally called the saturation region. However, we prefer not to use this term here, as it has already become established in quite a different sense for bipolar transistors. In this latter case, it is used — in accordance with IEC recommendations — to denote the region to the left of the knee voltage.*

along the whole length of the channel, as shown in Fig. 8*a*, and no drain current can flow. Consequently V_P is the gate-source voltage at which the channel current becomes zero, and only a small gate leakage current remains (see Fig. 7 left). In n-channel junction FETs the gate potential must be made negative with respect to the source to achieve pinch-off. The sign of the pinch-off voltage is as follows:

for the n-channel junction FET: $V_P < 0$,
for the p-channel junction FET: $V_P > 0$.

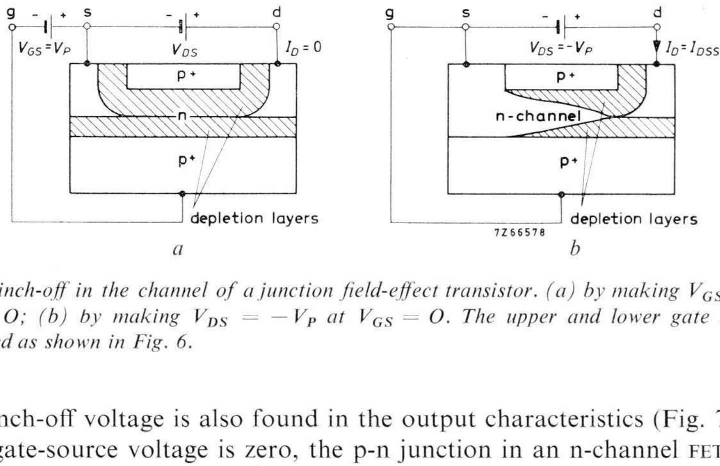


Fig.8 Pinch-off in the channel of a junction field-effect transistor. (a) by making $V_{GS} = V_P$ at $V_{DS} = 0$; (b) by making $V_{DS} = -V_P$ at $V_{GS} = 0$. The upper and lower gate zones are connected as shown in Fig. 6.

The pinch-off voltage is also found in the output characteristics (Fig. 7 right); if the gate-source voltage is zero, the p-n junction in an n-channel FET can be cut off by means of a positive drain-source voltage (Fig. 8*b*), which makes the n-type channel zone positive with respect to the p-type gate zones. Pinch-off will occur when $V_{DS} = -V_P$, in so far as the conductor resistance between the ends of the channel and the source or drain lead is negligible. This means that the characteristic for $V_{GS} = 0$ cuts the pinch-off limit at $V_{DS} = -V_P$ (point P in Fig. 7). In this case, the two depletion layers only touch at the drain end of the channel, because of the voltage drop caused by the drain current flowing through the channel resistance.

Since the positions of point P in Fig. 7 and of the foot of the $I_D - V_{GS}$ curve are both difficult to measure, it has been suggested [2] that V_P can be more accurately determined by plotting the ratio I_D/g_m (where g_m is the transconductance, see section 4.2) against the voltage V_{GS}. This should theoretically give a straight line, which when extrapolated cuts the V_{GS} axis at $V_{GS} = V_P$. As this is a rather unpractical method, a quantity $V_{(P)GS}$ has been introduced. This is the value of V_{GS} at an extremely small but measurable drain current, of the order 1 nA.

2.1.3. The drain-source short-circuit current, I_{DSS}

Another important d.c. characteristic of the field-effect transistor is I_{DSS}, the drain current in the pinch-off region at $V_{GS} = 0$ (see Figs 7 and 8*b*). (The second *S* in the subscript refers to the short-circuit between the source and the gate.) This current is called the (saturated) drain-source short-circuit current; its value depends, amongst other things, on the doping level of the channel zone and its geometrical form, and to a lesser extent on the impurity profile in a plane perpendicular to the junction. In nearly all cases however the following relation holds:

$$I_{DSS} \sim \frac{W}{L} \cdot \mu_V, \tag{1}$$

where

W = channel width (Fig. 6),
L = channel length (Fig. 6),
μ_V = mobility of charge carriers in channel (volume mobility).

As will be shown in section 2.1.4, the transconductance of a field-effect transistor at a given pinch-off voltage is proportional to I_{DSS}. To obtain a high transconductance therefore, the ratio W/L of the field-effect transistor should be made as large as possible.

Under normal operating conditions, the drain current of a junction field-effect transistor cannot be raised much above the value I_{DSS}, as the gate-channel p-n junctions will then be biased in the forward direction. In general, when the FET is used for amplification purposes, the quiescent current will be set lower than I_{DSS}, determined by the required dynamic range of the a.c. input signal.

The current I_{DSS} increases somewhat with the voltage V_{DS}, as the output characteristics are not absolutely horizontal in the pinch-off region as indicated in Fig. 7, but climb slightly with V_{DS} as shown in Fig. 1. Measured values of

I_{DSS} are therefore always quoted with the corresponding value of V_{DS}. The sign of I_{DSS} is given by the following:

for n-channel types: $I_{DSS} > 0$,
for p-channel types: $I_{DSS} < 0$.

2.1.4 Characteristics

In Fig. 8*b* we noticed that the wedge-shaped depletion layers at both sides of the channel at $V_{GS} = 0$ are due to the voltage drop V_{DS} caused by the drain current flowing through the channel resistance. In addition, it is possible to apply a negative gate-source voltage V_{GS}, which adds to the existing gate-to-channel voltage and gives a corresponding contribution to the expansion of the depletion layers. As a result of the applied V_{GS}, therefore, the current carrying channel becomes narrower and consequently its resistance increases.* This shows up in a smaller initial slope of the $I_D - V_{DS}$ characteristic (see Fig. 7). Because of the fact that V_{GS} contributes to the depletion layer, pinch-off occurs at a correspondingly lower value of the drain-source voltage (point P_1 in Fig. 7), given by:

$$V_{DS(P)} = V_{GS} - V_P. \tag{2}$$

This equation defines the pinch-off limit in Fig. 7. From the smaller initial slope together with the lower value of $V_{DS(P)}$ it follows that the value of I_D in the pinch-off region decreases more than proportionally with the applied voltage V_{GS}.

With the help of a number of simplifying assumptions,[1] the dependance of I_D on V_{GS} in the pinch-off region can be described by:

$$I_D = I_{DSS}\left\{1 - \frac{V_{GS}}{V_P}\right\}^n, \text{ with } V_{DS} \text{ constant and } \geqslant V_{DS(P)}. \tag{3}$$

This equation describes the transfer characteristic in the left part of Fig. 7. The exponent n in the equation is in practice roughly equal to 2; that is, the drain

*) *Even at $V_{GS} = O$ and $I_D = O$, a depletion layer is present across the gate channel junction, caused by the temperature dependent diffusion voltage (see also 4.1.1).*

current varies approximately as the square of the control voltage. This is why FETs offer lower distortion than bipolar transistors with their exponential transfer characteristics. Making similar assumptions, it has been shown [1] that the equation in the pre-pinch-off region is given by:

$$I_D = I_{DSS}\left\{\frac{2\,V_{DS}}{-V_P}\left(1-\frac{V_{GS}}{V_P}\right)-\frac{V_{DS}^2}{V_P^2}\right\} \text{ for } V_{DS} \leqslant V_{DS(P)}. \tag{4}$$

From (3), with $n = 2$, we can derive the transconductance in the pinch-off region:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = 2\frac{I_{DSS}}{-V_P}\left(1-\frac{V_{GS}}{V_P}\right) = \frac{2}{-V_P}\sqrt{I_{DSS}\cdot I_D} \text{ for } V_{DS} \geqslant V_{DS(P)}, \tag{5}$$

showing a linear dependence on V_{GS} and $\sqrt{I_D}$.

Similarly, from (4),

$$g_m = \frac{2\cdot I_{DSS}\cdot V_{DS}}{V_P^2} \text{ for } V_{DS} \leqslant V_{DS(P)}. \tag{6}$$

Thus, in pre-pinch-off, g_m is independant of V_{GS}. From equation (4) we can also derive the output conductance g_{os} or the incremental drain-source resistance r_{ds} in the pre-pinch-off area:

$$-g_{os} = \frac{\Delta I_D}{\Delta V_{DS}} = \frac{1}{r_{ds}} = 2\cdot\frac{I_{DSS}}{V_P^2}(-V_P + V_{GS} - V_{DS}),$$

$$\text{for } V_{DS} \leqslant V_{DS(P)}. \tag{7}$$

Equation (3) suggests that the output conductance in the pinch-off region is zero. This is because the equation is based on the assumption that the channel profile to the left of the pinch-off point in Fig. 6 is completely independent of drain current for $V_{DS} > V_{DS(P)}$. In fact, however, when the voltage V_{DS} increases, not only do the depletion layers expand in the direction of the drain lead, but the pinch-off point also shifts slightly towards the source. The channel thus becomes shorter, so that the drain current increases slightly with the drain-source voltage (see equation 1). The output characteristics (Fig. 7) are

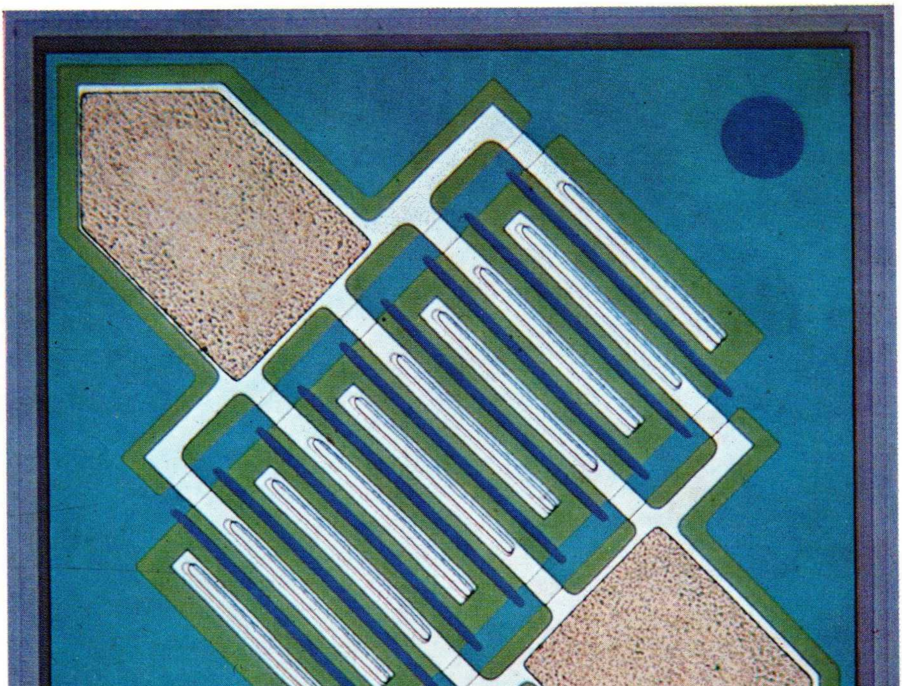


Plate A. Symmetrical construction of an n-channel junction FET (BFW10 . . . BFW13; see Fig. 9) yielding a low on-resistance and a low gate-capacitance.

thus not strictly horizontal beyond the pinch-off limit: so the field-effect transistor has a finite output conductance. This influence of the voltage V_{DS} on the length of the channel is stronger (and hence the output conductance is higher), as the channel becomes shorter. On the other hand, a short channel is desirable in connection with a high transconductance. With channel lengths of a few microns, the output conductance is about 100 times smaller than the transconductance.

2.2 Structure of junction field-effect transistors

The ratio W/L of a field-effect transistor (see Fig. 6) must be high if a high transconductance or a low on-resistance is required. On the other hand $W \cdot L$ is proportional to the gate-channel junction area and consequently to the gate-capacitance. Thus a low gate-capacitance requires a low $W \cdot L$ product. So an optimal design will aim at the lowest possible L and adapt W accordingly. A practical geometry of a FET is given in Plate A, where 9 channels are connected in parallel between interdigitated source and drain regions. Note that the construction is symmetrical so that source and drain contacts can be interchanged. Fig. 9 gives a cross-section through the transistor in a plane perpendicular to the contact fingers.

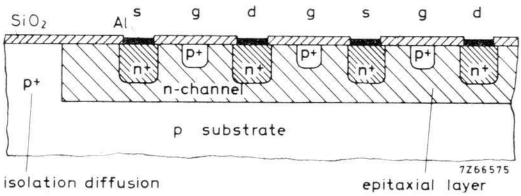


Fig.9 Cross-section through the crystal of the n-channel junction field-effect transistor BFW10, at right angles to the "teeth of the comb" of Plate A.

The starting material is a slice of highly doped (i.e. relatively low-ohmic) p-type silicon (the substrate), that is provided with an n-type epitaxial layer.

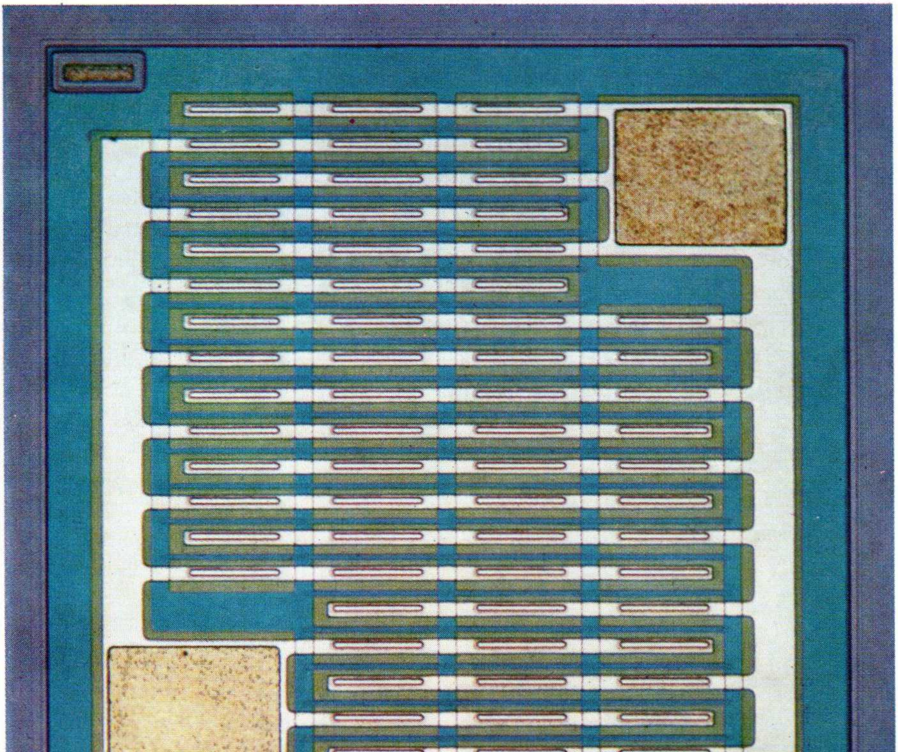


Plate B. Construction of an n-channel junction FET BSV78 to 80 in which W/L is about 5 times greater than in the FET of Plate A. This gives a very low on-resistance.

Using the planar technique, separate n-type islands are formed for each transistor on the slice by means of isolation diffusion. Next, thin p^+ strips are diffused, forming the upper gate-channel junction. These gate-zones are internally connected with the substrate, which forms the lower gate-channel junction, in front of and behind the plane of the paper in Fig. 9, where they meet the isolation diffusion.

In a final diffusion step, the source and drain regions are provided with highly conductive n^+ zones. This lowers the source and drain series resistance and ensures a good ohmic contact with the metal contact fingers that are vacuum deposited subsequently.

Plate *B* gives another example of a junction FET. In this case the aim was to achieve a very low on-resistance. This is realised by making W/L about 5 times greater than in the FET depicted in Plate *A*.

3 The MOS field-effect transistor

3.1 Mode of operation

Unlike the junction field-effect transistor, the MOS field-effect transistor has a metal gate electrode which is electrically insulated from the semiconductor crystal by a thin oxide film.[3,4]

This sequence of metal, oxide and semiconductor has given this type of transistor its name of MOS-FET.

Fig. 10 shows a cross-section of a MOS-FET. Two strongly doped n-type zones (n^+) are diffused into the p-type substrate for the source and drain. The metallic gate electrode forms a plate capacitor with the underlying substrate or channel region; the dielectric is formed by the oxide film. When the gate has a positive voltage with respect to the substrate, electrons in the substrate are attracted to and holes repelled from the silicon-silicon dioxide interface by polarisation, thus giving an n-type layer (inversion layer) under the dielectric between the source and the drain. This inversion layer is called "n-channel". When a drain-source voltage is applied a current I_D flows through this channel.

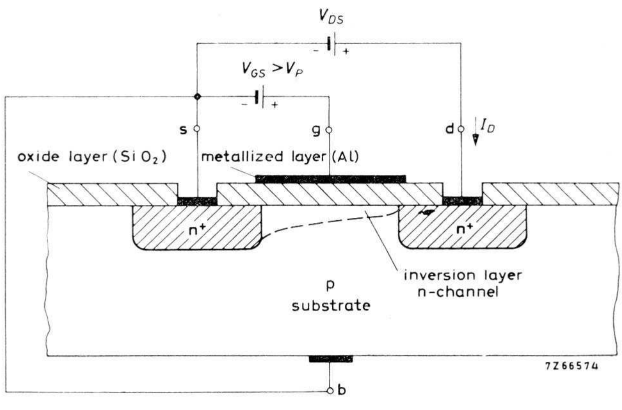


Fig.10 Schematic cross-section through a MOS field-effect transistor (MOS-FET), n-channel enhancement type ("normally-off").

Variation of the voltage V_{GS} changes the electron density, and hence the resistance of the n-channel, and therefore the current I_D. In contrast with the junction-FET however, the gate voltage of the MOS-FET can change sign without a gate current starting to flow.

3.2 Enhancement ("normally-off") and depletion („normally-on") types of MOS-FET

The type of MOS-FET previously described is an n-channel enhancement type; that is, the number of mobile charge carriers (electrons) must first be increased (enhanced) by applying a positive gate voltage. There is no channel present at zero gate voltage; since a positive drain voltage causes the p-n junction between the drain zone and the substrate to be cutt off, no current apart from leakage currents will flow between source and drain while the gate voltage remains zero.

The voltage V_{GS} at which appreciable current flow starts, due to the formation of an inversion layer, is called either the pinch-off voltage V_P (as with the junction-FET), or the threshold voltage V_T. Fig. 12*a* shows the family of characteristics of an enhancement type.

The opposite of an enhancement type is a depletion type, where a conducting

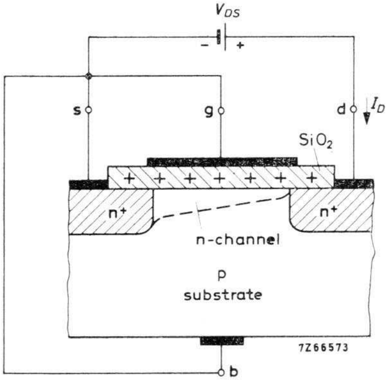


Fig.11 Schematic cross-section through a MOS field-effect transistor, n-channel depletion type ("normally-on").

channel is present even in the absence of a gate voltage. This effect is caused by the immobile positive ions which are always present in the oxide layer (see section 3.4). These ions give rise to an n-type inversion layer in the p-type substrate, even at $V_{GS} = 0$, so that a channel is formed. This is shown in Fig. 11.

When the gate voltage is made negative, the stock of mobile electrons in the n-channel is depleted, and the drain current falls to zero. When the gate voltage is positive, the electron density and hence the drain current is increased again as in the enhancement type. This means that a depletion type MOS field-effect transistor can be used in both the depletion and the enhancement mode (Fig. 12*b*). The junction-FET, on the contrary, is generally applied in the depletion mode, because enhancement mode operation results in forward biasing of the gate-to-channel diode.

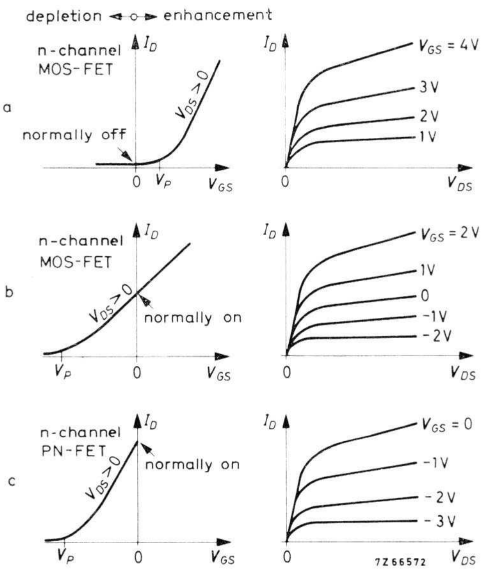


Fig.12 Examples of characteristics of field-effect transistors. (a) normally-off (enhancement type), (b) normally-on (depletion and enhancement type), (c) pure depletion-type (only found in junction FETs).

It would seem better to make use of the distinction between the two modes of operation: "normally on" and "normally off", as has been done in American literature. These two terms have the following significances:

normally on: an appreciable drain current flows at $V_{GS} = 0$,
normally off: practically no drain current flows at $V_{GS} = 0$.

The main advantage of such a classification of MOS-FETs is that it is based directly on a characteristic electrical property of the device and not on physical processes in which the user is not directly interested, and which have to be translated into terms of electrical performance.

It follows that the junction field-effect transistor fits into this classification as a "normally-on" type (Fig. 12*c*).

With normally-off types, the gate operating potential lies between the source and drain potentials; this is also the case with bipolar transistors, where the base potential lies between that of the emitter and collector. In normally-on types on the other hand, the gate potential lies outside the potential levels of drain and source, and an "automatic gate bias" can be derived with the aid of a resistor in the source lead (see Fig. 38*a*).

3.3 P-channel and n-channel MOS-FETs; symbols; normal and inverse operation

In p-type MOS-FETs the dopings shown in Fig. 10 are reversed, and the signs of the currents and voltages adjusted correspondingly. There are thus four possible types of MOS-FETs, as shown in Fig. 13.

The symbols used in Fig. 13 are now to be found in most American and European publications, though sometimes with slight variations; however they are not yet universally accepted. The arrow marks the substrate lead and indicates the direction of current-flow in the forward biased condition of the p-n junction. In MOS-FET symbols the gate lead is placed asymmetrically away from the source lead to aid distinguishing the drain from the source.

The symbols used for these devices should allow a distinction to be made between normally-on and normally-off types. The convention used here for this purpose, again of American origin, shows the thick line representing the channel as unbroken for normally-on types, and broken for normally-off types.

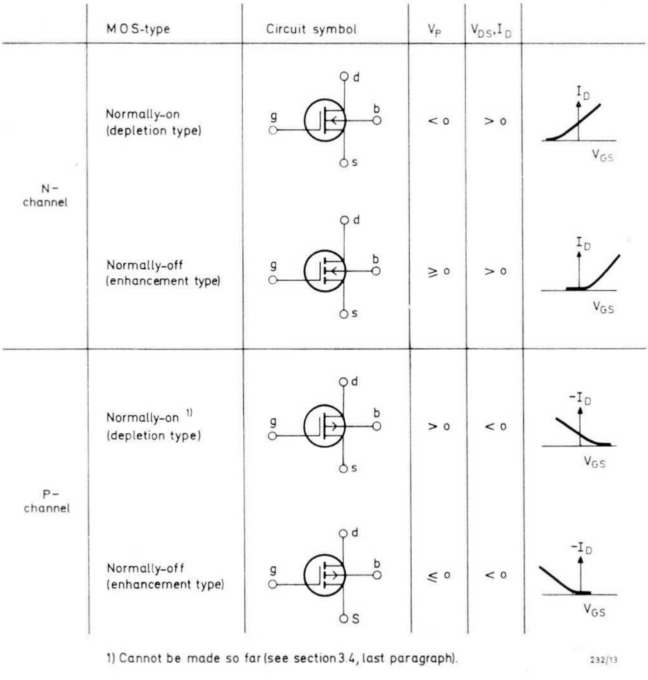


Fig.13 MOS field-effect transistors. The substrate terminal b (for "bulk") is generally connected to the source, the connection often being made internally.

3.4 The pinch-off voltage*

The pinch-off voltage V_P depends strongly on several factors which are: fixed charge in the oxide, the surface states at the silicon-silicon dioxide interface [4], and the substrate doping level. Proper control of the interface effects is essential if a reproducible pinch-off voltage is to be obtained sufficiently independent of temperature and age; this can only be achieved by using highly sophisticated technological processes.

*) *Other terms used for this quantity are the gate-source cut-off voltage V_{GSoff}, and especially for normally-off types, the threshold voltage V_T.*

As in the junction FET, the pinch-off voltage is the gate-source voltage at which the drain current becomes zero. V_P is thus to be found at the foot of the $I_D - V_{GS}$ characteristic. It is also the voltage at which the inversion layer starts forming in the channel region. There are three factors apart from the gate voltage which control this process (see Figs 14 and 15):

- the charges in the silicon-dioxide film, V_{ox};
- the charges of ionised impurity atoms in the depletion region, containing no mobile charge carriers, between the inversion layer and the neutral substrate $-V_{dc}$;
- traps in the oxide-silicon interface, which capture mobile charge carriers $-V_{trap}$.

These factors can be represented by equivalent gate-source voltages, denoted by V_{ox}, V_{dc} and V_{trap}. They give rise to a horizontal shift of the $I_D - V_{GS}$ characteristic, the foot of which would otherwise lie at $V_{GS} = 0$. To understand this, consider the normally-on n-channel MOS-FET shown in Fig. 14. Positive charges in the oxide layer can give rise to an n-type inversion channel in the p-type silicon, and hence to a current I_D; so the $I_D - V_{GS}$ characteristic is shifted to the left by a distance V_{ox}.

The voltage V_{dc} works in the opposite direction; this is the voltage required

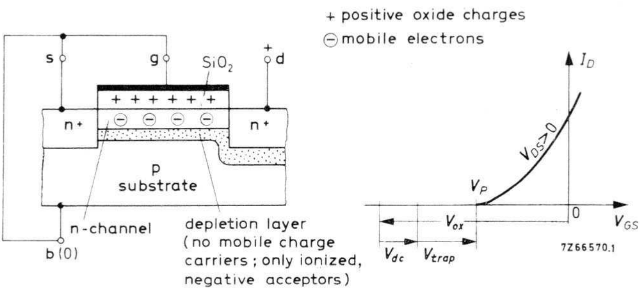


Fig.14 Elements of the pinch-off voltage V_P for a normally-on n-channel MOS-FET. A channel is already present at $V_{GS} = 0$. Normally-off n-channel types can be achieved by making V_{dc} high enough (high doping of the p-type substrate). The channel constriction at the drain end, caused by the drain current, is not shown here – drain current is assumed to be zero.

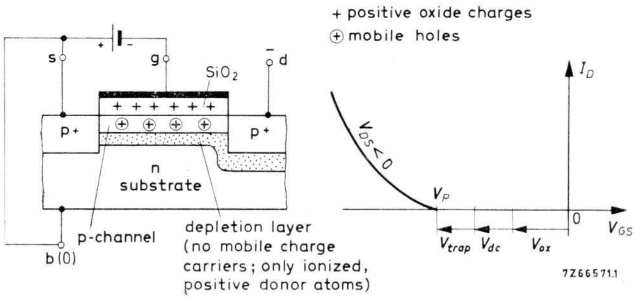


Fig.15 Elements of the pinch-off voltage V_P for a normally-off p-channel MOS-FET. A negative gate-source voltage is required for formation of the p-type inversion layer in the channel zone. The channel constriction at the drain end, caused by the drain current, is not shown here – drain current is assumed to be zero.

to invert the p-type silicon to n-type at the surface, in the absence of oxide film and traps. For this inversion, the holes originally present at the surface must be driven downwards away from it; the charges on the remaining fixed acceptor atoms will now appear as a negative space charge. To reach equilibrium they must be balanced by a positive charge of equal magnitude on the gate, so a positive voltage V_{dc} must be applied before drain current can flow. The $I_D - V_{GS}$ curve is thus shifted a distance V_{dc} to the right; the larger the acceptor space charge, the larger the shift. With a sufficiently high substrate doping level, a normally-off n-channel type will be achieved ($V_P > 0$); the transconductance falls with increased doping however [5].

Traps are crystal imperfections which can capture mobile charge carriers. Drain current can only start to flow when all traps are filled. With an n-channel type therefore, V_{trap} causes a shift of the characteristic to the right.

Consideration of the corresponding situation in a p-channel MOS-FET (Fig. 15) shows that when the oxide film is positively charged, all three factors V_{ox}, V_{dc} and V_{trap} act in the same direction, opposing drain current, and resulting in a normally-off p-type device. Since it is very difficult to make silicon-dioxide films with negative charges, p-channel MOS-FET are so far only found as normally-off (enhancement) types.

3.5 Characteristics

The $I_D - V_{DS}$ characteristics of MOS-FETs do not differ basically from those of the junction FET already considered. Typical families of MOS-FET characteristics are shown at Fig. 12. As with junction FETs, the drain current increases linearly with the drain-source voltage from $V_{DS} = 0$; the steepness of this increase is greater when the gate voltage is higher, since the inversion layer is then thicker and the channel resistance consequently lower. Because of the voltage drop along the channel due to the drain current, the channel becomes progressively thinner at the drain end as the drain current increases. The increase of I_D with V_{DS} thus becomes progressively slower, until a minimum channel cross-section is reached at the voltage $V_{DS(P)} = V_{GS} - V_P$ or at $V_{DG} = -V_P$. (See section 2.1.4, eq. 2). As with junction FETs, this effect is known as pinch-off.

In the pinch-off region, the drain current does not increase appreciably with V_{DS} at constant V_{GS}. Fig. 16 represents simply the conditions in the pinch-off region [6,7], showing a depletion layer between the drain diffusion area and the substrate. The part of the drain-source voltage above the value $V_{DS(P)}$ is dropped across this depletion layer, while the voltage drop across the channel stays roughly equal to $V_{DS(P)}$. The electrons reaching the left-hand edge of the depletion layer at the end of the channel are transported to the drain zone by the electric field in the depletion layer.

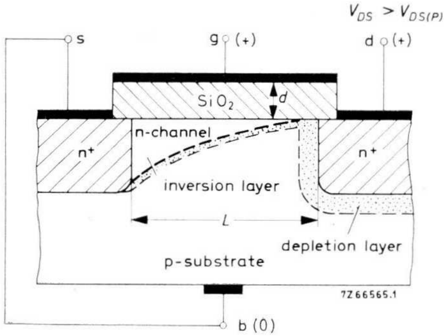


Fig.16 N-channel MOS-FET operating in the pinch-off region ($V_{DS} > V_{DS(P)}$).

Since the channel becomes somewhat shorter as the depletion layer grows, and the channel resistance consequently decreases slightly, the current in the pinch-off region will also increase a little. The smaller the relative change in channel length, the flatter will be the characteristic and hence the higher the output resistance of the transistor (see section 2.1.4, last paragraph).

With the aid of a number of simplifying assumptions,[3,4,5,6,7,14] the drain current in the pinch-off region can be written as:

$$I_D = \tfrac{1}{2}\beta\,(V_{GS} - V_P)^2, \tag{8}$$

where

$$\beta = \mu_S \cdot C_{ox} \cdot \frac{W}{L}, \tag{9}$$

μ_S = the surface mobility of the charge carriers in the channel;
$C_{ox} = \varepsilon \cdot \varepsilon_0/d$, the capacitance of the oxide layer per unit area (d = thickness of oxide layer, see Fig. 16);
W is the channel width (at right angles to the plane of the paper in Fig. 16);
L is the channel length, depending slightly on the drain-source voltage (Fig. 16).

The surface mobility μ_S is only about a quarter of the volume mobility μ_V, which determines the behaviour of the junction FET (eq. 1). As with the junction FET, the ratio W/L should be as large as possible, to ensure high transconductance.

The quadratic relation between the control voltage and the drain current (eq. 8) is an excellent approximation to the real behaviour of the MOS-FET over at least a 10 : 1 range of value of I_D. At high currents, errors arise because of the resistance of the conductors, while surface charges and the finite channel thickness begin to play a role at low currents.

For normally-on MOS-FETS, equation (8) is often written in the form:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2, \tag{10}$$

where $I_{DSS} = \tfrac{1}{2}\beta \cdot V_P^2$. (11)

I_{DSS} is the drain-source short-circuit current flowing at $V_{GS} = 0$ (see section 2.1.3).

3.6 The capacitance-voltage characteristic

The static and dynamic properties of the MOS-FET are largely determined by the "MOS capacitance" between the gate and the silicon. This capacitance depends on the gate-substrate voltage, and determination of the curve of this relationship, the MOS C-V curve, gives important information about the properties of the silicon/oxide interface; such information relates to conductivity of the silicon in the channel region, the surface charges, and traps.

A measurement based on the foregoing is often made on MOS-FETs to determine the gate-source short-circuit capacitance C_{gss} as a function of V_{GS}. This measurement, made with the source and drain connected, gives the capacitance-voltage characteristic shown at Fig. 17, the C-V curve.

At highly negative values of gate voltage V_G, excess holes are present in the silicon surface next to the oxide boundary, and C_{gss} is mainly determined by the oxide capacitance C_{ox}, that is by the dielectric constant and thickness of the oxide layer. As the gate voltage becomes less negative, a point is reached when the positive charge in the oxide is just balanced by the applied negative voltage and the hole concentration at the surface is equal to the bulk concentration. As the gate voltage increases further, a depletion layer with fewer holes is formed at the oxide surface, see Fig. 14; this acts like a capacitor C_{dc} in

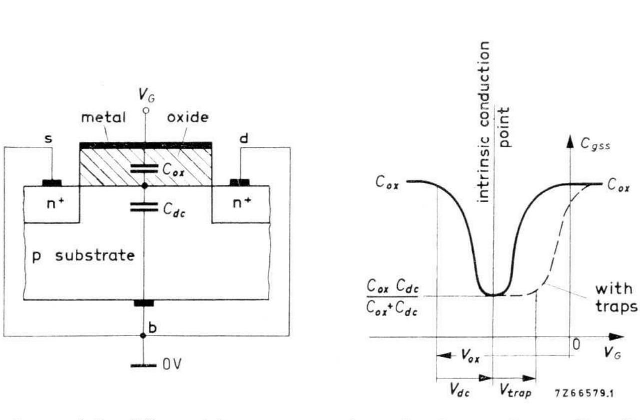


Fig.17 Dependence of the differential gate-source short-circuit capacitance C_{gss} (i.e. the capacitance for small signals) on the gate voltage for a normally-on n-channel MOS-FET.

series with C_{ox}. The resulting value of C_{gss} continues to decrease until a value of V_G is reached at which an n-type inversion channel starts forming at the surface of the silicon.

This n-channel connects the source and drain zones; that is, the capacitance C_{dc} now has a conducting channel shunted across it. As the gate voltage increases further, this shunt resistance progressively decreases, so that the resultant capacitance C_{gss} increases again to the value C_{ox}, because C_{dc} will be finally short-circuited.

If traps are present, they will delay the formation of the n-channel, because all the traps have to be filled firstly by electrons. The C_{gss} can rise again, as shown by the broken line in Fig. 17. At the point where the broken line starts to rise, the gate voltage is equal to the pinch-off voltage V_P. In determining the C-V curve of Fig. 17 it has been taken into account that the positive charges in the oxide film start to cause channel formation even at a negative gate voltage (see Fig. 14).

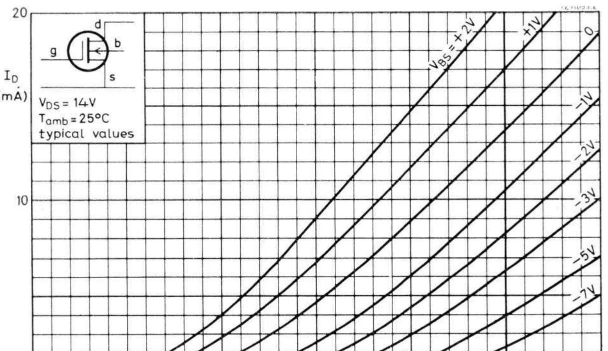


Fig.18 Influence of the source-substrate voltage V_{BS} on the control characteristic of a MOS field-effect transistor (n-channel MOS-FET BFR29 is used as an example).

3.7 The substrate as a control electrode

The drain current can also be controlled via the substrate lead *b*, if it is available separately. Fig. 18 shows the $I_D - V_{GS}$ characteristics for the normally-on n-channel MOS-FET BFR29. This device has two control electrodes, the gate and the substrate, which can be used to multiply two signals for instance, in mixer stages, analog applications etc.

However it must be remembered that when the substrate is used as a control electrode it acts as a junction gate. The substrate and the channel are separated by a depletion layer, Fig. 14. This results in the input resistance between the substrate and the source being lower than that between the insulated gate and the source.

3.8 Structure of MOS field-effect transistors

3.8.1 Overlap of the gate electrode

In normally-off types, the gate electrode must overlap the source and drain zones, since otherwise there will be regions at drain and source end of the channel where it is not possible to induce an inversion layer. The overlap leads to relatively high parasitic capacitances if the oxide film underneath the overlapping parts of the gate is not made much thicker than that above the channel. A method of constructing an overlap without high parasitic capacitances is described in the next section.

3.8.2 Structure of a depletion type MOS-FET

Positive charges in the oxide layer of a depletion MOS-FET create a conductive channel even at zero gate-source voltage. To prevent the occurrance of parasitic channels in parallel with the desired channel, it is necessary to make a closed structure, as for instance by surrounding the drain area completely by the gate area (see Plate *C*).

The device capacitances, and particularly the feedback capacitance, must be as low as possible in order to ensure optimal performance as a high frequency amplifier or as a chopper. The gate capacitance is determined physically by the area of gate metallisation and the thickness of gate oxide. High transconductance or low on-resistance require the oxide above the channel to be as thin

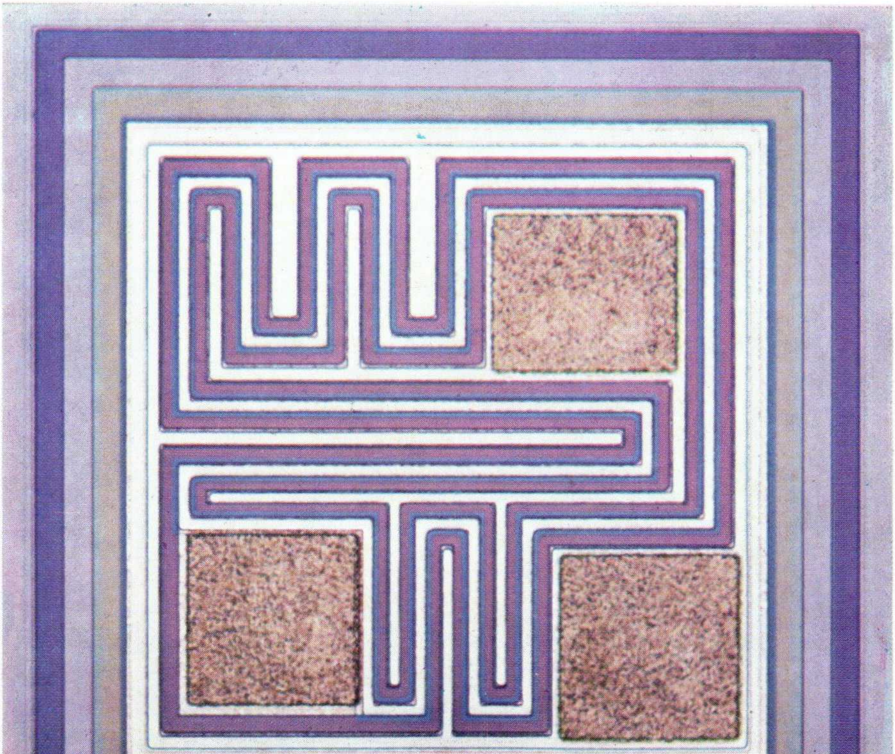


Plate C. Closed structure (drain surrounded by gate) of a depletion MOS-FET (BSV81).

as possible, typically 0.2 μm. In early MOS-FETS this thin oxide was also present above the source and drain regions next to the channel. Due to tolerances in the mask alignment it often happens that part of the gate metallisation extends above the source or drain areas, thus giving rise to quite high and varying input or feedback capacitances. In modern MOS-FETS like the one shown in Plate *C*, this problem has been overcome by means of a special diffusion technique that enables formation of a much thicker oxide layer under the overlapping parts of the gate electrode (see Fig. 19).

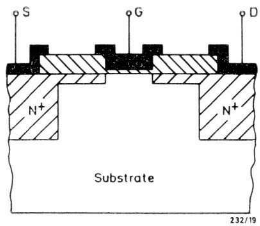


Fig.19 Cross-section through MOS-FET with one gate (see also Plate C).

The thin extensions of the source and drain diffusion areas are diffused from a thick doped oxide layer in which a small window has been etched in advance. A thin oxide layer (0.2 μm) is later grown in this window, forming the proper gate oxide, and matching perfectly with the proper channel. Tolerances due to the alignment of the gate metallisation mask in this case are far less critical.

3.8.3 MOS-FET WITH TWO GATES (MOS-FET TETRODE)

For v.h.f. and u.h.f. applications the feedback capacitance of a normal triode MOS-FET is too high (abt 0.5 pF). Much lower values (abt 0.02 pF) can be obtained by adding a second gate electrode, which can then also be used for automatic gain control. The structure of such a MOS-FET is shown in Fig. 20*a*.
When gate g_2 is earthed for high frequencies, feedback between the drain and gate g_1 is made extremely low because of the screening effect of gate g_2. The output conductance of the tetrode configuration is also very low, since the drain load resistance of the lower MOS-FET equals the transconductance of the

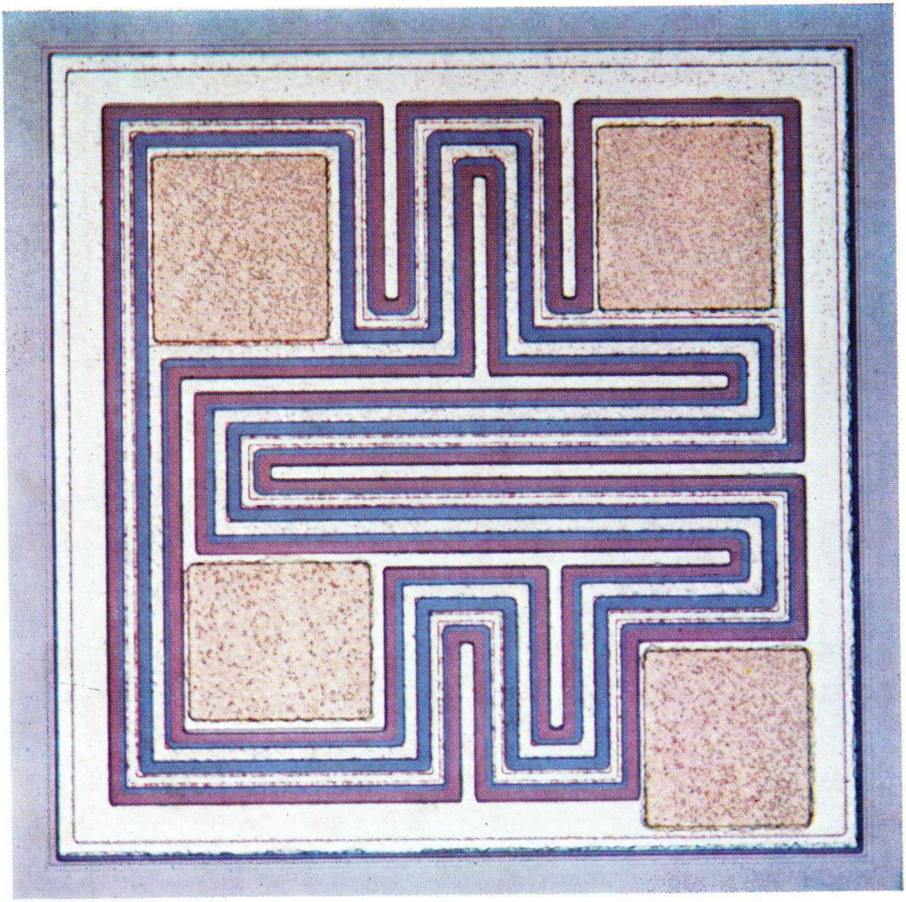
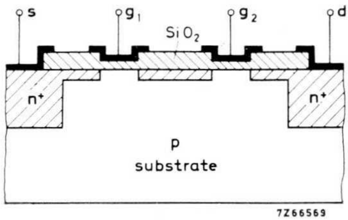
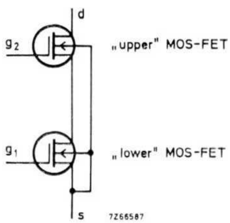


Plate D. Construction of a MOS-FET tetrode (BFS28). (See Fig. 20).

upper MOS-FET in Fig. 20*b*. Thus modulation of the drain-source voltage of the lower MOS-FET is relatively small.



a



b

Fig.20 (a) Cross-section through MOS field-effect transistor with two gates (MOS-FET tetrode, see Plate D). (b) Circuit diagram of the MOS-FET shown in Fig. 20a.

The MOS-FET tetrode shown in Plate *D* is the BFS28 and has the following data at $I_D = 10$ mA:

Transfer admittance at f = 1 kHz: typically 13 mΩ^{-1}
Feedback capacitance, C_{DG}: typically 25 fF
Output conductance at $f = 1$ kHz: typically 20 $\mu\Omega^{-1}$

For further details see our Data Handbook.

The MOS-FET tetrode has low h.f. noise, low cross-modulation and low intermodulation properties. An example of a circuit making use of a MOS-FET tetrode is given in Section 5.4.4.

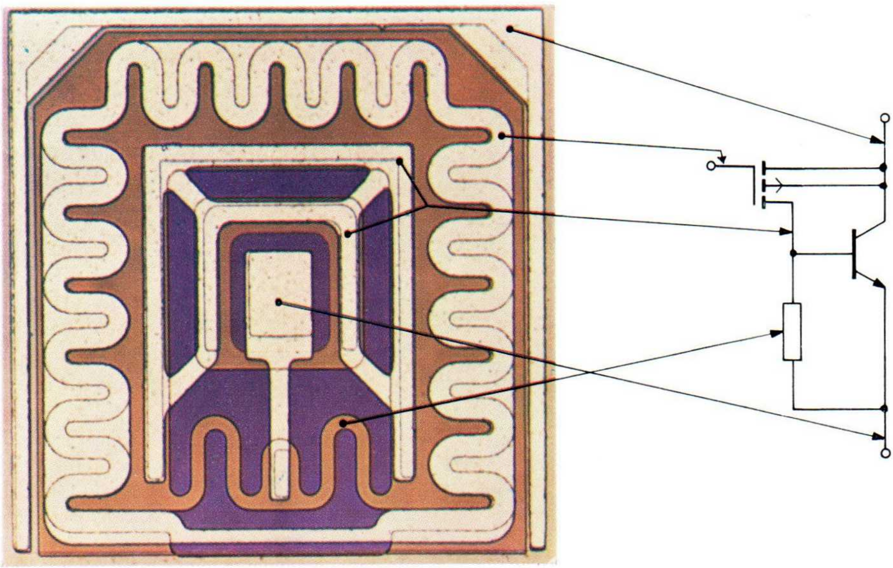


Plate E. Construction of the integrated circuit TAA320 comprising a p-channel enhancement MOS-FET, a bipolar transistor and a resistor.

3.8.4 An integrated circuit incorporating a MOS-FET and a bipolar transistor

A circuit with interesting properties is obtained if a MOS-FET is combined with a bipolar transistor as shown in Plate *E* (see section 5.4.3). The voltage across the resistor in the drain biases the bipolar transistor. The three components are integrated; Fig. 21 shows a schematic cross-section through the crystal.

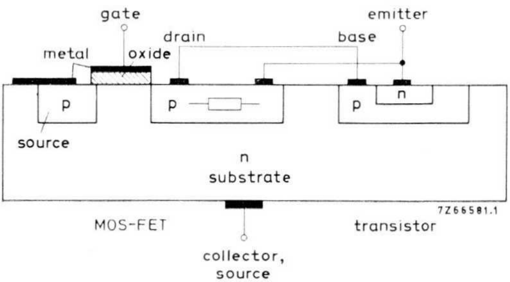


Fig.21 Schematic section through crystal of the integrated amplifier circuit TAA320 (See Plate E).

4 Electrical properties

4.1 D.C. characteristics

Two most important d.c. characteristics of field-effect transistors have already been discussed; they are the pinch-off voltage V_P and the drain-source short-circuit current I_{DSS}. The d.c. behaviour of a field-effect transistor can be described with their aid, as in the form of equation 10. Figs 22 and 23 give circuits which can be used for measurement of V_P and I_{DSS}.

Like the d.c. characteristics of bipolar transistors, V_P and I_{DSS} have a relatively large spread and are temperature dependent. This should be borne in mind when designing the adjustment of the operating point for these devices; it is dealt with in more detail in section 5.1.

Fig.22 Measurement of the pinch-off voltage V_P. The value of 1 µA given for I_D is an example only. V_P is often measured at lower drain currents.

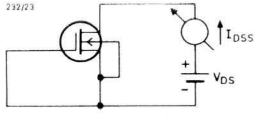


Fig.23 Measurement of the drain-source short-circuit current I_{DSS}.

4.1.1. Influence of temperature

Variation of drain current with temperature, but at constant V_{GS} and V_{DS}, is caused by two opposite effects. Firstly the mobility of charge carriers in the channel decreases with temperature; this effect on its own would cause a reduction in drain current (equations (1) and (3)).

Secondly the pinch-off voltage increases with temperature; this effect on its own would cause an increase in drain current (eq. (3)). The relative effects can be adjusted.

Fig. 24 shows typical dependence of the transfer characteristic on temperature. At the operating point Z the two temperature effects cancel each other and the drain current becomes temperature-independent [8]. This is valid for both junction and MOS field-effect transistors.

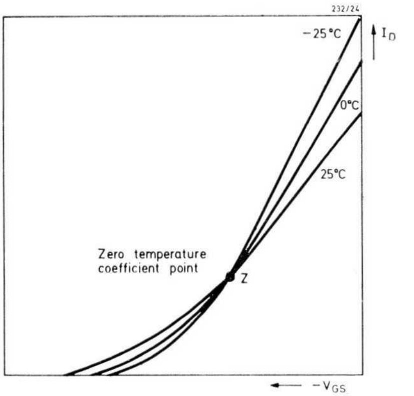


Fig.24 Temperature dependence of the $I_D - V_{GS}$ characteristic of an n-channel field-effect transistor. The compensation point Z is subject to manufacturing spread of the pinch-off voltage.

In Fig. 25*a* and *b* the drain current of junction field-effect transistors BFW12 and BFW13 is plotted as a function of temperature. It will be noted that at higher drain currents than that at point Z the temperature effect of mobility predominates; at lower currents the effect of pinch-off voltage predominates. This represents a basic difference between field-effect and bipolar transistors, the collector current of the latter always increasing with temperature. Consequently field-effect transistors do not exhibit thermal instability (run-away).

The temperature dependence of drain current in any FET can be represented by an equivalent voltage source E_{dr} and an equivalent current source I_{dr} at the input of a temperature-independent active element (see Fig. 26).

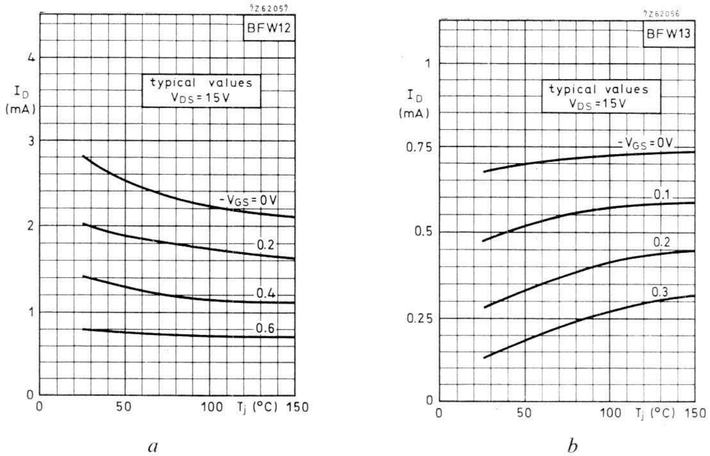


Fig.25 Temperature dependence of the drain current of two n-channel junction field-effect transistors. (a) In this case point Z in Fig. 24 is at a negative V_{GS} value, with predomination of temperature dependence of charge carrier mobility. (b) In this case point Z can be imagined as a positive V_{GS} value, with predomination of temperature dependence of V_P.

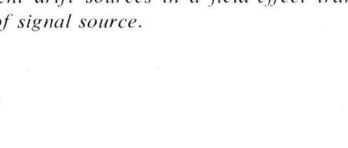


Fig.26 Temperature-dependent drift sources in a field-effect transistor. V_{dr} voltage drift; I_{dr} current drift; R_g resistance of signal source.

4.1.1(*a*) JUNCTION FIELD-EFFECT TRANSISTORS

The temperature dependence of the equivalent voltage and current sources for an n-channel junction field-effect transistor is given by:

$$\frac{\mathrm{d}E_{dr}}{\mathrm{d}T} = \left\{\frac{I_D}{g_{fs}} \cdot \frac{1}{\mu_V} \cdot \frac{\mathrm{d}\mu_V}{\mathrm{d}T}\right\} - \frac{\mathrm{d}V_P}{\mathrm{d}T} \quad \text{and} \tag{12}$$

$$\frac{\mathrm{d}I_{dr}}{\mathrm{d}T} \approx 0.15\, I_{GS} \text{ at } 300\text{ K}\,^*; \tag{13}$$

where

μ_V = volume mobility at the operating temperature in question;

$$\frac{1}{\mu_V} \cdot \frac{\mathrm{d}\mu_V}{\mathrm{d}T} \approx -6.10^{-3}/\text{degC at } T = 300\text{ K};$$

$$\frac{\mathrm{d}V_P}{\mathrm{d}T} \approx -2.2\text{ mV/degC at } 300\text{ K}\,^{**};$$

I_{GS} = gate-source current at the operating temperature in question ($I_{GS} < 0$).

It follows from eq. (12) that the voltage drift is zero at a certain value of drain current; such compensation is not possible with bipolar transistors. Point Z in Fig. 24 can be found by making $\mathrm{d}E_{dr}/\mathrm{d}T$ in eq. (12) equal to zero. The coordinate $V_{GS(Z)}$ of point Z can be calculated from eq. (4) which gives:

$$\frac{I_D}{g_{fs}} = \frac{1}{n}(V_{GS(Z)} - V_P) \tag{14}$$

Combining eqs (12) and (14) and substituting the values given for $(1/\mu_V)\cdot(\mathrm{d}\mu_V/\mathrm{d}T)$ and n (≈ 2),

$$V_{GS(Z)} - V_P \approx 0.73\text{ V at } 300\text{ K}. \tag{15}$$

This implies that any junction-FET biased at 0.73 V from V_P is biased at its zero temperature coefficient point. However, because of the relatively large

*) *This means that the gate leakage current doubles with a temperature rise of 7 degC.*

**) *The thermal drift of V_P equals the thermal drift of diffusion voltage V_{diff} of the gate-channel junction.*

manufacturing spread of pinch-off voltage, it is difficult to apply drift compensation in mass-produced equipment.

In cases where the device is not biased at $V_{GS(Z)}$, it may be useful to be able to predict the drift of V_{GS} for any drain current. From the previous equations it can be derived that drift referred to the input equals $2.2\,(1 - \sqrt{I_D/I_{D(Z)}})$ mV/degC. If the pinch-off voltage is 0.73 V, then from eq. (15) the compensation point is to be found at $V_{GS} = 0$ or at $I_D = I_{DSS}$.

4.1.1(*b*) MOS FIELD-EFFECT TRANSISTORS

The temperature dependence of the equivalent voltage (E_{dr}) and current (I_{dr}) sources of a MOS-FET is similar to that of a junction-FET. There are again two opposing effects: variation of mobility with temperature, reducing the drain current, and variation of pinch-off voltage with temperature, raising the drain current.

The contribution of mobility to the voltage drift of the MOS-FET is the same as for the junction-FET, that is the first term of equation (12). It is again proportional to the voltage $|V_{GS} - V_P|$; thus this part of the voltage drift can be varied by changing the gate-source voltage, and the operating point can be chosen so that the total voltage drift is reduced to zero in the region of a specific operating point[9]. The temperature coefficient of surface mobility has been found by measurement on various types of MOS-FET to be about -5.2×10^{-3}/degC. The temperature coefficients of surface mobility of MOS-FETs and of volume mobility of junction-FETs are thus similar.

The second term in equation (12), the thermal drift of V_P, is not determined exclusively by that of the diffusion voltage, as in the case of the junction-FET. The pinch-off voltage of a MOS-FET consists of the components V_{ox}, V_{dc} and V_{trap} (see Figs 14 and 15). The charges in the oxide film do not depend on the temperature, so V_{ox} does not cause any thermal drift. It follows that the thermal drift of V_P of a MOS-FET is determined therefore by the two remaining components, viz.:

(i) The temperature dependence of V_{dc} (Figs 14 and 15), which is given by $\partial V_{diff}/\partial T$ (equation 12), as with the junction-FET; in the case of the MOS-FET this quantity can vary from 1 mV/degC to 8 mV/degC, depending on doping level.

(ii) The temperature dependence of V_{trap}. Both V_{dc} and V_{trap} lead to an increase in drain current with a rise in temperature. The drift of V_{trap} can be kept below 5 mV/degC for MOS-FETS, compared with 2.2 mV/degC for junction-FETS.

It is difficult to make use of the zero voltage drift point of MOS-FETS in circuit design, because they have a relatively high gate voltage drift with time. They have a high l.f. noise (see section 4.4), and are also sensitive to high voltages at the gate (see section 4.1.4).

Theoretically the MOS-FET also has a current drift, determined like that of the junction-FET by the temperature dependence of the gate leakage current. However this current is so small (10^{-14} A), that it can be neglected.

4.1.2 THE GATE-LEAKAGE CURRENT

The best-known feature of FETS is their high input impedance in common source and in source-follower configurations as a result of the low gate leakage current at room temperature, usually of a few pico-amperes.

The leakage current figures quoted in specifications are usually those for I_{GSS}, the reverse current of the diode formed between the gate and the shorted drain/source, see Fig. 27. I_{GSS} changes sharply with temperature, as shown in Fig. 28.

Of much more importance to the user is the gate leakage current I_G under more usual operating conditions, that is with a current I_D flowing through, and a voltage V_{DS} across the FET. In practice this I_G will not substantially differ from I_{GSS}, provided the user is aware of certain phenomena and has therefore chosen the operating conditions wisely. These phenomena show up as a strong dependence of I_G on drain current I_D and on drain to source voltage V_{DS} if this voltage exceeds a few times the pinch-off voltage V_P (see Fig. 29).

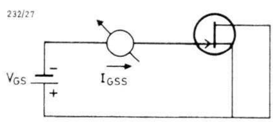


Fig.27 Circuit for measurement of the gate-source short-circuit leakage current I_{GSS}.

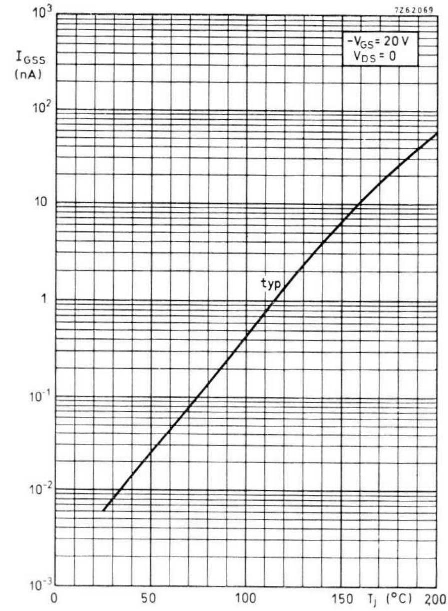


Fig.28 I_{GSS} as a function of temperature for the junction FETs BFW10/11.

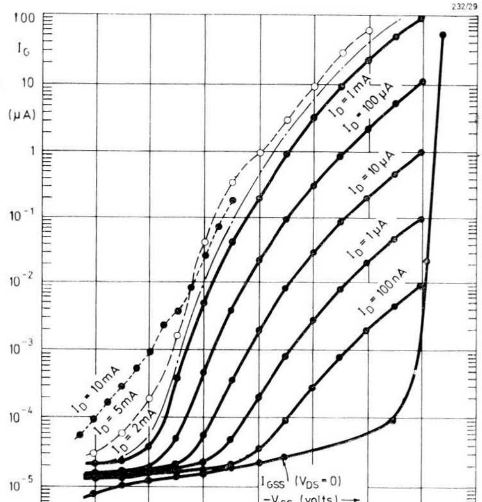


Fig.29 Typcial I_G vs. V_{DS} with I_D as a parameter, for BSV80 with $V_P = 2.5$ V. I_{GSS} is shown for comparison.

This effect has been explained in terms of impact-ionisation in the narrow end of the channel, when the electric field becomes so strong that it exceeds the critical field strength where the drift velocity of the electrons saturates.[10,11,12]. Due to these high fields, the impact-ionisation probability increases, and although the multiplication factor M is still very low, the resulting "excess" gate current becomes orders of magnitude higher than the low voltage leakage current. This "excess" gate current is proportional to the drain current because the volume of the high field zone in the channel is proportional to the drain current.

Thus the "excess" gate current is of importance when the FET is biased at high voltage and high current (see Fig. 30). The "excess" gate current increases only slightly with temperature, in contrast to the low voltage gate current, which increases exponentially (see Fig. 31).

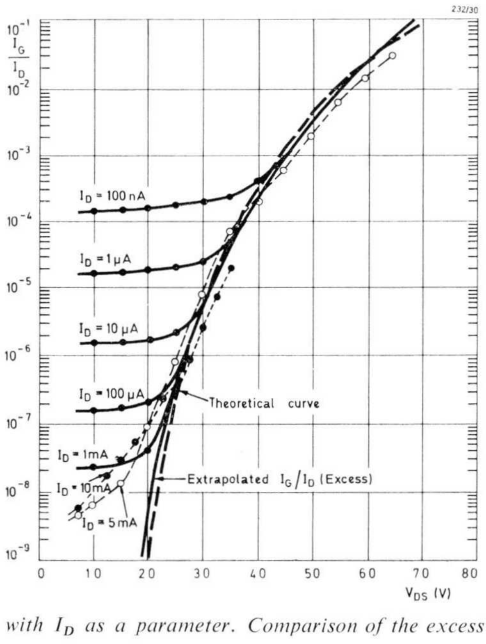


Fig.30 I_G/I_D vs. V_{DS} with I_D as a parameter. Comparison of the excess gate current with the theoretical curve.

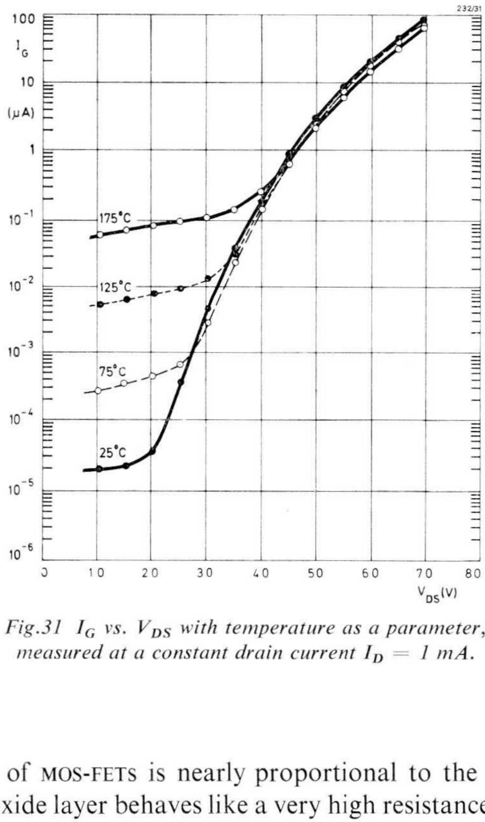


Fig.31 I_G vs. V_{DS} with temperature as a parameter, measured at a constant drain current $I_D = 1$ mA.

The gate current of MOS-FETs is nearly proportional to the drain-source voltage, because the oxide layer behaves like a very high resistance. The temperature coefficient is also much smaller than that of junction-FETs.

The substrate leakage current of MOS-FETs however has the same temperature and voltage-dependent behaviour as described for junction-FETs.[13].

4.1.3 Breakdown voltages

In junction field-effect transistors the maximum permissible voltages are determined by avalanche breakdown of the p-n junctions between gate and channel. In general, breakdown will start at the drain end of the channel, because this is where the highest reverse voltages across the p-n junction are found under normal operating conditions (see Fig. 6). It is seen from Fig. 7 that the breakdown voltage between drain and source is highest when $V_{GS} = 0$. As the reverse gate voltage increases ($V_{GS} < 0$), the breakdown voltage drops, since the total voltage across the p-n junction is the sum of the voltages V_{DS} and $-V_{GS}$. It follows that the drain-source breakdown voltage will decrease by the same amount as the gate-source reverse voltage is increased (in Fig. 7 by 1 V from one characteristic to the next), hence

$$V_{(BR)DSX} = V_{(BR)DSS} + V_{GS}, \tag{16}$$

where

$V_{(BR)DSX}$ is the breakdown voltage between drain and source with a given gate-source voltage;
$V_{(BR)DSS}$ is the breakdown voltage between the drain and the source when gate and source are short-circuited ($V_{GS} = 0$).

There is quite a high risk that the permissible dissipation in the transistor will be exceeded during measurement of the breakdown voltage $V_{(BR)DSS}$, since this measurement is carried out at a relatively high current. This risk can be avoided by measuring the drain-gate breakdown voltage $V_{(BR)DGO}$ with the source open-circuited, which closely corresponds with the voltage $V_{(BR)DSS}$. The current flowing in this case is only the very small leakage current I_{GDO}, and the dissipation is negligible. The principle of measurement of $V_{(BR)DGO}$ is shown in Fig. 32.

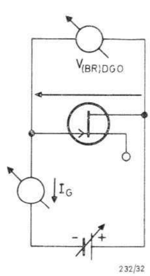


Fig.32 Measurement of the drain-to-gate breakdown voltage $V_{(BR)DGO}$.

In MOS-FETs the breakdown voltages between the gate and other electrodes depend on the thickness and purity of the oxide film. The breakdown phenomenon here is irreversible, because a short-circuit will be formed.

The maximum permissible drain-source voltage of the MOS-FET is determined by the breakdown voltage of the drain to substrate junction (see Fig. 16), when the substrate and source are short-circuited, which is generally the case. Experiments have shown that gate metallisation decreases the drain-source breakdown voltage.

4.1.4 Safety measures to be taken with MOS-FETs

Static charges on the gate electrode can give such high field strengths in the extremely thin oxide film as to lead to breakdown and destruction of the MOS-FET.

To safeguard the gates against damage due to accumulation of static charge during transport or handling, the leads are encircled by a ring of conductive rubber, which should be removed just after the transistor is soldered into the circuit. After having been soldered into the circuit, the resistances between the gate and the other terminals are generally low enough to allow undesirable static charges to leak away. If this is not the case, a protective circuit must be provided at the MOS-FET input, for example back to back voltage reference diodes. By using suitable feedback circuitry it can be ensured that this safety circuit does not affect the high d.c. input resistance (about 10^{14} ohms) which can be attained with MOS-FETS.

4.2 The small signal equivalent circuit

A small signal equivalent circuit is useful if the desired accuracy is not in conflict with the desired simplicity. This means that a small signal equivalent circuit is only valid in a restricted frequency range. Fig. 33 shows an equivalent circuit that is valid for junction FETS and MOS-FETS.

This equivalent circuit can be used up to two or three times the frequency determined by the input time constant $\tau_i = C_{gs'}/g_m$. At higher frequencies one has to take into account not only the series inductance of the electrode leads but also the series resistance in the drain and the phase shift of the mutual conductance g_m.

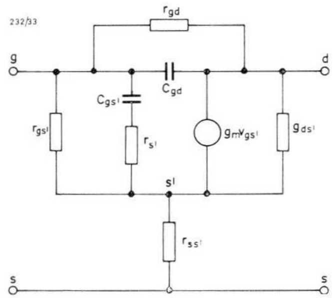


Fig.33 Small signal equivalent circuit for a FET.

The conducting channel can be considered as a transmission line with distributed capacitive and resistive elements. The equivalent circuit at Fig. 33 is composed of several components as follows:

a. The gate-to-source resistance $r_{gs'}$.
   At room temperature this resistance is about 10^{11} ohms for junction-FETS and about 10^{14} ohms for MOS-FETS. The higher the gate-leakage current, the smaller is this resistance.
b. The gate-to-drain resistance r_{gd}.
   The value of this resistance is similar to that of $r_{gs'}$. However in junction FETS, r_{gd} decreases above a certain drain-to-source voltage (see section 4.1.2).
c. The gate-to-source capacitance $C_{gs'}$.
   This capacitance represents the gate-to-channel capacitance formed by the depletion region in the channel, between pinch-off point and source, and is voltage dependent.
d. The loss resistance $r_{s'}$.
   This resistance represents a part of the channel resistance. An a.c. current which flows into the gate via the gate-channel capacitance also flows through the source-end of the conducting part of the channel. It has been found that a good approximation is given by:

$$\text{for junction-FETS} \quad r_{s'} = \frac{1}{3\,g_m}, \quad \text{for MOS-FETS} \quad r_{s'} = \frac{1}{5\,g_m}.$$

e. The gate-to-drain capacitance C_{gd}.
This capacitance is another part of the gate-to-channel capacitance, formed by the depletion region between pinch-off point and the drain-end, and is thus voltage dependent.
f. The mutual conductance g_m (see section 2.1.4) is determined by the impurity density in the channel, and its geometry.
The mutual conductance changes with current according to equation (5).
g. The drain-to-source conductance $g_{ds'}$ ($\approx g_{os}$ in common source configuration as used in section 2.1.4).
This conductance increases with current and decreases with drain-to-source voltage. The ratio of drain-to-source conductance to mutual conductance is smallest for FET types having the highest channel length (L); this ratio varies in general between 10^{-2} and 10^{-3} for junction-FETs and between 10^{-1} and 10^{-2} for MOS-FETs.
h. The source series resistance $r_{ss'}$.
This is a material resistance between the intrinsic source and the source contact.
It is about 10 to 20 ohms in practice.

The y-parameters and other four-pole parameters can be derived from the small signal equivalent circuit (see section 5.2).

4.3 Distortion

Distortion is caused by non-linearity of the transfer characteristic:

$$I_D = I_{DSS}(1 - V_{GS}/V_P)^n. \tag{17}$$

If $n = 2$, equation (17) contains only first and second order terms. However, since n is not exactly 2, FETs will produce also third and higher order terms. Making $n = 2$ would require all impurities to be concentrated in the middle of the channel (a spike profile [21]). In actual FETs the impurities are distributed over the whole channel height. Distortion decreases as $|1 - V_{GS}/V_P|$ increases, so the higher the d.c. drain current, the lower will be the distortion.

An important difference between FETs and bipolar transistors is the contribution of third harmonic distortion, which is much lower for FETs than for bipolars; this means that FETs exhibit relatively favourable intermodulation and cross-modulation figures.

4.4 Noise

The noise behaviour of FETs differs appreciably from that of bipolar transistors in that:

- the minimum noise figure is smaller at all frequencies;
- the optimum noise admittance for minimum noise figure is lower.

Four types of noise are to be found in FETs:

- thermal noise in the conducting channel;
- shot noise from the gate leakage current;
- l.f. noise ($1/f$ noise);
- shot noise from the substrate leakage current, in MOS-FETs only.

Noise behaviour in fourpoles is usually defined in the form of an equivalent voltage source E_n and an equivalent current source I_n at the input terminals of a noise-free device. The mean square values of E_n and I_n are:

$$e_n^2 = \overline{|E_n|^2} \approx 4\,kT\Delta f/g_m + \overline{|E_{lf}|^2}, \tag{18}$$

$$i_n^2 = \overline{|I_n|^2} \approx 4\,kT\Delta f\,g_m\,\omega^2\,\tau_i^2 + 2\,qI_G\Delta f, \tag{19}$$

$$\overline{Re\,E_n^*\,I_n} \approx 4\,kT\Delta f\,(0.5\,\omega\tau_i)^2, \tag{20}$$

$$\overline{Im\,E_n^*\,I_n} \approx 4\,kT\Delta f\,(0.85\,\omega\tau_i), \tag{21}$$

where

- the terms containing the factor $4\,kT$ are of thermal origin,
- the term $\overline{|E_{lf}|^2}$ represents the l.f. noise (see e_n in Fig. 34),
- the term $2\,qI_G\Delta f$ represents the shot noise (see i_n in Fig. 35), with I_G being the gate leakage current including excess gate current at high drain-source voltages (see section 4.1.2).

Equations (18) to (21) are valid for junction-FETs up to frequencies for which $\omega\tau_i < 1$, where $\tau_i = C_{gs}/g_m$; they are also valid for MOS-FETs with the restriction that all $4\,kT$ terms have to be multiplied by a factor of from 1 to 4, depending on the substrate doping.

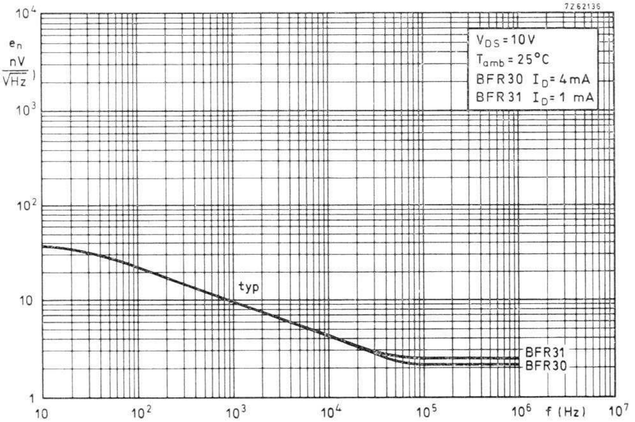


Fig.34 Equivalent noise voltage of a junction-FET as a function of frequency.

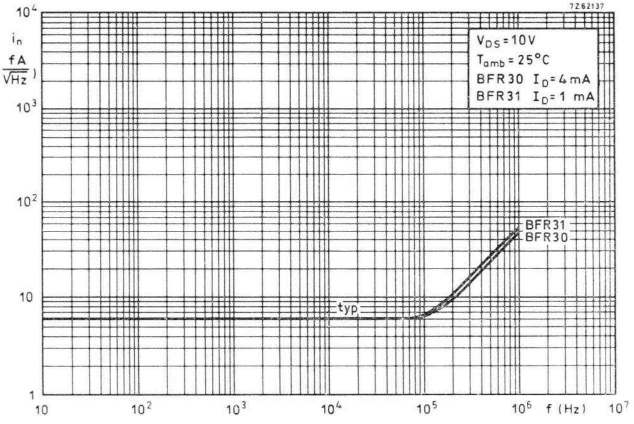


Fig.35 Equivalent noise current vs. frequency of a junction-FET.

The term $\overline{|E_{lf}|^2}$ is much higher for MOS-FETs than for junction-FETs (about 10^5 times). For MOS-FETs the shot noise term in equation (19) can be neglected in the majority of applications. Equations (18) to (21) lead to the conclusion that:

$$F_{min} \approx 1 + 1.1\ \omega\tau_i + 0.5\ \omega^2\tau_i^2 + \Delta F, \tag{22}$$

and

$$g_{s\ opt.} = 0.55\ \omega C_{gs} + g_{soo}, \tag{23a}$$

$$b_{s\ opt.} = -0.7\ \omega C_{gs}, \tag{23b}$$

$$\Delta F \text{ in equation (22)} = \frac{\overline{|E_{lf}|}}{2\ kT} \cdot \sqrt{\frac{2q \cdot I_G}{\Delta f}},$$

and

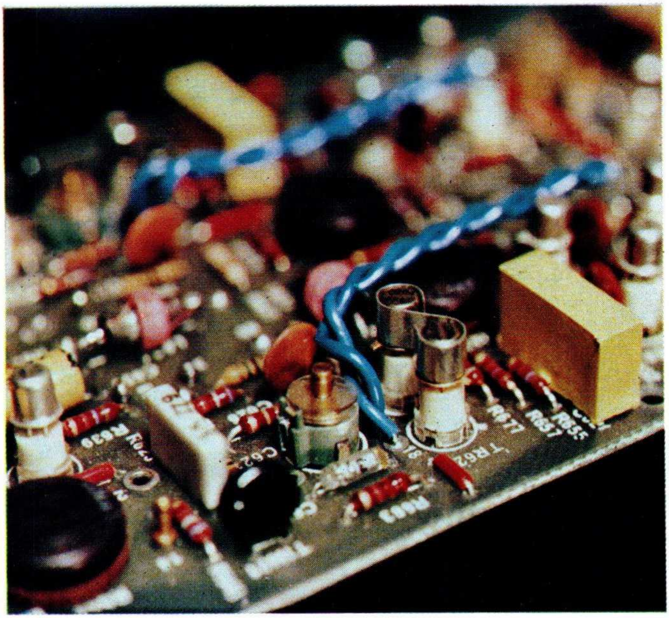
$$g_{soo} \text{ in equation } (23a) = \frac{1}{\overline{|E_{lf}|}} \cdot \sqrt{(2q \cdot I_G \cdot \Delta f)}.$$

The terms ΔF and g_{soo} are of importance when calculating noise at audio frequencies. For junction-FETs the value of ΔF at 100 kHz is about equal to the sum of the other frequency dependent terms in equation (22).

4.5 D.C. stability

The operating point of a field-effect transistor will change with time, even at constant temperature; this instability occurs particularly with MOS-FETs, and is due to charge displacements in the oxide film, and to charging and discharging of traps at the oxide/semi-conductor interface. These processes can have time constants of up to several weeks.[14]

The disturbance in the charge equilibrium leads to a horizontal shift of the transfer characteristic (Figs 14 and 15). For example, if a large positive voltage is applied to the gate of an n-channel MOS-FET for a long time (say half an hour) the $I_D - V_{GS}$ characteristic will be found to be shifted to the left after the voltage is removed. In this way a normally-off MOS-FET can temporarily become a normally-on MOS-FET. The shift of the transfer characteristic will be greater as the voltage applied to the gate is higher; it also increases with temperature and with the duration of the period for which the gate voltage is applied. After some time, however, the characteristic will no longer shift. By means of special treatment of the silicon-dioxide film, such as incorporation of phosphorus, it has proved possible to appreciably reduce the long-term drift. For example, the equivalent gate-source voltage drift $\Delta V_{GS}/\Delta t$ of modern field-effect transistors at constant temperature after one hour of operation, amounts to about 5 mV/h for a MOS-FET and 5 µV/h for a junction-FET. Using the differential amplifier principle, the equivalent differential long-term voltage drift will again be reduced by a factor of about 10.



Detail of the input stage of an oscilloscope showing a specially selected matched pair of n-channel FETs (similar to the BFS21/21A family) which are thermally coupled by means of a metal S-clip. (Photograph by courtesy of Telequipment Ltd, England).

5 Circuits with field-effect transistors

5.1 The operating point

The operating point of a field-effect transistor in an amplifier is determined by the quiescent drain-source voltage V_{DS} and the quiescent drain current I_D (see Fig. 36).

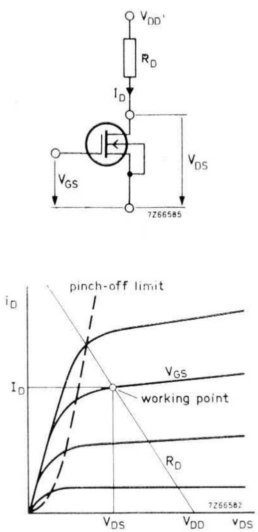


Fig.36 Fixing the operating point of junction and MOS field-effect transistors.

It is not generally a good idea to fix the quiescent voltage V_{GS}, as the quiescent drain current will then be subject to a relatively large spread in the $I_D - V_{GS}$ characteristic. The corresponding spread of the operating point and the subsequent decrease of the dynamic range become more marked with larger values of drain resistance R_D. However a high value of R_D is often desirable to obtain high voltage amplification; consequently the spread of I_D should be as low as possible.

Apart from the manufacturing spread, the influence of temperature and of supply voltage on the operating point should also be taken into account.

In the simplest case, the operating point can be set with the aid of a separate supply source V_{GG}, as shown in Fig. 37. The gate leakage current which flows through R_G (= 100 MΩ) increases exponentially with temperature. If this would result in an increase of the gate leakage current to 10 nA, it would lead to a change of 10 nA $\times$ 100 MΩ = 1 V in the gate voltage, the direction of change being such as to make the drain current increase.

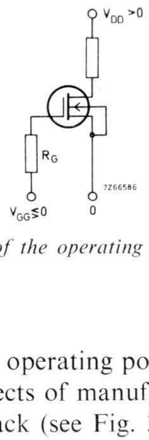


Fig.37 Simple circuit for adjustment of the operating point of junction and MOS field-effect transistors.

As with bipolar transistors, the operating point of field-effect transistors can also be stabilised against the effects of manufacturing spread and temperature changes by means of d.c. feedback (see Fig. 38).

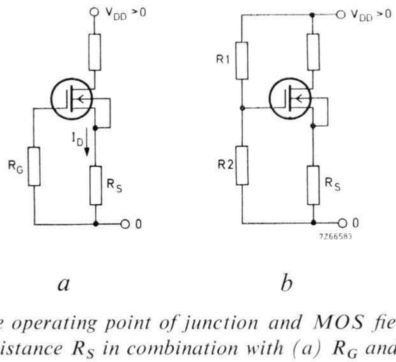


Fig.38 Stabilisation of the operating point of junction and MOS field-effect transistor by d.c. feedback with a source resistance R_S in combination with (a) R_G and (b) R_1/R_2.

The feedback is obtained by means of the source resistance R_S. A.C. feedback can be prevented by shunting R_S with a decoupling capacitor. The stabilising effect on the drain current is improved by making the voltage $I_D R_S$ across the resistance high with respect to the voltage $V_{GS} - V_P$. This is true for the influence of both manufacturing spreads and temperature. For operation in the depletion mode the very simple circuit of Fig. 38*a* can be used ($-V_{GS} = I_D R_S$). For operation in the enhancement mode it is necessary to have a voltage divider R_1/R_2 (Fig. 38*b*).

Fig. 39 shows a method of stabilising the operating point which is only suitable for enhancement mode operation. Its stabilising effect is based on d.c. feedback via resistors R_D and R_K. Since the gate current is zero, this circuit operates at $V_{DS} = V_{GS}$. The voltage drop $I_D R_D$ has the same effect as the voltage drop $I_D R_S$ in the circuit of Fig. 38*a*, but can be made much higher. Thus stabilisation is much better than that obtained with the circuits of Figs 38*a* and *b*. Resistor R_K also produces a.c. feedback, which reduces not only the input resistance but also the voltage amplification of the circuit. Assuming an infinite input resistance for the MOS-FET, the input resistance of the circuit will be:

$$R_i = \frac{v_i}{i_K} = \frac{R_K}{1 + |A|}, \tag{24}$$

where $|A|$ is the voltage amplification in the common-source configuration without feedback.

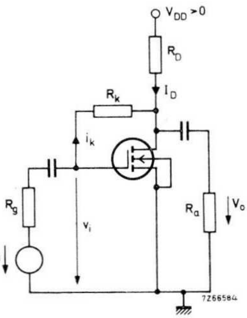
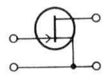
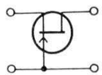
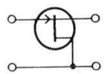


Fig.39 Stabilisation of the operating point of a normally-off MOS-FET by means of drain-gate feedback via R_D and R_K. (R_K reduces the input impedance).

Table I. y-parameters for three circuit configurations.

	input admittance $y_{11} = y_i$	reverse transfer admittance $y_{12} = y_r$	forward transfer admittance $y_{21} = y_f$	output admittance $y_{22} = y_o$	
common source	y_{is} $= j\omega\,(C_{gs} + C_{dg}) +$ $+ \omega^2\, C_{gs}{}^2\, r_{gs}$	$y_{rs} = -j\omega\, C_{dg}$	y_{fs} $= g_m - j\omega\, C_{dg}$	y_{os} $= g_{ds} +$ $+ j\omega\,(C_{ds} + C_{dg})$	
common gate	y_{ig} $= j\omega\,(C_{gs} + C_{dg}) +$ $+ g_{ds} + \omega^2\, C_{gs}{}^2\, r_{gs} +$ $+ g_m$	y_{rg} $= -g_{ds} - j\omega C_{ds}$	y_{fg} $= -g_m - g_{ds} -$ $-j\omega\, C_{ds}$	y_{og} $= j\omega\,(C_{dg} + C_{ds}) +$ $+ g_{ds}$	
common drain	y_{id} $= j\omega\,(C_{gd} + C_{gs}) +$ $+ \omega^2\, C_{gs}{}^2\, r_{gs}$	y_{rd} $= -j\omega\, C_{gs} -$ $- \omega^2\, C_{gs}{}^2\, r_{gs}$	y_{fd} $= -g_m - j\omega\, C_{gs} -$ $- \omega^2\, C_{gs}{}^2\, r_{gs}$	y_{od} $= j\omega\,(C_{ds} + C_{gs}) +$ $+ g_{ds} +$ $+ \omega^2\, C_{gs}{}^2\, r_{gs}$	 7Z66588

5.2 Basic circuit configurations

There are three basic circuit configurations for FETS:
1. common source configuration (CSC);
2. common gate configuration (CGC);
3. common drain configuration (CDC).

The nomenclature follows the same system as for bipolar transistors: the first index concerns input (i), forward (f), reverse (r) or output (o). The second index indicates the circuit configuration being considered (s, g or d).

In Table I a matrix is given of the y-parameters in the three configurations. They are derived from the small signal equivalent circuit (Fig. 33).

The choice of configuration depends on the circuit designers requirements with respect to:

- Input impedance (high in CSC and CDC).
- Impedance matching to signal source and load for maximum power gain or minimum noise.
- Signal handling (minimum distortion). The smaller the input signal voltage the lower will be the distortion. Thus for the same available signal power the distortion is lowest in common gate configuration (lowest input impedance).

5.3 Typical applications of junction field-effect transistors

5.3.1 Television camera preamplifier using FETs in cascode

The output signal from a TV camera tube should be amplified with as little noise as possible. Since the output impedance of the camera tube is very high, bipolar transistors cannot be used in the input stage of the amplifier. Junction FETS on the other hand give a very good signal-to-noise ratio.

The circuit described here was developed for a PLUMBICON® 55 875 camera tube. The output of this tube can be represented by a signal current generator I_s in parallel with a capacitor C_p (approx. 12 pF) (Fig. 40a). The voltage across C_p is inversely proportional to frequency, whereas the output of the amplifier should be frequency independent.

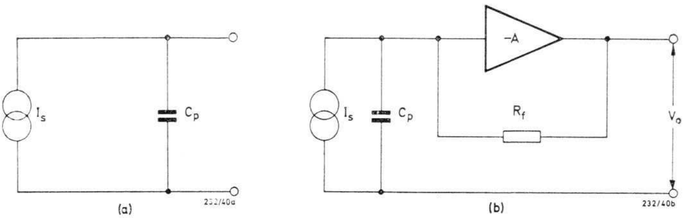


Fig.40 (a) Equivalent circuit of the output of the Plumbicon® tube. (b) The camera pre-amplifier with feedback applied.

The flat frequency response is obtained by applying overall current feedback as shown in Fig. 40*b*. In this case, assuming that the amplifier voltage gain is high, $V_o = I_s R_f$. However, at frequencies above 0.5 MHz the voltage gain begins to fall off, so that high frequency response is improved by partial decoupling of the feedback loop as illustrated in Fig. 41.

To meet the signal-to-noise ratio requirement, FETs are used in the first stage, because they are less noisy than bipolar transistors when operating with this order of signal-source capacitance C_p. However full advantage cannot be taken of the lower noise figures unless two FETs are used in cascode configuration. With a single FET input stage the Miller capacitance reduces the gain at high frequencies and the noise contribution from the second stage becomes too high. A cascode arrangement of a bipolar transistor and a FET is also too noisy; two FETs in cascode give the best performance, and the signal-to-noise ratio of the amplifier is then mainly determined by the input stage noise.

A complete circuit of the preamplifier is shown in Fig. 42. Type BSV79 was chosen for the input stage because its input capacitance is optimum for minimum noise ($C_{is} = C_p$), whilst its g_{fs}/C_{is} ratio is similar to other types of FET.

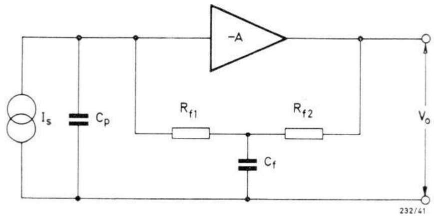


Fig.41 The pre-amplifier feedback loop shown partially decoupled.

In this circuit the collector voltage of the output transistor TR_5 should be set at 28 V by adjusting potentiometer R_1, to avoid clipping of the output waveform at maximum signal amplitude. The drain current of the FETs is then approximately 18 mA. The voltage gain is adjusted by potentiometer R_{20}, and the frequency response by pre-set capacitor C_{12}.

Table II summarises some characteristics of the preamplifier shown at Fig. 42.

Table II. Some characteristics of the preamplifier in Fig. 42.

Forward transfer impedance V_o/I_s (frequency range 40 Hz to 5.5 MHz, $R_L = 75\ \Omega$):	1×10^6 V/A
Output impedance:	75 Ω
Signal-to-noise ratio (ratio of peak-to-peak output voltage to total r.m.s. noise voltage, at $I_s = 300$ nA (peak-to-peak), through a frequency range of 40 Hz to 5.5 MHz):	approx. 46 dB

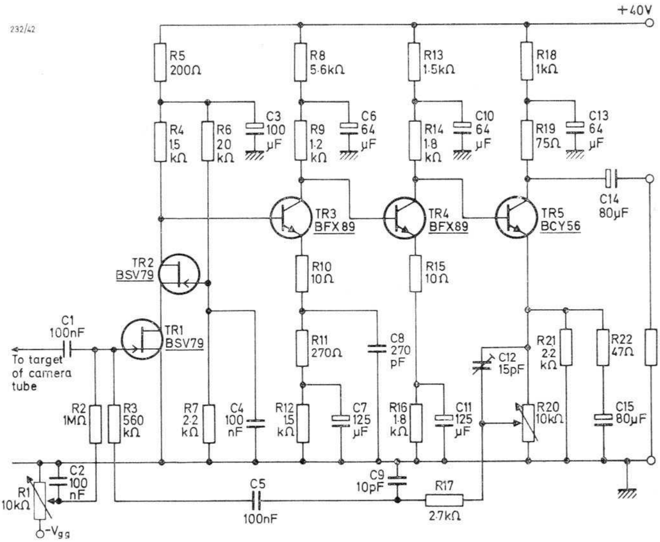


Fig.42 Camera pre-amplifier using cascoded BSV79 FETs in the input stage.

The r.m.s. noise voltage at the output of the preamplifier is shown as a function of frequency in Fig. 43.

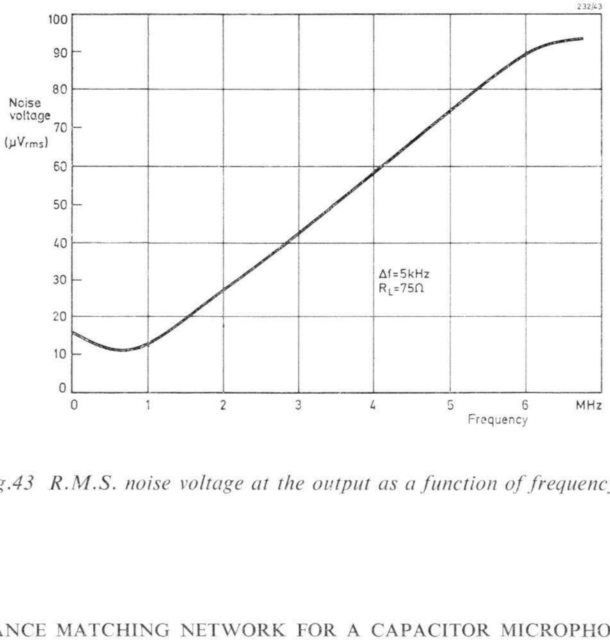


Fig.43 R.M.S. noise voltage at the output as a function of frequency.

5.3.2 IMPEDANCE MATCHING NETWORK FOR A CAPACITOR MICROPHONE

A capacitor microphone is inherently unsuitable for driving a bipolar transistor. If the input impedance of the transistor were high enough to give a reasonable transfer ratio, the noise factor would also be high; conversely if the input impedance were low enough to give sufficiently low noise factor, the transfer ratio would be inadequate. The field-effect transistor can be used advantageously for stepping down the high microphone impedance. Its noise contribution remains extremely small, even at high source impedances. The noise contribution of an impedance matching circuit embodying a BFW11 field-effect transistor as a source follower will now be considered.

The equivalent circuit of a capacitor microphone consists of a signal voltage source E_s in series with a capacitance C_s, as shown in Fig. 44*a*.

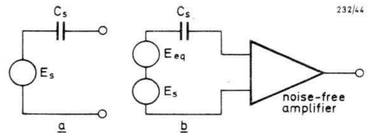


Fig.44 Equivalent circuit of a capacitor microphone, (a) without, and (b) with noise voltage source due to an impedance matching network.

Typically, the sensitivity S of the microphone can be taken to be 1 mV/μbar, and its capacitance C_s to be about 33 pF. When the microphone is connected to an impedance matching circuit, the noise contribution of the latter can be represented by a second voltage source E_{eq} in series with E_s, as shown in Fig. 44*b*.

Fig. 45 shows a representative impedance matching circuit making use of a field-effect transistor. R_p is the bias resistor and is generally in the order of a few hundred megohms. The drain current of the field-effect transistor is adjusted to the required value by means of a load resistance R_L of, say, 3 kΩ. However, since this resistance is shunted by $1/g_m$ (where g_m denotes the transconductance), an impedance of less than 1 kΩ is usually presented to the following stage so that the latter can be equipped with a conventional transistor in common collector configuration without noticeably contributing towards the noise. Its emitter resistance can easily be matched to the cable which links the microphone to its amplifier.

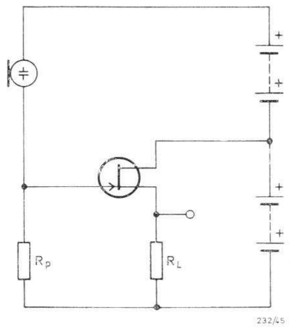


Fig.45 Field-effect transistor in an impedance matching network for a capacitor microphone.

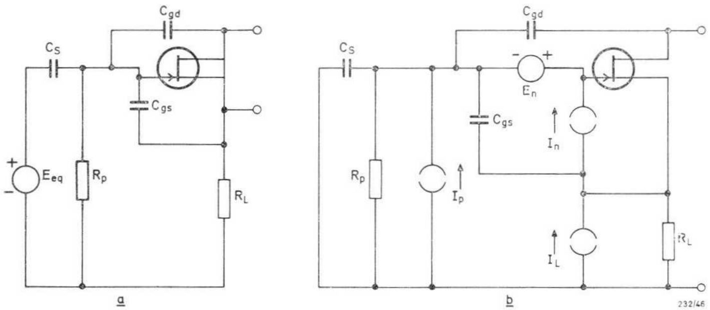


Fig.46 (a) Equivalent circuit of the network of Fig. 45. (b) Expanded equivalent circuit showing current and voltage sources responsible for the noise contribution of the network.

A simple equivalent circuit showing the noise voltage source is given in Fig. 46*a*. For purposes of analysis this circuit can be expanded into the more detailed form of Fig. 46*b* in which the several factors responsible for development of the equivalent noise voltage E_{eq} are separately indicated. As shown in the drawing, these are:

E_n – the equivalent noise voltage of the field-effect transistor;
I_p – the noise current of resistor R_p;
I_L – the noise current of resistor R_L;
I_n – the equivalent shot noise current source due to the gate leakage current.

These noise sources are defined by the expressions:

$$\Delta\overline{|E_n|^2} = A\Delta f/f + 4\,kT\Delta f/g_m, \tag{25}$$

$$\Delta\overline{|I_p|^2} = 4\,kT\Delta f/R_p, \tag{26}$$

$$\Delta\overline{|I_L|^2} = 4\,kT\Delta f/R_L, \tag{27}$$

$$\Delta\overline{|I_n|^2} = 2\,qI_G\Delta f, \tag{28}$$

in which the factor A varies slightly with the drain current and voltage, k is Boltzmann's constant (8.62×10^{-5} eV/degK), T the absolute temperature, q the electron charge (1.6×10^{-19} C) and I_G denotes the gate current.

The variation of the equivalent noise is given by:

$$\Delta\overline{|E_{eq}|^2} = \frac{\Delta\overline{|I_p|^2}}{\omega^2 C_s^2} +$$

$$+ \frac{\Delta\overline{|I_n|^2}\,\{(g_m - 1/R_p)^2 + \omega^2 C_{is}^2\}}{\omega^2 C_s^2\,(g_m^2 + \omega^2 C_s^2)} +$$

$$+ \frac{(\Delta\overline{|E_n|^2} g_m^2 + \Delta\overline{|I_L|^2})\,\{1/R_p^2 + \omega^2\,(C_s + C_{is})^2\}}{\omega^2 C_s^2\,(g_m^2 + \omega^2 C_s^2)}, \tag{29}$$

in which C_{is} denotes the input capacitance $C_{gd} + C_{gs}$ of the transistor. For audio frequencies

$$g_m^2 \gg \omega^2\,(C_s + C_{is}) \gg 1/R_p^2,$$

so eq. (29) can be simplified to:

$$\begin{aligned}\Delta\overline{|E_{eq}|^2} &= (\Delta\overline{|I_p|^2} + \Delta\overline{|I_n|^2})/\omega^2 C_s^2 + \\ &+ (\Delta\overline{|E_n|^2} + \Delta\overline{|I_L|^2}/g_m^2)\,(1 + C_{is}/C_s)^2.\end{aligned} \tag{30}$$

In measuring subjective judgement of noise (see following section on "Acoustic Considerations") it is customary to put the bandwidth Δf in eqs (25) to (28) equal to:

$$\Delta f = \tfrac{1}{2} f \sqrt{2},$$

which gives

$$\overline{|E_{eq}|^2} = \int_{\frac{1}{2}f\sqrt{2}}^{f\sqrt{2}} (\Delta\overline{|E_{eq}|^2}/\Delta f)\,\mathrm{d}f,$$

whence, from eq. (30) and eqs (25) to (28):

$$\overline{|E_{eq}|^2} = \frac{2\times 10^{-2}}{f C_s^2}\left(\frac{4\,kT}{R_p} + 2qI_G\right) + \left(1 + \frac{C_{is}}{C_s}\right)^2 \left(\frac{2\,kTf\sqrt{2}}{2g_m/3 + R_L g_m^2} + A\log_e\frac{5}{3}\right). \tag{31}$$

Given the values:

$C_s = 33$ pF	$R_p = 250$ MΩ	$g_m \approx 1$ mA/V
$C_{is} < 5$ pF	$R_L = 3$ kΩ	$A = 10^{-13}$ V^2

it can be calculated from eq. (31) that with the maximum gate current I_G of 0.5 nA:

$$\overline{|E_{eq}|^2} = 4.6 \times 10^{-9}/f + 0.7 \times 10^{-13} + 1.6 \times 10^{-17} f,$$

and with the typical gate current I_G of 0.1 nA:

$$\overline{|E_{eq}|^2} = 2.0 \times 10^{-9}/f + 0.7 \times 10^{-13} + 1.6 \times 10^{-17} f.$$

In Fig. 47 these values of $\overline{|E_{eq}|^2}$ have been plotted as functions of f.

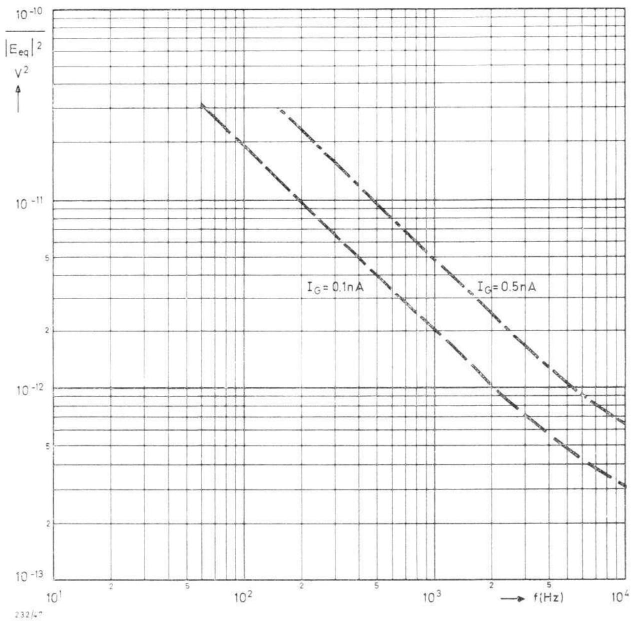


Fig.47 Graphical representation of the equations of $\overline{|E_{eq}|^2}$ *for two values of the gate current* I_G.

To relate the voltage E_{eq} to an equivalent noise, we must take into account the sensitivity of two transducers: the microphone and the human ear. As has already been stated, the sensitivity of the microphone may be taken to be 1 mV/μbar. The sensitivity of the human ear to noise with a bandwidth Δf centered around a given frequency f (where $\Delta f = \frac{1}{2} f \sqrt{2}$) is indicated by the loudness level contours of Fig. 48. Along the ordinate of the graph, objectively measured sound pressure levels p_{rel} are expressed in decibels relative to a pressure p_{0dB} of 2×10^{-4} μbar; along the abcissa, frequency is represented on a scale divided into octave intervals. The family of numbered curves shows how subjective judgement of noise loudness varies with frequency, the standard of comparison on which each curve is based being a 1 kHz reference note.

For the subjective increments of acoustic noise by which the curves are separated, the unit of measurement is the phon. Thus, at 1 kHz a loudness increment of 1 phon corresponds exactly to a sound pressure increment of 1 dB. Below that frequency 1 phon corresponds to less than 1 dB and above it to more than 1 dB, in proportion to the curvature and divergence of the curves.

In the frequency range covered by the graph, noises of equal pressure level seem to the human ear to grow louder as their frequency rises; moreover, as the trends and spacing of the curves indicate, the effect is more pronounced at low frequencies and loudness levels than at high.

To find what the noise voltage E_{eq} means in terms of acoustic noise superimposed on the output of the microphone, the ratio of E_{eq} to the sensitivity S of the microphone can be expressed as an equivalent sound pressure p_{eq}: thus

$$p_{eq} = E_{eq}/S. \tag{32}$$

The ratio (expressed in dB) of p_{eq} to the 0 dB reference pressure ($p_{0dB} = 2 \times 10^{-4}$ μbar) then indicates the sound pressure level p_{rel} that corresponds to the noise voltage E_{eq}:

$$p_{rel} = 20 \log (p_{eq}/p_{0dB}) = 20 \log (E_{eq}/S p_{0dB}). \tag{33}$$

Working this out for several frequencies throughout the audio range, a curve can be derived which, by superposition on the loudness level contours of Fig. 48 indicates the apparent noise contribution at any frequency. The curve drawn in dash-dot line in Fig. 48 shows the result when $\overline{E_{eq}}$ is worked out on the basis of the maximum value of I_G (0.5 nA), and the curve in broken line when it is worked out on the basis of the typical value (0.1 nA).

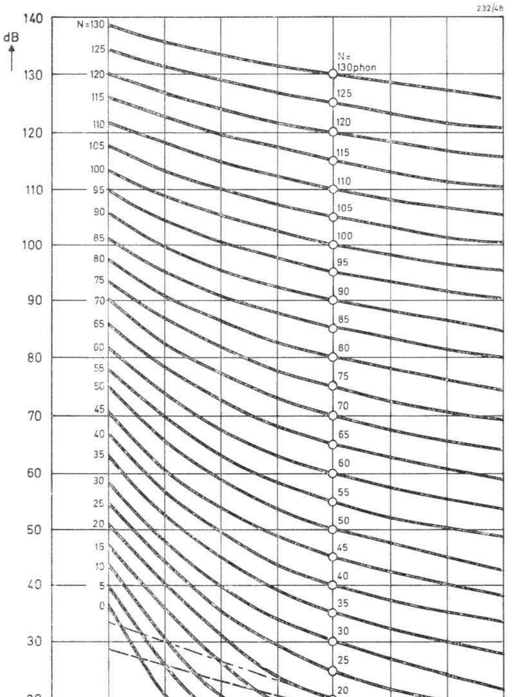


Fig.48 Loudness level contours, showing how the subjective impression of loudness varies with frequency. The ordinate of the graph represents the sound pressure level expressed in decibels relative to 2×10^{-4} μbar. The curves are contours of equal apparent loudness relative to a 1 kHz tone at the sound pressure levels indicated by the numbers adjoining them.

The two curves superimposed on the loudness level contours of Fig. 48 represent sound pressure levels: what they mean in terms of apparent noise can be interpreted by reference to the contours they cross. At 4 kHz, for example, the dash-dot line indicates a sound pressure level p_{rel} of about 16 dB, and at that frequency such a level corresponds to a noise loudness level of about 21 phon. Hence, if I_G is maximum (0.5 nA), the noise contribution of the matching network at 4 kHz is 21 phon; similarly, if I_G is only 0.1 nA (broken line curve), the sound pressure level at 4 kHz is about 13 dB and the noise contribution of the matching network 18 phon.

At lower frequencies, though the sound pressure level equivalent of the noise voltage rises, it does so less steeply than the loudness level contours; hence the noise contribution of the matching network diminishes. Thus, at 250 Hz the sound pressure level indicated by the broken line curve is about 23 dB, corresponding to a noise contribution of only about 13 phon.

That the two curves show the noise contribution of the network to be negligible throughout the frequency range of interest can be appreciated by reference to Table III, in which average ambient noise levels encountered in spaces designed for various uses are shown.

Table III. Average ambient noise levels in various enclosed spaces.

broadcasting studio	15 phon
concert hall, theatre (500 seats)	20 phon
class room, music room, television studio, conference room (50 seats), sleeping room	25 phon
conference room (20 seats), cinema, hospital, church, courtroom, library, living room	30 phon
private office	40 phon
restaurant	45 phon
gymnasium	50 phon
office (with typewriters)	50 phon
workshop	65 phon

From these considerations it is apparent that the BFW11 field effect transistor connected as a source follower can easily satisfy the most stringent requirements likely to be imposed on an impedance matching network for a capacitor microphone. The same is not true, however, if it is connected in common source configuration. In that case the noise due to the load resistance R_L is augmented by the noise current I_{ef} of the emitter follower to be driven, giving an increase in E_{eq} that amounts to:

$$\Delta\overline{|E_{eq}|^2} \approx \overline{|I_{ef}|^2}/g_m{}^2.$$

This may turn out to be as large as the contribution due to the thermal noise voltage E_n of the field effect transistor.

5.3.3 Preamplifier for a wide-band oscilloscope

Until recently the vertical preamplifiers of nearly all oscilloscopes were equipped with an electron tube in the input stage. Attempts to replace the tube by a transistor were hampered by two drawbacks inherent to bipolar transistors: first their input impedance was too low and, second, to keep the base current down, the collector current had to be adjusted to such a low value that the gain at high frequencies fell far short of what was needed in an oscilloscope.

With the development of unipolar devices – such as the field-effect transistor – both drawbacks can now be overcome. In the vertical preamplifier to be described, the BFW10 field-effect transistor is used both for the signal input and for the vertical shift control.

The preamplifier shown in Fig. 49 is a three-stage differential amplifier having outputs in antiphase with each other. Of the two inputs one is for the signal, and the other for adjusting the d.c. bias that governs the vertical shift. The field-effect transistors at both inputs are connected as source followers to provide a low enough source impedance for the BFY90 transistors of the following stage to ensure that their gain will remain constant at high frequencies.

Owing to its low input capacitance, high input impedance, and low output impedance, a source follower is particularly suitable for use in the input stage. During ordinary use of an oscilloscope it may happen that too high a voltage is accidentally applied to the signal input of the preamplifier; measures must therefore be taken to safeguard all the transistors. In the circuit shown, the measures taken are twofold; the network R_2R_3 between the signal input and the gate of TR_1 limits the gate current, and the clamping diodes D_1 and D_2 limit both positive and negative excursions of the source voltage.

If a high positive voltage is applied to the signal input, diode D_1 and the diode formed by the gate-source junction of the field-effect transistor are driven into conduction, the current through them being determined by resistor R_2. Under these circumstances the gate current of the field-effect transistor may reach at most 10 mA. If a high negative voltage is applied, the current through the field-effect transistor decreases and D_2 becomes conductive; in that case the source of TR_1 and the base of TR_3 will be clamped to a potential of approximately -0.7 V with respect to earth, even if the gate-drain breakdown voltage of TR_1 is exceeded. Here again the resistors R_2 and R_3 limit the intensity of the gate

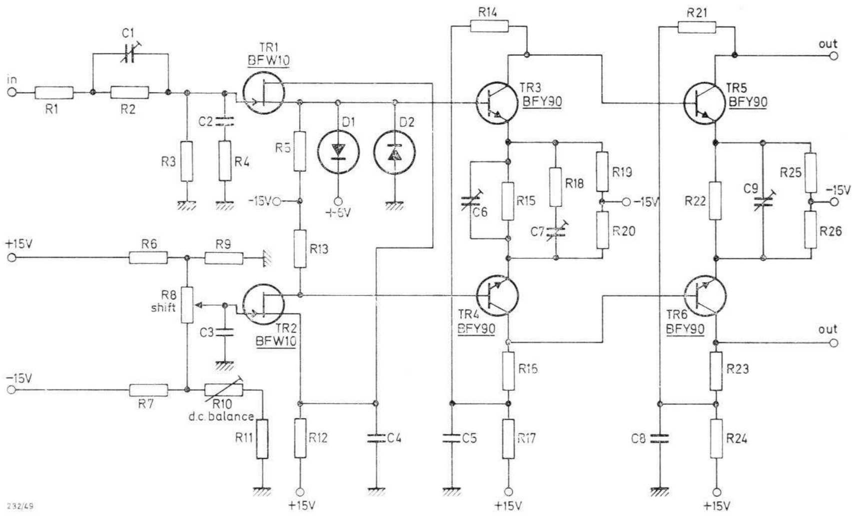


Fig.49 Three-stage vertical pre-amplifier for an oscilloscope with a pair of field-effect transistors in the signal input and the vertical shift control in the first stage.

$R_1 = 47\ \Omega$	$R_{13} = 3.9\ k\Omega$	$R_{25} = 1.5\ k\Omega$
$R_2 = 300\ k\Omega$	$R_{14} = 100\ \Omega$	$R_{26} = 1.5\ k\Omega$
$R_3 = 700\ k\Omega$	$R_{15} = 100\ \Omega$	$C_1 = 20\ pF$
$R_4 = 2.2\ k\Omega$	$R_{16} = 100\ \Omega$	$C_2 = 1.5\ pF$
$R_5 = 3.9\ k\Omega$	$R_{17} = 330\ \Omega$	$C_3 = 0.1\ \mu F$
$R_6 = 10\ k\Omega$	$R_{18} = 56\ \Omega$	$C_4 = 0.1\ \mu F$
$R_7 = 10\ k\Omega$	$R_{19} = 1.7\ k\Omega$	$C_5 = 0.1\ \mu F$
$R_8 = 500\ \Omega$ (potentiometer)	$R_{20} = 1.7\ k\Omega$	$C_6 = 6\ pF$
$R_9 = 100\ \Omega$	$R_{21} = 50\ \Omega$	$C_7 = 6\ pF$
$R_{10} = 100\ \Omega$	$R_{22} = 27\ \Omega$	$C_8 = 0.1\ \mu F$
$R_{11} = 50\ \Omega$	$R_{23} = 50\ \Omega$	$C_9 = 5\ pF$
$R_{12} = 680\ \Omega$	$R_{24} = 56\ \Omega$	*Diodes D_1 and D_2 are type BAW62.*

current. However, if they are allowed to persist, the reverse currents due to high negative voltages can cause damage to the field-effect transistor, so care should be taken not to keep the probe in contact with such a voltage any longer than necessary.

Capacitor C_1 shunting R_2 prevents undue attenuation of high-frequency signals by the gate-drain and gate-source capacitances. When a high voltage step function is applied to the signal input, C_1 is charged; for a short period a part of the charge current flows through the gate of the field-effect transistor, and during this period the field-effect transistor dissipates energy in the form of heat. The dissipated energy is practically equal to the energy stored in capacitor C_1 at full charge. The maximum permissible surge energy the field-effect transistor can withstand is 10 μWs, whence:

$$(1/2)\, C_1 V_{max}^2 < 10^{-5} \text{ Ws}. \tag{34}$$

Taking the maximum voltage permissible at the signal input to be about 300 V, according to eq. (34) the value of C_1 must be less than 200 pF.

In a test arrangement, rapid voltage transients of 300 V applied to the input by means of a mercury switch did not cause noticeable harm to the transistor.

The field-effect transistor would, of course, be equally well protected if the diodes were connected to the gate, but then the capacitances of the diodes would unduly increase the total input capacitance. Moreover, their leakage currents would then lead to extra thermal drift.

The field-effect transistor has an input impedance of about 10^{12} Ω, so the input impedance of the preamplifier is mainly accounted for by $R_2 + R_3 =$ 1 MΩ. The real part of the input impedance of the circuit measured at the gate of the field-effect transistor is negative for frequencies higher than 10 MHz. This is due to the capacitive load of the source follower and the phase shift of the transconductance of the field-effect transistor caused by the transit time of the electrons in the channel. At about 300 MHz the phase shift reaches 45°. To maintain a positive impedance at all frequencies, a resistor R_4 is connected in series with capacitor C_2 across the input. The positive real part of this impedance $(1/\omega^2 C_2^2 R_3)$ then overcompensates the negative real part of the source follower impedance, so that the input impedance remains positive for all frequencies. Fig. 50 is a plot of the input impedance as a function of frequency. Fig. 51 is a similar plot of its real part, the input resistance, which is positive for frequencies below 400 MHz.

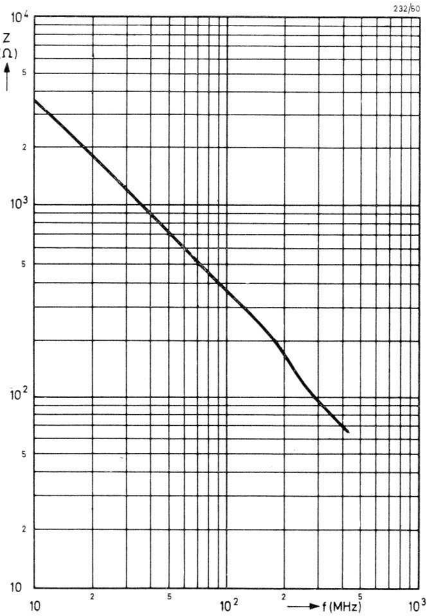


Fig.50 Input impedance of the pre-amplifier as a function of frequency.

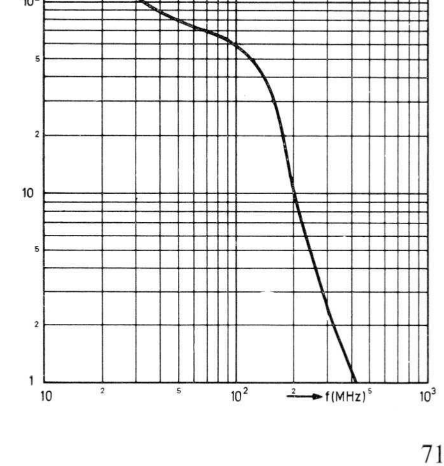


Fig.51 Input resistance of the pre-amplifier as a function of frequency.

Since the gain must remain constant from d.c. to 300 MHz, the voltage gain per stage must be kept low. The gain can be stabilized by means of the adjustable shunt capacitor C_1 and the trimming capacitors in the emitter circuits of the second and third stages. Capacitor C_1 must be so dimensioned that:

$$R_2 C_1 = R_3 \{C_2 + C_{gd} + (1 - \alpha) C_{gs}\},$$

in which C_{gd} is the gate-drain capacitance, C_{gs} the gate-source capacitance, and α the voltage gain of TR_1. Then the voltage attenuation between signal input and the gate of the field-effect transistor will be the same for a.c. and d.c. and equal to $R_3/(R_2 + R_3)$.

From d.c. to 300 MHz the gain is about 3. For an input step function with a rise time of about 0.3 ns the rise time at the output is about 0.9 ns, and there is less than 10% overshoot.

As with bipolar transistors, drift phenomena due to aging are much less pronounced in field-effect transistors than in electron tubes, and thus can be neglected.

However the thermal voltage drift of a FET input stage should not be neglected. Equation (12) gives the thermal drift of one FET.

The circuit under consideration is a difference amplifier, so if the thermal drift voltages of the second and third stages are neglected, and if the two field-effect transistors are thermally coupled, the total thermal voltage drift referred to the signal input will be:

$$\frac{\mathrm{d}\Delta V_{GS}}{\mathrm{d}T} = \frac{1}{\mu} \cdot \frac{\mathrm{d}\mu}{\mathrm{d}T} \left\{ \left(\frac{I_D}{g_{fs}} \right)_1 - \left(\frac{I_D}{g_{fs}} \right)_2 \right\} + \frac{\Phi_1 - \Phi_2}{T}, \tag{35}$$

where the subscripts 1 and 2 refer to transistors TR_1 and TR_2.

Thus the total drift voltage depends on the vertical shift setting, the thermal coupling of TR_1 and TR_2, and the difference between their respective transconductances. With the worst possible mismatch between the field-effect transistors, the drift was found not to exceed 4 mV/degC. If matching is given due attention, the drift voltage can be limited to about 0.5 mV/degC or less at zero shift setting.

In the range from d.c. to 300 MHz the effective noise signal measured with open-circuit input was less than 0.2 mV, which is within the width of the electron beam on the screen of even the most sensitive oscilloscope.

5.3.4 A D.C. TO 100 MHz UNITY-GAIN AMPLIFIER WITH FET INPUT

The amplifier described below is especially developed for use as a signal-probe amplifier for oscilloscopes or similar amplifiers in which a very low d.c. offset voltage is of utmost importance. To this end, two matched FETs are used in the input stage. Other attractive features of this unity gain amplifier are:

- the input impedance at 25 °C comprises a resistive part $> 10^9\ \Omega$ in parallel with a capacitive part < 4 pF;
- the offset voltage is adjustable to zero;
- the bandwidth is more than 100 MHz (-3 dB) at a 50 Ω load impedance;
- non-linear distortion less than 5 % for input voltages up to 0.5 V;
- output impedance typically 10 Ω.

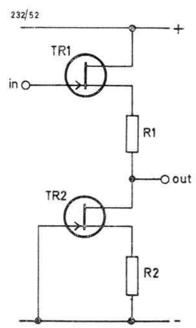


Fig.52 Simplified circuit diagram of the input stage.

Fig. 52 shows the simplified circuit of the input stage. The current source (TR_2, R_2) determines the current through the matched FETs (TR_1, TR_2). Hence

$$I_D \cdot R_2 = -V_{GS2} = -V_{GS1} \text{ (at } I_{out} = 0).$$

Thus, for $R_1 = R_2$,

$$I_D R_2 = I_D R_1 \text{ and } I_D R_1 + V_{GS1} = 0.$$

This means that the d.c. level at the output equals that at the input.

The output impedance of the input stage is found by adding the output resistance of TR_1 to R_1, that is 300 Ω + 200 Ω = 500 Ω.

Fig. 53a shows the circuit of the complete amplifier. Emitter follower TR_3 (BFY90) is connected to the first stage to bring the output impedance down to about 10 Ω. To ensure that $I_D R_1$ equals $I_D R_2$, the base current of TR_3 must be negligible with respect to I_D, which is the case when $h_{fe\ TR3} > 80$. With the aid of R_3 the V_{BE} of TR_3 is made equal to the diode voltage across D_1 so that thermal drift of TR_3 is compensated by that of D_1 and thus hardly affects the total offset voltage. Capacitor C can be adjusted to obtain the best possible frequency characteristic.

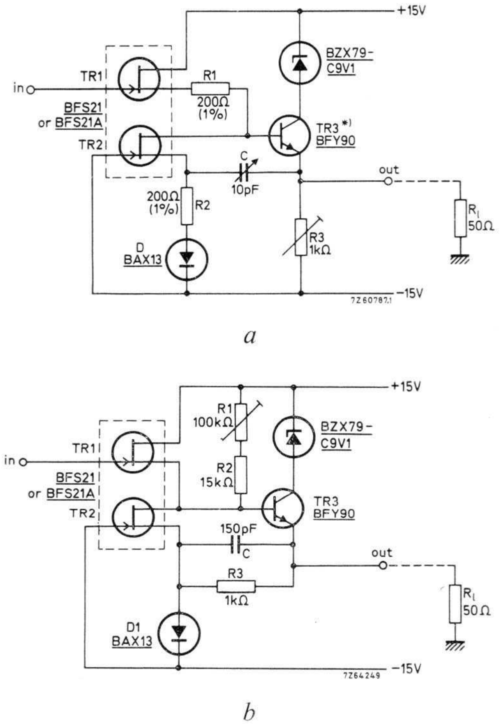


*Fig.53 (a) Circuit diagram of the complete amplifier. *BFY90 with $h_{fe} > 80$ so that its base current is negligible with respect to the drain current of the FETs. (b) Modified circuit diagram of the complete amplifier for use with an unselected BFY90.*

Fig. 53*b* shows another circuit diagram of the complete amplifier in which an unselected BFY90 can be used. Here the base current of TR_3 is supplied via R_1, R_2 (the offset voltage can be made zero by adjustment of R_1). Furthermore R_1 and R_2 of Fig. 53*a* are made zero to obtain a low output impedance of the input stage, and the emitter current of TR_3 flows through D_1 to improve the matching between V_{BE} and V_D.

The polar frequency diagram of Fig. 54 shows the gain and phase angle of the amplifier of Fig. 53*a* versus frequency at a load impedance of 50 Ω. By increasing the load impedance to 100 Ω, the gain will stay unity (0 dB) up to 200 MHz.

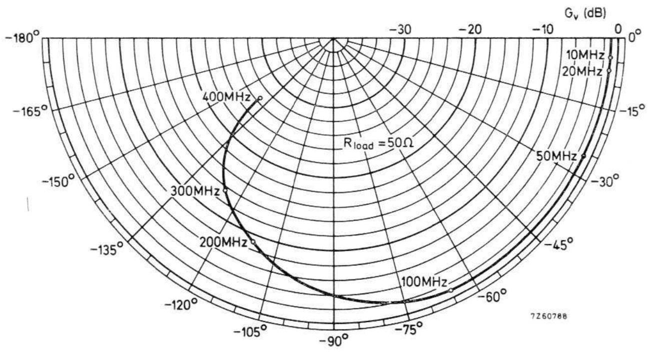


Fig.54 Polar diagram of the gain and phase angle versus frequency at a load impedance of 50 Ω for the circuit of Fig. 53a.

5.3.5 Field-effect transistors in a pre-amplifier for use with solid-state radiation detectors

Solid-state radiation detectors operate on the release by incident radiation of electron-hole pairs in the depletion layer of a reverse-biased p-n junction. The electric field generated by the bias voltage drives the charge carriers out of the depletion layer and the charge, which is proportional to the energy of the incident radiation, is fed to the input of the pre-amplifier. The output voltage of the pre-amplifier is proportional to the input charge, and therefore to the energy of the incident radiation.

These detectors offer several advantages over conventional types of radiation detector – for example, the resolution of a solid-state detector shows an improvement of a factor of about 10 over that of a scintillation counter. However, the output signal from the solid-state device is very much smaller than that derived from other types of detector *, and a high-gain amplification system must be used in conjunction with the device.

The resolution and stability of the electronic circuitry associated with a solid-state radiation detector play an important part in the overall performance of the energy-measuring system and low-noise amplification is therefore essential.

Fig. 55 is a block diagram of the electronics associated with a solid-state detector. The amplified signal is fed to a pulse-height analyser which sorts incoming pulses into a series of channels, each one corresponding to a narrow energy range. A threshold amplifier may be included to reduce the number of channels required for high-energy radiation.

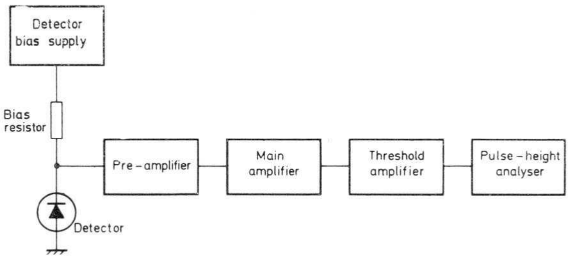


Fig.55 Block diagram of the electronics associated with solid-state detectors.

Fig. 56 shows a high-gain pre-amplifier circuit using low-noise BFW11 field-effect transistors in the charge-sensitive section. Capacitive feedback ensures that a large capacitive load is presented to the detector to minimise the effects of changes in wiring capacitance and detector capacitance. The active input

* The sensitivity of some radiation detectors expressed in coulombs per electron-volt is: Si-detector: 0.42×10^{-19} C/eV;/Ge-detector: 0.55×10^{-19} C/eV; gas-detector: 0.53×10^{-17} C/eV; Scintillator-detector: 0.53×10^{-15} C/eV.

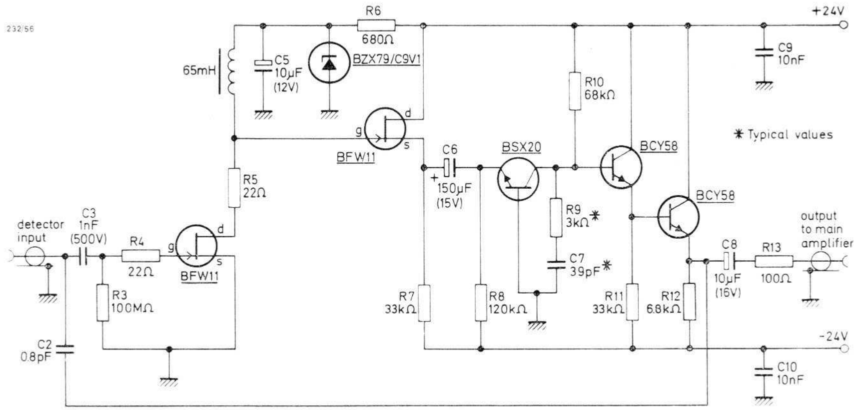


Fig.56 Pre-amplifier using field-effect transistors for silicon surface-barrier detector.

capacitance of the pre-amplifier is approximately equal to the product of feedback capacitance and loop gain, and its conversion gain (the ratio of output voltage amplitude to input charge) is approximately equal to the reciprocal of the active feedback capacitance. The decay time-constant of the charge-sensitive section is kept small to avoid loss of resolution at high counting rates due to pulse pile-up.

The remaining transistors form a conventional voltage amplifier, the high value of feedback ensuring high stability over extended periods of measurement. The pre-amplifier may be combined with a main amplifier with an input impedance of 100 Ω or higher.

The pre-amplifier converts into a voltage the charge released in the detector, its sensitivity being expressed either in terms of the detector output (volts per coulomb) or in terms of the energy of the incident radiation (volts per keV). The output of the pre-amplifier is then fed to the main amplifier. Since the noise generated by the pre-amplifier is dependent on the time-constant of the main amplifier, bandwidth-limiting elements, such as differentiating and integrating networks, in the main amplifier are designed to minimise the noise contribution of the amplification system as a whole.

Fig. 57 shows the noise contribution of the pre-amplifier, expressed as an equivalent noise charge in keV, as a function of detector capacitance and main-amplifier time-constant. Since the magnitude of the charge released in the detector by a given radiation depends on the material of which the detector is made, the noise contribution is specified separately for silicon and germanium detectors. The minimum noise contribution of the pre-amplifier is indicated by the dotted line.

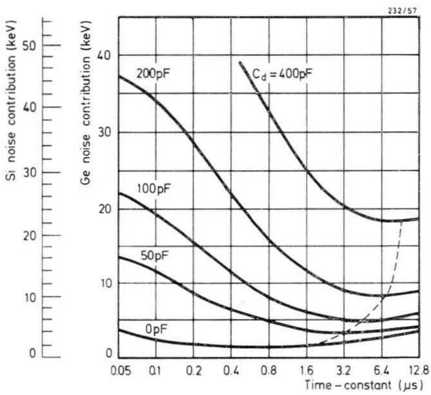


Fig.57 Noise contribution of pre-amplifier as a function of detector capacitance and amplifier time-constant.

5.3.6 The junction-FET in switching circuits

An ideal switch has zero on-resistance and infinite off-resistance, but all practical switches depart from this ideal to some extent. The circuit of a practical switch, showing the principal sources of error, is given in Fig. 58.

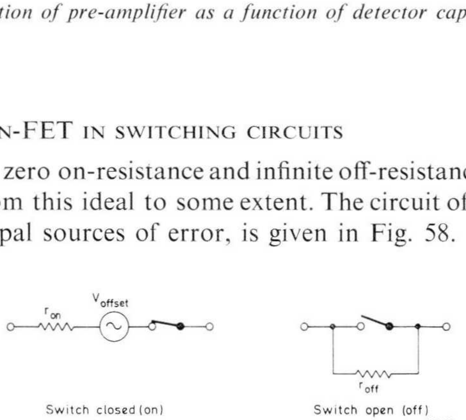


Fig.58 Errors generated by practical switch.

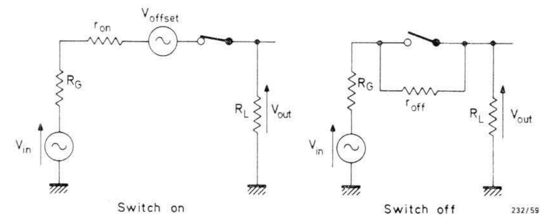


Fig.59 Elementary switching circuit.

The magnitude of the error may be calculated by considering the circuits of Fig. 59 in which V_{in} is the input voltage, V_{out} the output voltage, R_G the impedance of the signal source and R_L the load resistance.

When the switch is closed (on-state) the output voltage is ideally equal to the input voltage, but in practice:

$$V_{out} = V_{in} \cdot \frac{R_L}{R_L + r_{on} + R_G} + V_{offset}.$$

For minimum error the term $R_L/(R_L + r_{on} + R_G)$ must approach unity; that is, r_{on} should be very much smaller than R_L and R_G, and R_L should be much greater than R_G. The offset voltage must be as low as possible.

When the switch is open (off-state) the output voltage should be zero, but in fact is given by:

$$V_{out} = V_{in} \cdot \frac{R_L}{R_L + r_{off} + R_G}.$$

For minimum error, r_{off} should be very much higher than R_L and R_G.

The mechanical switch has a very high off-resistance and a very low on-resistance, but its operation is slow and it has an offset voltage in the on-state. The bipolar transistor has a higher on-resistance and lower off-resistance than the mechanical switch, and its offset voltage and switching speeds are higher. The FET switch has a low on-resistance and high off-resistance, and no offset voltage.

FETs have no storage of minority charge carriers in the channel such as occurs at the base in bipolar transistors. This means that the delay-time t_d during switch-on, and the storage-time t_s during switch-off are very short. Therefore the turn-on and turn-off times of the FET are mainly determined by the external circuitry and not by the physical properties of the FET itself.

The FET switch

An n-channel FET is switched off when the gate is negative with respect to the source. The resistance between drain and source is then about 10 GΩ. In practice, the turn-off voltage must be more negative than the sum of the pinch-off voltage and the greatest negative input signal. The FET is switched on when the gate-to-source potential is zero. The resistance between drain and source is then low, about 25 Ω for the BSV78.

Compensation of temperature variations

In the off-state the leakage current of the device produces an error voltage which may be neglected at room temperatures. The variation of leakage current may be compensated by connecting a reverse-biased diode, whose leakage current matches that of the FET, between the load and a positive supply.

In the on-state the channel resistance r_{on} also varies with temperature, the rate of change being approximately $+0.7\%$/degC. This variation may be compensated, if necessary, by connecting a thermistor in series with the FET.

Transient spikes

Small transient spikes may appear at the output of a FET switch, irrespective of the input signal. These spikes are caused mainly by the displacement of majority charge carriers during formation and elimination of the depletion layer in the channel. For increasing rise and fall times of the gate drive voltage the spikes decrease in height but increase in width. The total amount of charge associated with the spike depends only on the amplitude of the drive voltage.

Switching circuit configurations

(*a*) *Series switch.* In this configuration the switch is connected in series with the source and load, and a drive voltage is applied to the gate to alternatively connect the load to the signal source and disconnect it. This circuit is particularly suitable when the generator resistance is low. Fig. 60 shows a series switch which may be used for relatively high values of input signal and Fig. 61 shows the switching waveforms.

To switch the device on, V_{GS} must be zero. If the turn-on drive voltage is higher than the highest positive input voltage, diode D_1 will be reverse-biased and a high-value resistor R_1 ensures that V_{GS} is zero and the device saturated. To keep the value of drain current low a high value of load resistor R_L is required. In this circuit high load resistance minimises the on voltage error, but has the disadvantage of increasing the discharge time-constant ($C_{gd}R_L$) and thereby reducing the switching speed.

The on voltage error for the series switch is given by:

$$\Delta V_{on} = \frac{V_{in}(R_G + r_{on})}{R_G + r_{on} + R_L},$$

and the off voltage error by:

$$\Delta V_{off} = R_L I_{DG},$$

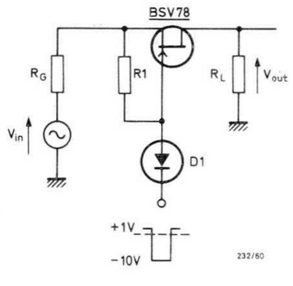


Fig.60 Series switch.

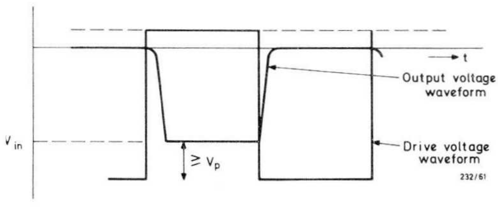


Fig.61 Switching waveform.

where I_{DG} is the gate-to-drain leakage current. Since the leakage is very low at room temperatures, R_L may be selected for minimum on error.

(*b*) *Shunt switch.* In the shunt switch configuration shown in Fig. 62 the FET is connected in parallel with the load and is switched between cut-off and zero bias. Ideally, during cut-off the input signal appears across the load and, during saturation, zero signal appears across the load; but in practice there are on and off voltage errors. This circuit is better suited to applications in which the generator resistance is high. Resistor R_1 prevents the input being short-circuited when the FET is turned on.

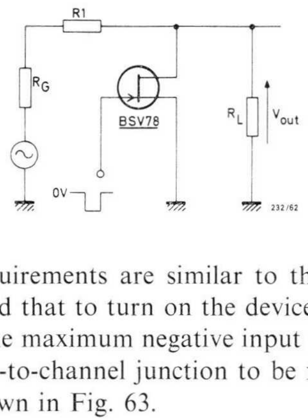


Fig.62 Shunt switch.

The drive requirements are similar to those already described, but it should be remembered that to turn on the device the drive voltage is reduced only to the value of the maximum negative input voltage, because a lower value would allow the gate-to-channel junction to be forward biased. The switching waveforms are shown in Fig. 63.

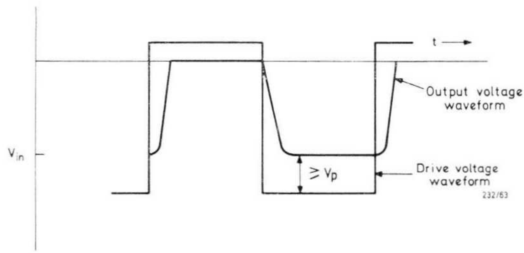


Fig.63 Switching waveform.

The on voltage error is given by:

$$\Delta V_{on} = \frac{V_{in}\, r_{on}}{R_G + r_{on}}.$$

and the off voltage error by:

$$\Delta V_{off} = (I_{DG} R_G + V_{in}) \frac{R_L}{R_G + R_L}.$$

Because this configuration is usually used in applications where the source resistance R_G is high, R_L must be very high to minimise the off voltage error. The output of the switch may be fed into a FET amplifier to achieve this high value of load resistance.

(*c*) *Series/shunt switch.* A series/shunt switch offers the advantages of both series and shunt circuits and allows compensation of some of the errors associated with each. The special advantage of the circuit is that the combination provides a low-resistance discharge path which allows high-frequency operation. Fig. 64 shows a series/shunt circuit using two n-channel FETs. A simple series circuit is followed by a shunt circuit, their drive voltages being in antiphase. The high load resistance required by the series switch for minimum error is provided by the high source resistor, which also ensures minimum error in the shunt circuit.

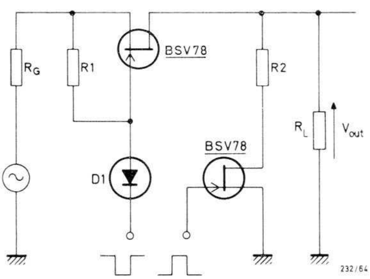


Fig.64 Series/shunt switch.

For a series/shunt switch the on voltage error is given by:

$$\Delta V_{on} = \frac{R_L \{I_{DG2} (R_G + r_{on1}) + V_{in}\}}{R_G + r_{on1} + R_L},$$

and the off voltage error by:

$$\Delta V_{off} = I_{DG1} \cdot \frac{r_{on2} R_L}{r_{on2} + R_L}.$$

Applications

FET switches may be used either as choppers or as analogue switches, both applications requiring the high off-resistance, low on-resistance, low capacitance and high switching speed which the FET provides.

A series of FET analogue switches may be used in a data acquisition system as shown in Fig. 65. The drive signals are timed to switch on each FET in sequence so that the amplifier accepts information from one signal source at a time while the remaining sources are disconnected. Compensation should be provided for the off error voltages, the total of which appears at the amplifier input.

Fig. 66 shows a bidirectional switch using three BSV78 FETs for use in multiplex switching circuits. This switch can handle voltages up to $\pm$ 30 V and currents up to $\pm$ 100 mA, opening at zero gate voltage and closing at a gate voltage of 6 V. The series resistance of the closed switch is 50 Ω, and the leakage resistance of the open switch greater than 10 GΩ. Switching times are less than 100 ns.

The use of FETs in sample and hold circuits in analogue memories allows small storage capacitors to be used, because errors due to stray capacitances are very low in FET circuitry. Thus accuracy is superior to that obtained with bipolar transistor switches, and aperture times may be very much shorter. Fig. 67 shows a sample and hold circuit. The output of the series switch is fed to the storage capacitor, connecting the input signal directly to the storage capacitor when the FET is switched on.

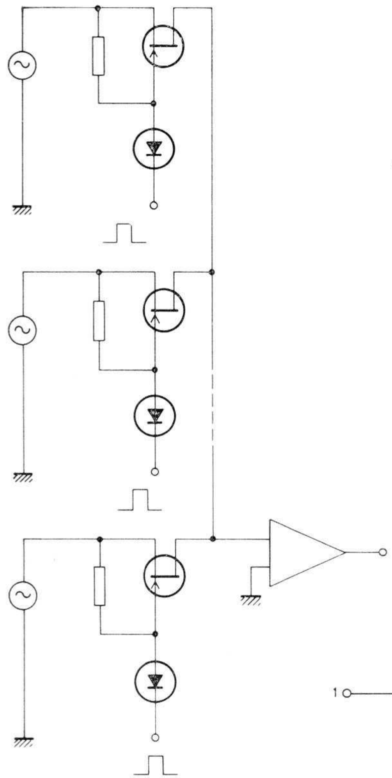


Fig.65 Analogue switches in data acquisition system.

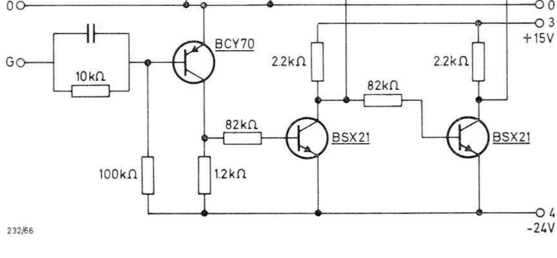


Fig.66 Bidirectional switch.

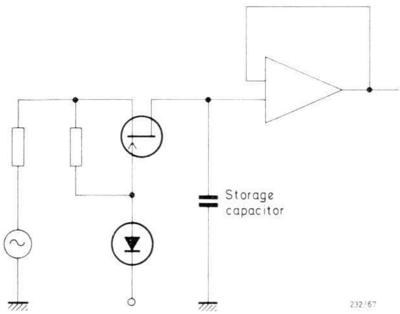


Fig.67 Sample and hold circuit.

5.3.7 THE JUNCTION-FET AS A CURRENT SOURCE

When a FET is biased in the pinch-off region, its drain current is almost independent of drain voltage. Thus the device can be used as a constant current source. When so used, a depletion type FET has three advantages over a bipolar transistor:

1. The FET can be biased with only one source resistance (see Fig. 68).
2. As a consequence the FET current source can also be used as a current sink (see Fig. 69).
3. By an appropriate choice of the source resistance, the FET can be biased at or close to its zero temperature coefficient point (see Fig. 24), thus making the drain current almost independent of change in temperature.

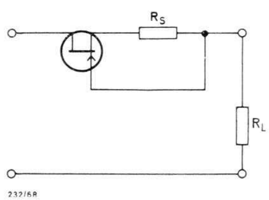


Fig.68 FET as a current source.

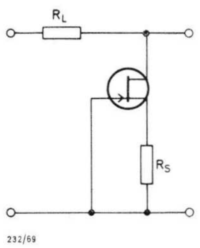


Fig.69 FET used as a current sink

As compared to the bipolar transistor, the FET has the disadvantage of a relatively high knee voltage ($= V_P$). Below this voltage the current is dependent on the drain voltage.

The important parameters of a constant current source are output conductance and temperature coefficient.

Output conductance

The FET constant current source (see Fig. 70*a*) can be represented by an ideal current source with a conductance g_o shunted across it (Fig. 70*b*), which has the value:

$$g_o = \frac{g_{os}}{1 + g_{fs} \cdot R_S},$$

where g_{os} is the output conductance of the FET. Taking BFW11 as an example, with $R_S = 2\ \text{k}\Omega$, then $I_D = 1$ mA, $g_{fs} = 2.3$ mA/V, and $g_{os} = 12\ \mu\Omega^{-1}$. Then g_o of the current source will be $2.15\ \mu\Omega^{-1}$.

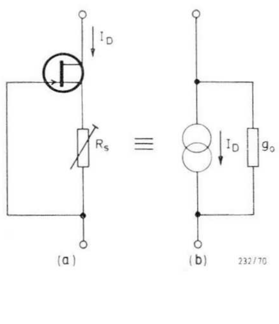


Fig.70 FET constant current source and its equivalent circuit diagram.

Temperature coefficient

The temperature coefficient of the current source will be zero when the FET is biased at point Z of Fig. 24, which means that V_{GS} will have the value of $V_{GS(Z)}$ given by equation (15).

When the FET is biased at a point other than Z, its temperature coefficient will be:

$$\frac{1}{I_D} \cdot \frac{\mathrm{d}I_D}{\mathrm{d}T} = \frac{1}{\mu} \cdot \frac{\mathrm{d}\mu}{\mathrm{d}T} \cdot \frac{V_{GS} - V_{GS(Z)}}{V_{GS} - V_P} = \frac{\mathrm{d}\Phi}{\mathrm{d}T}\left(1 - \sqrt{\frac{I_D}{I_{D(Z)}}}\right).$$

Assume $V_{GS} - V_{GS(Z)}$ to be $\pm$ 0.1 V, then $V_{GS} - V_P = 0.83$ V or 0.63 V, and $(1/I_D) \cdot (\mathrm{d}I_D/\mathrm{d}T) = 0.72 \times 10^{-3}$ or 0.072% per degC and 0.95×10^{-3} or 0.095% per degC.

As $V_{GS(Z)} - V_P$ increases about 2.2 mV/degC, the temperature coefficient of the current will not be zero for a current source used at temperatures differing from the one at which the FET has been biased for zero-drift working point. For instance, for $\Delta T = 45$ °C, $V_{GS} - V_{GS(Z)} \approx 0.1$ V, so that the temperature coefficient is about 0.1% per degC. However this temperature coefficient will be reduced by a factor of $1 + g_{fs} \cdot R_S$ because of the feedback provided by the bias resistor in the source.

Applications

The voltage across a voltage reference diode can be made practically independent of supply voltage variations by feeding the diode via a FET current source. In Fig. 68 for instance, this can be achieved by replacing R_L by a voltage-reference diode, as in Fig. 71.
Assuming g_o to be 2.15 $\mu\Omega^{-1}$ and r_z to be 100 Ω, supply voltage variations are reduced by a factor of about

$$\frac{1}{g_o \cdot r_z} = \frac{1}{2.15 \times 10^{-4}} = 4640.$$

The circuit of Fig. 72 is a linear sweep generator using two FETS; TR_1 is a source follower and TR_2 supplies a constant current. Since the drain current of TR_1 is held constant by TR_2, the gate-to-source voltage remains constant and the output voltage accurately follows the gate voltage. When the switch is opened, capacitor C_1 charges, the charging current being the sum of the current flowing through resistor R_1 and the gate current of the FET. The latter is very small (the gate leakage current) because the gate-to-source diode is reverse biased. Thus the charging current is effectively determined by resistor R_1 only and is constant. The fall in gate voltage is therefore linear and, as the output voltage follows the gate voltage, the slope of the output waveform is also linear.

The switch may be a bipolar transistor or a FET and the circuit may be used to generate a sawtooth waveform. The capacitor charging time is controlled by selection of capacitor and resistor R_1 values.

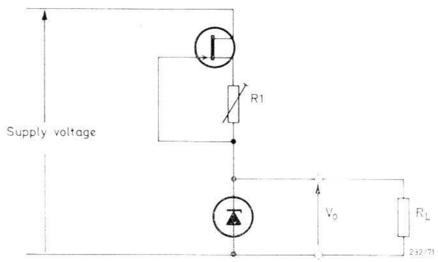


Fig.71 Stabilized current source for voltage reference diode.

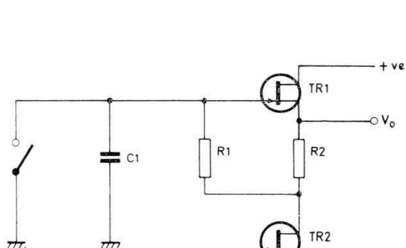


Fig.72 Linear sweep generator using FETs.

5.3.8 FET-PAIR AS A DIFFERENTIAL AMPLIFIER

Field-effect transistors have three points in their favour when compared with bipolars for use as input devices in operational amplifiers, electromedical amplifiers (ECG and EEG) and other differential amplifiers, viz:

- high input impedance,
- small input and offset current,
- low noise contribution when driven from high source impedances.

A drawback with FET pairs is their comparatively high offset voltage and its variation with temperature (thermal drift), with common mode input voltage, and with supply voltage. This drawback arises because of the relatively small transconductance of FETs, and also implies a comparatively high influence of other circuit components on the offset voltage of the whole amplifier and on its variations.

Offset voltage, common mode rejection, supply sensitivity and thermal drift

The offset voltage of a FET-pair is defined as the difference of the gate-to-source voltages when the FETs are biased for equal drain currents (I_D), equal drain-source voltages (V_{DS}) and equal ambient temperature (T).

$$V_{GS1} - V_{GS2} = \Delta V_{GS} = \mathrm{f}\,(I_D, V_{DS}, T) \text{ (see Fig. 73).} \tag{36}$$

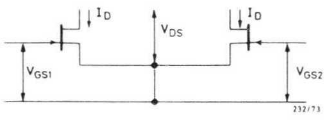


Fig.73 Basic circuit diagram of a FET-pair used as a differential amplifier, giving the current and voltage definitions.

A change of ΔV_{GS} with I_D, V_{DS} and T, according to equation (36) is equal to:

$$\mathrm{d}\Delta V_{GS} = \frac{\partial \Delta V_{GS}}{\partial I_D} \cdot \mathrm{d}I_D + \frac{\partial \Delta V_{GS}}{\partial V_{DS}} \cdot \mathrm{d}V_{DS} + \frac{\partial \Delta V_{GS}}{\partial T} \cdot \mathrm{d}T, \tag{37}$$

in which

$$\frac{\partial \Delta V_{GS}}{\partial I_D}=\frac{\partial V_{GS1}}{\partial I_D}-\frac{\partial V_{GS2}}{\partial I_D}=\frac{1}{g_{fs1}}-\frac{1}{g_{fs2}}=\Delta\left(\frac{1}{g_{fs}}\right), \tag{38}$$

$$\frac{\partial \Delta V_{GS}}{\partial V_{DS}}=\frac{\partial V_{GS1}}{\partial V_{DS}}-\frac{\partial V_{GS2}}{\partial V_{DS}}=\left(-\frac{g_{os}}{g_{fs}}\right)_1-\left(-\frac{g_{os}}{g_{fs}}\right)_2=-\Delta\left(\frac{g_{os}}{g_{fs}}\right), \tag{39}$$

and according to equation (12)

$$\frac{\partial \Delta V_{GS}}{\partial T}=\frac{\partial V_{GS1}}{\partial T}-\frac{\partial V_{GS2}}{\partial T}=\frac{1}{\mu}\cdot\frac{\mathrm{d}\mu}{\mathrm{d}T}\cdot I_D\cdot\Delta\left(\frac{1}{g_{fs}}\right)-\Delta\left(\frac{\mathrm{d}V_P}{\mathrm{d}T}\right). \tag{40}$$

Equations (36) to (40) are used to determine the contribution of the FET-pair (as differential input stage of an amplifier) to the total offset voltage, the common-mode-rejection, supply sensitivity and thermal drift of the whole amplifier.

A change in the common mode input voltage V_{CM} changes the drain currents I_D and the drain voltages V_{DS}. The applied circuit configuration then determines the factors $\mathrm{d}I_D/\mathrm{d}V_{CM}$ and $\mathrm{d}V_{DS}/\mathrm{d}V_{CM}$, which when multiplied respectively with the matching factors of the FET-pair $\Delta(1/g_{fs})$ and $\Delta(g_{os}/g_{fs})$ give the contribution of the FET-pair to the common mode rejection ratio CMRR by means of equation (37):

$$(\mathrm{CMRR})^{-1}=\frac{\mathrm{d}\Delta V_{GS}}{\mathrm{d}V_{CM}}=\Delta\left(\frac{1}{g_{fs}}\right)\cdot\frac{\mathrm{d}I_D}{\mathrm{d}V_{CM}}-\Delta\left(\frac{g_{os}}{g_{fs}}\right)\cdot\frac{\mathrm{d}V_{DS}}{\mathrm{d}V_{CM}}. \tag{41}$$

The contribution of the FET-pair to the supply sensitivity is determined in the same way:

$$\frac{\mathrm{d}\Delta V_{GS}}{\mathrm{d}V_S}=\Delta\left(\frac{1}{g_{fs}}\right)\cdot\frac{\mathrm{d}I_D}{\mathrm{d}V_S}-\Delta\left(\frac{g_{os}}{g_{fs}}\right)\cdot\frac{\mathrm{d}V_{DS}}{\mathrm{d}V_S}, \tag{42}$$

where V_S is the supply voltage; and for the thermal drift:

$$\frac{\mathrm{d}\Delta V_{GS}}{\mathrm{d}T}=\Delta\left(\frac{1}{g_{fs}}\right)\left(\frac{\mathrm{d}I_D}{\mathrm{d}T}+\frac{1}{\mu}\cdot\frac{\mathrm{d}\mu}{\mathrm{d}T}\cdot I_D\right)-\Delta\left(\frac{g_{os}}{g_{fs}}\right)\cdot\frac{\mathrm{d}V_{DS}}{\mathrm{d}T}-\Delta\left(\frac{\mathrm{d}V_P}{\mathrm{d}T}\right). \tag{43}$$

The maximum values of matching parameters of the FET-pair BFS21A are given in Table IV, for $V_{DS} = 15$ V.

Table IV. Maximum values of matching parameters for BFS21A at $V_{DS} = 15$ V.

	$I_D = 100\ \mu$A	$I_D = 200\ \mu$A	$I_D = 500\ \mu$A
ΔV_{GS}	10 mV	10 mV	10 mV
$\Delta\left(\frac{1}{g_{fs}}\right)$	37.5 Ω	20 Ω	7.5 Ω
$\Delta\left(\frac{g_{os}}{g_{fs}}\right)$	0.5×10^{-3}	0.5×10^{-3}	0.5×10^{-3}
$\frac{\partial \Delta V_{GS}}{\partial T}$	40 μV/degC	40 μV/degC	40 μV/degC

Circuit configurations using a FET-pair as the differential input stage

The circuit configuration determines the values of the factors

$$\frac{\mathrm{d}I_D}{\mathrm{d}V_{CM}}, \frac{\mathrm{d}V_{DS}}{\mathrm{d}V_{CM}}, \frac{\mathrm{d}I_D}{\mathrm{d}V_S}, \frac{\mathrm{d}V_{DS}}{\mathrm{d}V_S}, \frac{\mathrm{d}I_D}{\mathrm{d}T} \text{ and } \frac{\mathrm{d}V_{DS}}{\mathrm{d}T}$$

given in equations (41), (42) and (43).

Fig. 74 shows six basic circuit configurations. The FETs are arranged as common drain amplifiers in Figs 74*a*, *b* and *c*, and as common source amplifiers in Figs 74*d*, *e* and *f*. The low output impedance of the common drain amplifiers allows the use of integrated operational amplifiers as output devices without the necessity of modifications to the recommended frequency compensation networks.

Modification of the recommended frequency compensation networks is necessary however when the input stage is a common source amplifier, because of its high output impedance; consequently, circuits using discrete devices will then be preferred, to allow high bandwidth and slew-rate.

As far as offset voltage, CMRR and thermal drift are concerned, there is not much to choose between common drain and common source configurations.

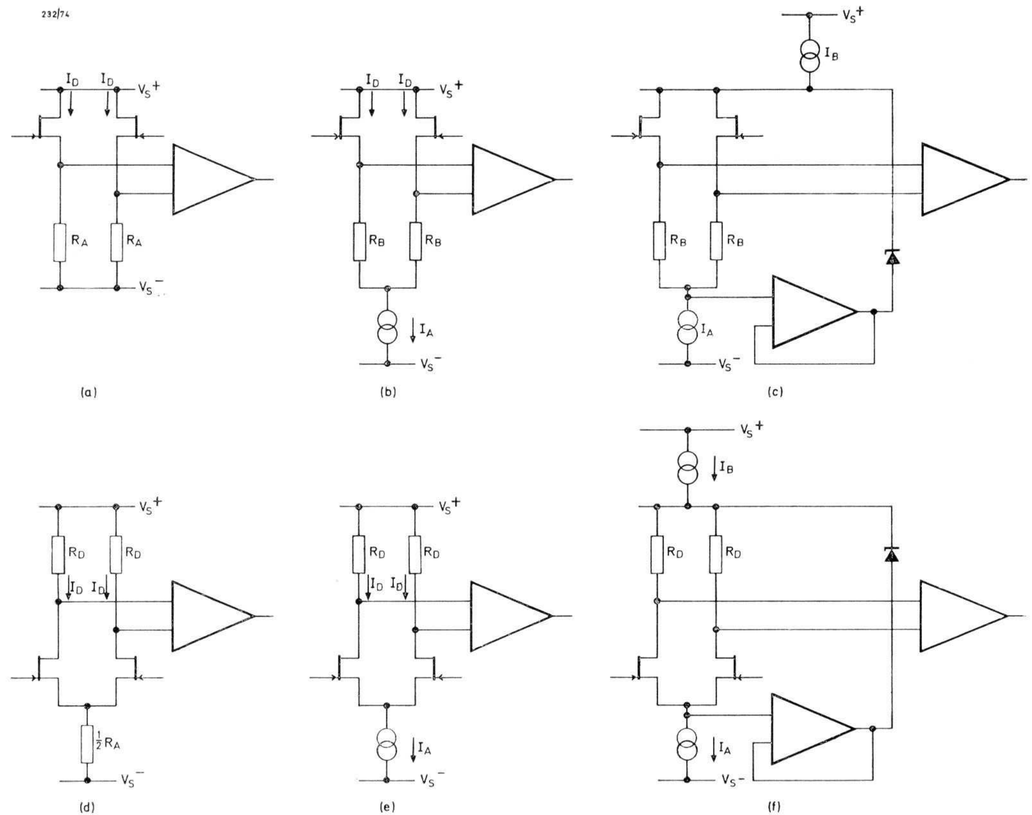


Fig.74 Basic circuit configurations of a FET-pair used as a differential input stage.

In Figs 74*a* and *d* the drain current is determined by resistors R_A:

$$I_D = \frac{V_{CM} - V_S^- - V_{GS}}{R_A}, \tag{44}$$

where V_{CM} is the input common mode voltage, and V_S^- the supply voltage on the negative rail. The drain-source voltage is equal to:

$$V_{DS} = V_S^+ - V_{CM} \text{ (see Fig. 74}a\text{)}, \tag{45}$$

or

$$V_{DS} = V_S^+ - V_{CM} - \frac{R_D}{R_A}(V_{CM} - V_S^- - V_{GS}) \text{ (see Fig. 74}d\text{)}. \tag{46}$$

The six circuit factors listed at the beginning of this subsection are derived from equations (44), (45) and (46):

$$\frac{\mathrm{d}I_D}{\mathrm{d}V_{CM}} = \frac{1}{R_A}; \quad \frac{\mathrm{d}I_D}{\mathrm{d}V_S^-} = -\frac{1}{R_A}; \quad \frac{\mathrm{d}I_D}{\mathrm{d}T} = -\frac{1}{R_A}\frac{\mathrm{d}V_{GS}}{\mathrm{d}T}.$$

In the case of Fig. 74*a*:

$$\frac{\mathrm{d}V_{DS}}{\mathrm{d}V_{CM}} = -1; \quad \frac{\mathrm{d}V_{DS}}{\mathrm{d}V_S^+} = 1; \quad \frac{\mathrm{d}V_{DS}}{\mathrm{d}T} = 0;$$

and in the case of Fig. 74*d*:

$$\frac{\mathrm{d}V_{DS}}{\mathrm{d}V_{CM}} = -1 - \frac{R_D}{R_A}; \quad \frac{\mathrm{d}V_{DS}}{\mathrm{d}V_S^-} = \frac{R_D}{R_A}; \quad \frac{\mathrm{d}V_{DS}}{\mathrm{d}T} = \frac{R_D}{R_A}\cdot\frac{\mathrm{d}V_{GS}}{\mathrm{d}T}.$$

To obtain $\mathrm{d}V_{GS}/\mathrm{d}T$, see equation (12).

The contribution of the FET-pair to the CMRR can be obtained via equation (41), the supply sensitivity via equation (42) and the thermal drift via equation (43).

CMRR

The CMRR and thermal drift are calculated as examples: suppose $I_D = 0.2$ mA, $R_A = 80$ kΩ and $R_D = 10$ kΩ. Referring to Table IV, Fig. 74*a*,

$$(\text{CMRR})^{-1} = \frac{20}{80}\times 10^{-3} + 0.5\times 10^{-3} = 0.75\times 10^{-3} \text{ or } 62.5 \text{ dB}.$$

Fig. 74*d*,

$$(\text{CMRR})^{-1} = \frac{20}{80} \times 10^{-3} + (1 + 1/8) \times 0.5 \times 10^{-3} = 0.81 \times 10^{-3} \text{ or } 62 \text{ dB}.$$

Both these values of CMRR are unacceptably low. A slight improvement of a few dB can be obtained by minimising $\mathrm{d}I_D/\mathrm{d}V_{CM}$ by means of current source $I_A = 2I_D$ (see Figs 74*b* and *e*), or by minimising $\mathrm{d}V_{DS}/\mathrm{d}V_{CM}$ by means of current source I_B, voltage source V_Z and a unity gain amplifier. However a much greater improvement (about 40 dB) can be obtained when both $\mathrm{d}I_D/\mathrm{d}V_{CM}$ and $\mathrm{d}V_{DS}/\mathrm{d}V_{CM}$ are minimised simultaneously (see Figs 74*c* and *f*).

Thermal drift

Since $\mathrm{d}I_D/\mathrm{d}T$ and $\mathrm{d}V_{DS}/\mathrm{d}T$ are very small ($g_{fs} \cdot R_A \gg 1$), $\mathrm{d}\Delta V_{GS}/\mathrm{d}T$ (equation (43)) reduces to $\partial\Delta V_{GS}/\partial T$ (equation (40)), so that $\mathrm{d}\Delta V_{GS}/\mathrm{d}T \approx \partial\Delta V_{GS}/\partial T =$ typically 20 μV/degC. Although CMRR and supply sensitivity are considerably improved in the circuits of Fig. 74*c* and *f*, thermal drift is not improved and can be even worse than in the simpler circuits. Therefore special attention has to be paid to the thermal stability of I_A, I_B and V_Z, to obtain low $\mathrm{d}I_D/\mathrm{d}T$ and $\mathrm{d}V_{DS}/\mathrm{d}T$.

Matching of other components

Apart from the circuit configuration, one has to pay attention to the contribution of the circuit components (drain resistors, source resistors, other biasing resistors, second stage) to the complete amplifier offset and its variations, which can be appreciable when the transconductance of the individual FETs is not high enough.

Resistors R_D in Figs 74*d*, *e* and *f*:
Inequality of these resistors causes an extra offset voltage equal to

$$\Delta V_{GS}' = \frac{\Delta I_D}{g_{fs}} \cdot \frac{\Delta R_D}{R_D},$$

in which $\Delta R_D = R_{D1} - R_{D2}$.

Furthermore, since $I_D \neq 0$, an extra drift term is introduced:

$$\frac{\mathrm{d}\Delta V_{GS}'}{\mathrm{d}T} = \frac{1}{\mu} \cdot \frac{\mathrm{d}\mu}{\mathrm{d}T} \cdot \frac{\Delta I_D}{g_{fs}} = \frac{1}{\mu} \cdot \frac{\mathrm{d}\mu}{\mathrm{d}T} \cdot \frac{I_D}{g_{fs}} \cdot \frac{\Delta R_D}{R_D}.$$

Another extra drift term is caused by the difference of the temperature coefficients $\Delta\alpha = \alpha_1 - \alpha_2$ of the resistors R_D:

$$\frac{\mathrm{d}\Delta V_{GS}''}{\mathrm{d}T} = \frac{1}{4} \cdot \frac{I_D}{g_{fs}} \cdot \Delta\alpha.$$

Let $I_D = 200$ μA; $g_{fs} = 1$ mA/V, $\Delta\alpha /= 50$ ppm/degC, $\Delta R_D/R_D = 1\%$, and

$$\frac{1}{\mu} \cdot \frac{\mathrm{d}\mu}{\mathrm{d}T} = -6 \times 10^{-3}/\mathrm{degC},$$

then $\Delta V_{GS}' = 2$ mV; $\mathrm{d}\Delta V_{GS}'/\mathrm{d}T = -12$ μV/degC; $\mathrm{d}\Delta V_{GS}''/\mathrm{d}T = 2.5$ μV/degC. Exactly the same calculation as was valid for R_D also holds for R_A and R_B in Figs 74*a*, *b* and *c*.

The common mode rejection is affected by inequality of the resistors R_A in Fig. 74*a*, thus:

$$\frac{\mathrm{d}\Delta V_{GS}}{\mathrm{d}V_{CM}} = \frac{1}{g_{fs} \cdot R_A} \cdot \frac{\Delta R_A}{R_A},$$

and amounts to 125 μV/V when $\Delta R_A/R_A = 10^{-2}$ and $g_{fs} \cdot R_A = 80$.

In Fig. 74*d*,

$$\frac{\mathrm{d}\Delta V_{GS}}{\mathrm{d}V_{CM}} = \frac{1}{g_{fs} \cdot R_A} \cdot \frac{\Delta R_D}{R_D}.$$

These contributions will disappear when the resistors R_A are replaced by current sources I_A.

The offset current of the output amplifier:

The offset current ΔI_D of the output amplifier causes the drain currents to differ, resulting in extra contributions to the offset and drift of the entire amplifier.

In the common source amplifier:

$$(\Delta V_{GS})_{CS}' = -\frac{I_{D1} - I_{D2}}{g_{fs}} = -\frac{\Delta I_D}{g_{fs}},$$

and in the common drain amplifier:

$$(\Delta V_{GS})_{CD}' = -\frac{I_{D1} - I_{D2}}{g_{fs}} = -\frac{\Delta I_D}{g_{fs}}.$$

Extra thermal drift terms arise since ΔI_D changes with temperature:

$$\left(\frac{\mathrm{d}\Delta V_{GS}}{\mathrm{d}T}\right)_{CS}' = -\left(\frac{\mathrm{d}\Delta V_{GS}}{\mathrm{d}T}\right)_{CD}' = -\frac{1}{g_{fs}} \cdot \frac{\mathrm{d}\Delta I_D}{\mathrm{d}T} = -\frac{\gamma}{g_{fs}} \cdot \Delta I_D,$$

in which $\gamma = -7 \times 10^{-3}$/degC.

Another extra drift term is caused by change of difference of the drain currents:

$$\left(\frac{\mathrm{d}\Delta V_{GS}}{\mathrm{d}T}\right)_{CS}'' = -\left(\frac{\mathrm{d}\Delta V_{GS}}{\mathrm{d}T}\right)_{CD}'' = \frac{1}{\mu} \cdot \frac{\mathrm{d}\mu}{\mathrm{d}T} \cdot \frac{\Delta I_D}{g_{fs}}.$$

Since $(1/\mu) \cdot (\mathrm{d}\mu/\mathrm{d}T) \approx \gamma$, the extra drift terms partially compensate for each other, in common drain and common source configurations.
If

$$g_{fs} = 1 \text{ mA/V}, \ \Delta I_D = 100 \ n\text{A}, \ \frac{1}{\mu} \cdot \frac{\mathrm{d}\mu}{\mathrm{d}T} = -6 \times 10^{-3}/\text{degC},$$

then

$$\left|\frac{\mathrm{d}\Delta V_{GS}}{\mathrm{d}T}\right|' = 7 \ \mu\text{V/degC}$$

and

$$\left|\frac{\mathrm{d}\Delta V_{GS}}{\mathrm{d}T}\right|'' = 6 \ \mu\text{V/degC}.$$

The input current and the offset voltage of the output amplifier also cause extra offset and drift of the entire amplifier, but may be neglected in practical cases.

Worked examples of FET- input operational amplifiers

Fig. 75 shows a simple operational amplifier similar to that of Fig. 74*a*. The offset voltage of the amplifier is balanced out by means of potentiometer R_6. Resistor R_{10} is required only if the amplifier is capacitively loaded.

The values of frequency compensation components R_9, C_1 and C_2 have been chosen to give unconditional stability for all values of closed loop gain down to unity.

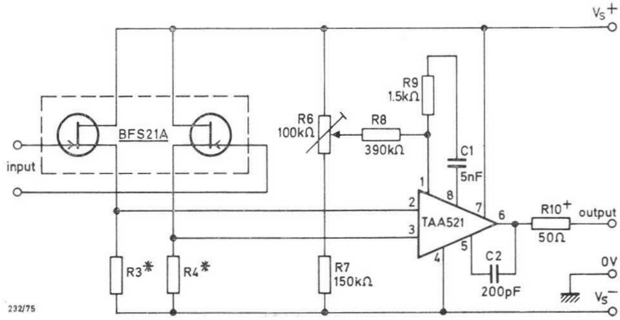


Fig.75 Practical circuit for a FET pair used as a differential input stage for an operational amplifier. For $V_S = \pm 9$ V, $R_3 = R_4 = 47$ kΩ $\pm 1\%$. For $V_S = \pm 15$ V, $R_3 = R_4 = 82$ kΩ $\pm 1\%$.

Fig. 76 shows a more complicated circuit, similar to Fig. 74*f*, where discrete components are used for high bandwidth and slew rate. Frequency compensation for unconditional stability for all values of closed loop gain down to unity is achieved by resistor R_C and capacitor C_C between the drains. The offset voltage of the amplifier is balanced out by means of potentiometer R_P.

The drain current is stabilized by means of current source $TR_3 - TR_4 - TR_5$, which has small output conductance (current mirror configuration), small supply sensitivity (biasing by means of voltage regulator diode D_1), and small temperature coefficient (D_1 and D_2 compensate for each others temperature coefficients).

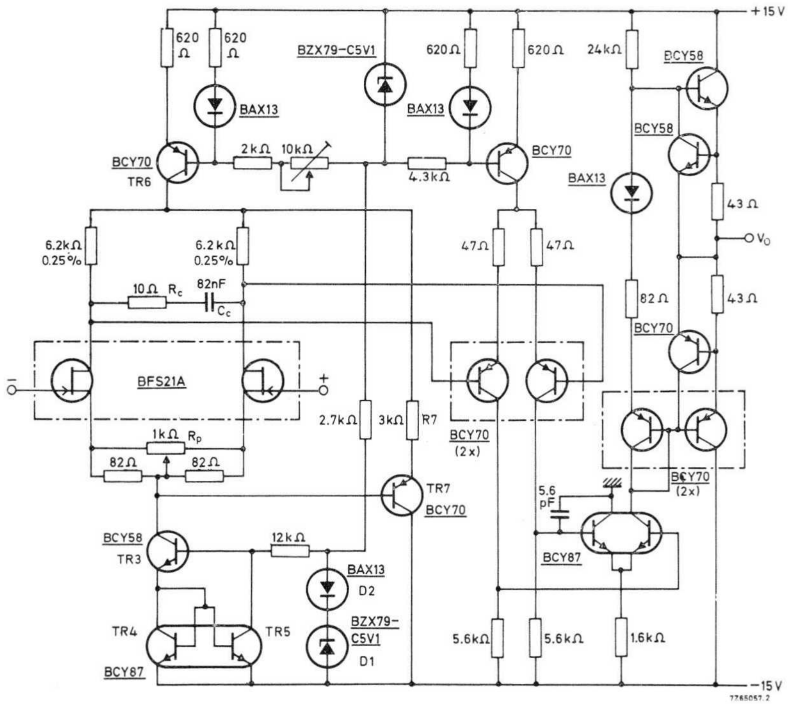


Fig.76 Circuit diagram of a high CMRR operational amplifier.

Current source TR_6 supplies the FET-pair and transistor TR_7. Thus the current through resistor R_7 and hence the drain-source voltage of the FET-pair is stabilized. Transistor TR_7 ensures that the collector current of TR_3 flows through the FET-pair.

The second and third stages are conventional differential stages. The output stages are of the push-pull type with quiescent current stabilisation and overload protection.

Data for both amplifiers are given in Table V.

Table V. Comparison of data for amplifiers in Figs 75 and 76.

	Fig. 75	Fig. 76
voltage gain	$>$ 80 dB	$>$ 90 dB
unity gain bandwidth	$>$ 0.5 MHz	$>$ 3 MHz
slew rate	—	$>$ 8 V/μs
differential input impedance	$> 10^{11}$ Ω//4 pF	$> 10^{11}$ Ω in parallel with 4 pF
common mode input impedance	$> 10^{11}$ Ω//4 pF	$> 10^{11}$ Ω in parallel with 4 pF
offset voltage (initial) typical	5 mV, adjustable	5 mV, adjustable
thermal drift, typical	20 μV/degC	20 μV/degC
common mode rejection ratio	$>$ 60 dB	$>$ 100 dB ($-10\ \mathrm{V} \leqslant V_{CM} \leqslant 10\ \mathrm{V}$)
supply sensitivity	$<$ 1 mV/V	$<$ 100 μV/V
time drift of offset voltage	$<$ 50 μV/month	$<$ 50 μV/month
common mode voltage range	$\pm$ 7 V	$\pm$ 10 V
output voltage	$\pm$ 10 V	$\pm$ 10 V
output current	$\pm$ 5 mA	$\pm$ 10 mA
the output is short circuit proof	no	yes

5.3.9 The FET as a voltage-controlled resistor

Fig. 77 shows the output characteristics of a junction FET or a MOS-FET for relatively small positive and negative values of V_{DS} in the pre-pinch off region ($V_{DS} < V_{GS} - V_P$). It can be seen that all the characteristics pass through the origin (no offset) and are symmetrical and relatively linear. This means that the FET can be used as a variable resistance in such devices as a voltage-controlled (remotely) attenuator, an analogue multiplier, an amplitude modulator, or a bandwidth controlled filter.

From equation (6), the drain source resistance (see Fig. 78) is given by:

$$r_{ds} = \frac{V_P{}^2}{2I_{DSS}} \cdot \frac{1}{V_{GS} - V_P - V_{DS}}. \tag{47}$$

This means that r_{ds} is a non-linear resistance because of its dependence on V_{DS}.

For large V_{DS} signals, the linearity can be improved appreciably by means of feedback from the drain to the gate as shown in Fig. 79. Equal resistances R_1 and R_2 are used to make

$$V_{GS} = \tfrac{1}{2}(V_{contr} + V_{DS}). \tag{48}$$

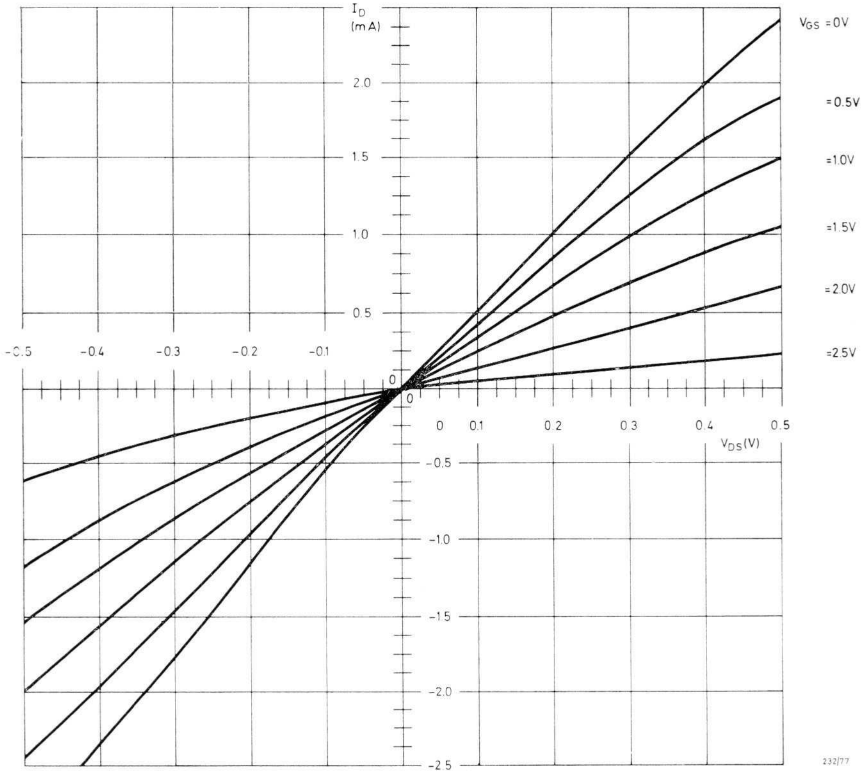


Fig.77 Characteristics of a FET as a symmetrical voltage-controlled resistor.

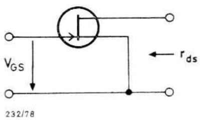


Fig.78 Circuit illustrating the drain source resistance r_{ds}.

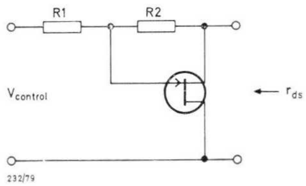


Fig.79 Linearization of r_{ds} by means of feedback.

this equation, in combination with that for I_D gives:

$$I_D = I_{DSS}\left\{\frac{2V_{DS}}{-V_P}\left(1-\frac{V_{GS}}{V_P}\right)-\left(\frac{V_{DS}}{V_P}\right)^2\right\} \tag{49}$$

$$= I_{DSS}\cdot\frac{V_{DS}}{-V_P}\left(2+\frac{V_{contr}}{-V_P}\right). \tag{50}$$

Consequently, I_D is directly proportional to V_{DS}, which means that r_{ds} is constant.

In practice, equation (49) deviates to some extent, which means that r_{ds} will still show some non-linearity. In Table VI, the influence of feedback on three FETs is shown. This has been determined by measuring the harmonic content of the drain current with a sinewave drain voltage ($\hat{V}_{ds} = 0.1$ V, $f = 1$ kHz). The characteristics of the devices ranged from high values to low values of I_{DSS} and V_P:

FET 1 high values,
FET 2 medium values,
FET 3 low values,

It can be seen from Table VI that for a reasonably linear characteristic, feedback is essential and that high values of I_{DSS} and V_P are preferred. The tabel is valid for junction FETs as well as for MOS-FETs. For junction FETs, we should take into account that the non-linearity increases appreciably when V_{GS} becomes positive (forward current through gate-channel diode). For MOS-FETs, the substrate-drain diode must not be biased in the forward direction. This can be prevented by making the substrate several volts negative.

Table VI. Harmonic Distortion Measurements ($\hat{V}_{ds} = 0.1$ V)

		FET 1		FET 2		FET 3	
		distortion (%)		distortion (%)		distortion)%)	
		2nd harmonic	3rd harmonic	2nd harmonic	3rd harmonic	2nd harmonic	3rd harmonic
without	$r_{ds\ on}$	0.1	0.2	0.2	0.2	0.9	0.8
feedback	$10 \times r_{ds\ on}$	10	2	12	2	16	1.5
with	$r_{ds\ on}$	0.1	0.2	0.1	0.1	0.2	0.2
feedback	$10 \times r_{ds\ on}$	0.2	0.7	0.5	1	4	0.5

[1]) $r_{ds\ on}$ is the resistance at $V_{contr} = 0$.

5.3.10 RF APPLICATIONS OF FETS IN COMMUNICATIONS RECEIVERS

The junction FET is now widely used in the r.f. stages of h.f., v.h.f. and u.h.f. receivers, since it offers superior performance in terms of two increasingly critical factors, cross-modulation and intermodulation. It also has noise properties equal to bipolar transistors. Cross-modulation is the transfer of the modulation on one carrier to the carrier of another signal. Intermodulation occurs when two or more interfering off-tune signals mix to produce a signal within the receiver passband. Both of these effects are caused by non-linearity in the transfer characteristic of the active device, their degree depending on the third and higher odd terms in the transfer characteristic for an amplifier, and the fourth and higher even terms for a mixer. Clearly, if the active device had a perfectly square-law characteristic neither effect would occur, but both bipolar transistors and FETs have higher order terms in their characteristics. The FET, however, is superior to the bipolar transistor in this respect. For example, taking impedance differences into account, a 12 dB improvement in cross-modulation in a narrow-band f.m. system, and a 20 dB improvement in a v.h.f. broadcast receiver, can be achieved by replacing a bipolar mixer by a FET.

Table VII compares the noise performance of FETs and bipolar transistors in various circuit configurations.

Circuit configurations

The cross-modulation and intermodulation performance of a circuit are functions of the interfering signal voltage level. In the common-source configuration, the voltage level of any interfering signal is stepped-up by the matching transformer necessitated by a high input resistance. The input resistance in the common-gate configuration is low so that for the same power input the interfering signal voltage level appearing at the input part of the device is higher for the common-source configuration. Thus, cross-modulation and intermodulation occur at lower levels in a common-source amplifier and, for best performance, the common-gate circuit is preferred. This argument also applies to mixer circuits, where the input signal should be applied to the source and the local oscillator output to the gate for best results.

The most superior gain and noise figures are shown in Table VII to be obtained from a neutralised common-source amplifier. However, since the

Table VII. Noise performance at r.f.

frequency	device	configuration	R_S	source reactance	R_i (approx.)	neutralising	NF	gain
100 MHz	FET	common-source	1 kΩ	tuned	20 kΩ	yes	2 dB	18 dB
		common-gate	200 Ω	tuned	200 Ω	no	4 dB	12 dB
		cascode	1 kΩ	tuned	3 kΩ	no	3 dB	17.5 dB
	bipolar	common-base	100 Ω	opt. C	20 Ω	no	2 dB	15 dB
		common-base	20 Ω	tuned	20 Ω	no	3 dB	17 dB
470 MHz	FET	common-source	1 kΩ	tuned	1 kΩ	yes	4 dB	12 dB
		common-gate	67 Ω	opt. C	140 Ω	no	4.5 dB	11 dB
		common-gate	67 Ω	tuned	140 Ω	no	5.5 dB	10 dB
	bipolar	common-base	66 Ω	opt. C	50 Ω	no	4.2 dB	12 dB
		common-base	50 Ω	tuned	50 Ω	no	5 dB	15 dB
		common-emitter	50 Ω	tuned	70 Ω	no	5 dB	20 dB

values of feedback capacitance and input impedance are high, neutralisation is needed to maintain stability. Otherwise, the load impedance, and consequently the gain, must be low. The common-gate amplifier, on the other hand, has low feedback capacitance and gives stable gain well into the u.h.f. band. Clearly, the choice of configuration must depend on the relative emphasis placed on cross-modulation and intermodulation, noise and gain in each application.

A third possibility is also available. This is the cascode circuit which provides a compromise between the good noise performance of the common-source circuit and the good stability of the common-gate circuit. The load of the common-source stage is the input impedance of the common-gate stage (about 200 Ω at 200 MHz), giving stability without neutralisation but still requiring extreme care in construction because the stability factor is not high.

Biasing arrangements

If a negative line or a high-voltage positive line is available, either a source resistance or constant current source can be used for biasing. It is important to appreciate the effect of a wide spread in I_{DSS} values on bias arrangement; the device should not be biased at $V_{GS} = 0$ V because the current with high $-I_{DSS}$ devices would be unacceptably large. Normally, the device is operated at a value of V_{GS} equal to half the pinch-off voltage V_P. In the mixer, a bias voltage of $V_P/2$ is used because this value results in a minimum for the fourth order term in the transfer characteristic and, therefore, minimum cross-modulation and intermodulation. It should be remembered that the peak local oscillator amplitude should not exceed $V_P/2$, otherwise non-linearities increase and eventually the gate-source junction is driven into conduction.

A disadvantage of the cascode circuit is the large h.t. supply needed to drive both devices into the saturation region.

Practical circuits

Amplifiers

Figs 80 to 82 show three r.f. amplifier circuits using BFW11 FETs in the common-source, common-gate and cascode configurations.

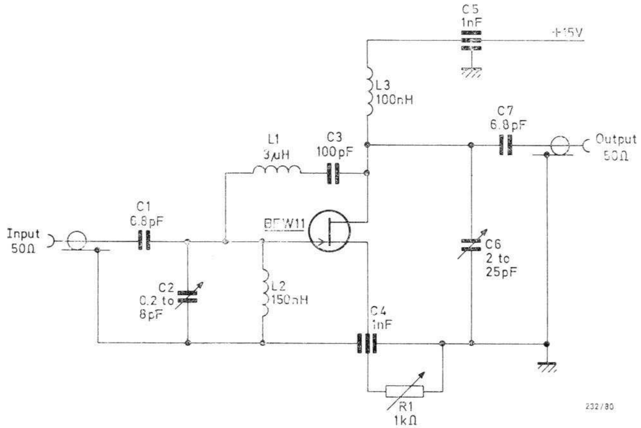


Fig.80 100 MHz common-source amplifier.

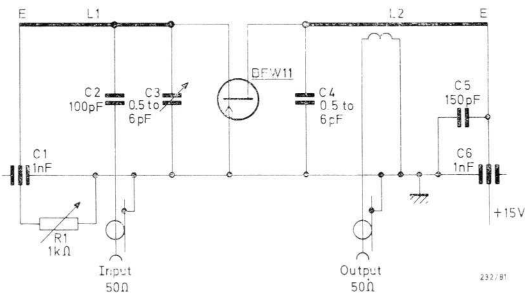


Fig.81 470 MHz common-gate amplifier. L_1 = 6 cm of 1/4 in o/d Cu, tap at 4 cm from E; L_2 = 7 cm of 1/4 in o/d Cu, tap at 4 cm from E. Characteristic impedance of line = 70 Ω.

For a 100 MHz neutralised common-source amplifier (Fig. 80) fed from an optimum source resistance of 1 kΩ, a noise figure of 2 dB is typical. A similar amplifier designed for 470 MHz operation would give a noise figure of 4 dB. The common-gate amplifier of Fig. 81 gives less gain than the previous circuit and slightly inferior noise performance. For the 470 MHz amplifier shown, the noise figure is typically 5.5 dB and the power gain 11 dB. By off-tuning the input slightly the noise figure may be improved to 4.5 dB, but this is not a practical solution in a tuned amplifier. Fig. 82 shows a 100 MHz cascode circuit with a typical noise figure of 3 dB. The two devices should be selected for similar values of I_{DSS}.

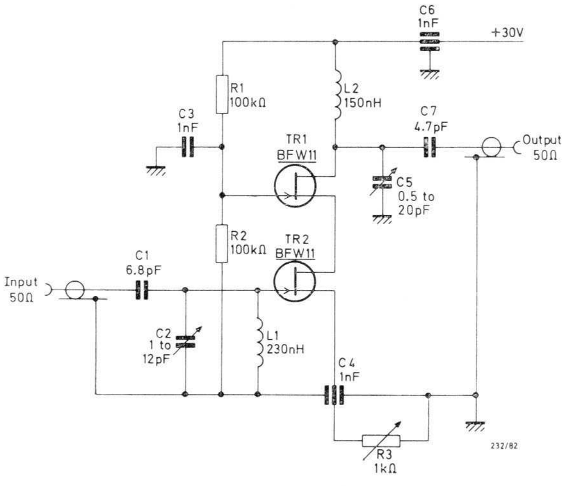


Fig.82 100 MHz cascode amplifier.

Mixers

A mixer circuit is shown in Fig. 83. The FET is biased at $V_{GS} = V_P/2$ and, again, careful circuit design is necessary to allow for a spread in values of I_{DSS}. With no oscillator drive I_D is set to 2 mA.

The input signal is applied to the source and the local oscillator signal to the gate. With this arrangement a noise figure of 9 dB is typical. A capacitively-tuned $\lambda/4$ transmission line is used as the tuning element for signal and local oscillator inputs. When using FETs in mixer circuits the limiting factor in the conversion gain is often the dynamic impedance of the coil in the output circuit. In this design, the value is 25 kΩ, giving an unloaded Q of 75 at 30 MHz. The conversion gain and signal blocking characteristics of the circuit are given in Figs 84 and 85, respectively.

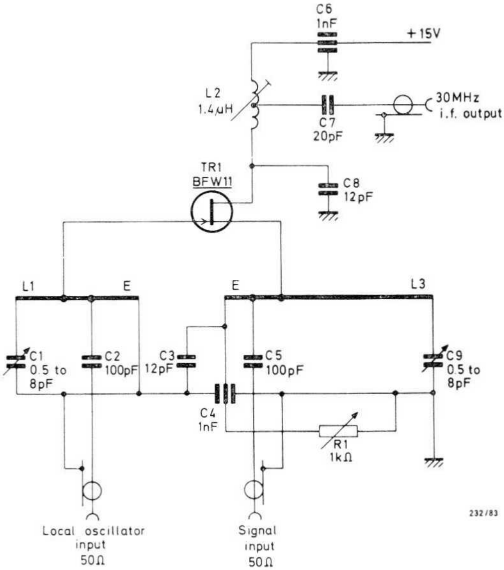


Fig.83 Mixer circuit. L_1 = 8.5 cm of 1/4 in o/d Cu, gate tap at 2.6 cm from E, l.o. input at 1.5 cm from E; L_3 = 8.5 cm of 1/4 in o/d Cu, signal input tap at 0.9 cm from E, source at 1.7 cm from E. Characteristic impedance of line = 70 Ω.

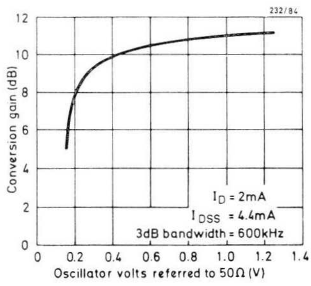


Fig.84 Conversion gain as a function of oscillator volts.

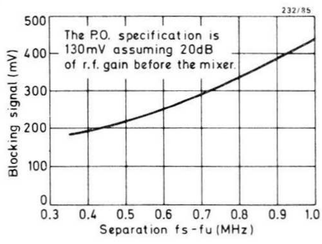


Fig.85 Blocking signal as a function of frequency separation.

5.4 Typical applications of MOS field-effect transistors

5.4.1 Chopper-stabilized d.c. amplifier with an n-channel BSV81 MOS-FET low-level chopper

A very small d.c. voltage E_i has first to be amplified to a much higher voltage V_o before it can be measured. The amplifier, however, has an offset voltage V_{of} which will affect the accuracy of measurement. The influence of V_{of} on V_o can be expressed in the formula

$$V_o = G_v\,(E_i + V_{of}),$$

G_v being the voltage gain. The formula shows that V_{of} is thought to be present at the input of the amplifier. V_{of} can be split up into an offset e.m.f. E_{of} and an offset current I_{of} times the internal resistance R_s of the generator (see Fig. 86), so

$$V_{of} = E_{of} + I_{of} \cdot R_s.\text{*)}$$

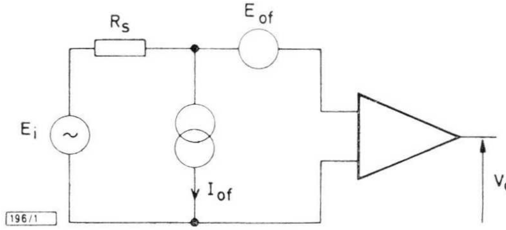


Fig.86 Equivalent circuit of the amplifier input.

The amplifier to be used can be chosen from two main groups of amplifier: d.c.-coupled amplifiers (bipolar and FET operational amplifiers) and parametric amplifiers (dielectric and chopper-stabilized d.c. amplifiers). The E_{of} of the last group is about one hundredth, its I_{of} about one tenth to one thousandth of the E_{of} and I_{of} of the first group. Moreover the temperature drift of E_{of} and I_{of}

*) The I_{of} used in this formula is given at the end of sub-section 5.4.1 and includes the change of E_{of} (measured at $R_s = 0$) with a changing R_s. Therefore this I_{of} differs from I_{of} that actually flows through R_i.

is much lower for the last group. This makes amplifiers of the last group more suitable for the purpose mentioned above especially as chopper-stabilized d.c. amplifiers are easy to realise.

Generally a chopper-stabilized d.c. amplifier comprises five stages plus an oscillator, the type of which is irrelevant. The stages are shown in Fig. 87 in which stage 1 is the chopper, an on-off device converting a d.c. voltage into a square wave voltage of half the amplitude of the d.c. voltage. Stage 2 is the a.c. amplifier for amplifying the square wave voltage. It is decoupled for d.c. by connecting it to stage 1 and stage 3 by means of capacitors. Stage 3, the demodulator, converts the amplified square wave voltage into a d.c. voltage which is proportional to E_i. It preferably consists of an on-off device which is operated in synchronism with the chopper (one oscillator driving stages 1 and 3). This has the advantage that the polarity of the d.c. output is determined by that of E_i so that overall feedback can be applied. Stage 4 is a low-pass filter for removing the chopping frequency and its harmonics. Stage 5 is a d.c. amplifier for transforming the output of the demodulator (low-pass filter) from a high to a low impedance.

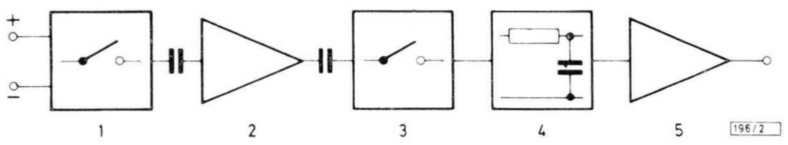


Fig.87 Block diagram of a chopper-stabilized amplifier.

There are various versions of choppers. One of them, the photo chopper, is rather expensive and only of use at low chopping frequencies; a fact which limits the frequency of the signal to be amplified. When FETs are used in choppers they have the drawback of too large a drain-to-gate capacitance. Likewise, bipolar transistors have too large an emitter-to-base capacitance. Both capacitances introduce voltage spikes into the a.c. amplifier. Moreover, bipolar transistors introduce an offset voltage due to their non-zero emitter-collector voltage when conducting. However, the BSV81 MOS-FET has a drain-to-gate capacitance of less than 0.5 pF. Also, a MOS-FET has no static offset-voltage, and a very small gate leakage current, and hence this device is inherently suitable.

The reason why minimisation of the voltage spikes is so important is that, apart from an offset voltage of the d.c. amplifier, they are the only reason for an offset voltage in chopper-stabilized d.c. amplifiers. V_{of} is partly caused by an offset current I_{of} flowing through the signal source. I_{of} originates from the fact that the sum of the charges, injected via the gate-to-channel capacitance of a MOS-FET into the signal carrying circuit during turning on and turning off, is not zero. The remaining part E_{of} of V_{of} is caused by the voltage spikes at the input of the a.c. amplifier. The spikes represent a chopped a.c. signal which is amplified by the a.c. amplifier, demodulated and integrated. The resulting d.c. voltage at the output of the d.c. amplifier can be transferred to E_{of} by dividing the d.c. voltage by the open loop voltage gain of the chopper-stabilized amplifier (see Fig. 87). (Here E_{of} and I_{of} both are functions of R_s.)

Another reason why voltage spikes should be reduced as far as possible is that they may bottom the last stages of the a.c. amplifier which causes an extra drift component in E_{of}. Bottoming has to be prevented by means of a smoothing network such as the integrating capacitor in the feedback path of the first operational amplifier of the a.c. amplifier (C_{11} and C_{12}) in Fig. 88.

Fig. 88 shows the complete chopper-stabilized d.c. amplifier. The chopper includes two BSV81 MOS-FETS (TR_1 and TR_2) which are driven by square wave voltages on their gates in such a way that when TR_1 is on, TR_2 is off, and vice versa. The source of TR_1 is the non-inverting amplifier input and that of TR_2 the inverting input which is used for overall feedback. The drain-source resistance of a BSV81 is less than 100 Ω for the on state and more than 1 GΩ for the off state at a gate-to-source voltage of 0 V and −6 V respectively. The chopper transforms any d.c. input voltage to an a.c. voltage with an amplitude of half the d.c. voltage. This is only true when $R_iC_8 \gg 1/f_c$ and $C_8 \gg C_i$ (R_i is the input resistance and C_i the input capacitance of the a.c. amplifier; f_c is the chopping frequency). For an off-time that is equal to the on-time and for $C_i \ll C_8$ and $f_cC_8R_i \gg 1$, the input impedance R_{in} of the chopper-stabilized d.c. amplifier is determined by the input impedance of the a.c. amplifier as follows:

$$\frac{1}{R_{in}} = \frac{1}{4R_i} + C_i f_c.$$

For $R_i = 1$ MΩ, $C_i = 10$ pF, $C_8 = 100$ nF and $f_c = 1$ kHz, R_{in} will be about

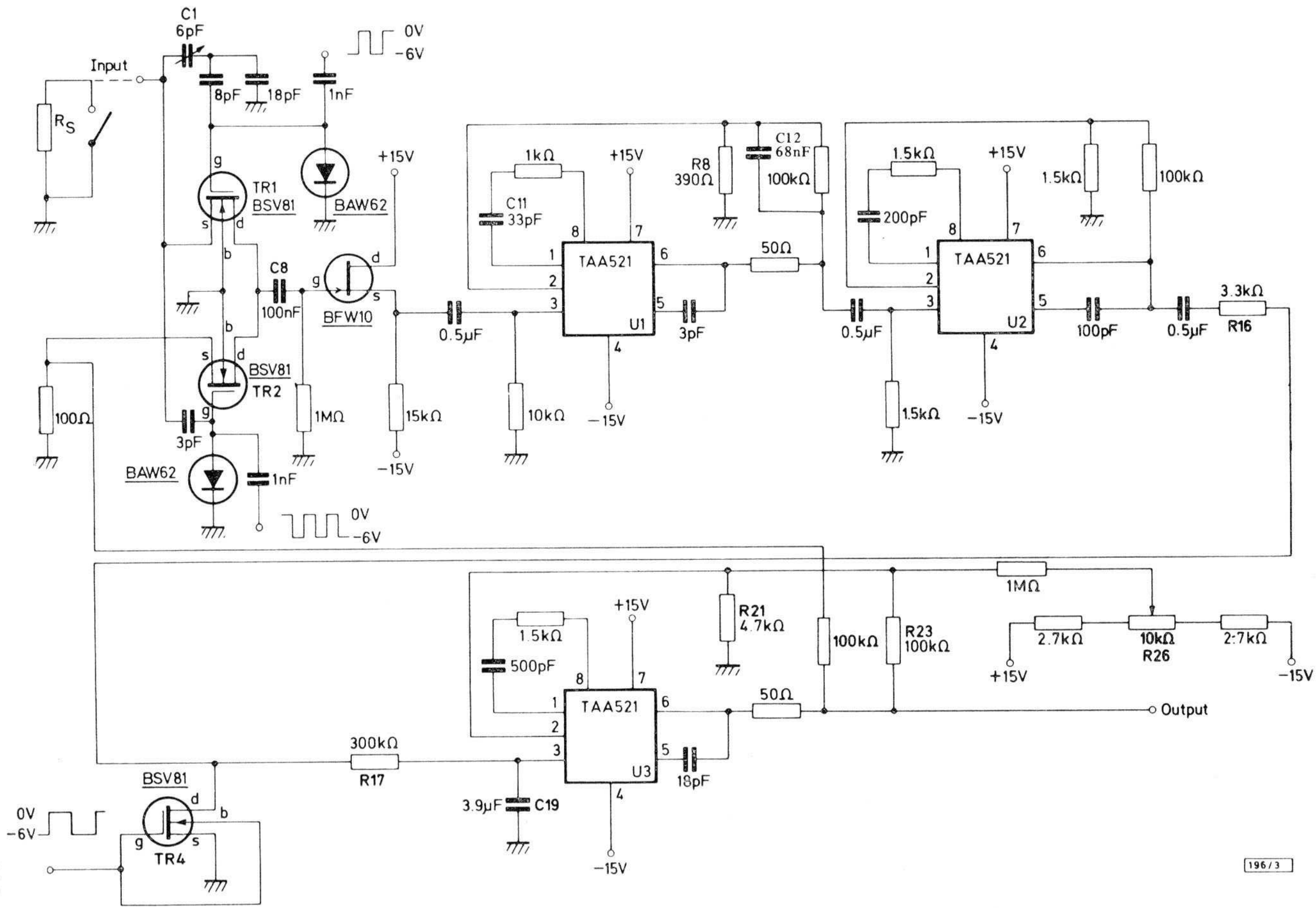


Fig.88 Circuit diagram of a chopper-stabilized amplifier.

4 MΩ. This high R_{in} could be obtained by using a FET source follower as the a.c. input stage (high R_i in combination with low noise).

Since the source impedance (preceding low-pass filter) of the d.c. amplifier is high, the offset voltage and the thermal drift of the d.c. amplifier is also rather high (approximately 50 mV and 500 μV/degC). Since the contribution to E_{of} of the chopper-stabilized d.c. amplifier is found by dividing the total offset voltage of the d.c. amplifier by the total gain of the preceding stages, this gain should be as high as possible. In our case this gain is $\frac{1}{2}$ (chopper) times 250 (first a.c. stage) times 60 (second a.c. stage) times 0.67 (demodulator) or 5000 times, making the contribution of the offset voltage of the d.c. amplifier to E_{of} about 10 μV and to the thermal drift of E_{of} about 100 nV/degC.

An a.c. coupling is used between U_1 and U_2 to reject low frequency noise originating from the stages preceding U_2.

The BSV81 MOS-FET demodulator (TR_4) is driven in phase with TR_1. Its dynamic range is +10 V to −5 V, provided the substrate is connected to the gate. The negative limit is confined by the chosen minimum gate voltage of −5 V and by the substrate-drain diode (an n-channel MOS-FET has a p-substrate); the positive limit by the repetitive peak gate-to-all-other-terminals voltage. R_{16} protects TR_4 against too high a drain current caused by a suddenly rising output level of the a.c. amplifier.

The low-pass filter R_{17}, C_{19} that smoothes the 1 kHz ripple of the demodulator output is also intended to shape the frequency characteristic of the complete chopper-stabilized d.c. amplifier. Its RC-time is 1.2 s which means that its −3 dB point lies at 0.13 Hz and its roll-off is 6 dB/octave up to 300 Hz (approximately one third of the chopping frequency f_c).

To set the open-loop voltage gain and the output impedance of the chopper-stabilized d.c. amplifier at the chosen values of 10^5 (100 dB) and 0.1 Ω respectively, a voltage gain of 20 has been chosen for the d.c. amplifier (by an appropriate choice of feedback resistors R_{21} and R_{23}). The 6 dB/octave roll-off extends from 0.13 Hz to about 300 Hz at which frequency the open-loop voltage gain is 33 dB. At higher frequencies the roll-off increases as the chopping frequency is approached. No instability phenomena will set in, provided the overall feedback does not cause the closed-loop voltage gain to drop below 33 dB. A safe value for this gain is 39 dB which makes the feedback-factor $39 - 100 = -61$ dB or less than 0.1% of the open-loop voltage gain.

The offset is minimised as follows. To minimise I_{of}, capacitor C_1 is adjusted for an equal offset voltage V_{of} at two different signal-source impedances, namely $R_s = 10$ kΩ and $R_s = 0$ Ω (see Fig. 88). The offset voltage V_{of} is further reduced as far as possible by adjusting R_{26} with which a compensating offset voltage of some tens of millivolts is introduced at the input of the d.c. amplifier.

The drift of the offset e.m.f. and current is determined by the temperature coefficient of the mobility of the majority carriers in the channel, by the drift of the threshold voltage of the MOS-FETs and, to a small extent, by the d.c. amplifier.

The measured E_{of} and I_{of} and their drifts of the adjusted chopper-stabilized d.c. amplifier are:

$$E_{of} < 10\ \mu V;\quad \text{drift of } E_{of} \approx 50\ \text{nV/degC},$$

$$I_{of} < 100\ \text{pA};\quad \text{drift of } I_{of} \approx 1.2\ \text{pA/degC}.$$

5.4.2 Multivibrator with long pulse duration

Due to their high input impedance, MOS-FETs can give large time constants. In the multivibrator shown in Fig. 89, the MOS transistor BFR29 permits the use of 68 MΩ resistors which, in combination with 1 μF capacitors, give square waves having a period of 2 minutes.

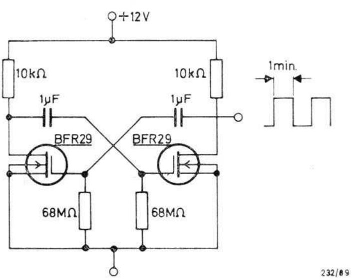


Fig.89 Multivibrator with long pulse duration.

5.4.3 4 W AMPLIFIER WITH THE INTEGRATED CIRCUIT TAA320

The TAA320 is a monolithic integrated circuit comprising three components: a MOS transistor of the p-channel enhancement type, an n-p-n silicon transistor and a resistor. The circuit, shown schematically in Fig. 90, is mounted in a TO-18 envelope. The biasing resistor R adjusts the operating current (I_S) of the MOS transistor. Since its transconductance is proportional to $\sqrt{I_S}$, resistor R must be as small as possible to obtain maximum gain; on the other hand a low value reduces amplification of the silicon transistor. A value of about 1 kΩ gives optimum overall transconductance of the whole integrated circuit. The TAA320 has advantages in that it combines a high transconductance (g_{fs}) with a high input impedance and a low noise level.

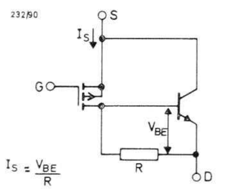


Fig.90 Electrical circuit of the TAA320.

Fig. 91 shows the circuit of a 4 W amplifier with a transformerless class-A push-pull output stage. The two BD115 output transistors are in series for d.c. voltages; a supply voltage of 200 V is thus required. The quiescent current flowing through these two transistors is about 50 mA. The a.c. control voltage for output transistor TR_2 is provided by the voltage drop of the collector current of TR_1 across the resistor R_9, and is fed to the base of TR_2 via capacitor C_3. The base signal of TR_2 is thus in anti-phase with the base signal of TR_1, as is required for the push-pull operation. As the collector current of TR_1 increases, that of TR_2 decreases (and *vice-versa*). The amplitude of the loudspeaker current (about 100 mA at full load) is double the collector-current amplitude of TR_1 or TR_2.

The resistor R_4 gives a.c. feedback from the output to the source resistor R_5. The input resistance (1 MΩ) is determined by the gate resistor R_1. Resistor R_2 makes the quiescent current of the TAA320 practically independent of the manufacturing spread of the pinch-off voltage.

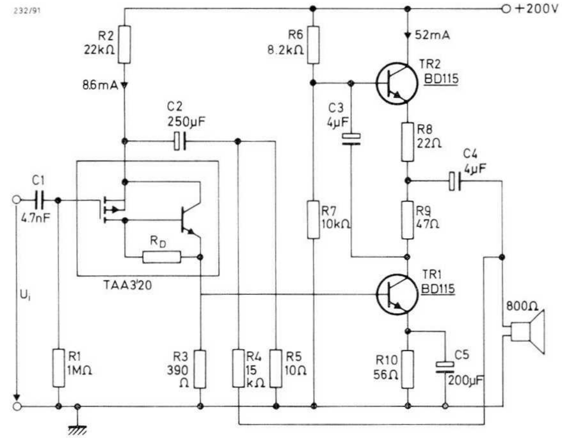


Fig.91 Circuit of a 4 W amplifier for a crystal pick-up input using the integrated circuit TAA320 and a transformerless push-pull class-A output stage.

The equivalent wide-band noise voltage (50 Hz to 15 kHz) referred to the input is 25 µV on the average. This gives a signal-to-noise ratio of 67 dB at an output voltage $V_{i(rms)} = 67$ mV ($P_o = 4$ W). The frequency range of the circuit extends from 50 Hz to 20 kHz. The distortion factor is given as a function of the output power in Fig. 92. Table VIII summarises typical data of the circuit of Fig. 91.

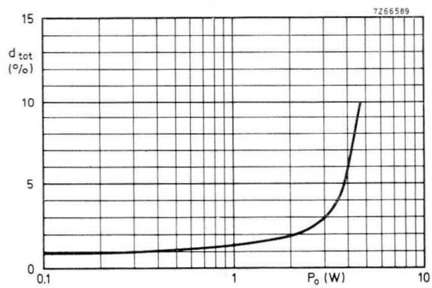


Fig.92 Distortion factor of the circuit of Fig. 91.

Table VIII. Typical characteristics of the amplifier of Fig. 91.

	lower-limit devices	typical	upper limit devices	unit
v_i (for $P_o = 50$ mW)	11	7.5	5.7	mV
v_i (for $P_o = 4$ W)	100	67	52	mV
I_C (of BD115s)	47	52	57	mA
I_D (of TAA320)	8.4	8.6	8.7	mA
$P_{o\ max}$ ($d_{tot} = 10\%$)	3.9	4.5	5	W
S/N ratio (at $v_i = 100$ mV)	—	72	—	dB
Feedback	8	12	20	dB

The frequency characteristic is flat from 50 Hz to above 20 kHz.

5.4.4 BFS28 MOS TETRODE TRANSISTOR AS AN AMPLIFIER, MIXER AND OSCILLATOR

The transfer characteristic of the MOS transistor closely follows a quadratic form, and this fact makes the MOS transistor particularly suitable for use in front end of communication receivers. The quadratic characteristic gives the MOS transistor superior performance in cross-modulation, intermodulation and blocking, when compared with bipolar transistors used in similar applications. The reason for this is that such distortion is generated mainly by the third order and higher odd order terms in the characteristic of any type of amplifier, or the fourth order and higher even order terms in a mixer. These third and higher orders in the MOS characteristic are very small.

The BFS28 is an n-channel dual-gate MOS transistor which is extremely stable at high frequencies. It possesses all the main requirements for u.h.f. amplification and mixing: in addition to its excellent cross-modulation, intermodulation and blocking performance, it also has a good conversion gain and a good noise figure.

BFS28 as an amplifier at 200 MHz

Measurements have been performed using a test amplifier operating at 200 MHz. The nominal d.c. setting was $V_D = 17$ V, $I_D = 10$ mA and $V_{G2} = +8$ V. The circuit is shown in Fig. 93.

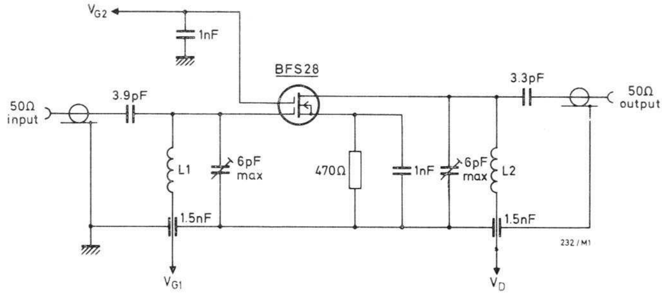


Fig.93 200 MHz amplifier.
L_1 = 2 turns of 18 s.w.g. wire (1.22 mm dia.), length 2 mm, i.d. 8 mm
L_2 = 2 turns of silvered 20 s.w.g. (0.914 mm dia.), wire length 20 mm, i.d. 14 mm.

The figures in table IX indicate the performance obtained with this circuit compared with a bipolar transistor BF200 used in a similar type of circuit.

Table IX

type	gain (dB)	noise figure (dB)
BFS28	18.0	3.9
BF200	16.0	5.1

Gain

Full gain control was obtainable with a change of voltage of V_{G2S} from +8 to −8 V. A comparison of Fig. 94 with Fig. 95 shows that the gain is some 2 dB higher than with the BF200 bipolar transistor.

Noise figure

The noise figure of the BFS28 is slightly better than that of the bipolar transistor (see Figs 94 and 95).

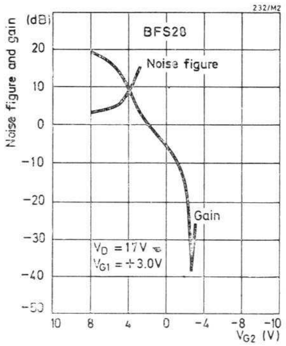


Fig.94 Noise figure and gain versus gate voltage for BFS28.

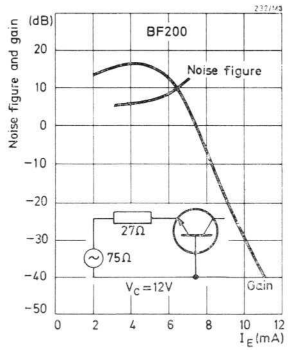


Fig.95 Noise figure and gain versus emitter current for BF200, plotted for comparison with Fig. 94.

Cross-modulation

The cross-modulation performance of the BFS28 is better, by a factor of about five, than the cross-modulation of the bipolar transistor (see Fig. 96).

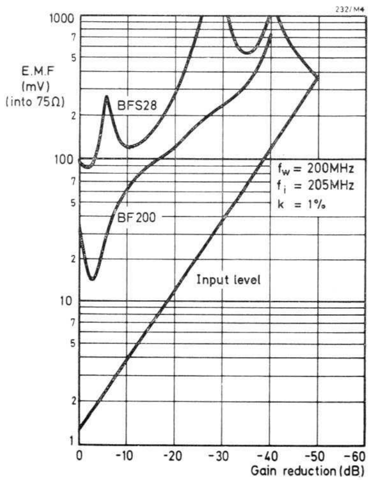


Fig.96 Interfering e.m.f. versus gain to give $k = 1\%$ for BFS28 and BF200.

Intermodulation

Since intermodulation is caused by the same high order terms in the transfer characteristic that produce cross-modulation, the intermodulation performance may be expected to improve by the same factor (five) as cross-modulation.

Blocking

A blocking test was applied to the mixer and this revealed that an interfering signal of 85 mV (across 50 Ω), at 400 kHz separation from the carrier, produced a 3 dB attenuation of the carrier. The British Post Office specifies a minimum of 12.7 mV under these conditions: therefore r.f. amplification of up to 16.5 dB can be interposed between the aerial and the mixer without causing the receiver blocking performance to exceed the specified limit.

Mobile receivers

The excellent performance of mixers and r.f. stages using BFS28 makes the device highly suitable for use in mobile receivers. In this application the channel separation is necessarily small and the channels themselves are constantly in use. The proximity of channels demands that intermodulation and cross-modulation should be at a minimum.

BFS28 as an amplifier at 470 MHz

To utilise the performance of the BFS28 at u.h.f., a strip-line amplifier has been constructed to operate at 470 MHz. The use of strip-lines offers several advantages: they are easier to construct with accurate inductance and capacitances than are lumped-component circuits; stray reactances are more easily controlled; construction in general is easier; production-line assembly is facilitated; they are more compact and lighter; the technique is easily extended for higher frequencies.

The material used for the strip-line amplifier was ptfe-loaded glass-fibre, copper-clad on both sides giving a thickness of 1.6 mm. The dielectric constant of the insulation material was 50 and the thickness was 1.55 mm. The resonant line width was 1 mm, and the ratio of free-space wavelength to effective wavelength (λ_o/λ_m) was 1.47. The line characteristic impedance was 100 Ω. The lines thus constructed give a loaded Q of about 50 and offer a load of 5 kΩ at their resonant frequency. A capacitance of about 3 pF was required for tuning to the required 470 MHz.

The circuit of the amplifier is shown in Fig. 97. The 100 pF capacitors at the input and output offer a very low impedance. Gate 2 is heavily decoupled to

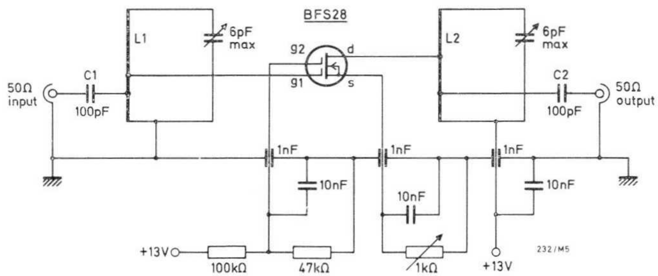


Fig.97 470 MHz amplifier.

L_1 = 52.6 mm length, 1 mm width ⎫ on copper-clad 1.6 mm thickness
L_2 = 50.8 mm length, 1 mm width ⎭ p.t.f.e.-loaded glass fibre.

maintain it at r.f. earth potential, and similar decoupling is used with the other d.c. connections. A power gain of typically 75 dB is obtainable with BFS28 used in this circuit.

BFS28 as a mixer at 470 MHz

Mixing at 470 MHz with the BFS28 can be carried out by applying the signal to Gate 1 and injecting the local oscillator output into the source; Gate 2 is kept well decoupled. The approach has been used in the mixer shown in Fig. 98.

The strip-line design was used, as with the amplifier discussed previously. The standard y-parameter technique was used to design the mixer: the signal and oscillator input tuned circuits are of high Q, and so, for an input signal at 470 MHz, the source tuned to 440 MHz can be considered as earthed. Similarly, the transistor can be regarded as operating in the common-gate mode for the local oscillator injection.

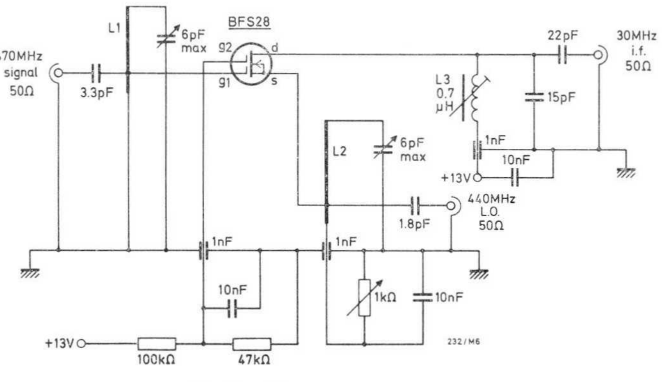


Fig.98 470 MHz frequency mixer.

L_1 = 52.2 mm length, 1 mm width } on copper-clad 1.6 mm thickness
L_2 = 47.1 mm length, 1 mm width } p.t.f.e.-loaded glass fibre.
L_3 = 16.5 turns of 0.450 mm wire on 4.5 mm former.

Performance

The following conditions were applied to the circuit of Fig. 98.

$$V_{DS} = +13\text{ V}$$
$$V_{G2S} = +\ 4\text{ V}$$
$$\text{signal e.m.f.} = 2\text{ mV (into 50 }\Omega)$$
$$\text{local oscillator e.m.f.} = 2\ \ \text{V (into 50 }\Omega)$$

For optimum gain conditions, the gain obtained was 9.8 dB average for several samples of BFS28. For optimum noise conditions, the noise figure was 13.3 dB with a conversion gain of 8.8 dB, averaged over several samples. (The optimum gain conditions occur at $I_D \approx 3$ mA and $V_{G1S} \approx -1.5$ V. The optimum noise conditions occur at $I_D \approx 1$ mA and $V_{G1S} \approx -2$ V.)

BFS28 at higher frequencies

The BFS28 has been used in amplifiers and mixers at frequencies up to 600 MHz with success. No detailed measurements of performance are available, but an experimental amplifier at 600 MHz, similar to the 470 MHz circuit described earlier, gave a gain of 6 dB.

Protection of the BFS28

The insulated gate of the BFS28 is capable of being broken down and permanently damaged if a high voltage surge is applied at the gate terminal. This may become significant when mobile receivers using BFS28 transistors as the first r.f. amplifier are subjected to high induced surge voltage in the aerial, either by mobile spark ignition equipment, static,or by local lightning.

One method of protecting the gate against such surges, is to connect two diodes in anti-parallel across the gate input and chassis; with suitably chosen diodes, these remain almost open circuit at signal voltage levels and have no significant effect on the input impedance; they become operative, and offer a low resistance path, only when the surge voltage exceeds the diode conduction voltage.

When, however, such a pair of diodes is added across a BFS28 (or any similar transistor) there is a degradation of the quadratic transfer characteristic, and therefore the cross-modulation and intermodulation both increase.

Probably the best arrangement for a receiver front end is therefore to use a bipolar transistor as the first r.f. amplifier and use a BFS28 for any succeeding r.f. amplification and for the mixer. In this way, the need for diode protection is generally removed, and the cross-modulation and intermodulation are still kept at a minimum.

If the pair of anti-parallel diodes is required in any application then the diode type BAV45 should be employed. These diodes have been specially developed for this purpose (amongst others) and have an extremely low leakage current over a wide temperature range combined with a low capacitance. In this kind of application the leakage current will be about 5 pA and the capacitance less than 1.3 pF. The BAV45 is a two-lead TO-18 device.

BFS28 as a crystal-controlled oscillator

One application in which the BFS28 excels is as a low-noise crystal-controlled oscillator. Using the BFS28 it is possible to generate an extremely pure oscillation with only negligible side-band frequencies or noise. This purity of response derives from the fact that the device is essentially a majority-carrier device and its output capacitance does not vary with output voltage.

A transmitter-driver using the BFS28 as the crystal-controlled oscillator-multiplier is shown in Fig. 99: the final output is 50 mW.

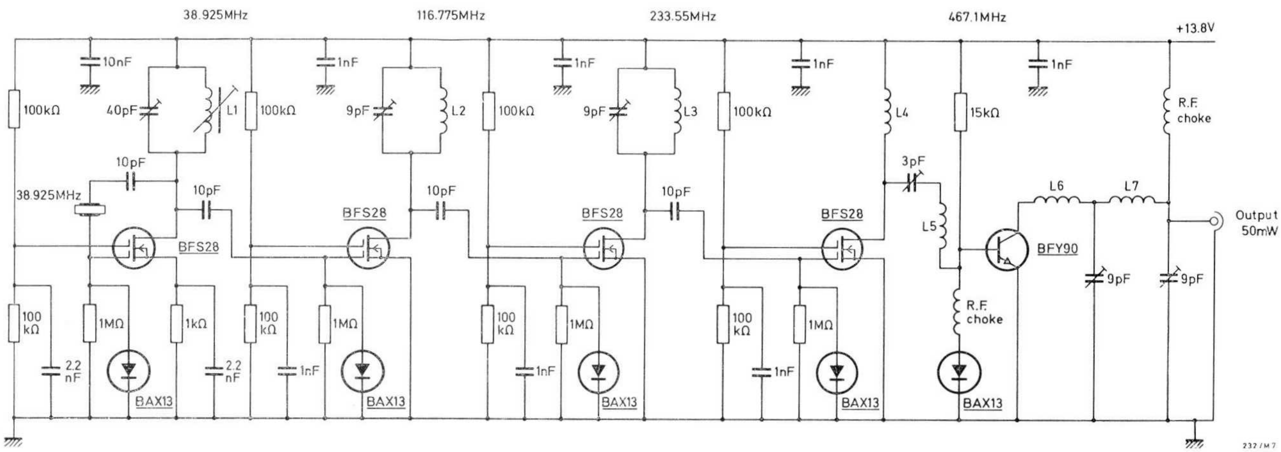


Fig.99 470 MHz transmitter-driver circuit

L_1 10 turns 28 s.w.g. (0.508 mm dia.), 7 mm dia., close-wound
L_2 5 turns 18 s.w.g. (1.22 mm dia.), 6 mm dia., 10 mm long
L_3 2 turns 16 s.w.g. (1.63 mm dia.), 6 mm dia., 7 mm long
L_4 3/4 turn 14 s.w.g. (2.03 mm dia.), 7 mm dia.
L_5 1 turn 18 s.w.g. (1.22 mm dia.), 6 mm dia.
L_6 2 turns 18 s.w.g. (1.22 mm dia.), 6 mm dia, 5 mm long
L_7 1 turn 16 s.w.g. (1.63 mm dia.), 6 mm dia.

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